Features

- SPARC V8 High Performance Low-power 32-bit Architecture
  - LEON2-FT 1.0.13 compliant
  - 8 Register Windows
- Advanced Architecture:
  - On-chip Amba Bus
  - 5 Stage Pipeline
  - 16 kbyte Multi-sets Data Cache
  - 32 kbyte Multi-sets Instruction Cache
- On-chip Peripherals:
  - Memory Interface
    - PROM Controller
    - SRAM Controller
    - SDRAM Controller
  - Timers
    - Two 24-bit Timers
    - Watchdog Timer
  - Two 8-bit UARTs
  - Interrupt Controller with 4 External Programmable Inputs
  - 32 Parallel I/O Interface
  - 33MHz PCI Interface Compliant with 2.2 PCI Specification
- Integrated 32/64-bit IEEE 754 Floating-point Unit
- Fault Tolerance by Design
  - Full Triple Modular Redundancy (TMR)
  - EDAC Protection
  - Parity Protection
- Debug and Test Facilities
  - Debug Support Unit (DSU) for Trace and Debug
  - IEEE 1149.1 JTAG Interface
  - Four Hardware Watchpoints
- Speed Optimized Code RAM Interface
  8, 16 and 40-bit boot-PROM (Flash) Interface Possibilities
- Operating range
  - Voltages
    - 3.3V +/- 0.30V for I/O
    - 1.8V +/- 0.15V for Core
  - Temperature
    - -55°C to 125°C
- Clock: 0MHz up to 100MHz
- Power consumption: 1W at 100MHz
- Performance:
  - 86MIPS (Dhrystone 2.1)
  - 23MFLOPS (Whetstone)
- Radiation Performance
  - Total dose radiation capability (parametric & functional): 60Krads (Si)
  - SEU error rate better than 1 E-5 error/device/day
  - No Single Event Latchup below a LET threshold of 70 MeV.cm²/mg
- Package MCGA 349
- Mass: 9g
- Development Kit Including
  - AT697 Evaluation Board
  - AT697 Sample
  - GRMON Development Tool

Rad-Hard 32 bit SPARC V8 Processor

AT697E

Rev. 4226G–AERO–05/09

Description

The AT697 is a highly integrated, high-performance 32-bit RISC embedded processor based on the SPARC V8 architecture. The implementation is based on the European Space Agency (ESA) LEON2 fault tolerant model. By executing powerful instructions in a single clock cycle, the AT697 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The AT697 is designed to be used as a building block in computers for on-board embedded real-time applications. It brings up-to-date functionality and performance for space application.

The AT697 only requires memory and application specific peripherals to be added to form a complete on-board computer.

The AT697 contains an on-chip Integer Unit (IU), a Floating Point Unit (FPU), separate instruction and data caches, hardware multiplier and divider, interrupt controller, debug support unit with trace buffer, two 24-bit timers, Parallel and Serial interfaces, a Watchdog, a PCI Interface and a flexible Memory Controller. The design is highly testable with the support of a Debug Support Unit (DSU) and a boundary scan through JTAG interface.

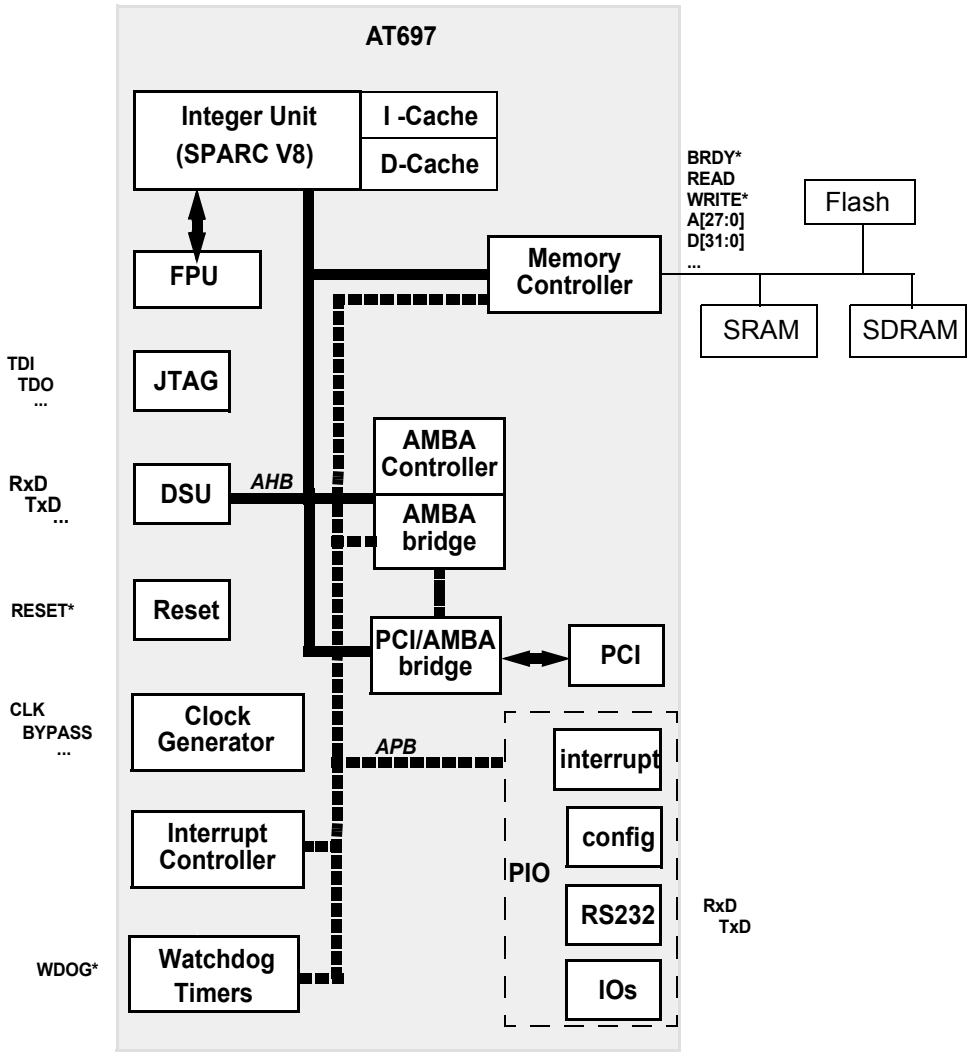
An Idle mode holds the processor pipeline and allows Timer/Counter, Serial ports and Interrupt system to continue functioning.

The processor is manufactured using the Atmel 0.18 µm CMOS process. It has been especially designed for space, by implementing on-chip concurrent transient and permanent error detection and correction.

The AT697E is the first version of the AT697 processor. A second version of the AT697 processor, the AT697F, is under development.

The AT697F will have improved radiation capabilities (up to 100Krad) and will correct all the bugs described in the AT697E errata sheet. The AT697F will be pinout compatible with the AT697E.

Figure 1. AT697 Block Diagram



Pin Configuration

MCGA349 package

Table 1. AT697E MCGA349 pinout

	A	B	C	D	E	F	G
1			VDD18	VSS18	PIO[6]	PIO[1]	$\overline{\text{RAMS[1]}}$
2		VSS18	VDD18	PIO[0]	N.C.	PIO[4]	$\overline{\text{RAMS[2]}}$
3	VDD18	VDD18	VSS18	VCC33	PIO[2]	N.C.	$\overline{\text{RAMOE[3]}}$
4	VSS18	VDD18	PIO[9]	N.C.	PIO[5]	PIO[3]	$\overline{\text{RAMS[4]}}$
5	N.C.	N.C.	PIO[11]	N.C.	N.C.	VSS33	$\overline{\text{RAMOE[1]}}$
6	PIO[13]	PIO[10]	VCC33	Reserved	CB[0]	N.C.	VSS33
7	CB[1]	VSS33	N.C.	PIO[15]	VSS33	PIO[12]	PIO[7]
8	CB[6]	CB[4]	D[2]	VCC33	CB[7]	CB[2]	PIO[8]
9	D[3]	N.C.	D[1]	VSS33	D[6]	VCC33	CB[3]
10	D[8]	D[5]	VCC33	VSS33	Reserved	D[10]	D[4]
11	D[12]	VSS33	VCC33	D[13]	D[7]	D[15]	N.C.
12	D[17]	D[18]	D[11]	VSS33	D[14]	D[16]	D[19]
13	D[21]	D[23]	VCC33	VCC33	VSS33	VSS33	A[1]
14	D[25]	N.C.	D[22]	D[27]	N.C.	VSS33	A[3]
15	D[30]	N.C.	D[26]	D[29]	N.C.	N.C.	A[12]
16	VSS18	VSS18	D[28]	VCC33	N.C.	N.C.	A[6]
17	VDD18	VDD18	VSS18	D[31]	N.C.	A[7]	VSS33
18		VSS18	VDD18	VCC33	A[0]	A[4]	A[8]
19			VDD18	VSS18	A[2]	VSS33	A[9]

Table 2. AT697E MCGA349 pinout (suite)

	H	j	k	l	m	n	p
1	$\overline{\text{RAMOE[0]}}$	VSS33	READ	DSUACT	$\overline{\text{BEXC}}$	VCC33	$\overline{\text{SDWE}}$
2	$\overline{\text{RAMOE[2]}}$	$\overline{\text{ROMS[1]}}$	TCK	DSURX	SDCLK	VSS33	PCI_CLK
3	VCC33	$\overline{\text{ROMS[0]}}$	TDI	DSUTX	DSUBRE	SDDQM[1]	VSS33
4	$\overline{\text{RAMOE[4]}}$	$\overline{\text{RWE[0]}}$	TDO	DSUEN	SDDQM[2]	N.C.	$\overline{\text{SDCS[0]}}$
5	$\overline{\text{RWE[1]}}$	$\overline{\text{WRITE}}$	VSS33	TMS	N.C.	SDDQM[3]	$\overline{\text{SDCAS}}$
6	$\overline{\text{RWE[3]}}$	$\overline{\text{RWE[2]}}$	$\overline{\text{IOS}}$	VSS33	VSS33	$\overline{\text{GNT}}$	A/D[24]
7	$\overline{\text{RAMS[0]}}$	N.C.	TRST	SDDQM[0]	VSS33	VCC33	A/D[30]
8	$\overline{\text{RAMS[3]}}$	VCC33	$\overline{\text{OE}}$	$\overline{\text{BRDY}}$	VCC33	A/D[21]	A/D[18]
9	CB[5]	PIO[14]	VSS33	$\overline{\text{SDRAS}}$	A/D[22]	A/D[16]	A/D[17]
10	D[9]	D[0]	N.C.	A/D[14]	VSS33	$\overline{\text{PERR}}$	$\overline{\text{IRDY}}$

	H	j	k	l	m	n	p
11	D[20]	A[5]	A[16]	N.C.	A/D[12]	A/D[9]	A/D[15]
12	D[24]	A[14]	A[26]	VDD_PLL	$\overline{\text{AGNT[3]}}$	A/D[1]	A/D[8]
13	N.C.	VCC33	A[21]	N.C.	N.C.	VSS33	A/D[5]
14	A[10]	VCC33	A[27]	LOCK	SKEW[1]	A/D[0]	$\overline{\text{AGNT[1]}}$
15	N.C.	VSS33	VCC33	A[24]	Reserved	BYPASS	CLK
16	A[11]	VSS33	A[23]	$\overline{\text{RESET}}$	LFT	$\overline{\text{AREQ[2]}}$	VSS33
17	A[19]	A[17]	VSS33	VCC33	$\overline{\text{WDOG}}$	N.C.	VSS33
18	A[13]	A[18]	A[22]	VSS33	VSS_PLL	$\overline{\text{AREQ[3]}}$	N.C.
19	A[15]	A[20]	A[25]	$\overline{\text{ERROR}}$	SKEW[0]	VCC33	$\overline{\text{AREQ[1]}}$

Table 3. AT697E MCGA349 pinout (suite 2)

	r	t	u	v	w
1	$\overline{\text{REQ}}$	VSS18	VDD18		
2	N.C.	$\overline{\text{SDCS[1]}}$	VDD18	VSS18	
3	$\overline{\text{PCI\_RST}}$	A/D[31]	VSS18	VDD18	VDD18
4	N.C.	A/D[29]	VCC33	VSS18	VSS18
5	N.C.	N.C.	A/D[26]	N.C.	A/D[28]
6	N.C.	A/D[27]	IDSEL	VSS33	A/D[25]
7	$\overline{\text{SYSEN}}$	VSS33	VCC33	$\overline{\text{C/BE[3]}}$	A/D[23]
8	VSS33	VSS33	$\overline{\text{FRAME}}$	A/D[20]	A/D[19]
9	$\overline{\text{TRDY}}$	VCC33	N.C.	$\overline{\text{C/BE[2]}}$	VSS33
10	$\overline{\text{PCI\_LOCK}}$	$\overline{\text{DEVSEL}}$	$\overline{\text{STOP}}$	VCC33	VCC33
11	VSS33	VCC33	VSS33	$\overline{\text{C/BE[1]}}$	$\overline{\text{SERR}}$
12	N.C.	A/D[11]	PAR	VSS33	A/D[13]
13	VCC33	A/D[7]	A/D[10]	VSS33	VSS33
14	VCC33	VSS33	$\overline{\text{C/BE[0]}}$	A/D[4]	A/D[6]
15	N.C.	A/D[2]	VCC33	N.C.	A/D[3]
16	N.C.	VCC33	N.C.	VDD18	VSS18
17	VCC33	$\overline{\text{AGNT[0]}}$	VSS18	VDD18	VDD18
18	N.C.	$\overline{\text{AGNT[2]}}$	VDD18	VSS18	
19	$\overline{\text{AREQ[0]}}$	VSS18	VDD18		

Notes: 1. ‘Reserved’ pins shall not be driven to any voltage
2. N.C. refers to unconnected pins

QFP256 Package

Table 4. AT697E MQFP256 pinout

pin number	pin name	pin number	pin name	pin number	pin name
1	VCC33	31	TCK	61	PIO1
2	$\overline{\text{PCI\_REQ}}$	32	TMS	62	PIO2
3	$\overline{\text{PCI\_GNT}}$	33	VSS	63	PIO3
4	PCI_CLK	34	TDI	64	PIO4
5	$\overline{\text{PCI\_RST}}$	35	TDO	65	PIO5
6	$\overline{\text{SDCS0}}$	36	$\overline{\text{WRITE}}$	66	PIO6
7	VSS	37	READ	67	VCC33
8	VDD18	38	$\overline{\text{OE}}$	68	PIO7
9	$\overline{\text{SDCS1}}$	39	$\overline{\text{IOS}}$	69	PIO8
10	$\overline{\text{SDWE}}$	40	VCC33	70	PIO9
11	$\overline{\text{SDRAS}}$	41	$\overline{\text{ROMS0}}$	71	VSS
12	VSS	42	$\overline{\text{ROMS1}}$	72	VDD18
13	VSS	43	$\overline{\text{RWE0}}$	73	PIO10
14	$\overline{\text{SDCAS}}$	44	$\overline{\text{RWE1}}$	74	PIO11
15	VCC33	45	$\overline{\text{RWE2}}$	75	Reserved
16	SDDQM0	46	$\overline{\text{RWE3}}$	76	PIO12
17	SDDQM1	47	$\overline{\text{RAMOE0}}$	77	PIO13
18	SDDQM2	48	$\overline{\text{RAMOE1}}$	78	PIO14
19	SDDQM3	49	$\overline{\text{RAMOE2}}$	79	PIO15
20	SDCLK	50	$\overline{\text{RAMOE3}}$	80	VCC33
21	$\overline{\text{BRDY}}$	51	$\overline{\text{RAMOE4}}$	81	CB0
22	$\overline{\text{BEXC}}$	52	$\overline{\text{RAMS0}}$	82	CB1
23	VSS	53	VCC33	83	CB2
24	VSS	54	$\overline{\text{RAMS1}}$	84	CB3
25	DSUEN	55	$\overline{\text{RAMS2}}$	85	VCC33
26	DSUTX	56	$\overline{\text{RAMS3}}$	86	CB4
27	DSURX	57	VSS	87	CB5
28	DSUBRE	58	VDD18	88	CB6
29	DSUACT	59	$\overline{\text{RAMS4}}$	89	CB7
30	TRST	60	PIO0	90	D0

Table 5. AT697E MQFP256 pinout (suite)

pin number	pin name	pin number	pin name	pin number	pin name
91	VCC33	**124**	D25	157	A19
92	D1	**125**	D26	158	A20
93	D2	**126**	D27	159	A21
94	D3	**127**	D28	160	A22
95	D4	**128**	D29	161	VSS
96	D5	**129**	D30	162	VCC33
97	D6	130	VCC33	163	A23
98	Reserved	131	D31	164	A24
99	VCC33	132	N.C.	165	A25
100	D7	133	A0	166	A26
101	D8	134	A1	167	A27
102	D9	135	VSS	168	$\overline{\text{WDOG}}$
103	D10	136	VDD18	169	$\overline{\text{ERROR}}$
104	D11	137	A2	170	VCC33
105	D12	138	A3	171	$\overline{\text{RESET}}$
106	VCC33	139	A4	172	Reserved
107	D13	140	VCC33	173	LOCK
108	D14	141	A5	174	SKEW1
109	D15	142	A6	175	SKEW0
110	D16	143	A7	176	BYPASS
111	D17	144	A8	177	VSS_PLL
112	VSS	145	A9	178	FLT
113	D18	146	A10	179	VDD_PLL
114	VCC33	147	VCC33	180	CLK
115	D19	148	A11	181	VCC33
116	D20	149	A12	182	$\overline{\text{PCI\_AREQ3}}$
117	D21	150	A13	183	$\overline{\text{PCI\_AGNT3}}$
118	D22	151	A14	184	$\overline{\text{PCI\_AREQ2}}$
119	D23	152	A15	185	VSS
120	D24	153	A16	186	VDD18
121	VSS	154	VCC33	187	$\overline{\text{PCI\_AGNT2}}$
122	VDD18	155	A17	188	$\overline{\text{PCI\_AREQ1}}$
123	VCC33	156	A18	189	VCC33

Table 6. AT697E MQFP256 pinout (suite 2)

pin number	pin name	pin number	pin name	pin number	pin name
190	$\overline{\text{PCI\_AGNT1}}$	**213**	A/D12	236	A/D19
191	$\overline{\text{PCI\_AREQ0}}$	**214**	A/D13	237	$\overline{\text{SYSEN}}$
192	$\overline{\text{PCI\_AGNT0}}$	**215**	A/D14	238	A/D20
193	A/D0	**216**	A/D15	239	VCC33
194	VCC33	**217**	VCC33	240	A/D21
195	A/D1	**218**	$\overline{\text{C/BE1}}$	241	A/D22
196	A/D2	**219**	PAR	242	A/D23
197	A/D3	220	$\overline{\text{SERR}}$	243	IDSEL
198	A/D4	221	$\overline{\text{PERR}}$	244	$\overline{\text{C/BE3}}$
199	VSS	222	VCC33	245	VCC33
200	VDD18	223	$\overline{\text{PCI\_LOCK}}$	246	A/D24
201	VCC33	224	$\overline{\text{STOP}}$	247	A/D25
202	A/D5	225	$\overline{\text{DEVSEL}}$	248	A/D26
203	A/D6	226	$\overline{\text{TRDY}}$	249	VSS
204	A/D7	227	VCC33	250	VDD18
205	$\overline{\text{C/BE0}}$	228	$\overline{\text{IRDY}}$	251	A/D27
206	VSS	229	$\overline{\text{FRAME}}$	252	VCC33
207	VCC33	230	VSS	253	A/D28
208	A/D8	231	$\overline{\text{C/BE2}}$	254	A/D29
209	A/D9	232	A/D16	255	A/D30
210	A/D10	233	VCC33	256	A/D31
211	A/D11	234	A/D17		
212	VCC33	235	A/D18		

Notes: 1. ‘Reserved’ pins shall not be driven to any voltage

2. N.C. refers to unconnected pins

Pin Description

IU and FPU Signals

A[27:0] - Address bus (output)

A[27:0] bus carries the addresses during accesses to external memory. When access to cache memory is performed, the address of the last external memory access remains driven on the address bus.

D[31:0] - Data bus (bi-directional)

D[31:0] bus carries the data during accesses to memory. The processor automatically configures the bus as output and drive the lines during write cycles.
During accesses to 8-bit areas, only D[31:24] are used.
During accesses to 16-bit areas, only D[31:16] are used.

CB[7:0] - Check bits (bi-directional)

CB[6:0] bus carries the EDAC checkbits during memory accesses. CB[7](1) takes the value of tcb[7] in the error control register. Processor only drives CB[7:0] during write cycles to areas programmed to be EDAC protected.

Note: 1. CB[7] is implemented to enable programming of flash memories. When only 7 bits are useful for EDAC protection, 8 are needed for programming.

Memory Interface Signals

General management

OE* - Output enable (output)

This active low output is asserted during read cycles on the memory bus.

BRDY* - Bus ready (input)

When driven low, this input indicates to the processor that the current memory access can be terminated on the next rising clock edge. When driven high, this input indicates to the processor that it must wait and not end the current access.

READ - Read cycle (output)

This active high output is asserted during read cycles on the memory bus.

WRITE* - Write enable (output)

This active low output provides a write strobe during write cycles on the memory bus.

PROM

ROMS*[1:0] - PROM chip-select (output)

These active low outputs provide the chip-select signal for the PROM area. ROMS*[0] is asserted when the lower half of the PROM area is accessed (0 - 0x10000000), while ROMS*[1] is asserted for the upper half.

SRAM

RAMOE*[4:0] - RAM output enable (output)

These active low signals provide an individual output enable for each RAM bank.

RAMS*[4:0] - RAM chip-select (output)

These active low outputs provide the chip-select signals for each RAM bank.

RWE* [3:0] - RAM write enable (output)

These active low outputs provide individual write strobes for each byte. RWEN[0] controls D[31:24], RWEN[1] controls D[23:16], etc.

I/O

IOS* - I/O select (output)

This active low output is the chip-select signal for the memory mapped I/O area.

SDRAM Interface

SDCLK - SDRAM clock (output)

SDRAM clock provides the SDRAM interface clock reference.

SDCAS* - SDRAM column address strobe (output)

This active low signal provides a common CAS for all SDRAM devices.

SDCS*[1:0] - SDRAM chip select (output)

These active low outputs provide the chip select signals for the two SDRAM banks.

SDDQM[3:0] - SDRAM data mask (output)

These active low outputs provide the DQM signals for both SDRAM banks.

SDRAS*- SDRAM row address strobe (output)

This active low signal provides a common RAS for all SDRAM devices.

SDWEN - SDRAM write strobe (output)

This active low signal provides a common write strobe for all SDRAM devices.

System Signals

CLK - Processor clock (input)

The CLK input provides the main processor clock reference.

RESET* - Processor reset (input)

When asserted, this active low input will reset the processor and all on-chip peripherals.

WDOG* - Watchdog time-out (open-drain output)

This active low output is asserted when the watchdog expires.

BEXC* - Bus exception (input)

This active low input is sampled simultaneously with the data during accesses on the memory bus. If asserted, a memory error will be generated.

ERROR* - Processor error (open-drain output)

This active low output is asserted when the processor has entered error state and is halted. This happens when traps are disabled and a synchronous (un-maskable) trap occurs.

PIO[15:0] - Parallel I/O port (bi-directional)

These bi-directional signals can be used as inputs or outputs to control external devices.

BYPASS - PLL bypass (input)

When driven to VCC, this active high input set the PLL in bypass mode. The device is then directly clocked by the external clock. When grounded, the device is clocked through the PLL.

SKEW[1:0] - Clock tree skew (input)

These input signals configurate the programmable skew on the triplicated clock trees.

LOCK - PLL lock (output)

This active high output is asserted when the PLL output (internal node) is locked at the frequency corresponding to four times the input command.

LFT - PLL passive low pass filter (input)

This input is used to connect the PLL passive low pass filter.

DSU Signals

DSUACT - DSU active (output)

This active high output is asserted when the processor is in debug mode and controlled by the DSU.

DSUBRE - DSU break enable (input)

A low-to-high transition on this active high input will generate break condition and put the processor in debug mode.

DSUEN - DSU enable (input)

The active high input enables the DSU unit. If de-asserted, the DSU trace buffer will continue to operate but the processor will not enter debug mode.

DSURX - DSU receiver (input)

This active high input provides the data to the DSU communication link receiver

DSUTX - DSU transmitter (output)

This active high input provides the output from the DSU communication link transmitter.

JTAG

TCK - Test Clock (input)

Used to clock serial data into boundary scan latches and control sequence of the test state machine. TCK can be asynchronous with CLK.

TMS - Test Mode select (input)

Primary control signal for the state machine. Synchronous with TCK. A sequence of values on TMS adjusts the current state of the TAP.

TDI - Test data input (input)

Serial input data to the boundary scan latches. Synchronous with TCK

TDO - Test data output (output)

Serial output data from the boundary scan latches. Synchronous with TCK

TRST - Test Reset (input)

Resets the test state machine. Can be asynchronous with TCK. Shall be grounded for end application.

PCI Arbiter

AREQ*[3:0] - PCI bus request (Input)

When asserted, these active low inputs indicate that a PCI agent is requesting the bus.

AGNT*[3:0] - PCI bus grant (Output)

When asserted, these active low outputs indicate that a PCI agent is granted the PCI bus.

PCI interface

A/D[31:0] - PCI Address Data (bi-directional)

Address and Data are multiplexed on the same PCI pins.

During the address phase, A/D[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases, A/D[07::00] contain the least significant byte and A/D[31::24] contain the most significant byte.

C/BE[3:0]* - PCI Bus Command and Byte Enables (bi-directional)

During the address phase of a transaction, C/BE[3::0]* define the bus command. During the data phase, C/BE[3::0]* are used as Byte Enables. The Byte Enables are valid for the entire data phase.

PAR - Parity (bi-directional)

The number of "1"s on A/D[31::00], C/BE[3::0]*, and PAR equals an even number

FRAME* - Cycle Frame (bi-directional)

It is driven by the current master to indicate the beginning and duration of an access. FRAME* is asserted to indicate a bus transaction is beginning. While FRAME* is asserted, data transfers continue. When FRAME* is deasserted, the transaction is in the final data phase or has completed.

IRDY* - Initiator Ready (bi-directional)

IRDY* indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY* is used in conjunction with TRDY*. During a write, IRDY* indicates that valid data is present on A/D[31::00]. During a read, it indicates the master is prepared to accept data.

TRDY* - Target Ready (bi-directional)

TRDY* indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY* is used in conjunction with IRDY*. During a read, TRDY* indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data.

STOP* - Stop (bi-directional)

STOP* indicates the current target is requesting the master to stop the current transaction.

PCI_LOCK* - Lock (bi-directional)

PCI_LOCK* indicates an atomic operation to a bridge that may require multiple transactions to complete.

IDSEL - Initialization Device Select (input)

Initialization Device Select is used as a chip select during configuration read and write transactions.

DEVSEL* - Device Select (bi-directional)

When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL* indicates whether any device on the bus has been selected.

REQ* - PCI bus request (output)

REQ* indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own REQ* which must be tri-stated while PCI_RST* is asserted.

GNT* - PCI Bus Grant (input)

GNT* indicates to the agent that access to the bus has been granted. This is a point-to-point signal. Every master has its own GNT* which must be ignored while PCI_RST* is asserted.

PCI_CLK - PCI clock (input)

PCI_CLK provides timing for all transactions on PCI. All other PCI signals, except PCI_RST*, are sampled on the rising edge of PCI_CLK and all other timing parameters are defined with respect to this edge.

PCI_RST* - PCI Reset (input)

Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state.

PERR* - Parity Error (bi-directional)

Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR* pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR* is one clock for each data phase that a data parity error is detected.

SERR* - System Error (bi-directional)

System Error is for reporting address parity errors, data parity errors on the special cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

SYSEN* - PCI Host (input)

This active low input specifies the configuration of the device. At boot-up time, if SYSEN* is sampled at a low level, the device is configured as the host of the PCI bus. If SYSEN* is sampled at a high level, the device is configured as a satellite.

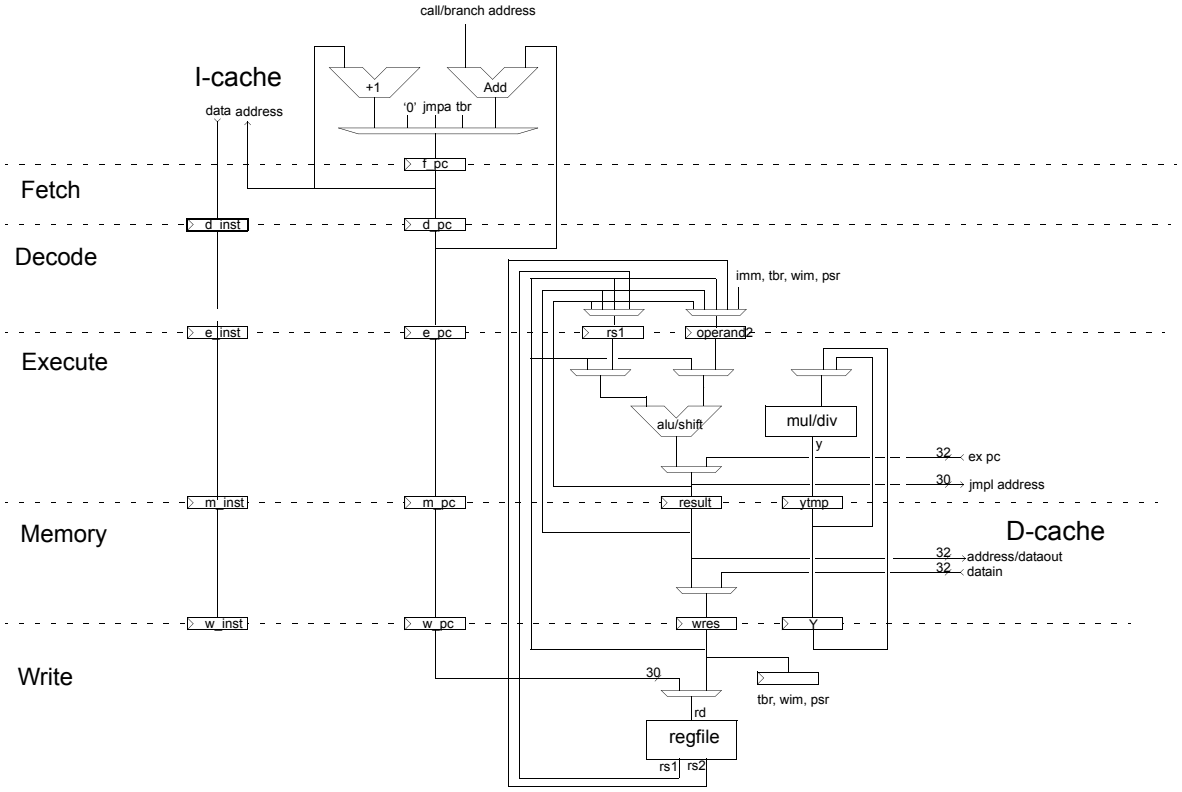
AT697 CPU Core

This section discusses the SPARC core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

SPARC Architecture Overview

The AT697 CPU core is based on the LEON2 architecture.

Figure 2. Block diagram of the AT697 Integer Unit architecture



The AT697 integer unit (IU) implements SPARC integer instructions as defined in SPARC Architecture Manual version 8. The IU is designed for highly dependable space and military applications by including fault tolerance features.

To execute instructions at a rate approaching one instruction per clock cycle, the IU employs a five-stage instruction pipeline that permits parallel execution of multiple instructions.

- Instruction Fetch: If the instruction cache is enabled, the instruction is fetched from the instruction cache. Otherwise, the fetch is forwarded to the memory controller. The instruction is valid at the end of this stage and is latched inside the IU.
- Decode: The instruction is decoded and the operands are read. Operands may come from the register file or from internal data bypasses. CALL and Branch target addresses are generated in this stage.
- Execute: ALU, logical, and shift operations are performed. For memory operations and for JMPL/RETT, the address is generated.
- Memory: Data cache is accessed. For cache reads, the data will be valid by the end of this stage, at which point it is aligned as appropriate. Store data read out in the Execute stage is written to the data cache at this time.

- Write: The result of any ALU, logical, shift, or cache read operations re written back to the register file.

All five stages operate in parallel, working on up to five different instructions at a time. A basic 'single-cycle' instruction enters the pipeline and completes in five cycles.

By the time it reaches the write stage, four more instructions have entered and are driving through the pipeline behind it. So, after the first five cycles, a single-cycle instruction exits the pipeline and a single-cycle instruction enters the pipeline on every cycle. Of course, a 'single-cycle' instruction actually takes five cycles to complete, but they are called single cycle because with this type of instruction the processor can complete one instruction per cycle after the initial five-cycle delay.

In order to maximize performance and parallelism, the AT697 SPARC implementation uses powerful AMBA bus. Instructions in the program memory are executed with a five level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle.

Program Counters

Two 32-bit program counters (PC and nPC) are provided. The 32-bit PC contains the address of the instruction currently being executed by the IU. The nPC holds the address of the next instruction to be executed (assuming a trap does not occur).

When a trap occurs, the PC address is saved in the local register (l1) while the nPC address is saved in the local register (l2). When returning from trap, l1 value is copied back to PC and l2 value is copied back to nPC.

ALU - Arithmetic Logic Unit

The high-performance ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate memory address are executed. The implementation of the architecture also provide a powerful multiplier/divider supporting both signed and unsigned multiplication/division.

Support for high performance 64-bit operation is also provided.The 32-bit Y register contains the most significant word of the double-precision product of an integer multiplication, as a result of either an integer multiply instruction, or of a routine that uses the integer multiply step instruction. The Y register also holds the most significant word of the double-precision dividend for an integer divide instruction.

Register File - Windows

The fast access register file contains 8 SPARC register windows. Each window consists in a 32-register set. When a program is running, it has access to 32 32-bit processor registers which include 8 global registers plus 24 registers that belong to the current register window.

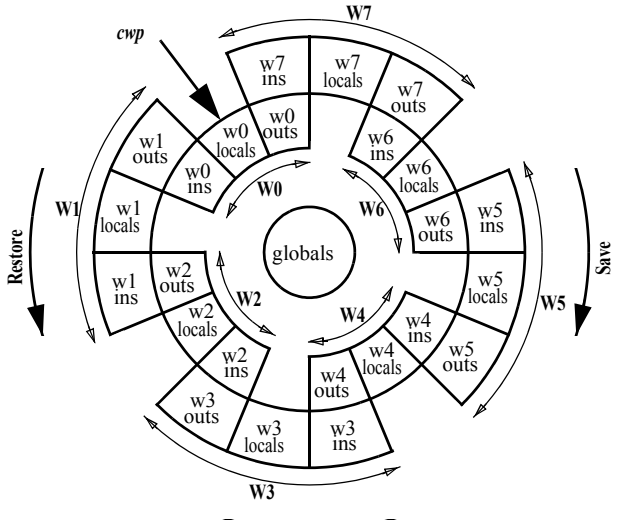
- The first 8 registers in the window are called the in registers' (*i0-i7*). When a function is called, these registers may contain arguments that can be used.
- The next 8 are the 'local registers' (*l0-l7*) which are scratch registers that can be used for anything while the function executes.
- The last 8 registers are the 'out registers' (*o0-o7*) which the function uses to pass arguments to functions that it calls.

AT697 register file implementation is based on two dual-port rams. The first dual-port ram corresponds to %rs1 operand of a SPARC instruction while the second corresponds to %rs2 operand. The two dual-port rams contents are always equal.

When one function calls another, the calling function can choose to execute a SAVE instruction. This instruction decrements an internal counter, the current window pointer (*cwp)*, shifting the register window downward. The caller's *out* registers then become

the calling function's *in* registers, and the calling function gets a new set of *local* and *out* registers for its own use. Only the pointer changes because the registers and return address do not need to be stored on a stack. The RETURN instruction acts in the opposite way

Figure 3. Overlapping Windows



The Window Invalid Mask register (WIM) is controlled by supervisor software and is used by hardware to determine whether a window overflow or underflow trap is to be generated by a SAVE, RESTORE, or RETT instruction.

When a SAVE, RESTORE, or RETT instruction is executed, the current value of the CWP is compared against the WIM register. If the SAVE, RESTORE, or RETT instruction would cause the CWP to point to an "invalid" register set, a window_overflow or window_underflow trap is caused.

To prevent erroneous operations from SEU errors in the main register file, each word is protected with a 7-bit EDAC checksum. The EDAC checksums are checked when the register is used as operand in an instruction. Any single-bit error is corrected and written back to the register file before the instruction is executed. If an un-correctable error is detected, a register hardware error trap (trap 0x20) is generated.

The protection can be enabled/disabled by programming the 'di' bit from register file protection control register. By setting the 'te' bit, errors can be inserted in the register file to test the protection function. When the 'te' bit is set, the register checksum is combined with the 'tcb' field before being written to the register file.

Due to the presence of the two dual-port rams for register file implementation, the following rules apply to the error injection test process.

- Test checkbits TCB[2:0] is Xored with checkbit[6:4] corresponding to the %rs1 operand.
- Test checkbits TCB[5:3] is Xored with checkbit[6:4] corresponding to the %rs2 operand.

Here is a simple example for the test of a single error in register file %rs1

```
! 0x32 =
!   register file test enable
!   tcb[2:0] = 0x4
!   tcb[5:3] = 0x1
```

```
    mov 0x32, %l1
    mov %l1, %asr16
! clear %l3
! =>  write 0x0 to %l3
!       forces 0x08 as checkbit for %l3 (error insertion in %rs1 dual-port ram)
    mov %g0, %l3
! disable EDAC test mode
    mov %g0, %asr16
! access to %l3 as %rs1 operand
! => single error detection and correction
    add %l3,%l2,%l1
```

A correction counter ‘cnt’ is provided for error management. The ‘cnt’ field is incremented each time a register correction is performed. It saturates at “111”.

State Register

The State Register (PSR) contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the Status Register is updated after all ALU operations, as specified in the SPARC architecture specification. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The state also provides some global information on the current window used, the authorized interrupts and peripheral (FPU and coprocessor) presence. A global interrupt management is provided through the processor state register. Trap and Interrupts can be individually enabled/disables from within this register.

Instruction Set

AT697 instructions fall into six functional categories: load/store, arithmetic/logical/ shift, control transfer, read/write control register, floating-point, and miscellaneous. Please refer to SPARC V8 Architecture manual that presents all the implemented instructions.

Floating Point Unit

The FPU is designed to provide execution of single and double-precision floating-point instructions. During the execution of floating-point instructions the processor pipeline is held.

The FPU is designed for highly dependable space and military applications, by including fault tolerance features like error detection and correction and triple modular redundancy.

The FPU depends upon the IU to access all addresses and control signals for memory access. Floating-point loads and stores are executed in conjunction with the IU, which provides addresses and control signals while the FPU supplies or stores the data. Instruction fetch for integer and floating-point instructions is provided by the IU.

The FPU contains 32 32-bit floating-point ***f*** registers, which are numbered from f[0] to f[31]. Unlike the windowed *r* registers, at a given time an instruction has access to any of the 32 *f* registers. The *f* registers can be read and written by FPop (FPop1/FPop2 format) instructions, and by load/store single/double floating-point instructions (LDF, LDDF, STF, STDF).

Rounding Direction

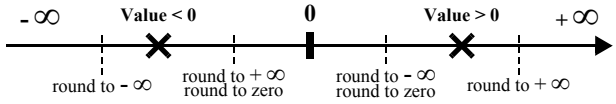
Rounding direction for floating point results is built according to the ANSI/IEEE Standard 754-1985.

In this way,

- 0 = round to nearest

- 1 = round to zero
- 2 = round to +infinity
- 3 = round to -infinity

Figure 4. Rounding Direction Schematic



Fault Tolerance

The processor has been especially designed for space application. To prevent erroneous operations from single event transient (SET) and single event upset (SEU) errors, the AT697 processor implements a set of protection features including :

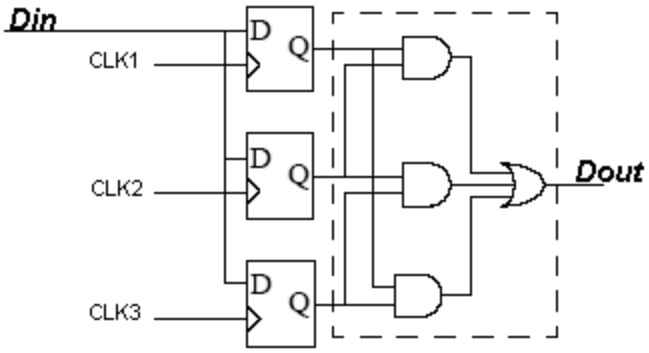
- Full triple modular redundancy (TMR) architecture

  The TMR architecture is based on a fully triplicated clock distribution (CLK1, CLK2 and CLK3). The PCI clock and the CPU clock are built as three-clock trees. The same triplication is applied to the PCI reset and to the CPU reset. See figure 5 for an overview of the TMR architecture.

  Programmable skews on the clock trees are also provided to prevent the processor from arbitrary single-event transient errors.

  Refer to the ‘clock’ section for detailed information on TMR implementation and skew implementation.
- EDAC protection on Regfile
- EDAC protection on external memory interface
- Parity protection on instruction and data caches

Figure 5. TMR structure - Clock triplication principle



Watch Points

The integer unit contains four hardware watch-points allowing generation of a trap on an arbitrary memory address range. Any binary aligned address range can be watched (the two less significant bits are ignored)

Each watch-point consists in a pair of application-specific registers

- break address register
  The break address defines a reference address for testing.
- mask register
  The mask indicates which bits of the break address register are to be effectively taken in account during address test

Configuration

A watchpoint is enabled setting logical one at least one of the three bits IF, DI or DS in the watchpoint address and mask registers. When all three bits are set logical zero, the watchpoint is disabled.

If the instruction fetch bit (IF) from the watchpoint address register is set logical one, any attempt to fetch an instruction from one of the address defined by ADDR and MASK results in a trap generation.

If the data store bit (DS) from the watchpoint address register is set logical one, any attempt to store data to one of the address defined by ADDR and MASK results in a trap generation.

If the data load bit (DL) from the watchpoint mask register is set logical one, any attempt to load a data from one of the address defined by ADDR and MASK results in a trap generation.

Operation

To detect if an address is part of the memory address range that traps, address bit 31 down to bit 2 are Xored with the ADDR field from the watchpoint address register.

This operation is based on the following segmentation of an address.

Table 7. Address Segmentation

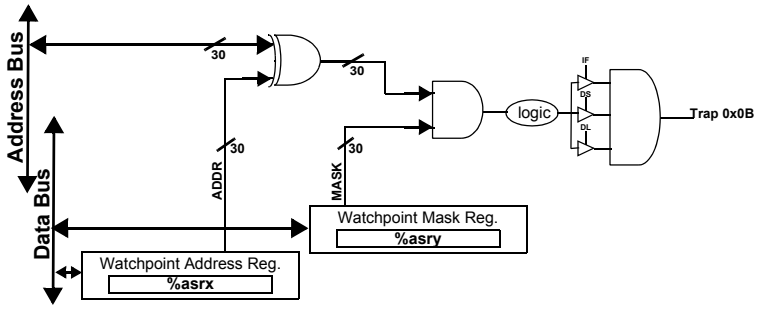
bit num.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
field	Address																														ignored	

With such segmentation, it is possible to define trap segment from 4bytes up to 1Gbyte.

The result of the Xor is then Anded with the MASK field of the watchpoint mask register.

If the result is zero, this indicates that address specified is in the watched range. Then, a watchpoint hit error is generated. Trap 0x0B is generated. If result is different from zero, address is out of the watched address range.

Figure 6. Watchpoint Hit Principle



Traps and Interrupts

Overview

The AT697 supports two types of traps:

- synchronous traps
- asynchronous traps also called interrupts.

Synchronous traps are caused by hardware responding to a particular instruction: they occur during the instruction that caused them. Asynchronous traps occur when an external event interrupts the processor. They are not related to any particular instruction and occur between the execution of instructions.

A trap is a vectored transfer of control to the supervisor through a special trap table that contains the first four instructions of each trap handler. The trap base address (TBR) of the table is established by supervisor and the displacement, within the table, is determined by the trap type.

A trap causes the current window pointer to advance to the next register window and the hardware to write the program counters (PC & nPC) into two registers of the new window.

Synchronous Traps

The AT697 follows the general SPARC trap model. The table below shows the implemented traps and their individual priority.

Table 8. Trap Overview

Trap	TT (trap type)	Priority	Description
reset	0x00	1	Power-on reset
write error	0x2b	2	Write buffer error
instruction_access_exception	0x01	3	Error during instruction fetch Edac uncorrectable error during instruction fetch
illegal_instruction	0x02	5	UNIMP or other un-implemented instruction
privileged_instruction	0x03	4	Execution of privileged instruction in user mode
fp_disabled	0x04	6	FP instruction while FPU disabled
cp_disabled	0x24	6	co-processor instruction while co-processor disabled
watchpoint_detected	0x0B	7	Instruction or data watchpoint match
window_overflow	0x05	8	SAVE into invalid window
window_underflow	0x06	8	RESTORE into invalid window
register_hadrware_error	0x20	9	register file uncorrectable EDAC error
mem_address_not_aligned	0x07	10	Memory access to un-aligned address
fp_exception	0x08	11	FPU exception

data_access_exception	0x09	13	Access error during load or store instruction
tag overflow	0x0A	14	Tagged arithmetic overflow
divide_exception	0x2A	15	Divide by zero
trap_instruction	0x80 -0xFF	16	Software trap instruction (TA)

Traps Description

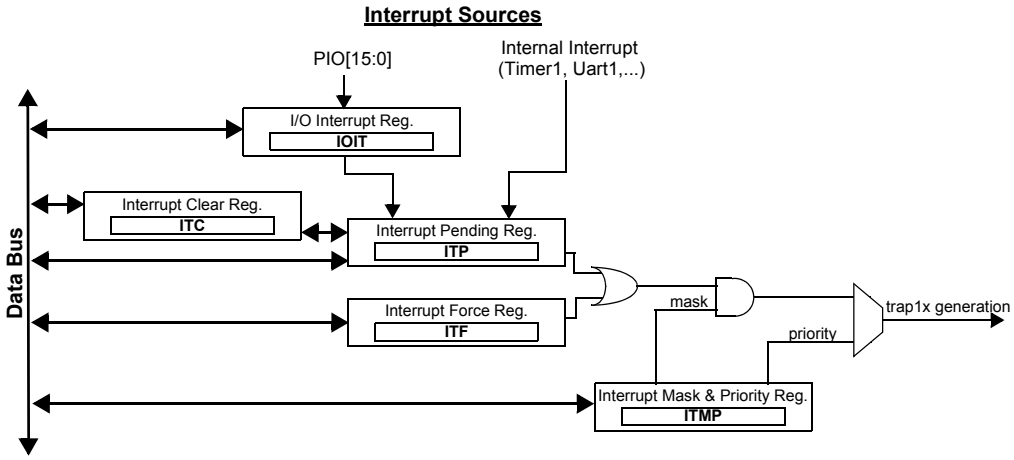
- reset - A reset trap is caused by an external reset request. It causes the processor to begin executing at virtual address 0. After a Reset Trap, no special memory states are defined exept the PSR's 'et' and 's' bits that are initialized respectively '0' and '1'.
- write error - An error exception occurred on a data store to memory.
- instruction_access_exception - A blocking error exception occurred on an instruction access.
- illegal_instruction - An attempt was made to execute an instruction with an unimplemented opcode, or an UNIMP instruction, or an instruction that would result in illegal processor state.
- privileged_instruction - An attempt was made to execute a privileged instruction while supervisor bit (s) in PSR is '0' (not in supervisor mode).
- fp_disabled - An attempt was made to execute an FPU instruction while FPU is not enabled or not present.
- cp_disabled - An attempt was made to execute a co-processor instruction while co-processor is not enabled or not present.
- watchpoint_detected - An instruction fetch memory address or load/store data memory address matched the contents of a pre-loaded implementation-dependent "watchpoint" register.
- window_overflow - A SAVE instruction attempted to cause the current window pointer (CWP) to point to an invalid window in the WIM.
- window_underflow - A RESTORE or RETT instruction attempted to cause the current window pointer (CWP) to point to an invalid window in the WIM.
- register_hardware_error - An error exception occurred on a *read only* register access.
  A register file uncorrectable error was detected.
- mem_address_not_aligned - A load/store instruction would have generated a memory address that was not properly aligned according to the instruction, or a JMPL or RETT instruction would have generated a non-word-aligned address.
- fp_exception - An FPU instruction generated an IEEE_754_exception and its corresponding trap enable mask (TEM) bit was 1, or the FPU instruction was unimplemented, or the FPU instruction did not complete, or there was a sequence or hardware error in the FPU. The type of floating-point exception is encoded in the FSR's *ftt* field.
- data_access_exception - A blocking error exception occurred on a load/store data access. EDAC uncorrectable error.
- tag_overflow - A tagged arithmetic instruction was executed, and either arithmetic overflow occurred or at least one of the tag bits of the operands was non zero.
- trap_division_by_zero - An integer divide instruction attempted to divide by zero.
- trap_instruction - A software instruction (Ticc) was executed and the trap condition evaluated to true.

When multiple synchronous traps occur at the same cycle (i.e hardware errors), the highest priority trap is taken, and lower priority traps are ignored.

Asynchronous Traps / Interrupts

The AT697 handles 11 interrupts. Interrupts can be due to external interrupt requests not directly related to any particular instruction or can be due to exception caused by particular previously executed instruction.

Figure 7. Interrupt Controller Block Diagram



Operation

When an interrupt is generated, the corresponding bit is set in the interrupt pending register (ITP). The pending bits are ANDed with the interrupt mask register and then forwarded to the priority selector. The highest interrupt from priority level 1 will be forwarded to the IU - if no unmasked pending interrupt exists on priority level 1, then the highest unmasked interrupt from priority level 0 is forwarded.

When the IU acknowledges the interrupt, the corresponding pending bit will automatically be cleared.

Interrupt can also be forced by setting a bit in the interrupt force register. In this case, the IU acknowledgement will clear the force bit rather than the pending bit.

After reset, the interrupt mask register is set to all zeros while the remaining control registers are undefined.

Interrupt List

The following table presents the assignement of the interrupts.

Table 9. Interrupt Overview

Interrupt	TT (Trap Type)	Source
15	0x1F	unused
14	0x1E	PCI
13	0x1D	unused
12	0x1C	unused
11	0x1B	DSU trace buffer
10	0x1A	unused
9	0x19	Timer 2
8	0x18	Timer 1
7	0x17	I/O interrupt [3]

Interrupt	TT (Trap Type)	Source
6	0x16	I/O interrupt [2]
5	0x15	I/O interrupt [1]
4	0x14	I/O interrupt [0]
3	0x13	UART 1
2	0x12	UART 2
1	0x11	Internal bus error

I/O interrupts

As an alternate function of the general purpose interface, the AT697 allows to input interrupt from external devices. Up to four external interrupts can be programmed at the same time. The four interrupts are assigned to interrupt 4, 5, 6 and 7.

Each I/O interrupt consists of four fields in the I/O interrupt register (IOIT) : ENx, LEx, PLx and ISELx.

An I/O interrupt is enabled setting logical one the ENx bit in the IOIT register. Setting this bit logical zero disables the interrupt. The ISELx field in the IOIT register defines which port of the general purpose interface should generate I/O interrupt x. The port can be selected from within PIO[15:0] and D[15:0]*.

Each I/O interrupt can have its trigger mode and its polarity individually configured. When the LEx bit is set logical one, the corresponding I/O interrupt is edge triggered. If the polarity bit (PLx) is driven logical one the interrupt triggers when a rising edge is applied on the pin. If the polarity bit is driven logical zero the interrupt triggers when a falling edge is applied on the pin.

When the LEx bit is set logical zero, the corresponding I/O interrupt is level sensitive. If the polarity bit (PLx) is driven logical one the interrupt triggers when a high level is applied on the pin. If the polarity bit is driven logical zero the interrupt triggers when a low level is applied on the pin.

The following table summarizes the I/O interrupt configurations.

Table 10. I/O Interrupt Configuration

LEx	PLx	Trigger
0	0	low level
0	1	high level
1	0	falling edge
1	1	rising edge

Interrupt Priority

The 15 interrupts handled by the AT697 are prioritised, with interrupt 15 (TT = 0x1F) having the highest priority and interrupt 1 (TT = 0x11) the lowest.

It is possible to change the priority level of an interrupt using the two priority levels from the interrupt mask and priority register (ITMP). Each interrupt can be assigned to one of two levels as programmed in the Interrupt mask and priority register. Level 1 has higher priority than level 0. Within each level the interrupts are prioritised.

Cache Memories

Overview

The AT697 processor implements a Harvard architecture with separate instruction and data buses, connected to two independent cache controllers. In order to improve the speed performance of the cpu core, multi-set-caches are used for both instruction and data caches.

The cache replacement policy used for both instruction and data caches is based on the LRU algorithm. The least recently used (LRU) set of the cache is replaced when new data need to be stored in cache.

Cache mapping

Most of the main memory areas can be cached. The cacheable areas are the PROM and RAM areas. The following table presents the caching capabilities of the processor.

Table 11. Cache Capability List

Address Range	Area	Cache status
0x00000000 - 0x1FFFFFFF	PROM	Cached
0x20000000 - 0x3FFFFFFF	I/O	Non-cacheable
0x40000000 -0x7FFFFFFF	RAM	Cached
0x80000000 -0xFFFFFFFF	Internal	Non-cacheable

Operation

During normal operation, the processor accesses instructions and data using ASI 0x8 - 0xB as defined in the SPARC standard.

Using the LDA/STA instructions, alternative address spaces as caches can be accessed. ASI[3:0] are used for the mapping when ASI[7:4] have no influence on operation.

- Access with ASI 0 - 3 will force a cache miss, update the cache if the data was previously cached or allocate a new line if the data was not in the cache and the address refers to a cacheable location.
- Access to ASI 4 and 7 will force a cache miss and update the cache if the data was previously cached.

The following table shows the ASI implementation on the AT697.

Table 12. ASI Usage

ASI	Usage
0x0, 0x1, 0x2, 0x3	Forced cache miss (replace if cacheable)
0x4, 0x7	Forced cache miss (update on hit)
0x5	Flush instruction cache
0x6	Flush data cache
0x8, 0x9, 0xA, 0xB	Normal cached access (replace if cacheable)
0xC	Instruction cache tags
0xD	Instruction cache data
0xE	Data cache tags
0xF	Data cache data

Note: Please refer to the SPARC v8 specification for detailed information on ASI usage.

Instruction Cache

Overview

The AT697 instruction cache is a multi-set cache of 32 kbyte divided in 4 memory sets. Multi-set-cache use improves speed performance of the core. The instruction cache is divided into cache lines with 32 bytes of data. Each line has a cache tag associated with it consisting of a tag field and one valid bit per 4-byte sub-block.

Cache Control

The instruction cache operations are controled with the cache control register (CCR).

Operation

On an instruction cache miss to a cachable location, the instruction is fetched and the corresponding tag and data line updated. The instruction cache always works in one of three modes:

- disabled,
- enabled
- or frozen.

The instruction cache current state is reported in the instruction cache state field (ICS) of the cache controler register (CCR).

Disabled mode

If disabled, no cache operation is performed and load and store requests are passed directly to the memory controller.

Enabled mode

If enabled, the cache operates as described above. In the frozen state, the cache is accessed and kept in synchronisation with the main memory as if it was enabled, but no new lines are allocated on read misses.

Freeze mode

If the freeze on interrupt bit (IF) bit is set logical one on the cache control register (CCR), the instruction cache is frozen when an asynchronous interrupt is taken. This can be beneficial in real-time system to allow a more accurate calculation of worst-case execution time for a code segment. The execution of the interrupt handler will not evict any cache lines and when control is returned to the interrupted task, the cache state is identical to what it was before the interrupt.

If a cache has been frozen by an interrupt, it can only be enabled again by enabling the cache in the CCR. This is typically done at the end of the interrupt handler before control is returned to the interrupted task.

Burst fetch

An instruction burst fetch mode can be enabled setting logical one the burst fetch bit (IB) in the cache control register. If the burst fetch is enabled, the cache line is filled from main memory starting at the missed address and until the end of the line. At the same time, the instructions are forwarded to the IU. If the IU cannot accept the streamed instructions due to internal dependencies or multi-cycle instruction, the IU is halted until the line fill is completed.

If the IU executes a control transfer instruction during the line fill, the line fill will be terminated on the next fetch. If instruction burst fetch is enabled, instruction streaming is enabled even when the cache is disabled. In this case, the fetched instructions are only forwarded to the IU and the cache is not updated.

Cache Flush

Instruction cache can be flushed by executing the FLUSH instruction, setting logical one the flush instruction cache bit (FI) in the cache control register, or writing any location with ASI=0x5. The flush operation takes one cycle per line during which the IU will is not halted, but during which the cache is disabled. When the flush operation is completed, the cache will resume the state indicated in the cache control register.

Error reporting

If a memory access error occurs during a line fill with the IU halted, the corresponding valid bit in the cache tag is not set. If the IU later fetches an instruction from the failed address, a cache miss will occur, triggering a new access to the failed address.

If the error remains, an instruction access error trap (tt=0x1) is generated.

Instruction Cache Parity

Error detection of cache tags and data is implemented using two parity bits per tag and per 4-byte data sub-block. The tag parity is generated from the tag value and the valid bits. The data parity is derived from the sub-block data. The parity bits are written simultaneously with the associated tag or sub-block and checked on each access. The two parity bits correspond to the parity of odd and even data (tag) bits.

If a tag parity error is detected during a cache access, a cache miss is generated. The tag and the data are automatically updated. All valid bits except the one corresponding to the newly loaded data are cleared. Each error is reported in the instruction cache tag error counter from the CCR. The instruction cache tag error counter (ITE) is incremented after each instruction cache tag error detection.

If a data sub-block parity error occurs, a miss is also generated but only the failed sub-block is updated with data from main memory. Each error is reported in the instruction cache data error counter from the CCR. The instruction cache data error counter (IDE) is incremented after each instruction cache data error detection.

Data Cache

Overview

The AT697 data cache is a multi-set cache of 16 kbyte divided in 2 memory sets. Multi-set-cache use improves speed performance. The data cache is divided into cache lines with 16 bytes of data. Each line has a cache tag associated with it consisting of a tag field and one valid bit per 4-byte sub-block.

Cache Control

The instruction cache operations are controled with the cache control register (CCR).

Operation

Write

The write policy for stores is write-through with no-allocate on write-miss. The write buffer (WRB) consists of three 32-bit registers used to temporarily hold store data until it is sent to the destination device. For half-word or byte stores, the stored data replicated into proper byte alignment for writing to a word-addressed device, before being loaded into one of the WRB registers.

The WRB is emptied prior to a load-miss cache-fill sequence to avoid any stale data from being read in to the data cache.

Read

On a data cache read-miss to a cachable location, 4 bytes of data are loaded into the cache from main memory.

Cache Flush

Data cache can be flushed by executing the FLUSH instruction, setting logical one the flush data cache bit (FD) in the cache control register, or writing any location with ASI=0x6. The flush operation takes one cycle per line during which the IU will is not halted, but during which the cache is disabled. When the flush operation is completed, the cache will resume the state indicated in the cache control register.

Error Reporting

Since the processor executes in parallel with the write buffer, a write error will not cause an exception to the store instruction. Depending on memory and cache activity, the write cycle may not occur until several clock cycles after the store instructions has completed. If a write error occurs, the currently executing instruction will take trap 0x2B.

Note: the 0x2B trap handler should flush the data cache, since a write hit would update the cache while the memory would keep the old value due the write error.

If a memory access error occurs during a data load, the corresponding valid bit in the cache tag will not be set. and a data access error trap (tt=0x09) is generated.

Data Cache Parity

Error detection of cache tags and data is implemented using two parity bits per tag and per 4-byte data sub-block. The tag parity is generated from the tag value and the valid bits. The data parity is derived from the sub-block data. The parity bits are written simultaneously with the associated tag or sub-block and checked on each access. The two parity bits correspond to the parity of odd and even data (tag) bits.

If a tag parity error is detected during a cache access, a cache miss is generated. The tag and the data are automatically updated. All valid bits except the one corresponding to the newly loaded data are cleared. Each error is reported in the instruction cache tag error counter from the CCR. The data cache tag error counter (DTE) is incremented after each data cache tag error detection.

If a data sub-block parity error occurs, a miss is also generated but only the failed sub-block is updated with data from main memory. Each error is reported in the data cache data error counter from the CCR. The data cache data error counter (DDE) is incremented after each data cache data error detection.

Data Cache Snooper

In addition to the cache controller, a snooper is implemented on the on-chip cache subsystem. The cache snooper is enabled setting logical one the snoop enable bit (DS) in the cache control register.

This snooper is able to verify if a master on the internal bus accesses and modifies some cached data. If a master accesses a data in memory and this data is cached, the snooper will invalidate the corresponding cache tag. Next time the IU will access the modified data, a cache miss will be generated due to not valid tag.

Diagnostic Cache Access

Tags and data in the instruction and data cache can be accessed through ASI address space 0xC, 0xD, 0xE and 0xF by executing LDA and STA instructions. Address bits making up the cache offset will be used to index the tag to be accessed while the least significant bits of the bits making up the address tag will be used to index the cache set.

Diagnostic read of tags is possible by executing an LDA instruction with ASI=0xC for instruction cache tags and ASI=0xE for data cache tags. The cache line and the cache set are indexed by the address bits making up the cache offset and the least significant bits of the address bits making up the address tag.

Similarly, the data sub-blocks may be read by executing an LDA instruction with ASI=0xD for instruction cache data and ASI=0xF for data cache data. The sub-block to be read in the indexed cache line and set is selected by A[4:2].

The tags can be directly written by executing a STA instruction with ASI=0xC for the instruction cache tags and ASI=0xE for the data cache tags. The cache line and cache set are indexed by the address bits making up the cache offset and the least significant bits of the address bits making up the address tag.

D[31:10] is written into the ATAG filed and the valid bits are written with the D[7:0] of the write data. The data sub-blocks can be directly written by executing a STA instruction with ASI=0xD for the instruction cache data and ASI=0xF for the data cache data. The sub-block to be read in the indexed cache line and set is selected by A[4:2].

Note: Diagnostic access to the cache is not possible during a FLUSH operation and will cause a data exception (trap=0x09) if attempted.

Memory Interface

Overview

The AT697 provides a 32-bit bus capable to interface PROM, memories mapped I/O devices, asynchronous static rams (SRAM) and synchronous dynamic rams (SDRAM). The memory bus can be configured either for 8-bit, 16-bit, 32-bit or 40-bit accesses. The memory controller manages up to 2 Gbytes of external memory. The following table presents the memory controller address map.

Table 13. Memory Controller address map

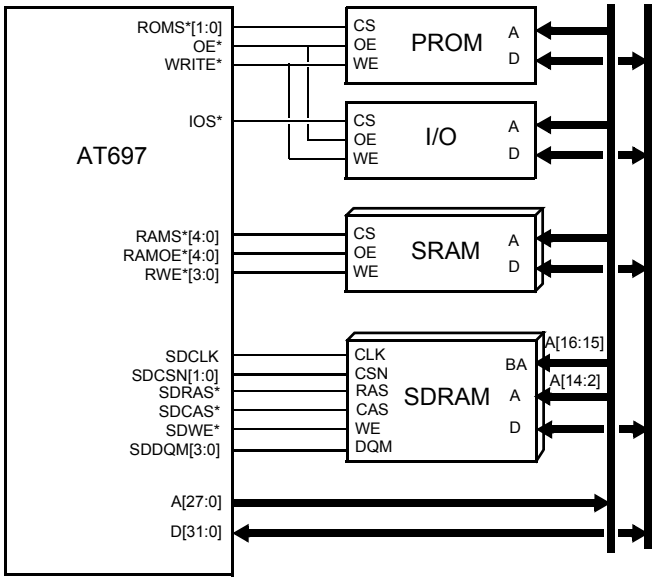
Address Range	Size	Mapping
0x00000000 - 0x1FFFFFFF	512M	PROM
0x20000000 - 0x2FFFFFFF	256M	I/O
0x40000000 - 0x7FFFFFFF	1G	SRAM/SDRAM

For applications that require smaller memory areas and/or smaller performances, it is possible to configure some memory spaces as 8-bit or 16-bit wide data bus.

All the configuration of the memory interface is done through the three memory controller registers : MCFG1, MCFG2 and MCFG3. MCFG1 is the register dedicated to PROM and IO configuration. SRAM and SDRAM are configured through MCFG2 and MCFG3.

Here is an overview of the 32-bit interconnection between the AT697 and external memories.

Figure 8. Memory Interface Overview



To improve the bandwidth of the memory bus, accesses to consecutive addresses can be performed in burst mode. Burst transfers will be generated when the memory controller is accessed using a burst request from the internal bus. These includes instruction cache-line fills, double loads and double stores. The timing of a burst cycle is identical to the programmed basic cycle with the exception that during read cycles, the lead-out cycle will only occurs after the last transfer.

RAM Interface

The memory controller gives the capability to control up to 1Gbyte of RAM. The global RAM area supports two RAM types : asynchronous static RAM (SRAM) and synchronous dynamic RAM (SDRAM).

SRAM interface

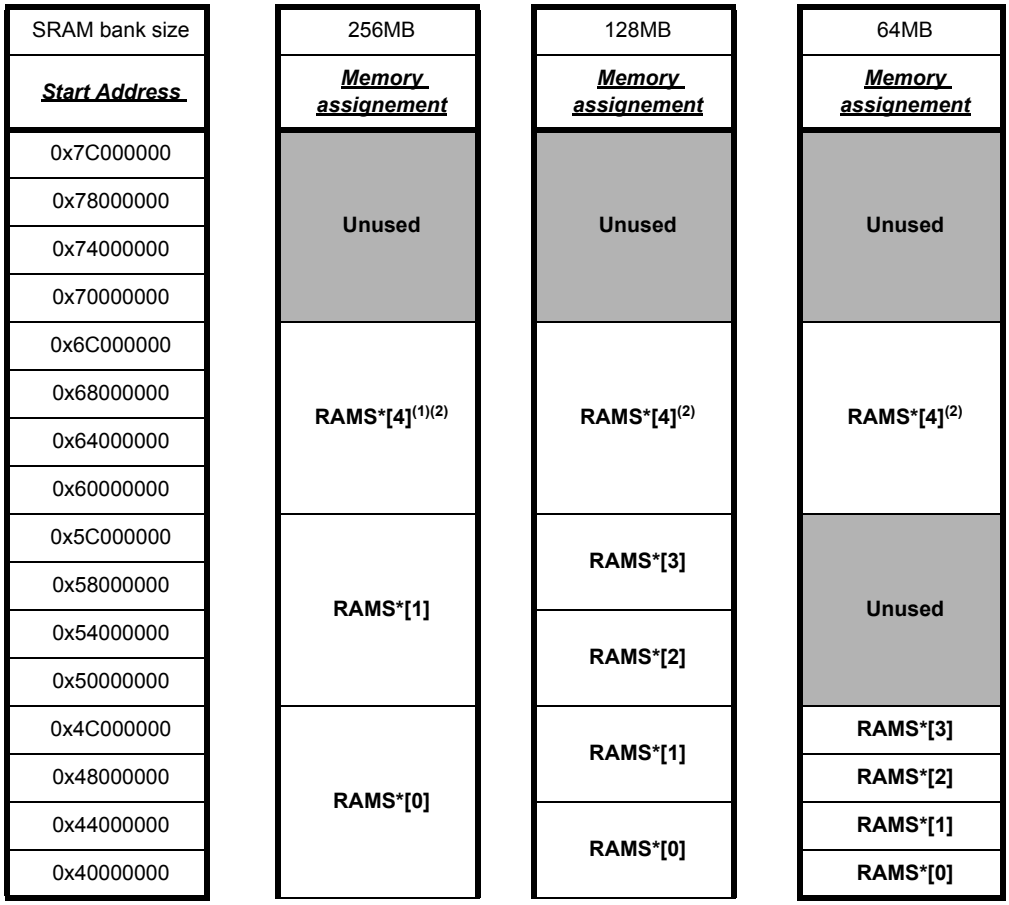
Overview

The SRAM interface can manage up to five SRAM banks. The control of the SRAM memory accesses uses a standard set of pin, including chip selects (RAMS*x), output enable (RAMOE*x) and write enable (RWE*x) lines.

The bank size of the four first banks of the SRAM area can be configured by setting the value of the SRAM bank size field in MCFG2. The bank size can be programmed in binary step from 8 Kbytes to 256 Mbytes. Whatever is the size of the four first banks, they are always contiguous. These memory banks are selected with RAMS*[3] down to RAMS*[0].

The fifth SRAM bank controlled by RAMS*[4] has a fix dimension. This bank always resides at the upper address 0x60000000. This bank is always 256 Mbytes large.

Figure 9. SRAM bank organisation



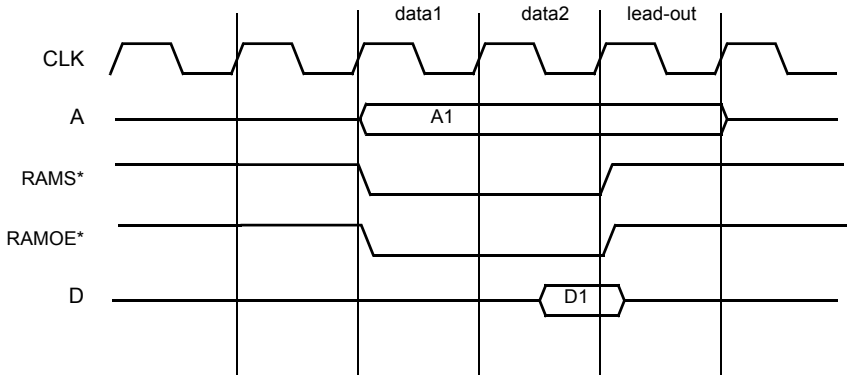
Notes:
1. If the SRAM bank size is set to 256Mbytes, SRAM bank 2 & bank 3 are in overlay with SRAM bank 4. In this case, bank 2 and bank 3 control signals are never asserted. Bank 4 has the priority.
2. When SDRAM is enabled, priority is given to the SDRAM. Any access to addresses higher than 0x60000000 is driven to SDRAM. No SRAM control is activated.

SRAM Read Access

A read access to SRAM consists in two data cycles and between zero and three wait-states. On non-consecutive accesses, a lead-out cycle is added after a read cycle to prevent bus contention due to slow turn-off time of memories or I/O devices. On consecutive accesses, no lead-out cycle is performed between the acesses but only one is performed at the end of the operations (RAMSN and RAMOE are not deasserted).

When a read access to SRAM is performed, a separate output enable signal is provided for each SRAM bank and it is only asserted when that bank is selected.

Figure 10. SRAM read cycle (0-waitstate)

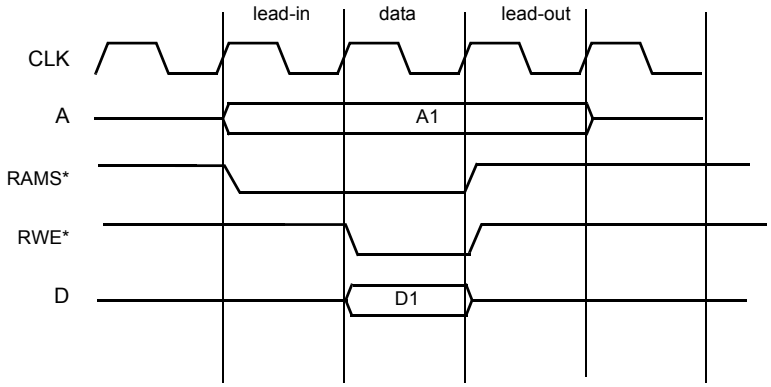


SRAM Write Access

Each byte lane has an individual write strobe (RAMWE*) to allow efficient byte and half-word writes.

Each write access to SRAM consists of three cycles and between zero and three wait-states. The three mandatory cycles are divided in one write setup cycle, one data cycle and one lead-out cycle.

Figure 11. SRAM write cycle (0-waitstate)



If the external memory use a common write strobe for the full 16- or 32-bit data, set the read-modify-write bit MCFG2. This will enable read-modify-write cycles for sub-word writes.

Waitstates

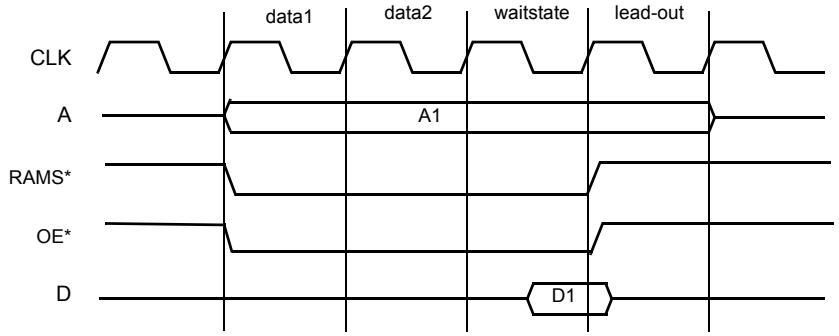
For application using slow SRAM memories, the SRAM controller provides the capability to insert wait-states during the SRAM accesses. Two types of wait-states can be inserted :

- Programmed delay, available for bank 0 up to bank 3

- ‘Hardware’ delay, available for bank 4 only

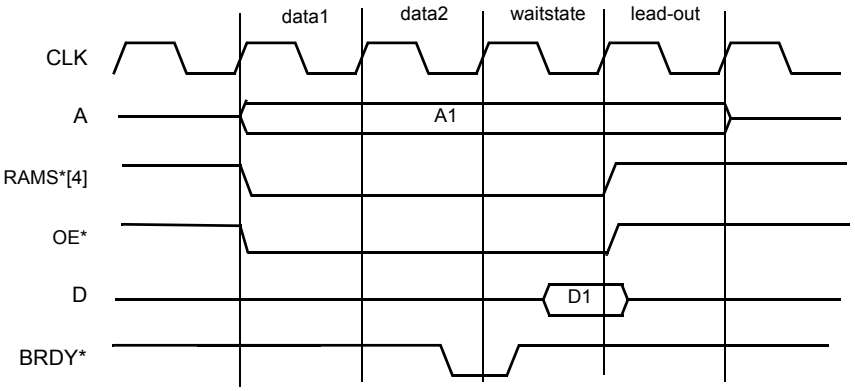
Up to three waitstates can be programmed for SRAM accesses. Read and write wait-states can be individually programmed. Setting the RAMRWS value in MCFG2 register defines the number of waitstates to insert during an SRAM read. Setting the RAMWWS value in MCFG2 register defines the number of waitstates to insert during an SRAM write.

Figure 12. RAM read access with one programmed waitstate



If the application needs more delay during the SRAM transfer, it is possible to introduce more delay by activating the hardware bus ready (BRDY*) detection in MCFG2. If the BRDY bit is driven logical one on MCFG2 and the BRDY* pin is set high, the processor wait before ending the transfer. As soon as the BRDY* pin is driven low, the processor ends the access. If the BRDY bit is driven logical zero on MCFG2, no additional delay is inserted.

Figure 13. RAM read access with one BRDY* controlled waitstate

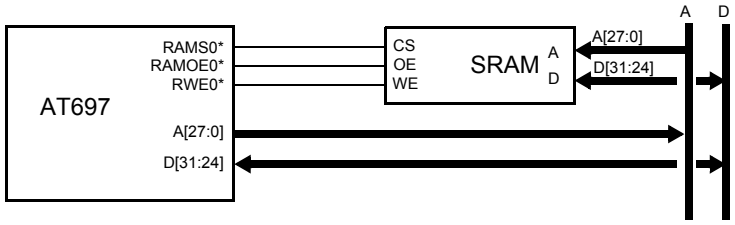


Bus width

To support applications with low memory and performance requirements, the SRAM area can be configured for 8-bit operations. The configuration of SRAM in 8-bit mode is done programming the SRAM bus width field in he memory configuration registers MCFG2.

When the SRAM bus is configured as an 8-bit wide bus, data 31 downto 24 shall be used as interface.

Figure 14. SRAM 8-bit bus width connection

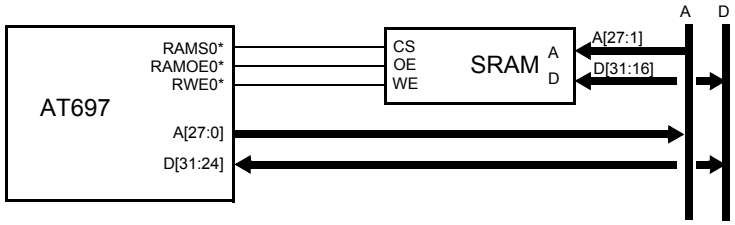


Since access to memory is always done on 32-bit word basis, read access to 8-bit memory will be transformed in a burst of four read cycles. If EDAC protection is active, 5 read cycles are necessary to complete the access (please refer to “Error Management - EDAC” on page 41 for more details). During write operation, only the necessary bytes are writen.

In addition to the 8-bit mode, the SRAM area can be configured for 16-bit accesses. In this configuration, the SRAM device is accessed with a burst of two 16-bit accesses. No EDAC protection can be used with suh configuration.

When the bus is configured as an 16-bit wide bus, data 31 downto 16 shall be used as interface.

Figure 15. SRAM 16-bit bus width connection



Write Protection

Write protection is provided to prevent accidental over-writing to the RAM area. Two block protection units are available for RAM area. Each one is controlled through a write protection register (WPRn). Two major fields are defined : a TAG and a MASK.

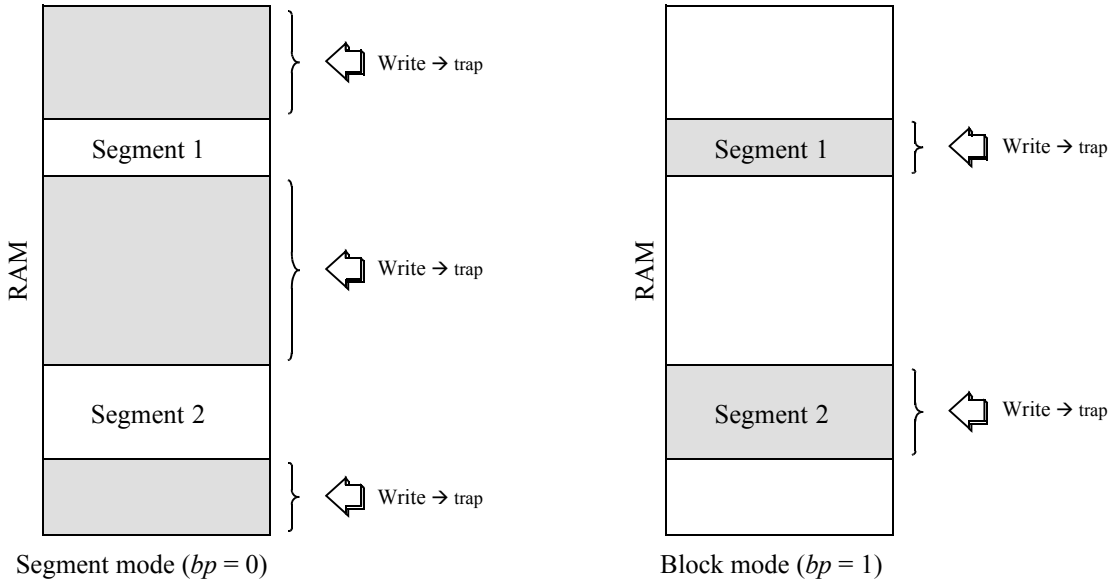
- The TAG defines the 15 most significant bits of the address of the block to be write protected.
- The Mask specifies which bits of the TAG are really relevant for the protection.

Operation

The write protection on the RAM area is enabled setting logical one the enable bit (EN) in the write protect register (WPRn). If this bit is set logical zero, no protection is activated.

Two protection modes can be programmed. If the block protect bit (BP) of the write protect register (WPRn) is set logical one the protection is active within the segment. If the BP bit is set logical zero, the exterior of the segment is protected.

Figure 16. RAM Protection Mode Overview



To detect if the written address is part of a protected segment (or block), address bit 29 down to bit 2 are Xored with the TAG field from the write protect register. This operation is based on the following segmentation of an address.

Table 14. Address Segmentation

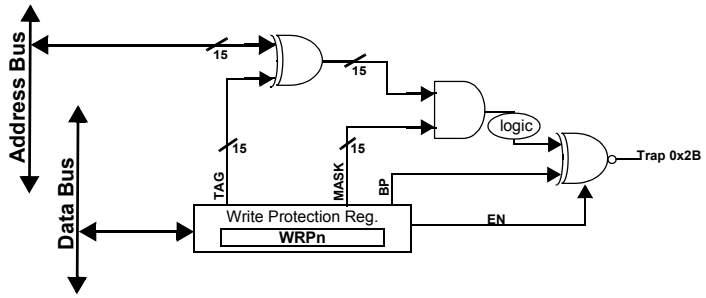
bit num.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
field	area		most significant byte															32Kbyte protected block														

With such segmentation, memory block in the range of 32Kbyte up to 1Gbyte can be protected.

The result of the Xor is then Anded with the MASK field of the write protect register.

If the result is zero, this indicates that address specified is in the protected range. If result is different from zero, address is out of the protected address range. If a write protection error is detected, the write cycle is stopped. Then, a memory access error is generated. Trap 0x2B is generated

Figure 17. RAM Write Protection Overview



SDRAM

The synchronous dynamic RAM interface can manage up to two SDRAM banks. The control of the SDRAM memory accesses uses a standard set of pin, including chip selects (SDCS*x), write enable (SDWE*), data masks (SDDQM*x) and clock lines.

The bank size of the two SDRAM banks can be configured by setting the value of the SDRAM bank size field in MCFG2. The bank size can be programmed in binary step from 4 Mbytes to 512 Mbytes.

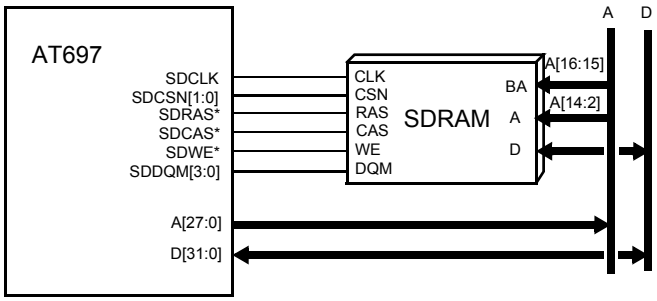
The controller supports 64M, 256M and 512M devices with 8 to 12 column-address bits, up to 13 row-address bits, and 4 banks. Only 32-bit data bus width is supported for SDRAM banks.

Address Mapping

The start address for the SDRAM banks depends upon the SRAM use in the application. If the the SRAM disable bit (SI) and the SDRAM enable bit (SE) are set logical one in the memory configuration register (MCFG2), the SDRAM start address is 0x40000000. If the the SRAM disable bit (SI) is set logical zero and the SDRAM enable bit (SE) is set logical one in the memory configuration register (MCFG2), the SDRAM start address is 0x60000000. If SE if set logical zero, no SDRAM can be used.

The address bus of the SDRAMs shall be connected to A[14:2], the bank address to A[16:15]. Devices with less than 13 address pins should only use the less significant bits of A[14:2].

Figure 18. SDRAM connection overview



SDRAM Timing Parameters

To provide optimum access cycles for different SDRAM devices some SDRAM parameters can be programmed through memory configuration register 2. The programmable SDRAM parameters are the following :

Table 15. SDRAM Programmable Timing Parameters

Function	Parameter	Range	Unit
CAS latency		2 - 3	clocks
Precharge to activate	t_{RP}	2 - 3	clocks
Auto-refresh command period	t_{RFC}	3 - 11	clocks
Auto-refresh interval		10 - 32768	clocks

SDRAM Commands

The SDRAM controller can issue three SDRAM commands. Commands to be executed are programmed through the SDRAM command field in the memory configuration register (MCFG2). When this field is writen with a non zero value, a SDRAM command is issued :

- if set to ‘01’, Precharge command is sent,
- if set to ‘10’, Auto-Refresh command is sent,
- if set to ‘11’, Load Mode Reg (LMR) is sent.

When the LMR command is issued, the CAS delay programmed in MCFG2 is used. The command field is cleared after a command is executed. When changing the value of the CAS delay, a LOAD-MODE-REGISTER command should be generated at the same time.

The SDRAM controller also provides a refresh command. It can be enabled by setting logical one the refresh enable bit (SDRREF) in the memory configuration register.

The Auto-Refresh command enables a periodical refresh for both SDRAM banks. The period between two Auto-Refresh command is programmed in the refresh counter reload field of the third memory configuration register (MCFG3).

Depending on SDRAM type, required period is typically 7.8 or 15.6µs. This corresponds to 780 or 1560 clock cycle at 100MHz.

Refresh period is calculated as $\text{Refresh Period} = \frac{\text{Reload value} + 1}{\text{sysclk}}$

SDRAM Initialisation

After reset, the SDRAM controller automatically performs the SDRAM initialisation sequence. It consists in PRECHARGE, two AUTO-REFRESH cycles and LOAD-MODE-REG on both banks simultaneously.
The controller programs the SDRAM to use page burst on read and single location access on write. A CAS latency of 3 is programmed by default. This value can be updated later by software.

SDRAM Read Access

A read cycle consists in three main operation. First, an ACTIVATE command to the desired bank and row is performed. Then, after the programmed CAS delay, a READ command is sent. The read cycle is terminated with a PRE-CHARGE command. No bank is left open between two accesses.

A burst read is performed if a burst access is requested on the internal bus.

SDRAM Write Access

A write cycles consists in three main operations. First, an ACTIVATE command to the desired bank and row is performed. Then, a WRITE command is sent. The write cycle is terminated with the PRE-CHARGE command.

A burst write on the internall bus generates a burst of write commands without idle cycles in-between.

Access Error

An access error can be indicated to the processor asserting the BEXC* signal. If enabled by setting logical one the BEXC* bit in the memory configuration register 1, the BEXC* signal is sampled with the data.

If the BEXC* signal is driven low by the external device during the access, an error response is generated on the internal bus.

- Trap 0x01 is taken if an instruction fetch is in progress
- Trap 0x09 is taken if a data space is in progress
- Trap 0x2B is taken if a data store is in progress

PROM Interface

Overview

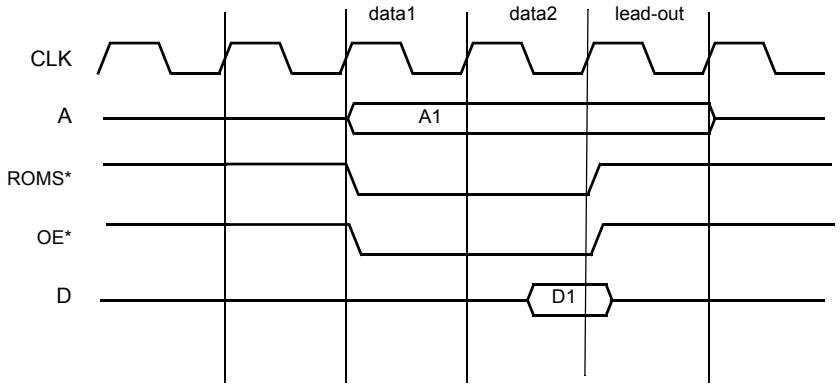
The memory controller give the capability to control up to 512Mbyte of PROM. The PROM interface can manage up to two PROM banks. The control of the PROM memory accesses uses a standard set of pin, including chip selects (ROMS*x), output enable (OE*), read (READ) and write (WRITE*) lines.

The bank size of the PROM banks is not programmable. The lower half part of the PROM area (0x00000000 up to 0x0FFFFFFF) is controlled by the ROMS0* PROM select signal. The upper half part of the PROM area (0x10000000 up to 0x1FFFFFFF) is controlled by the ROMS1* PROM select signal.

PROM Read Access

A read access to PROM consists in two data cycles and waitstates if any programmed. On non-consecutive accesses, a lead-out cycle is added after a read cycle to prevent bus contention due to slow turn-off time of memories or I/O devices. On consecutive accesses, no lead-out cycle is performed between the acesses but only one is performed at the end of the operations.

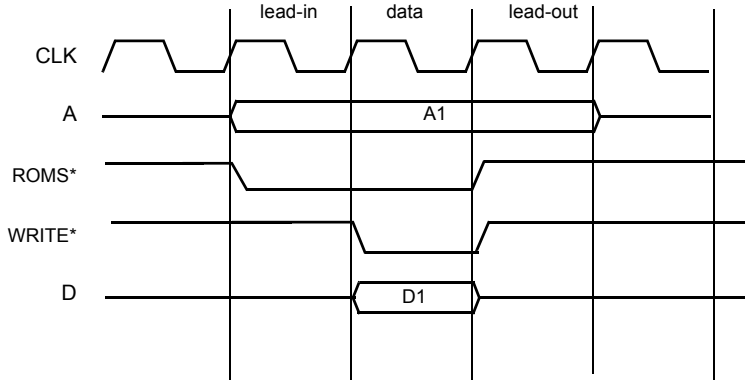
Figure 19. PROM Read Cycle (0 Waitstate)



PROM Write Access

Each write access to PROM consists of three cycles and of waitstates if any programmed. The three mandatory cycles are divided in one write setup cycle, one data cycle and one lead-out cycle. The write operation is strobed by the WRITE* signal.

Figure 20. PROM Write Cycle (0 waitstate)



Waitstates

For application using slow PROM memories, the PROM controller provides the capability to insert wait-states during the accesses. Two types of wait-states can be inserted :

- Programmed delay,
- ‘Hardware’ delay.

Up to 30 waitstates can be programmed for PROM accesses. Read and write waitstates can be individually programmed. Setting the PRRWS value in MCFG1 register defines the number of waitstates to insert during a PROM read access. Setting the PRWWS

value in MCFG1 register defines the number of waitstates to insert during a PROM write.

PRRWS and PRWWS field can be programmed to take values from 0 up to 15. The effective number of waitstates applied during an access is then twice the programmed value. In that way, programming two waitstates result in the insertion of four wait cycles during the access.

If the application needs more delay during the PROM access, it is possible to introduce more delay acting on the bus ready line (BRDY*). If the BRDY* pin is set high, the processor wait before ending the transfer. As soon as the BRDY* pin is driven low, the processor ends the access.

After a reset operation of the processor (or at power up), the read and write waitstates fields for the PROM area are set default to 15, resulting in 30 effective waitstates.

Write Protection

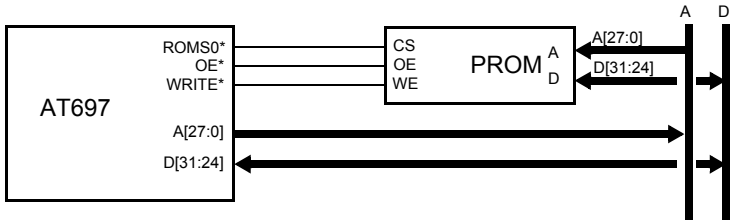
Write protection is provided to prevent accidental over-writing to PROM area. It is controlled through the PROM write enable bit (PRWE*) from the memory configuration register 1. When set 1, this bit enables write to PROM. When set 0, no PROM write cycle is available.

Bus width

To support applications with low memory and performance requirements, the PROM area can be configured for 8-bit operations. The configuration of PROM in 8-bit mode is done programming the ROM bus width field in he memory configuration registers MCFG1.

When the PROM bus is configured as an 8-bit wide bus, data 31 downto 24 shall be used as interface.

Figure 21. PROM 8-bit bus width connection

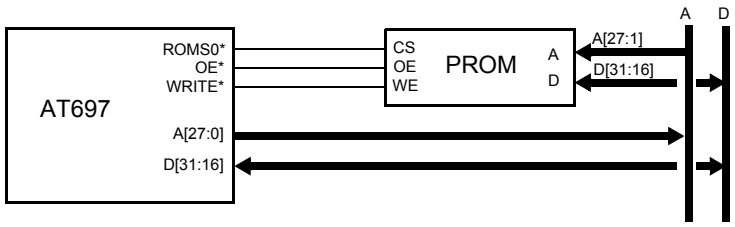


Since access to memory is always done on 32-bit word basis, read access to 8-bit memory will be transformed in a burst of four read cycles. If EDAC protection is active, 5 read cycles are necessary to complete the access (please refer to protection section for more details). During write operation, only the necessary bytes are writen.

In addition to the 8-bit mode, the PROM area can be configured for 16-bit accesses. In this configuration, the PROM device is accessed with a burst of two 16-bit accesses. No EDAC protection can be used with suh configuration.

When the bus is configured as an 16-bit wide bus, data 31 downto 16 shall be used as interface.

Figure 22. PROM 16-bit bus width connection



During power-up or reset operation, the PROM bus width field in MCFG1 is set with the value of PIO[1:0] inputs.

Access Error

An access error can be indicated to the processor asserting the BEXC* signal. If enabled by setting logical one the BEXC* bit in the memory configuration register 1, the BEXC* signal is sampled with the data.

- Trap 0x01 is taken if an instruction fetch is in progress
- Trap 0x09 is taken if a data space is in progress
- Trap 0x2B is taken if a data store is in progress

Memory Mapped I/O

Overview

The memory controller give the capability to control up to 256Mbyte of I/O. The I/O area consists in a single large bank. The control of the I/O area accesses uses a standard set of pin, including chip selects (IOS*x), output enable (OE*), read (READ) and write (WRITE*) lines.

The size of the I/O bank is not programmable. The entire I/O area (0x20000000 up to 0x2FFFFFFF) is controlled by the IOS* select signal.

I/O Read Access

A read access to I/O consists in a lead-in cycle, two data cycles, waitstates if any programmed and a lead-out cycle. On non-consecutive accesses, the lead-out cycle is used to prevent bus contention due to slow turn-off time of memories or I/O devices. On consecutive accesses, no lead-out cycle is performed between the acesses but only one is performed at the end of the operations.

The I/O select signal (IOSEL*) is delayed one clock to provide stable address.

Figure 23. single I/O read cycle with lead-out

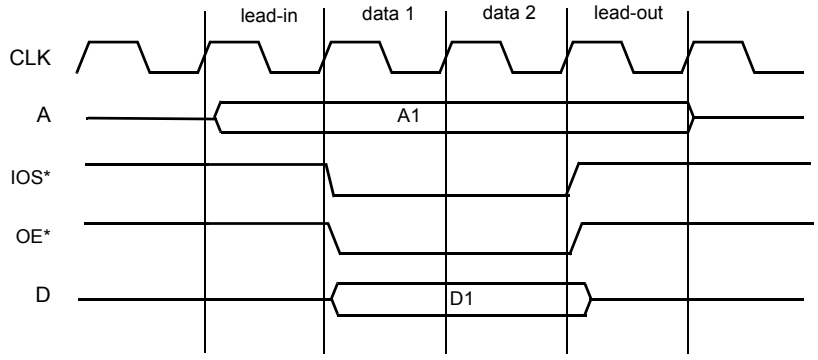
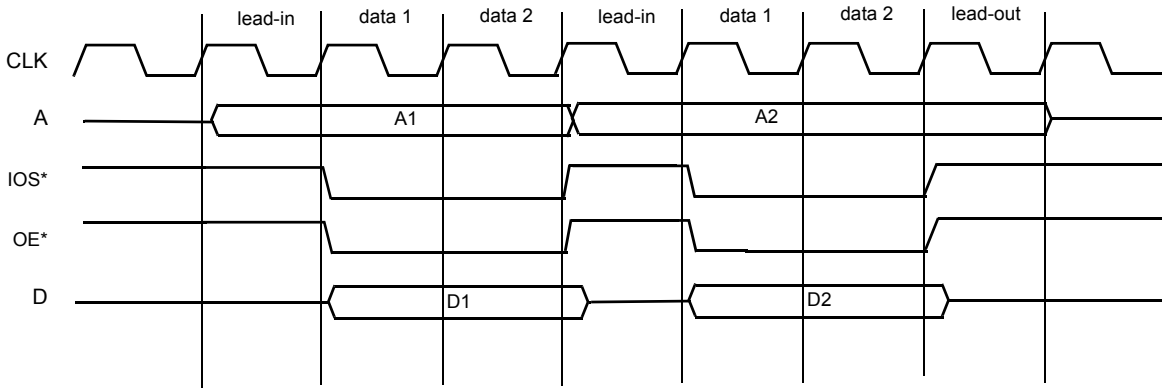


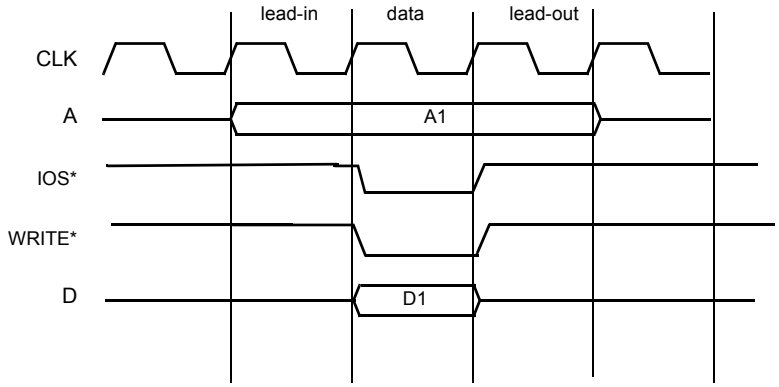
Figure 24. consecutive I/O read cycles without lead-out



I/O Write Access

Each write access to I/O consists of three cycles and of waitstates if any programmed. The three mandatory cycles are divided in one write setup cycle, one data cycle and one lead-out cycle. The write operation is strobed by the WRITE* signal.

Figure 25. I/O write cycle



Waitstates

For application using slow I/O devices, the I/O controller provides the capability to insert wait-states during the accesses. Two types of wait-states can be inserted :

- Programmed delay,
- 'Hardware' delay.

Up to 15 waitstates can be programmed for I/O accesses. Read and write waitstates are programmed simultaneously. Setting the IOWS field value in MCFG1 register defines the number of waitstates to insert during any access to/from I/O areas. IOWS field can be programmed to take values from 0 up to 15.

If the application needs more delay during the I/O access, it is possible to introduce more delay acting on the bus ready line (BRDY*). If the bus ready bit (BRDY*) is set logical one in MCFG1 and BRDY* pin is set high, the processor wait before ending the transfer. As soon as the BRDY* pin is driven low, the processor ends the access.

Write Protection

Read and write protections are provided to prevent accidental accesses to I/O area. Protection is controlled through the I/O protection ‘iop’ bit from the memory configuration register 1.

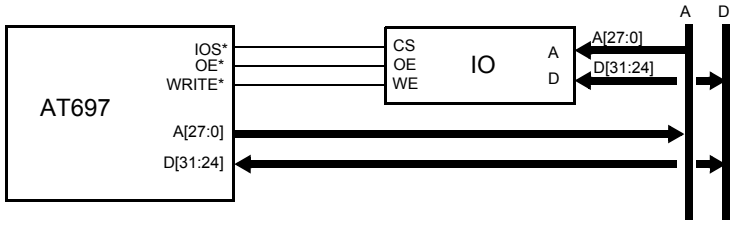
Bus width

To support applications with low memory and performance requirements, I/O area can be configured for 8-bit operations. The configuration of I/O in 8-bit mode is done programming the I/O bus width field in he memory configuration registers MCFG1.

In such configuration, I/O device is not accessed by multiple 8-bit accesses as other memory areas. Only one single access is performed

When the I/O bus is configured as an 8-bit wide bus, data 31 downto 24 shall be used as interface.

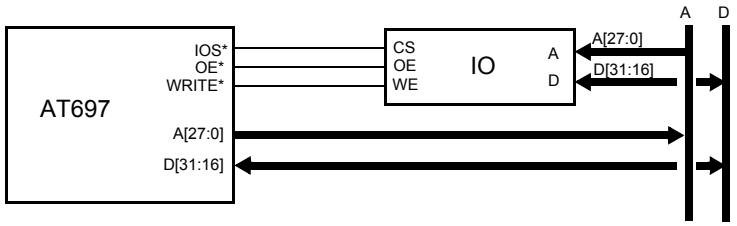
Figure 26. I/O 8-bit bus width connection



In addition to the 8-bit mode, the I/O area can be configured for 16-bit accesses. In such configuration, I/O device is not accessed by multiple 8-bit accesses as other memory areas. Only one single access is performed.

When the bus is configured as an 16-bit wide bus, data 31 downto 16 shall be used as interface.

Figure 27. I/O 16-bit bus width connection



Access Error

An access error can be indicated to the processor asserting the BEXC* signal. If enabled by setting logical one the BEXC* bit in the memory configuration register 1, the BEXC* signal is sampled with the data.

- Trap 0x01 is taken if an instruction fetch is in progress
- Trap 0x09 is taken if a data space is in progress
- Trap 0x2B is taken if a data store is in progress

Error Management - EDAC

Overview

The AT697 processor implements an on-chip error detector and corrector (EDAC). The on-chip memory EDAC can correct one error in a 32-bit word and detect two errors in a 32-bit word. The processor EDAC implemention enables data correction on-the-fly so that no timing penalty occurs during correction.

EDAC capability mapping

Data error management with the EDAC can be used on both PROM and RAM memory areas. The following table presents the EDAC protection capabilities provided by the processor.

Table 16. EDAC capability on Memories

Address Range	Area		EDAC Protected
0x00000000 - 0x1FFFFFFF	PROM	8 bits	yes
		16 bits	no
		32 bits	yes
0x20000000 - 0x3FFFFFFF	I/O	All	no
0x40000000 - 0x7FFFFFFF	RAM	8 bits	yes
		16 bits	no
		32 bits	yes

PROM protection

Setting logical one the PROM EDAC enable bit (PE) in the memory configuration register MCFG3, the data protection is enabled. For each read and write cycle to the PROM area the EDAC act as an error detector and an error corrector. When set logical zero, the EDAC is transparent for the PROM access.

At power-on or at reset, the value of the PE bit is directly copied from the PIO2 pin. In that way, it is possible to start the application with the EDAC enabled by driving high PIO2 during the power-on sequence (or reset sequence).

RAM protection

Setting logical one the RAM EDAC enable bit (RE) in the memory configuration register MCFG3, the data protection is enabled. For each read and write cycle to the RAM area the EDAC act as an error detector and an error corrector. When set logical zero, the EDAC is transparent for the RAM access.

Operation

The processor uses an EDAC based on a seven bit Hamming code that detects any double error on a 32-bit bus and corrects any single error on a 32-bit bus.

Hamming code

For each 32-bit data, a seven bit a 7-bit checksum is generated. The equations below show how the Hamming checkbits (CBx) are generated:

CB0 = D0 ^ D4 ^ D6 ^ D7 ^ D8 ^ D9 ^ D11 ^ D14 ^ D17 ^ D18 ^ D19 ^ D21 ^ D26 ^ D28 ^ D29 ^ D31

CB1 = D0 ^ D1 ^ D2 ^ D4 ^ D6 ^ D8 ^ D10 ^ D12 ^ D16 ^ D17 ^ D18 ^ D20 ^ D22 ^ D24 ^ D26 ^ D28

$\overline{CB2}$ = D0 ^ D3 ^ D4 ^ D7 ^ D9 ^ D10 ^ D13 ^ D15 ^ D16 ^ D19 ^ D20 ^ D23 ^ D25 ^ D26 ^ D29 ^ D31

$\overline{CB3}$ = D0 ^ D1 ^ D5 ^ D6 ^ D7 ^ D11 ^ D12 ^ D13 ^ D16 ^ D17 ^ D21 ^ D22 ^ D23 ^ D27 ^ D28 ^ D29

CB4 = D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D14 ^ D15 ^ D18 ^ D19 ^ D20 ^ D21 ^ D22 ^ D23 ^ D30 ^ D31

CB5 = D8 ^ D9 ^ D10 ^ D11 ^ D12 ^ D13 ^ D14 ^ D15 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31

CB6 = D0 ^ D1 ^ D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31

Write operation

When the processor performs a write operation to a memory protected by the EDAC, it also output the seven bit checksum on the CB[6:0] pins.

Read operation

During a read operation from a protected memory, the seven bit checksum is sampled from the CB[6:0] inputs. Then, the EDAC verify the checksum to check the presence of an error.

According to the checksum equations, the EDAC calculates its own checksum. Then a syndrome generator uses the calculated and the read checksum to qualify if there is no error, one error or two errors in the read word.

Correctable error

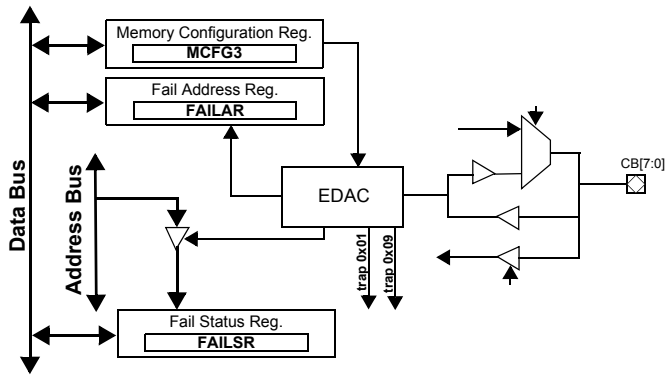
If a single error is detected, this leads to a correctable error. The correction is done on-the-fly during the current access and no timing penalty is induced. The read-modify-write bit (RMW) in MCFG2 shall be set to enable write back of the corrected data.

The correctable error detection event is reported in the fail address register (FAILAR) and in the fail status register (FAILSR). If unmasked, interrupt 1 (trap 0x11) is generated.

Uncorrectable error

If a double error is detected, this leads to an un-correctable error. An un-correctable error detection during a data access leads to a data access exception (trap 0x09). In case the double error is detected during instruction fetch, it leads to an instruction access error (trap 0x01).

Figure 28. EDAC overview



EDAC on 8-bit areas

EDAC protection on a memory configured in 8-bit mode is also possible but, the EDAC checksum bus (CB[7:0]) is not used. The protection is done by allocating the top 25% of the memory bank to the EDAC checksums.

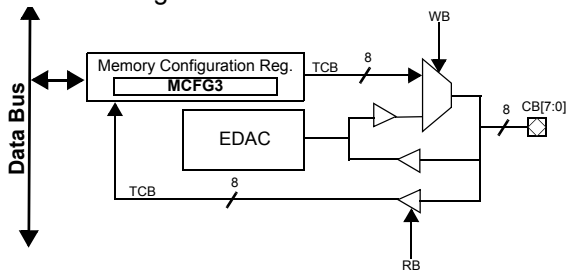
If the EDAC is enabled, a read access will read the data bytes from the nominal address, and the EDAC checksum from the top part of the bank. A write cycle is performed the same way. The memory assignement is then :

- 75% of the bank memory available as program or data memory,
- 18.75% used for checkbits
- 6.25% unused.

EDAC testing

The operation of the EDAC can be tested trough the MCFG3 memory configuration register.

Figure 29. EDAC testing overview



Write test

If the write bypass bit (WB) from MCFG3 is set logical one, the value of the test checksum from the TCB field replaces the normal checkbits during memory write cycles.

Read test

During memory read cycles, if the read bypass bit (RB) from MCFG3 is set logical one, the memory checkbits of the loaded data is stored to the test checkbit field (TCB) of MCFG3 .

Timer Unit

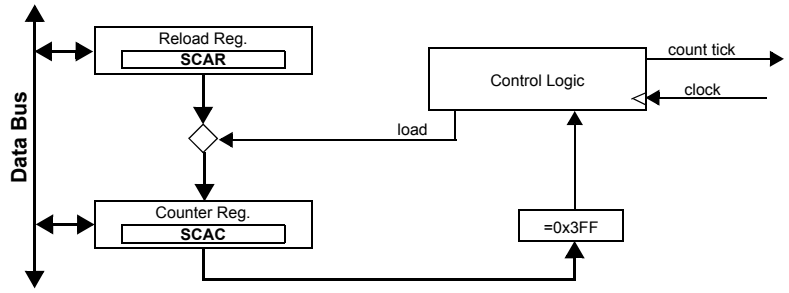
Prescaler

Timer/Counter1, Timer/Counter2 and the watchdog share the same prescaler.

The prescaler consists of a 10-bit down counter clocked by the system clock. The prescaler is decremented on each clock cycle. When the prescaler underflows, it is automatically reloaded with the content of the prescaler reload register. A count tick is generated for the two timers and the watchdog.

The effective division rate is equal to **prescaler reload register value + 1**.

Figure 30. Prescaler Block Diagram



Caution :

The two timers and watchdog share the same decrementer. The minimum allowed prescaler division factor is 4 (reload register = 3).

Timer/Counter 1 & Timer/Counter 2

Timer/Counter1, Timer/Counter2 are two general purpose 24-bit timers. They share the same decrementer. The timer value is then decremented each time the prescaler generates a timer pulse.

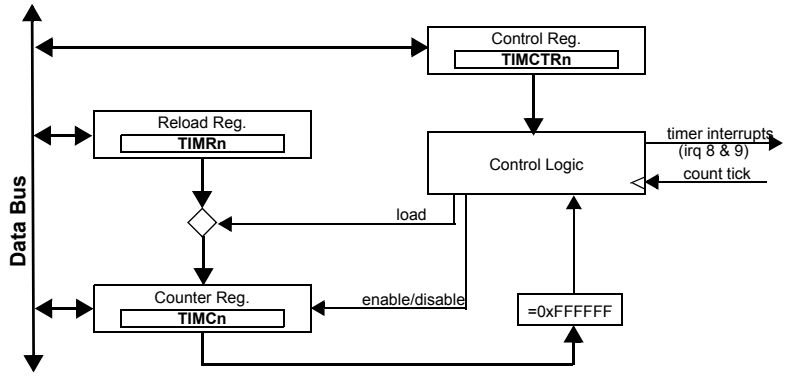
Each timer operation is controlled through a dedicated Timer Control register (TIMCTR). A timer is enabled/disabled by setting the enable bit (*en*) in the timer control register.

Each time a timer underflows, an interrupt is generated. These interrupts can be masked with the Interrupt Mask and Priority register (ITMP).

Setting the load bit (*rl*) in the Timer Control register, the content of the reload register (TIMR) is automatically reloaded in the Timer Counter register (TIMC) after an underflow and the timer continue running. If the reload bit is reset, the timer stops running after its first underflow.

Timer Counter can be forced with the Timer Reload value at any time by asserting the load bit (ld) in the Timer Control register.

Figure 31. Timer/Counter 1/2 Block Diagram



Watchdog

The watchdog operates the same way as the timers, with the difference that it is always enabled and upon underflow asserts the external signal WDOG. This signal can be used to generate a system reset.

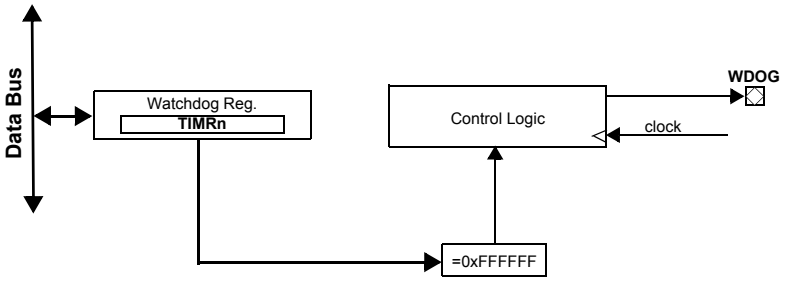
If the watchdog counter is refreshed by writing to WDG register before the counter reaches zero, the counter restarts counting from the new value.

If the counter is not refreshed before the counter reaches zero, WDOG signal is asserted.

After reset, the watchdog is automatically enabled and starts running.

Note: Reading *wdc* field of the watchdog register gives the loading (or re-loading) value, not the effective count value.

Figure 32. Watchdog Block Diagram



General Purpose Interface

The general purpose interface (GPI) consists in a 32-bit wide I/O port with alternate facilities.

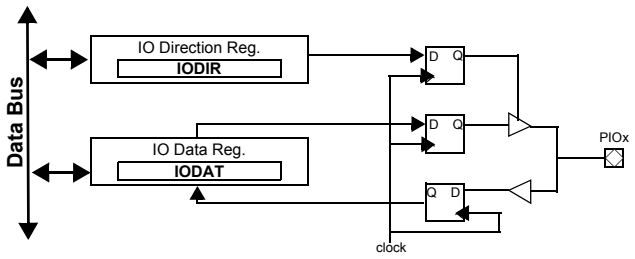
GPI as 32-bit I/O port

The interface is based on bi-directional I/O ports.The port is split in two parts, with the lower 16-bits accessible by the parallel IO pads and the upper 16-bits via the data bus.

lower 16-bits

The lower 16-bits of the general purpose interface are accessible through PIO[15:0]. All I/O ports have true Read-Modify-Write functionality when used as general I/O ports. This means that the direction of one port pin can be changed without unintentionally the direction of any other pin. The same applies when changing the drive value of the port.

Figure 33. I/O port block diagram - PIO[15:0]



configuring the pin

Each pin from PIO[15:0] consists of two register bits : IODIRx and IODATx. As shown in the “Register Description” section, the IODIRx bits are accessed at IODIR address and iodatx at IODAT address.

The IODIRxbit in the IODIR register selects the direction for port number x. If IODIRx is written logic one, the corresponding pin is configured as output. If written logic zero, the pin is configured as an input.

When the pin is configured as an input, a read of the IODATx bit in IODAT register returns the current value of the pin. When the pin is configured as an output, if a logical one is written to IODATx bit in IODAT register, the port x is driven high. If a logical zero is written to IODATx bit in IODAT register, the port x is driven low.

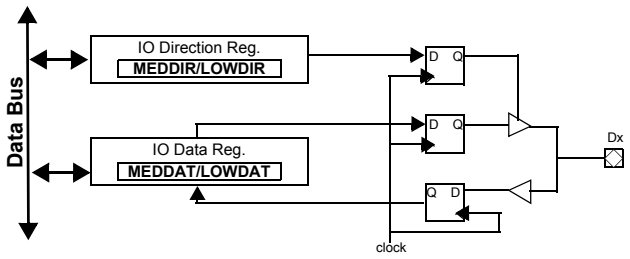
switching between input & output

When the port x is switched from input to output by switching IODIRx, the value of IODATx is immediatly driven on the corresponding pin.When switched from output to input by toggling IODIRx, the value from the pin is immediatly written to IODATx.

upper 16-bits

The upper 16-bits of the general purpose interface are accessible through D[15:0]. They can only be used when all memory areas (ROM, RAM and I/O) are 8-bit or 16-bit wide. If the SDRAM controller is enabled, the upper 16-bits cannot be used.

Figure 34. I/O port block diagram - D[15:0]



configuring the pin

The upper 16 bits of the general purpose interface can only be configured as outputs or inputs on byte basis. D[15:8] is referenced as the medium byte when D[7:0] is referenced as the lower byte.

Each byte from D[15:0] consists of two register fields. As shown in the “Register Description” section, the direction fields are accessed at IODIR address when data fields at IODAT address.

The MEDDIR bit and the LOWDIR bit in the IODIR register select the direction for respectively the medium byte (D[15:8]) and the lower byte (D[7:0]). If MEDDIR (or LOWDIR) is written logic one, the corresponding byte in D[15:0] is configured as output. If written logic zero, the byte is configured as an input.

When configured as an input, a read of the MEDDAT fileds in IODAT register returns the current value of D[15:8]. When configured as an output, the logical value from MEDDAT field in IODAT register is translated in physical values on D[15:8] bus.

When configured as an input, a read of the LOWDAT fileds in IODAT register returns the current value of D[7:0]. When configured as an output, the logical value from LOWDAT field in IODAT register is translated in physical values on D[7:0] bus.

switching between input & output

When the medium byte (or the lower) is switched from input to output by switching MEDDIR (or LOWDIR), the value of MEDDAT (or LOWDAT) is immediatly driven on the corresponding pin. When switched from output to input by toggling MEDDIR (or LOWDIR), the value from the pins are immediatly written to MEDDAT (or LOWDAT).

GPI Alternate functions

Most GPI pins have alternate functions in addition to being general I/O. Facilities like serial communication link, interrupt input and configuration are made available through these functions. The following table summaryses the assignement of the alternate functions.

Table 17. GPI alternate functions

GPI port pin	Alternate function
PIO[15]	TXD1 - UART1 transmitter data
PIO[14]	RXD1 - UART1 receiver data
PIO[13]	RTS1 - UART1 request-to-send
PIO[12]	CTS1 - UART1 clear-to-send
PIO[11]	TXD2 - UART2 transmitter data
PIO[10]	RXD2 - UART2 receiver data
PIO[9]	RTS2 - UART2 request-to-send

GPI port pin	Alternate function
PIO[8]	CTS2 - UART2 clear-to-send
PIO[3]	UART clock - Use as alternative UART clock
PIO[2]	EDAC enable - Enable EDAC checking at reset
PIO[1:0]	Prom width - Defines PROM bus width at reset

In addition to these alternate functions, each GPI interface pin can be configured as an interrupt input to catch interrupt from external devices. Up to four interrupts can be configured on the GPI interface by programming the I/O interrupt register (IOIT).

For a detailed description of the external interrupt configuration, please refer to the “Traps and Interrupts” section.

PCI Arbiter

A PCI arbiter is embedded on the AT697 chip. The¨PCI arbiter enables the arbitration of 4 PCI agents numbered from 3 downto 0. A round-robin algorithm is implemented as arbitration policy. The PCI arbiter is totally independent from the PCI interface

Operation

An Agent on the PCI bus requests the bus by driving low its REQ* line. When the arbiter determines that the bus can be granted to an agent, it drives low the corresponding GNT* line.

When the bus is granted to a PCI agent, the agent keeps the bus for only one transaction. If the agent desires more accesses, it shall continue to assert its REQ* line and wait to be granted the bus again.

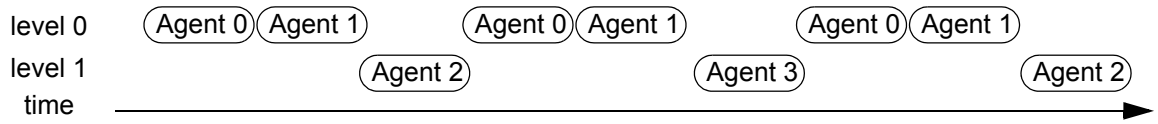
Round Robin

The round robin algorithm used for the arbitration is based on various loops with different priority levels. The implementation in the AT697 is based on two priority loops. A high priority loop is defined as level 0. A low priority loop is defined as level 1.

Operation

The arbitration is done checking the REQ* lines of the PCI agents one after each other. In first place, the loop with level 0 is checked. If a a REQ* is active and no master is currently granted ther bus, the corresponding GNT* line is driven low. Then, the agent is granted the bus. At each complete round-turn in level 0, one step is done in level 1. The following figure illustrates the operation of the arbitre.

Figure 35. Arbitre operation - Agent



With : agents 0 and 1 at level 0
agents 2 and 3 at level 1

If all agents have a request at the same time, the following probabilities of access are implemented:

- All agents in one level have equal probability
- All agents in level 1 together have the same probability of access as one agent in level 0.
- If no agent is in level 0, or no agent in level 0 has a request, all agents in level 1 are granted with equal probability

Bus Parking

As long as no bus request is active on the arbiter, the bus is granted to the last owner. It remains granted to the last owner until another agent requests the bus. When another request is asserted, re-arbitration occurs after one turnover cycle.

After reset, the bus is parked to agent 0. Agent 0 is the default owner after a reset operation.

Re-arbitration

When a master is managing a transfer and another one makes a request to the arbiter, re-arbitration occurs. Only one re-arbitration is performed during a transfer. A new arbitration will take place when the master which was granted the bus frees the bus. As long as all the PCI agents have no request pending, the arbitration is performed. A re-arbitration cycle also occurs when living the bus parking state.

Priority definition

Two different priority levels are defined for the PCI arbiter. Level 0 is defined as the high priority level. Level 1 defines the low priority level. Assignment of the PCI agents priority level is programmable through the arbiter configuration register (ACR).

Each PCI agent can be individually configured to operate either on level 0 or on level 1, except agent 3 that is defined by hardware with a low priority (level 1).

Setting logical one the Px bit in the arbiter configuration register leads the agents x to a low priority level. Setting this bit logical zero leads to a high priority.

After reset, all the PCI agents are configured in the low priority loop.

PCI Interface

Overview

The PCI interface implementation is compliant with the PCI 2.2 specification. It is a high performance 32-bit bus interface with multiplexed address and data lines. It is intended for use as an interconnect mechanism between processor/memory systems and peripheral controller components.

The AT697 processor embedds the In-Silicon PCI core. It is interfaced to the processor core through the PCI to AMBA bridge developped by the European Space Agency.

The PCI bus operations can be clocked at a frequency up to 33MHz, independently of the processor clock. Synchronization of the operation between PCI interface and AT697 core implies numerous FIFO usage. This implementation allows to use the device for Initiator (Master) and Target operations. In each mode single word and burst transfer can be executed.

Two different operating modes can be used with the PCI interface :

- Host Bridge
  The host-bridge connects the local bus of a processor to the PCI bus. Its PCI configuration registers are accessible locally by the processor, but not through PCI configuration cycles. Host-bridge initialises other satellite devices through PCI configuration commands.
- Sattelite
  The satellite is a PCI device, configurable via PCI configuration cycles and the idsel line, but not locally.

Both, host-bridge and satellites can be initiator and/or target on the bus. The present interface has universal functionality, allowing both operation modes. The mode is configured via an hardware bootstrap on the SYSEN* pin.

Some other features are supported by this interface like

- Target lock support
- Zero-latency Fast Back-to-Back transfers
- Zero wait state burst mode transfers
- Support for memory read line/multiple
- Support for memory write and invalidate commands
- Delayed read support
- Flexible error reporting by polling

The PCI bus is a multiplexed one. In this way, address and data through the same medium. That is why PCI communication is based on two phase burst transfer. Each transfer is composed of the following phases :

- An address phase
  During the address phase, the initiator of the communication drives the 32-bit address concerned by the transfer and the command involved through this transfer. The command defines the space area concerned with the transfer and the direction of the transfer.
- A data phase
  During the data phase the initiator of the communication drives the enable bit signal so that only active part of the bus is enabled. When reading, the initiator drives the enable bits and the target set the data on the bus.

PCI Initiator (Master)

The PCI initiator mode of the AT697 gives a direct memory-mapped (initiator) access to the PCI bus. Any access to a memory address in the PCI address range is automatically translated by the interface into the appropriate PCI transaction. In this configuration, the PCI bus is accessed by the same instructions as the main memory. The SPARC instruction set foresees various load/store instruction types. The PCI bus foresees 32 bit wide transactions with byte-enables for each byte lane.

Initiator Mapping

For standard operation, the PCI interface only works in a limited address range. The address range for such initiator transaction is limited to addresses between 0xA0000000 and 0xF0000000.

PCI addresses outside of this predefined range can be accessed only via DMA transactions.

Instructions of different width (byte, half-word, word, double) can be performed for each address of the PCI address range. The three low significant bits of the address A[2:0] are used to determine which PCI byte enable line C/BE*[3:0] should be active during the transaction.

According to the SPARC architecture, big-endian mapping is implemented, the most significant byte standing at the lower address (0x..00) and the least significant byte standing to the upper address (0x..03).

A byte-writing to A[1:0] = 00 results in the byte enable pattern 0111, indicating that the e most significant byte lane (bits 31:24) of the PCI data bus is selected.

The following table presents the transaction width authorized for PCI transfers.

Table 18. Byte Enable Settings

width	8	16	32	64
Assembler	ld[s/u]b, stb	ld[s/u]h, sth	ld, st	ldd, std
C-datatype	char	short	int	long long
A[2:0]=000	0111	0011	0000	0000 (burst)
A[2:0]=100	0111	0011	0000	not aligned
A[2:0]=x01	1011	not aligned	not aligned	not aligned
A[2:0]=x10	1101	1100	not aligned	not aligned
A[2:0]=x11	1110	not aligned	not aligned	not aligned

Note: PCI byte enables are active low.

For non-aligned accesses, the byte enable pattern (1111) is issued on PCI, to avoid destroying data in the remote PCI target.

Memory cycles

Many memory cycles such as memory-read/write and memory-read-line/write-invalidate can be issued from the processor with common SPARC instruction set. Selection of the command to execute is performed setting the value of the command field (CMD) in the PCI initiator configuration (PCIIC).

Setting logical ‘01’ the CMD field result in the generation of memory read/write access when PCI address is accessed. A logical value of ‘10’ result in a memory read line or write and invalidate on PCI address access.

For the memory commands the address issued on the PCI bus is a word address with bits (1:0) set to 00. This indicates that the linear incrementing mode is used.

operation

The following procedure shall be used to engage memory cycle on the PCI interface:

1. Select the initiator mode by setting logical one the MOD bit in the PCI initiator configuration register.
2. Select the memory load/store command or the memory read-line/write and invalidate command in the PCI initiator configuration register. The CMD field shall be set logical ‘01’ for simple load/store operation and shall be set logical ’11’ for read-line/write-&-invalidate.
3. Enabling the interrupt signalisation is optionnal. It can be enabled setting logical one the initiator error bits in the PCI interrupt enable register (PCIITE). Up to four interrupt sources can be defined : Initiator Error, Initiator Parity Error, PCI core error and system error.
4. Engage an access to a memory address mapped in the PCI address range.

IO transaction cycles

operation

The following procedure shall be used to engage I/O cycle on the PCI interface:

1. Select the initiator mode by setting logical one the MOD bit in the PCI initiator configuration register.
2. Select the I/O load/store command in the PCI initiator configuration register. The CMD field shall be set logical ‘00’ for I/O operation.
3. Enabling the interrupt signalisation is optionnal. It can be enabled setting logical one the initiator error bits in the PCI interrupt enable register (PCIITE). Up to four interrupt sources can be defined : Initiator Error, Initiator Parity Error, PCI core error and system error.
4. Engage an access to an I/O address mapped in the PCI address range.

Configuration cycles

Target selection

Accesses to a configuration address space requires the target device to be selected. Due to the address range limitation, the chip-select (IDSEL) connection necessary for device selection shall be done using only A/D[27:16]. This allows up to 12 PCI devices to be connected on the bus.

Devices with chip-select line connected to A/D[31:28] can’t be configured through standard operations. DMA configuration cycles shall be used to configure the devices connected to A/D[31:28].

The PCI bus configuration cycles can be performed using the same instructions as the main memory. To generate such configuration cycle with the standard instructions, the command type field (COMMSB) of the PCI initiator configuration register (PCIIC) shall be programmed to ‘01’.

Then, if a load (or store) cycle is performed to an addresss in the PCI address range, a physical configuration cycle is performed on the PCI bus. The full 32-bit address defined on the internal bus is propagated on the PCI bus. Once a target is selected (DEVSEL* asserted).

Operation

The following procedure shall be used to engage configuration cycle on the PCI interface:

1. Select the initiator mode by setting logical one the MOD bit in the PCI initiator configuration register.
2. Select the configuration load/store command in the PCI initiator configuration register. The CMD field shall be set logical ‘10’ for configuration operation.
3. Enabling the interrupt signalisation is optionnal. It can be enabled setting logical one the initiator error bits in the PCI interrupt enable register (PCIITE). Up to four interrupt sources can be defined : Initiator Error, Initiator Parity Error, PCI core error and system error.
4. Engage an access to an configuration space.

Limitation

Configuration cycles shall only be generated by the PCI host of the bus or by a PCI-to-PCI bridges.

Special cycles

By default, all requests are translated into single cycle PCI transactions, each transaction consisting in an address phase followed by a single data phase.

Linear incrementing store-word

Linear incrementing store-word sequences are translated into undetermined length PCI write bursts with up to a maximum of 255 words. The PCI burst mode is then maintained as long as possible. Read/write direction is unchanged and the address $A_{n+1} = A_n + 4$. When the sequence is discontinued, the PCI burst stops with a last data phase during which byte enables are 1111.

Double word load/store

Double word load/store requests can be executed as a two word bursts, the burst (one address phase, two data phases) on PCI.

A double word read is executed as a two word burst when the DWR bit is set logical one in the PCI initiator configuration register. When set logical zero, a double word read is translated to the PCI as two single read accesses.

A double word write is executed as a two word burst when the DWW bit is set logical one in the PCI initiator configuration register. When set logical zero, a double word write is translated to the PCI as a burst of undefined length as long as the addresses are sequential.

The double word mode accelerates the transfer on the PCI side except in cases, where linear incrementing bursts are done by subsequent storedouble instructions ($A_{n+1} = A_n + 8$). In this case the double word write bit DWW shall be set logical zero.

It is in general recommended to set logical one both DWR and DWW and to use the DMA to transfer large data blocks.

Fast back2back cycles

The PCI implementation only supports fast back2back cycles to the same target. Before using fast back-2-back transfers, fast back-2-back cycles shall be enabled setting logical one the bit COM9 in the status command register (PCISC). Bit COM9 shall only be set one if all targets on the bus support fast back-2-back transfers.

Issuing a fast back to back transfer is done setting logical one the B2B bit in the PCIDMA register.

Note: Fast back-2-back can only be generated by the initiator. It is not accepted by the AT697 PCI target.

Error reporting

Fatal (abort) and address parity errors

On a fatal error (or address parity error), the interface flushes all the current buffer requests and all other buffer requests. Then, the interface reports the fatal error driven logical one the pci core error (CMFER) in the PCi interrupt pending register.

The PCI core is restarted as soon as a new request is engaged.

Data parity errors

During load/read transactions, one PCI parity error is recoverable in hardware. If the PERR bit is set in the PCI initiator configuration register, the interface ignores the erroneous PCI data and retries the request.

However, if the data parity error persists at the same address, it is considered to be unrecoverable. Then, an error on the internal bus is detected and the PCI initiator error is reported in the IMIER bit of the PCI interrupt pending register.

Parity error is also impossible in cases where the transaction is already finished on the local bus when the error is detected/reported on the PCI bus. The parity error is then reported in the initiator parity error bit (IMPER) and error recovery must be done in software.

DMA transfer

A DMA facility is available on the AT697 processor. The DMA transfer are performed through the PCI interface. The DMA controller executes data transfer between the local memory and a remote target on the PCI bus.

The processor core only intervenes for the initiation of the transfer. Once transfer is initiated, DMA controller is fully autonomous. DMA transfers take place in background of the processor core activity. Thus, interrupts are provided to help to synchronise the application with start and end of the transfer.

The DMA interface executes only word-size transactions with all 4 byte lanes enabled.

Operation

The DMA is enabled setting logical one the MOD bit in the PCI initiator configuration register (PCIIC). To synchronize the application with the start and the end of the transaction, two interrupts can be enabled : DMAER for transfer control and IMIER for error control.

Each DMA sequence shall program the following parameters :

- PCI start address
- PCI command type
- number of words to be transferred
- the start address in the local memory

A DMA transfer is performed assuming the following operations are done in the given order :

1. Write the PCI start address of burst to the PCI start address register (PCISA). The PCISA register shall be re-writen each time a DMA transfer is initiated, even if the address is identical to the address of the previous DMA request.
2. Write together the PCI command and the number of words to be transfered in the PCI DMA configuration register (PCIDMA). Writing to the PCIDMA passes the PCI address, the word count and the PCI command to the PCI core and initiates the transaction on the PCI bus.

3. Write the start address in the local memory map to the PCI DMA address register (PCIDMAA).

Once the three operation are executed, data transfer is started in background. Once the specified number of words is transfered, the interface set logical one the dma end of transfer bit (DMAER) and generate an interrupt if enabled. Then DMA controller goes back to idle state.

Error Reporting

If the PCI core does not accept the DMA cycle request, the DMA state controller remains locked and an error is reported as initiator error with the IMIER bit set logical one. If the request on the PCI core was just delayed, rewriting PCIDMAA may succeed. If the problem persists, reset the interface by writing –1 (0xFFFFFFFF) to PCIIC.

Transfer Limitation

A DMA transaction may never cross a 1 KByte border. The value represented by PCIDMAA(9:2) + PCIDMA(7:0) must be less than 256. If this restriction is not respected, the data transfer stops at the 1 kByte border. Then the PCI core is flushed. Simultaneously, in the PCI interrupt pending register (PCIITP) the dma error bit (DMAER) and the initiator error bit (IMIER) are asserted logical one.

If enabled with the PCI interrupr enable register (PCIITE) and unmasked in the general interrupt mask register, the PCI interrupt 14 is generated (TT = 0x1E).

Debug Facilities

Not implemented for application use.

Target Mode Transfer

In the target mode, the PCI interface receives requests originated from remote PCI initiators (masters). Target data transfer is executed in background without AT697 core intervention. AT697 core can only intervenes is the configuration of the target.

- In host bridge mode the target is configured by the AT697 core
- In satellite mode the configuration is done by a remote device using the PCI command set

Target Programming

The target is configured through the following registers :

- PCISC register
  bits 0/1 for memory and I/O command response
  bit 6 for check of data and address parity error
  bit 7 for response to data and address parity error
- base address registers
  memory base address : MEMBAR1, MEMBAR2
  I/O base address : IOBAR
- PCITPA register to indicate the storage location
- PCITSC(7) bit to write data in memory

transaction Ordering

As specified in the PCI standard, delayed read functionality is implemented, obeying to the following rules:

- The interface stores one delayed read at a time. When a read request was retried (because local data not yet available), the interface remains locked for any other target read (targeting different addresses). The initiator of the original read has to repeat its request to the same address.
- A retried (delayed) read can be interrupted by one or more PCI write accesses. The PCI standard requires this write command to be processed first, to prevent a system lock-up.
- Meanwhile, the interface will prefetch read-data into the TXMT FIFO. After the (interfering) write, when the read request is repeated, and the requested data is available in the FIFO the delayed transfer completes normally.

All target read accesses are generally prefetching, also reads with I/O command. Once a start address is given, the interface prefetches up to 8 words into the TXMT FIFO. After the last required data word was transferred to PCI, the PCI core automatically flushes the FIFO to discard the unused prefetched data. The interface assumes the complete local address space to be ‘prefetchable’, defined here as the fact, that reading from an address does not alter the data. This behaviour is to be considered if non-prefetchable devices (for example the UART’s) shall be read through the PCI target.

PCI Error Reporting

According to the PCI standard error and status are implemented in the PCI status register. The PCI standard foresees a single parity check, by which bus-errors can be detected, but not corrected.

- Read data parity errors can eventually be retried by the hardware.
- In other cases, recovery must be done in software.

Therefore, events, which occur in the PCI interface or on the PCI bus, are saved in status bits, and optionally, the PCI interrupt (IRQ14) is asserted.

Different events can be selected to assert the interrupt. By the interrupt enable register (PCIITE) configuration you can select the interrupt events which will assert IRQ14. then an interrupt handler can read the interrupting event in the status register (PCIITP).

Furthermore, interrupts can be forced for test purposes by writing to PCIITF.

In host-bridge configuration, this allows an error detection by polling. Certain events and errors are also reported by the interface in the interrupt status register. For each bit of this register , interrupt generation can be programmed individualy. All PCI interrupt generated are then reported to AT697 core through the PCI interrupt (IT14). The different interrupt causes are distinguished by the interrupt status registers settings.

Please refer to the register description chapter for more details on interrupt status register.

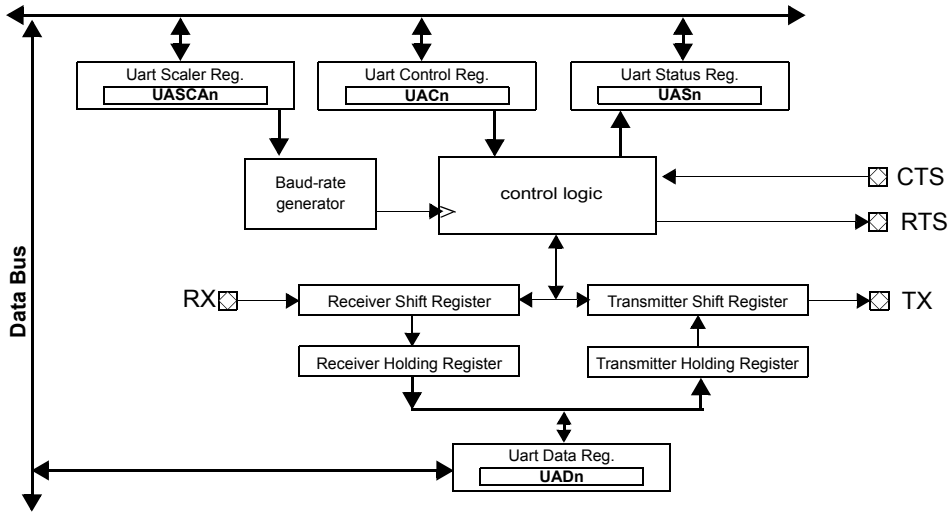
UARTs (UART1 and UART2)

The Universal Asynchronous Receiver and Transmitter (UART) is a highly flexible serial communication module. The AT697 implements two uarts : UART1 and UART2. Uarts on the processor are defined as alternate functions of the general purpose interface (GPI).

Overview

The two UART's provide double buffering. Each UART consists of a transmitter holding register, a receiver holding register, a transmitter shift register, and a receiver shift register. Each of these registers are 8-bit wide.

Figure 36. UART Block Diagram



Each UART is fully controlled by a set of four registers including :

- a control register
- a status register
- a scaler register
- and a data register

Serial Frame

A serial frame is defined to be one character of data bits with synchronisation bits (start and stop bits), and optionnaly a parity bit for error checking.

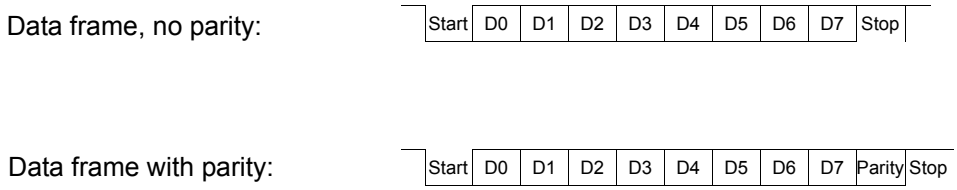
Frame formats

Two frame formats are accepted by the AT697 UARTs, the only difference being the presence or the absence of the parity bit. All the frames are built on an eight data bits basis.

A frame starts with the synchronization start bit followed by the least significant data bit. Then the next data bits, up to a total of eight, are succeeding, ending with the most significant bit. If enabled by setting the PE bit in the uart control register (UCRx), the parity bit is inserted after the data bits and before the stop bit.

The following figure illustrates the accepted frame formats.

Figure 37. Data frame format



Parity bit

The parity bit is calculated by doing an exclusive-or of all the data bits. The odd parity is configured setting logical one the PS bit in the uart control register (UACn). In this case, the result of the exclusive or is inverted. An even parity can be selected setting logical zero the PS bit.

If used, the parity bit is located between the last data bit and the stop bit of the serial frame.

The relation between the parity bit and data bits is as follows:

$$P_{even} = d_7 \oplus \ldots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 0$$
$$P_{odd} = d_7 \oplus \ldots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 1$$

$\mathbf{P_{even}}$ Parity bit using even parity

$\mathbf{P_{odd}}$ Parity bit using odd parity

$\mathbf{d_n}$ Data bit n of the character

Clock Generation

The clock generation logic generates the base clock for the Transmitters and Receivers. The bit rate of the UART is issued from the clock generator after a combination between the input clock of the clock module and a scaler.

Uart Clock

Two clock inputs can be used by the clock generator :

- An internal clock
- An external clock

Each UART can be configured to use either the internal or the external clock source by programming the EC bit in the uart control register (UACn). If set logical zero, the UART is clocked by the internal clock. If EC is set logical one, the UART is clocked by the external clock. When using the external configuration, the UART clock shall be provided by PIO[3] from the general purpose interface. This clock input is used as an alternate function for PIO[3].

caution :

When using the external clock source, the frequency of PIO[3] must be less than half the frequency of the system clock.

Baud Rate Generation

To generate the bit-rate, each UART has a programmable 12-bits clock divider (UASCAn). According to the configuration of the EC bit in the uart control register, the scaler is clocked either by the system or by an external clock.

Each time the scaler underflows, a UART tick is generated. The scaler is automatically reloaded with the value of the UART scaler register after each underflow. The resulting UART tick frequency should be 8 times the desired baud-rate.

The following equation shall be used to calculate the scaler value to define, depending on the clock source and the expected baud rate.

$$scaler = \frac{\frac{uartclk \times 10}{baudrate \times 8} - 5}{10}$$

variable description :

- ***uartclk*** : frequency of the uart clock
- ***baudrate*** : expected baud rate
- ***scaler*** : value to set in UASCAn to reach the expected baudrate

Communication Operations

UARTS operations are controlled through the uart control registers (UACn) and the Uart status registers (UASn).

Transmitter Operation

The transmitter is enabled setting logical one the TE bit in the UART control register. When ready to transmit, data is transferred from the transmitter holding register to the transmitter shift register and converted to a serial frame on the transmitter serial output pin (TX).

Following the transmission of the stop bit, if a new character is not available in the transmitter holding register, the transmitter serial data output remains high and the transmitter shift register empty bit (TS) in the UART status register is set logical one. Transmission resumes and the TS bit is cleared when a new character is loaded in the transmitter holding register.

If the transmitter is disabled, it will continue operating until the character currently being transmitted is completely sent out. The transmitter holding register cannot be loaded when the transmitter is disabled.

If flow control is enabled, the CTS input must be low in order for the character to be transmitted. If it is deasserted in the middle of a transmission, the character in the shift register is transmitted and the transmitter serial output then remains inactive until CTS is asserted again. If the CTS is connected to a receivers RTS, overrun can effectively be prevented.

Receiver Operation

The receiver is enabled for data reception when the receiver enable bit (RE) in the UART control register is set logical one. The receiver looks for a high to low transition of a start bit on the receiver serial data input pin. If a transition is detected, the state of the serial input is sampled a half bit clocks later. If the serial input is sampled high the start bit is invalid and the search for a valid start bit continues. If the serial input is still low, a valid start bit is assumed and the receiver continues to sample the serial input at one bit time intervals until the proper number of data bits and the parity bit have been assembled and one stop bit has been detected. During this process the least significant bit is received first.

The serial input is sampled three times for each bit and averaged to filter out noise.

The data is then transferred to the receiver holding register and the data ready bit (DR) is set logical one in the UART status register. The parity, framing and overrun error bits are set at the received byte boundary, at the same time as the receiver ready bit is set.

If both receiver holding and shift registers contain an un-read character when a new start bit is detected, then the character held in the receiver shift register will be lost and the overrun bit (OV) is set logical one in the UART status register.

If flow control is enabled, then the RTS will be negated (high) when a valid start bit is detected and the receiver holding register contains an un-read character. When the holding register is read, the RTS will automatically be reasserted again.

A correctly received byte is indicated by the data ready bit (DR) in the UART status register (UASn). In case of error (framing error, stop bit error,...), the respective bits FE, PE, ... are set logical one in the UART status register when the data ready bit remains logical zero.

Interrupt Generation

The two UARTs can be configured to generate interrupt each time a byte is received or a byte is sent.

If the TI bit in the UART control register is set logical one, an interrupt is issued after each character sending. If set logical zero, no interrupt is issued on character sending.

If the RI bit in the UART control register is set logical one, an interrupt is issued after each character reception. If set logical zero, no interrupt is issued after a character reception.

If the receiver interrupt is enabled, when error is detected during the reception of a character,an interrupt is generated. To identify the origin of the transaction failure, refer to the uart status register bits (OV, PE, TE) that indicate either it is a parity, a framing or an overrun error.

Loop back mode

If the LB bit in the UART control register is set, the UART will be in loop back mode. In this mode, the transmitter output is internally connected to the receiver input and the RTS is connected to the CTS. It is then possible to perform loop back tests to verify operation of receiver, transmitter and associated software routines. In this mode, the outputs remain in the inactive state, in order to avoid sending out data.

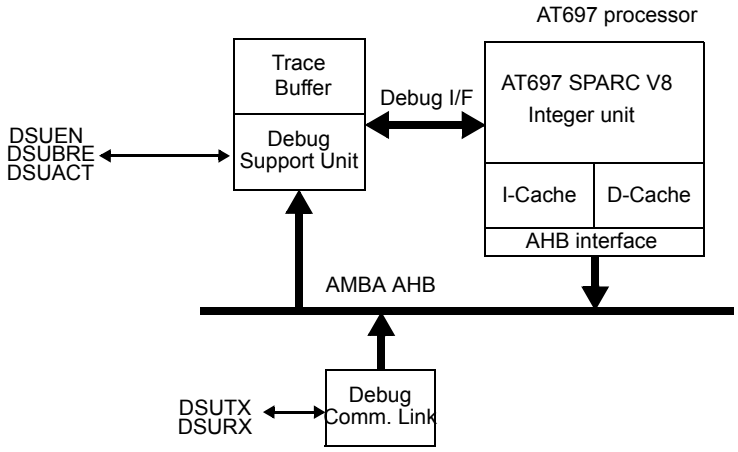
Debug Support Unit - DSU

Overview

The AT697 processor includes an hardware debug support unit to aid software debugging on target hardware. The support is provided through two modules: a debug support unit (DSU) and a debug communication link (DCL).

The DSU can put the processor in debug mode, allowing read/write access to all processor registers and cache memories. The DSU also contains a trace buffer which stores executed instructions or data transfers on the internal bus. The debug communications link implements a simple read/write protocol and uses standard asynchronous UART communications.

Figure 38. Debug Support Unit and Communication Link



It is possible to debug the processor through any master on the internal bus. The PCI interface is build in as a master on the internal bus. All debug features are available from any PCI master.

Debug Support Unit

The debug support unit is used to control the trace buffer and the processor debug mode. The DSU master occupies a 2 Mbyte address space on the internal bus. Through this address space, any other masters like PCI can access the processor registers and the contents of the trace buffer.

The DSU control registers can be accessed at any time, while the processor registers and caches can only be accessed when the processor has entered debug mode. The trace buffer can be accessed only when tracing is disabled or completed. In debug mode, the processor pipeline is held and the processor is controlled by the DSU. Entering the debug mode can occur on the following events:

- executing a breakpoint instruction (ta 1)
- integer unit hardware breakpoint/watchpoint hit (trap 0x0B)
- rising edge of the external break signal (DSUBRE)
- setting the break-now (BN) bit in the DSU control register
- a trap that would cause the processor to enter error mode
- occurrence of any, or a selection of traps as defined in the DSU control register
- after a single-step operation

- DSU breakpoint hit

The debug mode can only be entered when the debug support unit is enabled through an external pin (DSUEN). Driving the DSUEN pin high enables the debug mode. When the debug mode is entered, the following actions are taken:

- PC and nPC are saved in temporary registers (accessible by the debug unit)
- an output signal (DSUACT) is asserted to indicate the debug state
- the timer unit is (optionally) stopped to freeze the AT697 timers and watchdog

The instruction that caused the processor to enter debug mode is not executed, and the processor state is kept unmodified. Execution is resumed by clearing the BN bit in the DSU control register or by de-asserting DSUEN. The timer unit will be re-enabled and execution will continue from the saved PC and nPC. Debug mode can also be entered after the processor has entered error mode, for instance when an application has terminated and halted the processor. The error mode can be reset and the processor restarted at any address.

DSU Breakpoint

The DSU contains two breakpoint registers for matching either internal bus addresses or executed processor instructions. A breakpoint hit is typically used to freeze the trace buffer, but can also put the processor in debug mode.

Freeze operation can be delayed by programming the TDELAY field in the DSU control register to a non-zero value. In this case, the TDELAY value will be decremented for each additional trace until it reaches zero, after which the trace buffer is frozen. If the brake on trace freeze bit (BT) is set logical one in the DSU control register, the DSU forces the processor into debug mode when the trace buffer is frozen.

Note: Due to pipeline delays, up to 4 additional instruction can be executed before the processor is placed in debug mode.

A mask register is associated with each breakpoint, allowing breaking on a block of addresses. Only address bits with the corresponding mask bit set to ‘1’ are compared during breakpoint detection.

Time Tag

The DSU implements a time tag counter. This counter is decremented each clock as long as the processor is running. The counter is stopped when the processor enters debug mode. It is restarted when execution is resumed.

This time tag counter is stored in the trace as an execution time reference.

Trace Buffer

The trace buffer consists of a circular buffer that stores the executed instructions or the internal bus data transfers. The size of the trace buffer is 512 lines of 16 bytes**.** The trace buffer operation is controlled through the DSU control register (DSUC) and the trace buffer control register (TBC). When the processor enters debug mode, tracing is suspended.

The trace buffer can contain the executed instructions, the transfers on the internal bus or both (mixed-mode). The trace buffer control register (TBC) contains two counters (BCNT ans ICNT) that store the address of the trace buffer location that will be written on next trace. Since the buffer is circular, it actually points to the oldest entry in the buffer. The indexes are automatically incremented after each stored trace entry.

Instruction trace

The instruction trace mode is enabled setting logical one the trace instruction enable bit (TI) in the trace buffer control register (TBC).

During instruction tracing, one instruction is stored per line in the trace buffer with the exception of multi-cycle instructions. Multi-cycle instructions can be entered two or three times in the trace buffer :

- For store instructions, bits [63:32] correspond to the store address on the first entry and to the stored data on the second entry (and third in case of STD). Bit 126 is set logical one on the second and third entry to indicate this.
- A double load (LDD) is entered twice in the trace buffer, with bits [63:32] containing the loaded data.
- Multiply and divide instructions are entered twice, but only the last entry contains the result. Bit 126 is set for the second entry.
- For FPU operation producing a double-precision result, the first entry puts the MSB 32 bits of the results in bit [63:32] while the second entry puts the LSB 32 bits in this field.

Table 19. Trace buffer data allocation, Instruction tracing mode

Bits	Name	Definition
127	Instruction breakpoint hit	Set to ‘1’ if a DSU instruction breakpoint hit occurred.
126	Multi-cycle instruction	Set to ‘1’ on the second and third instance of a multi-cycle instruction (LDD, ST or FPOP)
125:96	DSU counter	The value of the DSU counter
95:64	Load/Store parameters	Instruction result, Store address or Store data
63:34	Program counter	Program counter (2 lsb bits removed since they are always zero)
33	Instruction trap	Set to ‘1’ if traced instruction trapped
32	Processor error mode	Set to ‘1’ if the traced instruction caused processor error mode
31:0	Opcode	Instruction opcode

When a trace is frozen, interrupt 11 is generated.

Bus Trace

The bus trace mode is enabled setting logical one the trace instruction enable bit (TA) in the trace buffer control register (TBC).

During bus tracing, one operation of the internal bus is stored per line in the trace buffer.

Table 20. Trace Buffer Data Allocation, Internal bus Tracing Mode

Bits	Name	Definition
127	AHB breakpoint hit	Set to ‘1’ if a DSU AHB breakpoint hit occurred.
126	-	Unused
125:96	DSU counter	The value of the DSU counter
95:92	IRL	Processor interrupt request input
91:88	PIL	Processor interrupt level (psr.pil)
95:80	Trap type	Processor trap type (psr.tt)

Bits	Name	Definition
79	Hwrite	AHB HWRITE
78:77	Htrans	AHB HTRANS
76:74	Hsize	AHB HSIZE
73:71	Hburst	AHB HBURST
70:67	Hmaster	AHB HMASTER
66	Hmastlock	AHB HMASTLOCK
65:64	Hresp	AHB HRESP
63:32	Load/Store data	AHB HRDATA or HWDATA
31:0	Load/Store address	AHB HADDR

Mixed Trace

In mixed mode, the buffer is divided on two halves, with instructions stored in the lower half and bus transfers in the upper half. The MSB bit of the AHB index counter is then automatically kept high, while the MSB of the instruction index counter is kept low.

DSU Memory Map

Table 21. DSU Map

Address	Register
0x800000c4	DSU UART status register
0x800000c8	DSU UART control register
0x800000cc	DSU UART scaler register
0x90000000	DSU control register
0x90000004	Trace buffer control register
0x90000008	Time tag counter
0x90000010	AHB break address 1
0x90000014	AHB mask 1
0x90000018	AHB break address 2
0x9000001C	AHB mask 2
0x90010000 - 0x90020000	Trace buffer
..0	Trace bits 127 - 96
...4	Trace bits 95 - 64
...8	Trace bits 63 - 32
...C	Trace bits 31 - 0
0x90020000 - 0x90040000	IU/FPU register file
0x90080000 - 0x90100000	IU special purpose registers
0x90080000	Y register
0x90080004	PSR register

Address	Register
0x90080008	WIM register
0x9008000C	TBR register
0x90080010	PC register
0x90080014	NPC register
0x90080018	FSR register
0x9008001C	DSU trap register
0x90080040 - 0x9008007C	ASR16 - ASR31 (when implemented)
0x90100000 - 0x90140000	Instruction cache tags
0x90140000 - 0x90180000	Instruction cache data
0x90180000 - 0x901C0000	Data cache tags
0x901C0000 - 0x90200000	Data cache data

The addresses of the IU/FPU registersis defined according to how many register windows has been implemented. The registers can be accessed at the following addresses (NWINDOWS = number of SPARC register windows = 8):

- %o*n*: 0x90020000 + (((psr.cwp * 64) + 32 + *n*) mod (NWINDOWS*64))
- %l*n*: 0x90020000 + (((psr.cwp * 64) + 64 + *n*) mod (NWINDOWS*64))
- %i*n*: 0x90020000 + (((psr.cwp * 64) + 96 + *n*) mod (NWINDOWS*64))
- %g*n*: 0x90020000 + (NWINDOWS*64) + 128
- %f*n*: 0x90020000 + (NWINDOWS*64)

Debug Operations

Instruction Breakpoints

To insert instruction breakpoints, the breakpoint instruction (ta 1) should be used. This will leave the four IU hardware breakpoints free to be used as data watchpoints. Since cache snooping is only done on the data cache, the instruction cache must be flushed after the insertion or removal of breakpoints. To minimize the influence on execution, it is enough to clear the corresponding instruction cache tag (which is accesible through the DSU).

The DSU hardware breakpoints should only be used to freeze the trace buffer, and not for software debugging since there is a 4-cycle delay from the breakpoint hit before the processor enters the debug mode.

Single Stepping

By writing the SS bit and reseting the BN bit in the DSU control register, the processor will resume execution for one instruction and then automatically enter debug mode.

DSU Trap

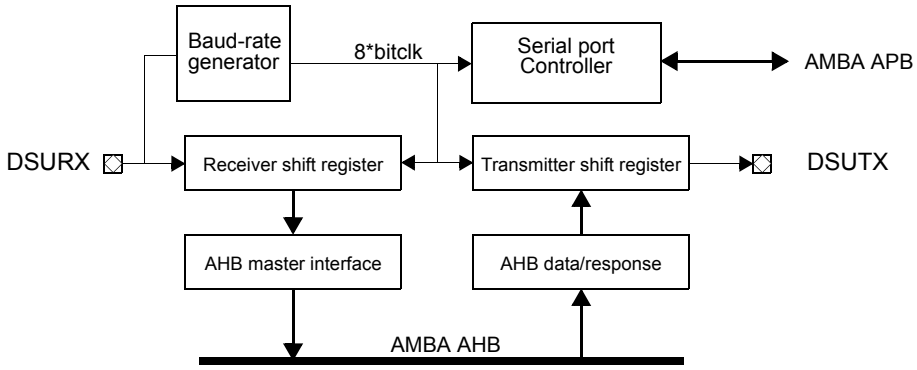
The DSU trap register (DTR) consists in a read-only register that indicates which SPARC trap type caused the processor to enter debug mode.

When debug mode is forced by setting the BN bit in the DSU control register, the trap type is 0x0B.

DSU Communication Link

DSU communication link consists of a UART connected to the internal bus as a master.

Figure 39. DSU Communication Link Block Diagram

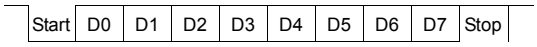


A simple communication protocol is supported to transmit access parameters and data. A link command consist of a control byte, followed by a 32-bit address, followed by optional write data. If the LR bit in the DSU control register is set, a response byte will be sent after each AHB transfer. If the LR bit is not set, a write access does not return any response, while a read access only returns the read data.

Data Frame

Data is sent on 8-bit basis.

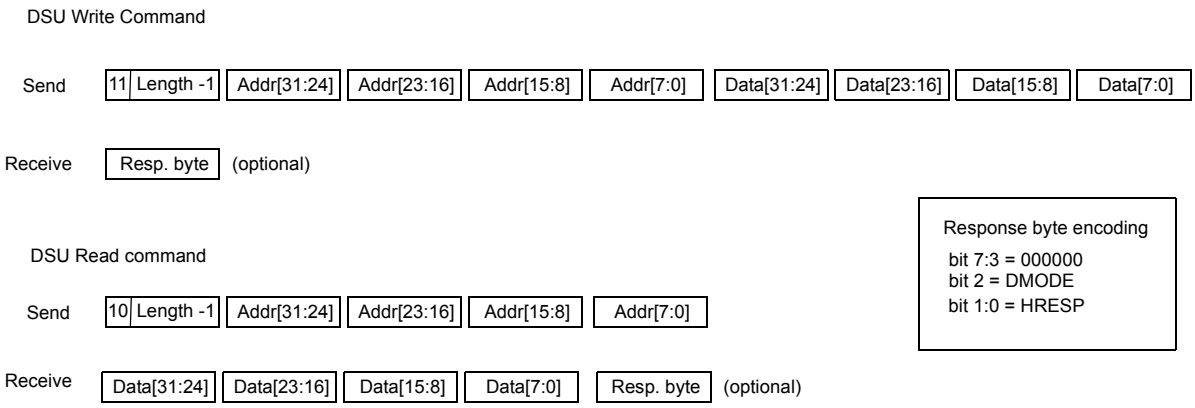
Figure 40. DSU UART Data Frame



Commands

Through the communication link, a read or write transfer can be generated to any address on the internal bus. A response byte is can optionally be sent when the processor goes from execution mode to debug mode. Block transfers can be performed be setting the length field to *n*-1, where *n* denotes the number of transferred words. For write accesses, the control byte and address is sent once, followed by the number of data words to be written. The address is automatically incremented after each data word. For read accesses, the control byte and address is sent once and the corresponding number of data words is returned.

Figure 41. DSU Commands



Clock Generation

The UART contains a 14-bit down-counting scaler to generate the desired baud-rate. The scaler is clocked by the system clock and generates a UART tick each time it underflows. The scaler is reloaded with the value of the UART scaler reload register after each underflow. The resulting UART tick frequency should be 8 times the desired baud-rate.

If not programmed by software, the baud rate will be automatically be discovered. This is done by searching for the shortest period between two falling edges of the received data (corresponding to two bit periods). When three identical two-bit periods has been found, the corresponding scaler reload value is latched into the reload register, and the BL bit is set in the UART control register. If the BL bit is reset by software, the baud rate discovery process is restarted. The baud-rate discovey is also restarted when a ‘break’ is received by the receiver, allowing to change to baudrate from the external transmitter. For proper baudrate detection, the value 0x55 should be transmitted to the receiver after reset or after sending break.

The best scaler value for manually programming the baudrate can be calculated as follows:

$$scaler = \frac{\frac{sysclk \times 10}{baudrate \times 8} - 5}{10}$$

Booting from DSU

By asserting DSUEN and DSUBRE at reset time, the processor will directly enter debug mode without executing any instructions. The system can then be initialised from the communication link, and applications can be downloaded and debugged. Additionally, external (flash) PROMs for standalone booting can be re-programmed.

JTAG Interface

Overview

The AT697 implements a standard interface compliant with the IEEE 1149.1 JTAG specification. This interface can be used for PCB testing using the JTAG boundary-scan capability.

The JTAG interface is accessed through five dedicated pins. In JTAG terminology, these pins constitute the Test Access Port (TAP).

The following table summarizes the TAP pins and there function at JTAG level.

Table 22. TAP Pins

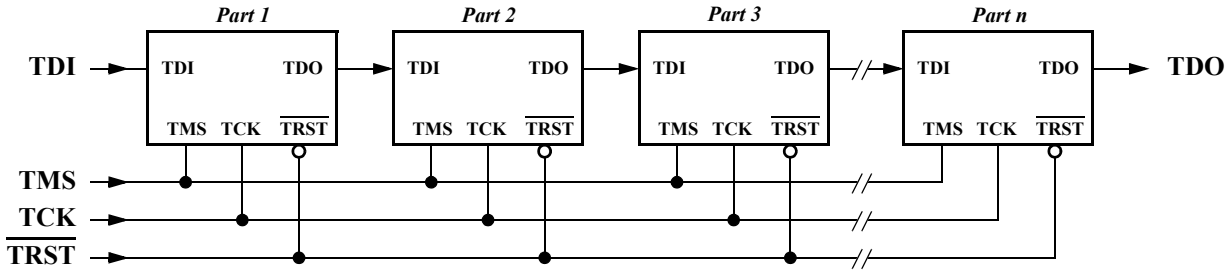
Pin	Name	Type	Description
TCK	Test Clock	Input	Used to clock serial data boundary into scan latches and control sequence of the test state machine. TCK can be asynchronous with CLK
TMS	Test Mode select	Input	Primary control signal for the state machine. Synchronous with TCK. A sequence of values on TMS adjusts the current state of the TAP.
TDI	Test Data Input	Input	Serial input data to the boundary scan latches. Synchronous with TCK
TDO	Test Data Output	Output	Serial output data from the boundary scan latches. Synchronous with TCK
TRST	Test Reset	Input	Resets the test state machine. can be asynchronous with TCK

For more details, please refer to the ‘IEEE Standard Test Access Port and Boundary Scan’ specification.

Any AT697 based system will contain several JTAG compatible chips. These are connected using the minimum (single TMS signal) configuration. This configuration contains three broadcast signals (TMS, TCK, and TRST,) which are fed from the JTAG master to all JTAG slaves in parallel, and a serial path formed by a daisy-chain connection of the serial test data pins (TDI and TDO) of all slaves.

The TAP supports a BYPASS instruction which places a minimum shift path (1 bit) between the chip’s TDI and TDO pins. This allows efficient access to any single chip in the daisy-chain without board-level multiplexing.

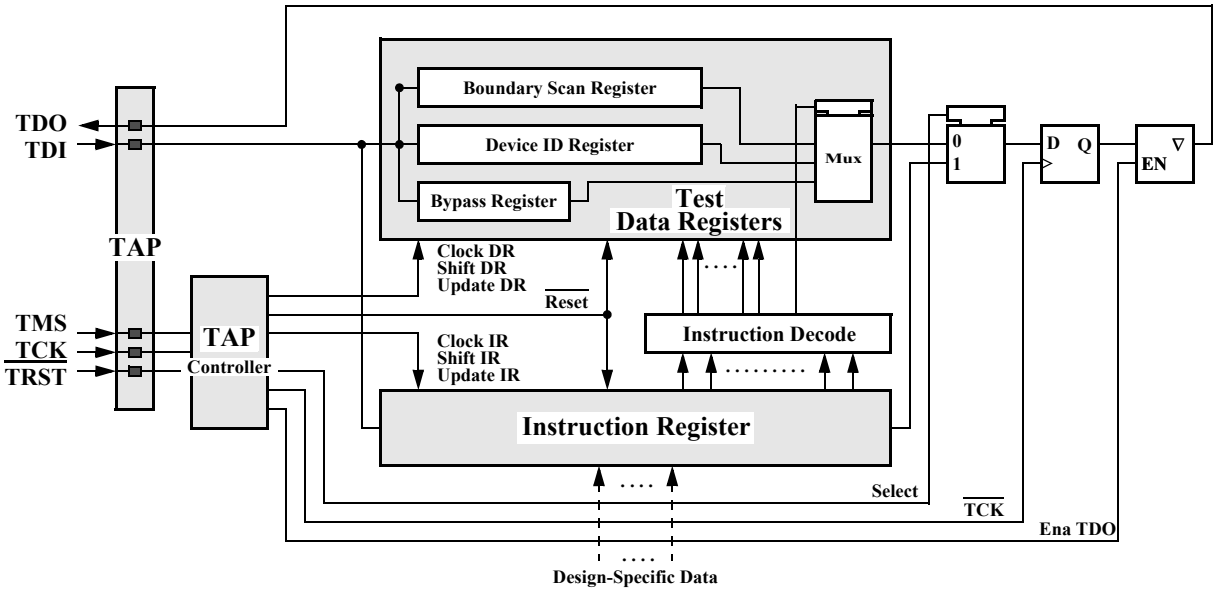
Figure 42. JTAG Serial connection using 1 TMS Signal



TAP Architecture

The TAP implemented in the AT697 consists of a TAP interface, a TAP controller, plus a number of shift registers including an instruction register (IR) and some registers .

Figure 43. AT697 TAP Architecture

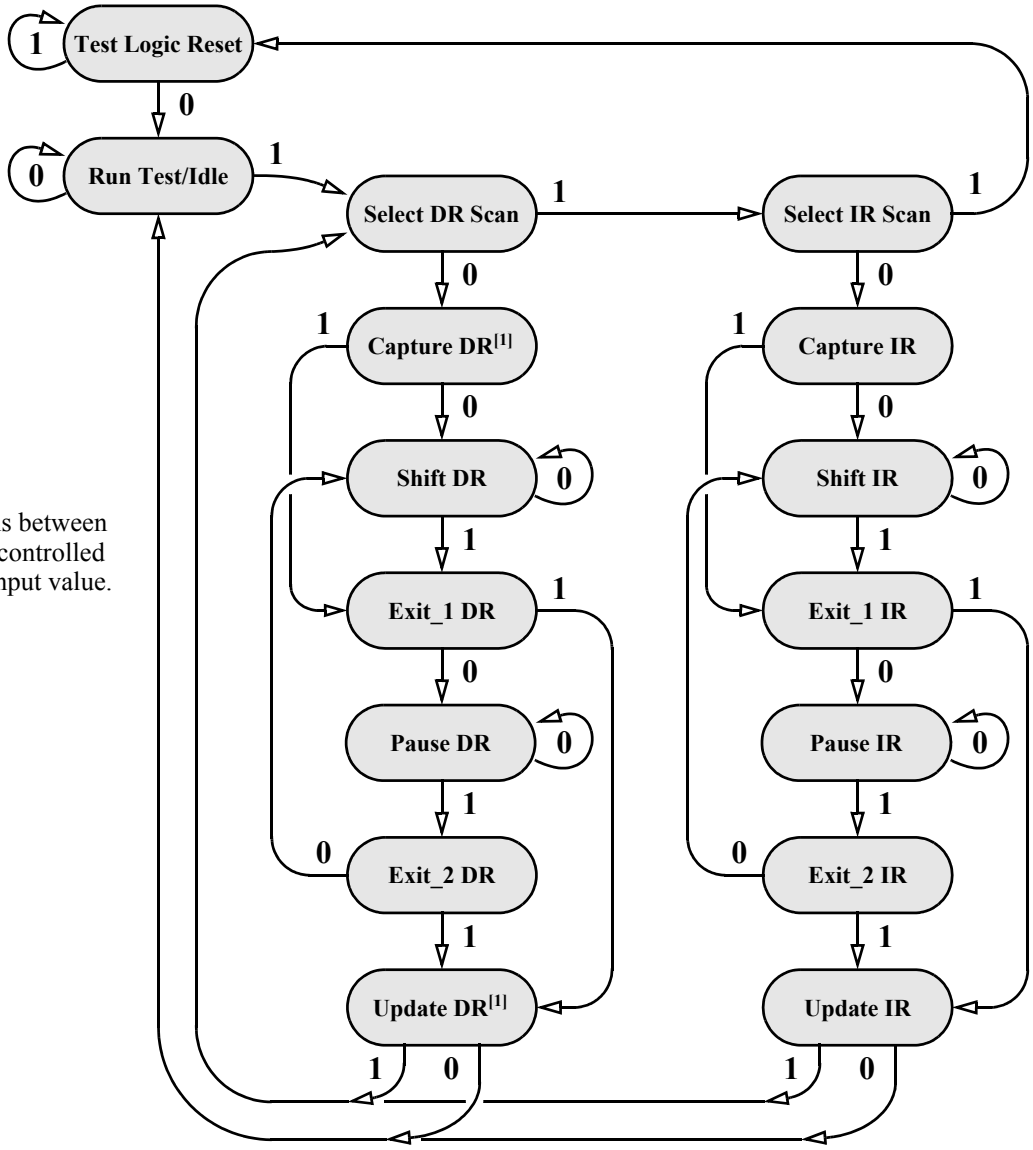


TAP Controller

The TAP controller is a synchronous finite state machine (FSM) which controls the sequence of operations of the JTAG test circuitry, in response to changes at the JTAG bus. (Specifically, in response to changes at the TMS input with respect to the TCK input.)

The TAP controller FSM implements the state (16 states) diagram as detailed in the following diagram. The IR is a 3-bit register which allows a test instruction to be shifted into the AT697. The instruction selects the test to be performed and the test data register to be accessed. Although any number of loops may be supported by the TAP, the finite state machine in the TAP controller only distinguishes between the IR and a DR. The specific DR can be decoded from the instruction in the IR.

Figure 44. TAP - State Machine



Transitions between states are controlled by TMS input value.

Due to the scan cell layout, "Capture DR" and "Update DR" are states without associated action during the scanning of internal chains.

TAP Instructions

The following instruction are supported by the AT697 TAP.

Table 23. TAP instruction set

Binary Value	Instruction Name	Data Register	Scan Chain Accessed
000	EXTEST	Boundary scan register	Boundary scan chain
001	SAMPLE/PRELOAD	Boundary scan register	Boundary scan chain
010	BYPASS	Bypass register	Bypassscan chain
111	IDCODE	Device id register	ID register scan chain

BYPASS

This instruction is binary coded "010"

It is used to speed up shifting at board level through components that are not to be activated.

EXTEST

This instruction is binary coded "000"

It is used to test connections between components at board level. Components output pins are controlled by boundary scan register during Capture DR on the rising edge of TCK.

SAMPLE/PRELOAD

This instruction is binary coded "001"

It is used to get a snapshot of the normal operation by sampling I/O states during Capture DR on the rising edge of TCK. It allows also to preload a value on the output latches during Update DR on falling edge of TCK. It do not modify system behaviour.

IDCODE

This instruction is binary coded "111"

Value of the IDCODE is loaded during Capture DR.

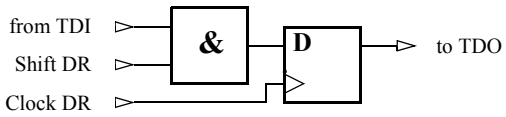
Test Data Registers

The following data registers are supported in the AT697 TAP:

Bypass Register

Bypass register containing a single shift register stage is connected between TDI and TDO.

Figure 45. Bypass Register Cell



Device ID register

Device ID register is a read only 32-bit register. It is connected between TDI and TDO.

Figure 46. Device ID Register

31 28	27 12	11 1	0
Vers.	**Part ID**	**Manufacturer's ID**	**Const.**
0001	1011 . 0110 . 0100 . 0101	000 . 0101 . 1000	1

ID. register value: 0x 1b64 50b1

Field Definitions:

[31:28]: Vers - Version number - 0x1

[27:12]: Part ID - Represent part number as assigned by Vendor- 0x b645

[11:01]: Manufacturer's ID - Represent manufacturer's ID as per JEDEC - 0x 058

[0]: Const - Constant tied to logic '1'.

Boundary Scan Register

A single scan chain consisting of all of the boundary scan cells (input, output and in/out cells).

- The purpose of the boundary scan is the support of scan-based board testing.

Boundary Scan register is connected between TDI and TDO.

To use the boundary scan feature, the PLL will be in bypass mode, i.e. BYPASS signal direction to VCC.

Checker Scan Register

A single scan chain consisting of all of the scan cells of IU parity checkers. The checkers scan is only used for factory test. Checkers scan register is connected between TDI and TDO.

Execution Mode

Reset Mode

When the RESET input is asserted for at least two cycles, the processor enters reset mode. Under this mode, the CPU and all the peripherals are halted. Only the following registers are affected by the reset. All other registers maintain their value or are undefined.

Table 24. Reset Operation

Register	Description	Reset Value
PC	program counter	0x0000 0000
nPC	new program counter	0x0000 0004
PSR	processor status register	et = 0 s = 1
CCR	cache control register	0x0000 0000
MCFG1[9:8]	PROM bus width	PIO[1:0]
MCFG3[8]	PROM EDAC enable	PIO[2]

When RESET is deasserted, execution restarts from address 0.

Debug Mode

Debug mode can be entered when the DSU is enabled through the external DSUEN pin. This allows read/write access to all processor registers and caches memories. In debug mode, the processor pipeline is held and the processor is controlled by the DSU.

Power-down/Idle Mode

AT697 can be idled by writing any value to the power-down register. During power-down mode, only the integer unit is halted. All other functions and peripherals operate as nominal.

When a single write to the idle register is performed, idle mode is entered on the next load instruction. Idle mode is terminated when an unmasked interrupt with higher level than the current processor interrupt level is pending. Then, the integer unit is re-enabled.

Here is a simple example allowing Idle mode entry :

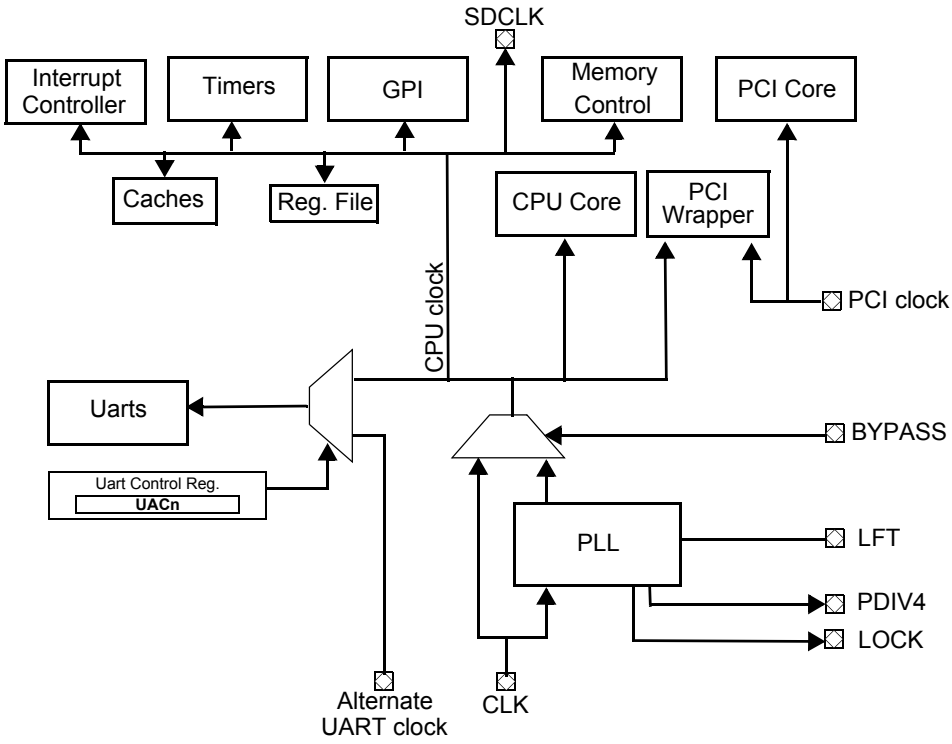
```
! write any value to Idle register
st %g2,[%g1 + 0x18]
! enter Idle mode
ld [%o1 + 0x08],%g3
```

System Clock

Overview

The AT697 clock system is mainly based on two main clock trees : the PCI clock and the CPU clock. The following figure presents the clock system of the processor and its distribution.

Figure 47. Clock Distribution



PCI Clock

The PCI clock is dedicated to the PCI Interface. It is used in particular by the PCI wrapper that shares its activity between the two clock domains.

External Clock

The PCI interface and its associated wrapper can only be driven from an external clock. The PCI clock shall be connected to the PCI_CLK pin of the PCI interface. This input shall be driven at a frequency in the range of 0 up to 33MHz.

CPU Clock

The CPU clock is routed to the parts of the system concerned with operation of the SPARC core. Examples of such modules are the CPU core itself, the register files... The CPU clock is also used by the majority of the I/O modules like Timers, Memory controller, Interrupt Controller, with the exception of the PCI Interface.

The CPU clock is driven either directly by an external oscillator or by the internal PLL.

External Clock

To drive the device directly from an external clock source, the CLK input shall be driven by an external clock generator while the BYPASS pin is driven high. In that way, the CPU clock is the direct representation of the clock applied to CLK.

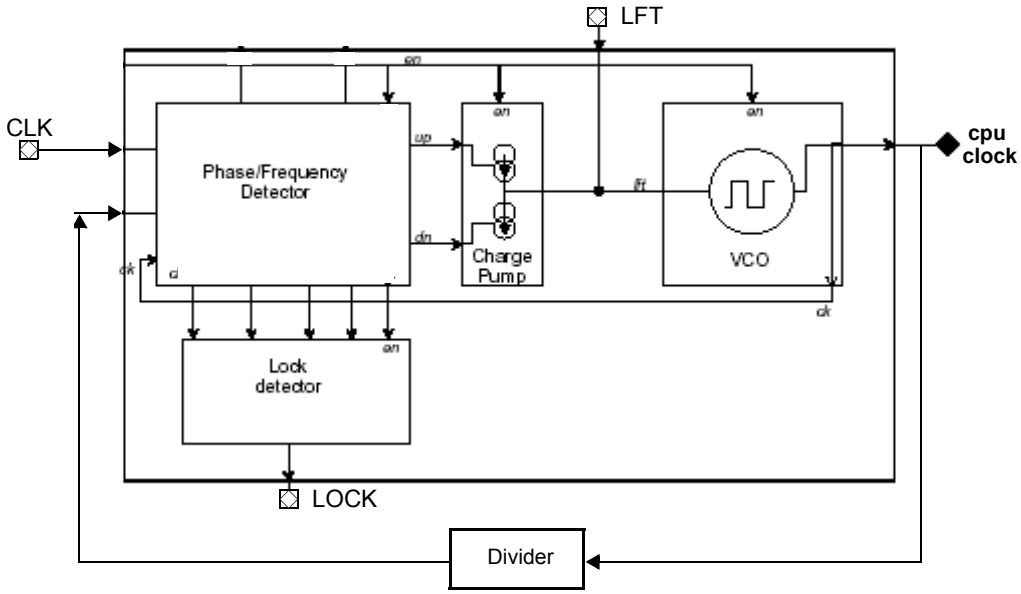
When the external CPU clock source is selected, the clock input can be driven at a frequency in the range of 0MHz up to 100MHz.

PLL

Overview

The CPU clock can be issued from the internal PLL. This PLL contains a phase/frequency detector, charge pump, voltage control oscillator, lock detector and divider.

Figure 48. PLL Block Diagram



The PLL implemented is configured by hardware to provide a cpu clock frequency four times the frequency of the input clock.

PLL control

The PLL control is done by hardware through dedicated ports, including a bypass, a clock input and a filter input.

The following table presents the assignement and functions of the PLL control signals.

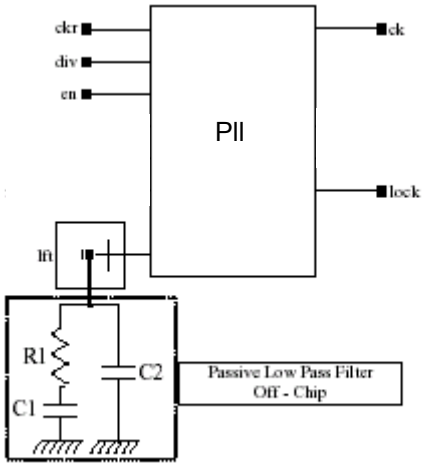
Table 25. PLL ports description

Pin name	Function
LFT	External passive loop filter input
LOCK	Lock
CLK	Board clock input
BYPASS	Bypass

PLL filter

To ensure the functionality of the PLL, an external low pass filter shall be connected to the filter input (LFT) of the PLL. Here is a presentation of the filter to setup on the LFT pin.

Figure 49. Low Pass Filter Connection



The optimal value for this filter are the following:

- R1 = 100 ohms +/- 10%
- C1 = 100nF +/- 10%
- C2 = 10nF +/- 10%

Operation

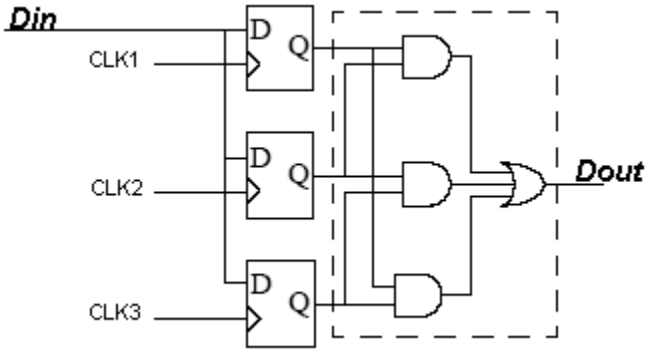
To drive the device from the internal PLL, the CLK input shall be driven by an external clock generator while the BYPASS pin is driven low. In that way, the CPU clock frequency is four time the frequency of the clock applied to CLK.

When the PLL based CPU clock source is selected, the clock input shall be driven at a frequency in the range of 20MHz up to 25MHz.

Fault Tolerance & Clock

To prevent erroneous operations from single event transient (SET) errors and single event upset (SEU), the AT697 processor is based on full triple modular redundancy (TMR) architecture.

Figure 50. TMR structure



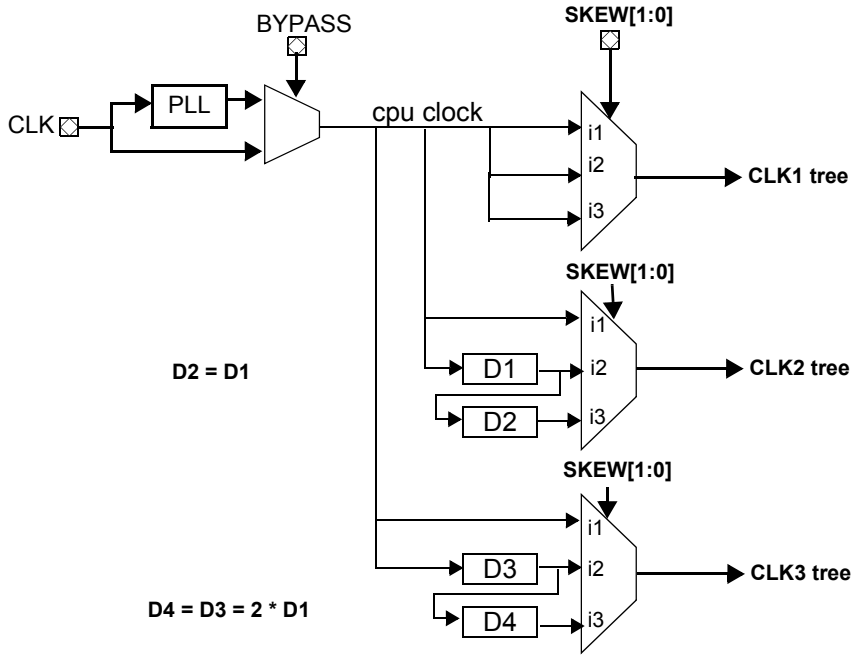
Such architecture is based on a fully triplicated clock distribution (CLK1, CLK2 and CLK3). In that way, each one of the PCI clock and the cpu clock are build as three-clock trees.

Skew

To prevent the processor from corruption by single event transient (SET) phenomenon, additional skew can be programmed on the clock trees. The two dedicated pins SKEW1 and SKEW0 are used to program the delay induced by the skew.

Here is a short description of the skew implementation :

Figure 51. CPU clock tree overview



Three configuration of skew are available :

- SKEW[1:0] = ’00’ : natural skew corresponding to the intrinsec routage of the chip
- SKEW[1:0] = ’01’ : medium skew ‘artificially’ injected
- SKEW[1:0] = ’10’ : maximum skew ‘artificially’ injected

The remaining configuration (SKEW[1:0] = ’11’) is reserved and must not be used at application level.

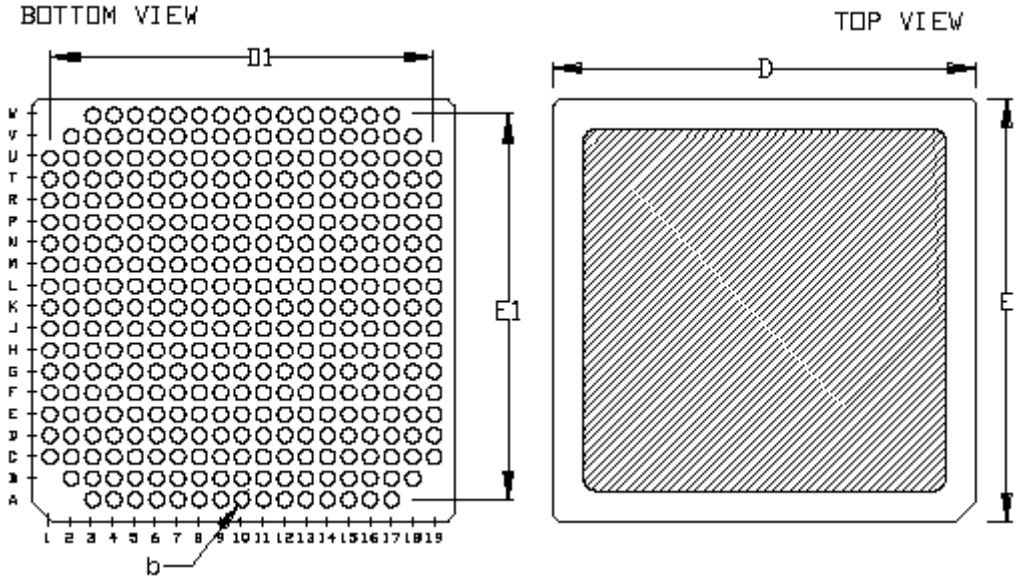
Table 26. SKEW assignements

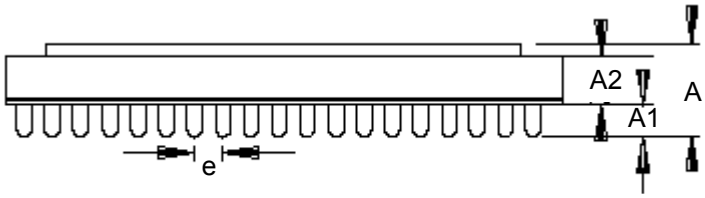
SKEW[1:0]	DELAY		Comments
	CLK1 -> CLK2	CLK1 -> CLK3	
‘00’	natural	natural	natural skew
‘01’	D1	D3	medium skew
‘10’	D1 + D2	D3 + D4	maximum skew
‘11’	Reserved		

Use of a high level of skew improves the efficiency of SET prevention but leads to an operating loss performance. Maximum speed is decreased and timings on the interfaces are slower than with natural skew. Refer to the ’Electrical Characteristics’ section for detailed timings at each skew.

Package - MCGA 349

Mechanical Outlines





	mm		inch	
	min	max	min	max
D/E	24,8	25,2	0,976	0,992
D1/E1	22,86		0,9	
A1	1,4	1,85	0,055	0,073
A2	2,4	3,45	0,094	0,136
A	4,3	5,9	0,169	0,232
b	0,79	0,99	0,031	0,04
e	1,27		0,05	

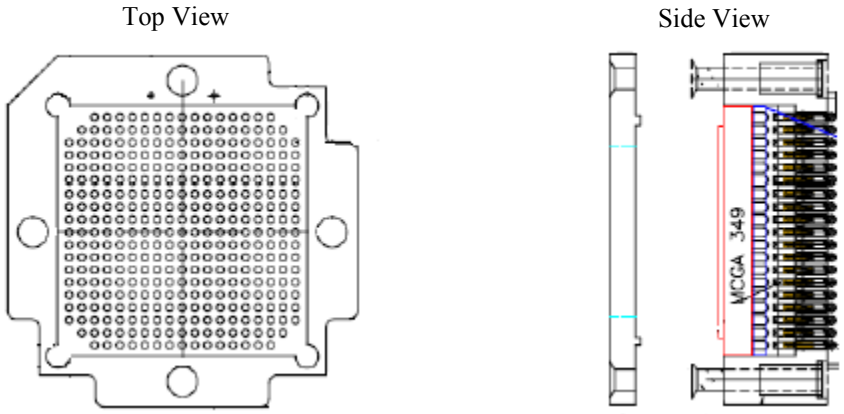
Socket / Adapter

In order to support MCGA 349 package on evaluation board that may require exchange of the chip, ATMEL had a dedicated socket developped by Adapters-Plus.

Socket reference

The reference of the socket for the MCGA349 package is **CL349SA1912F**.

Figure 52. CL349SA1912E socket



A direct link to information on this socket is available at: **http://www.adapt-plus.com/products/ic_sockets/datasheets/ds_MCGA_lockingskt.htm**

Provider

The **CL349SA1912F** socket is provided by Adapters-Plus :

Adapters-Plus

15 W 8TH STREET STE B.

Tracy, Ca 95376 - USA

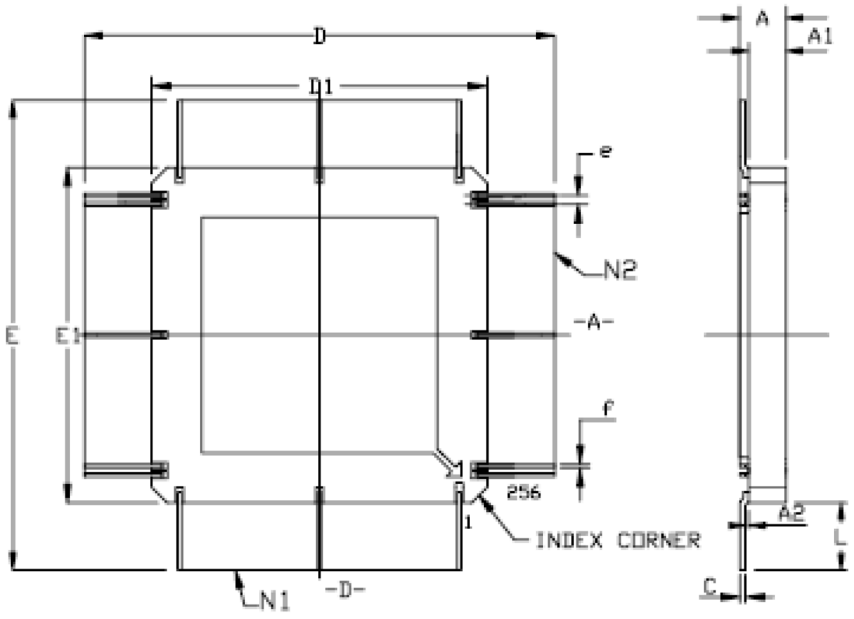
Phone: 209-839-0200

Fax: 209-839-0235

www.adapt-plus.com

QFP256 package

Package Description



	mm		mils	
	Min	Max	Min	Max
A	2. 41	3. 18	. 095	. 125
C	0. 10	0. 20	. 004	. 008
D	53. 23	55. 74	2. 095	2. 195
D1	36. 83	37. 34	1. 450	1. 470
E	53. 23	55. 74	2. 095	2. 195
E1	36. 83	37. 34	1. 450	1. 470
e	0. 508 BSC		. 020 BSC	
f	0. 15	0. 25	. 006	. 010
A1	2. 06	2. 56	. 081	. 101
A2	0. 05	0. 36	. 002	. 014
L	8. 20	9. 20	. 323	. 362
N1	64		64	
N2	64		64	

Registers Description

Table 27. Register legend

Address = 0x01010101

Bit Number	31	30	29	28	27	26	25	24	23	...	...	...	...	9	8	7	6	5	4	3	2	1	0
field name	field				reserved										bit								
access type	r=read access				w=write acces										r/w=read and write access								
default value after reset	0	100			1	x = undefined or non affected by reset																	

Integer Unit Registers

Table 28. Processor State Register- PSR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
impl				ver				n	z	v	c	reserved						ec	ef	pil				s	ps	et	cwp				
r				r				r/w				r/w						r	r	r/w				r/w			r/w				
0001				0001				x	x	x	x	xxxxxx						0	x	xxxx				1	x	0	xxxxx				

Bit Number	Mnemonic	Description
31..28	impl	Implementation or class of implementations of the architecture.
27..24	ver	Identify one or more particular implementations or is a readable and writable state field whose properties are implementation-dependent.
23	n	indicates whether the ALU result was negative for the last instruction modifying *icc* field. 1 = negative 0 = not negative.
22	z	indicates whether the ALU result was zero for the last instruction modifying *icc* field. 1 = zero 0 = not zero.
21	v	indicates whether the ALU result was within the range of (was representable in) 32-bit 2's complement notation for the last instruction that modified the *icc* field. 1 = overflow, 0 = no overflow.
20	c	indicates whether a 2's complement carry out (or borrow) occurred for the last instruction that modified the *icc* field. Carry is set on addition if there is a carry out of bit 31. Carry is set on subtraction if there is borrow into bit 31. 1 = carry, 0 = no carry.
13	ec	determines whether the implementation-dependent oprocessor is enabled. If disabled, a coprocessor instruction will trap. 1 = enabled, 0 = disabled. If an implementation does not support a coprocessor in ardware, PSR.EC should always read as 0 and writes to it should be ignored.
12	ef	determines whether the FPU is enabled. If disabled, a floating-point instruction will trap. 1 = enabled, 0 = disabled. If an implementation does not support a hardware FPU, PSR.EF should always read as 0 and writes to it should be ignored.
11..8	pil	identify the interrupt level above which the processor will accept an interrupt.

Bit Number	Mnemonic	Description
7	s	determines whether the processor is in supervisor or user mode. 1 = supervisor mode, 0 = user mode.
6	ps	contains the value of the S bit at the time of the most recent trap.
5	et	determines whether traps are enabled. A trap automatically resets ET to 0. When ET=0, an interrupt request is ignored and an exception trap causes the IU to halt execution, which typically results in a reset trap that resumes execution at address 0. 1 = traps enabled, 0 = traps disabled.
4..0	cwp	comprise the current window pointer, a counter that identifies the current window into the r registers. The hardware decrements the CWP on traps and SAVE instructions, and increments it on RESTORE and RETT instructions (modulo NWINDOWS).

Table 29. Window Invalid Mask - WIM

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								windows							
																								7	6	5	4	3	2	1	0
r																								r/w							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1

Bit	Mnemonic	Description
0 < n < 7	windows[n]	Indicated wether the window is a ‘valid’ or an ‘invalid’ one. ‘0’ : valid ‘1’ : invalid

The WIM can be read by the privileged RDWIM instruction and written by the WRWIM instruction.

Table 30. Y Register - Y

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
y																															
r/w																															
xxxx xxxx																															

The Y register can be read and written with the RDY and WRY instructions.

Table 31. Trap Base Address - TBR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
tba																				tt								reserved			
r/w																				r								r/w			
x																												0	0	0	0

Bit Number	Mnemonic	Description
31..12	tba	Trap Base Address This field contains the most-significant 20 bits of the trap table address.
11..4	tt	Trap Type This eight-bit field is written by the hardware when a trap occurs, and retains its value until the next trap. It provides an offset into the trap table.

The tba field is written by the WRTBR instruction. Use of WRTBR is don't care for tt field.

Table 32. Program Counters - PC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
address																															
0x0000 0000																															

The 32-bit PC contains the address of the instruction currently being executed by the IU.

When a trap occurs, the PC address is saved in the local register (l1). When returning from trap, l1 value is copied back to PC.

Table 33. New Program Counters - nPC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
address																															
0x0000 0004																															

The nPC holds the address of the next instruction to be executed (assuming a trap does not occur).

When a trap occurs, the nPC address is saved in the local register (l2). When returning from trap, l2 value is copied back to nPC.

Table 34. Watch Point Address Registers
Address : %asr24, %asr26, %asr28, %asr30

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
waddr																														reserved	if
r/w																														r	r/w
xxxx xxxx																														0	0

Bit	Mnemonic	Description
31..2	waddr	Defines the addresses range to be watched

Bit	Mnemonic	Description
0	if	Enable hit generation on instruction fetch 0 = disabled 1 = enabled

These registers are accessed using the RDASR/WRASR instructions

Table 35. Watch Point Mask registers
Address :%asr25, %asr27, %asr29, %asr31

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
wmask																														dl	ds
r/w																														r/w	r/w
xxxx xxxx																														0	0

Bit	Mnemonic	Description
31..2	wmask	Defines which bits are to be compared to waddr. 0 = comparison disabled 1 = comparison enabled
1	dl	Enable hit generation on data load 0 = disabled 1 = enabled
0	ds	Enable hit generation on data store 0 = disabled 1 = enabled

These registers are accessed using the RDASR/WRASR instructions

Table 36. Register File Protection Control Register
Address :%asr16

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																				cnt			tcb							te	di
r																				r/w			r/w							r/w	r/w
xxxx x																				000			x							0	0

Bit	Mnemonic	Description
11..9	cnt	Error counter. Incremented for each corrected error
8..2	tcb	Test checkbits
1	te	EDAC test enable 0 = disabled 1 = enabled

Bit	Mnemonic	Description
0	di	Disable EDAC function 1 = disabled 0 = enabled

This register is accessed using the RDASR/WRASR instructions.

Table 37. Window Registers

Type	Name	Definition
in	i7	return address
	i6	frame pointer
	i5	incoming parameter register 5
	i4	incoming parameter register 4
	i3	incoming parameter register 3
	i2	incoming parameter register 2
	i1	incoming parameter register 1
	i0	incoming parameter register 0
local	l7	local register 7
	l6	local register 6
	l5	local register 5
	l4	local register 4
	l3	local register 3
	l2	nPC (for RETT)
	l1	PC (for RETT)
	l0	local register 0
out	o7	temp
	o6	stack pointer
	o5	outgoing parameter register 5
	o4	outgoing parameter register 4
	o3	outgoing parameter register 3
	o2	outgoing parameter register 2
	o1	outgoing parameter register 1
	o0	outgoing parameter register 0

Table 37. Window Registers

Type	Name	Definition
global	g7	global register 7
	g6	global register 6
	g5	global register 5
	g4	global register 4
	g3	global register 3
	g2	global register 2
	g1	global register 1
	g0	global register 0 - always 0x00000000

Floating Point Unit Registers

Table 38. FPU Status register - FSR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rd		reserved		tem					ns	reserved		ver			ftt			reserved		fcc		aexc					cexc				
				nvm	ofm	ufm	dzm	nxm														nva	ofa	ufa	dza	nxa	nvc	ofc	ufc	dzc	nxc
r/w		r/w		r/w					r	r/w		r			r			r/w		r		r					r				
xx		xx		00000					x	xx		001			xxx			xx		xxx		xxxxx					00000				

Bit Number	Mnemonic	Description
31..30	rd	Rounding Direction Defines the rounding direction used by the AT697 FPU during a floating-point arithmetic operation.
27..23	tem	Trap Enable Mask *tem* field enable*s* traps caused by FPops. These bits are ANDed with the bits of the *cexc* (current exception field) to determine whether to force a floating-point exception to IU. All trap enable fields correspond to the similarly named bit in the *cexc* field. 0 = trap disabled 1 = trap enabled
22	ns	Causes the FPU to produce implementation-defined results that may not correspond to ANSI/IEEE Standard 754-1985. For instance, to obtain higher performance, implementations may convert a subnormal floatingpoint operand or result to zero when NS is set.
19..17	ver	Identify one or more particular implementations of the FPU architecture. For each SPARC IU implementation there may be one or more FPU implementations, or none. This field identifies the particular FPU implementation present.
16..14	ftt	Floating point trap type Identify floating-point exception trap types.when floating point exception occurs, the *ftt* field encodes the type of floating-point exception until an STFSR or another FPop is executed.

Bit Number	Mnemonic	Description
11..10	fcc	Contain the FPU condition codes. These bits are updated by floating-point compare instructions (FCMP and FCMPE). They are read and written by the STFSR and LDFSR instructions, respectively. FBfcc bases its control transfer on this field.
9..5	aexc	Accumulate IEEE floating-point exceptions while fp_exception traps are disabled using the TEM field. After an FPop completes, the TEM and *cexc* fields are logically *and*ed together. If the result is nonzero, an fp_exception trap is generated; otherwise, the new *cexc* field is *or*'d into the *aexc* field. Thus, while traps are masked, exceptions are accumulated in the *aexc* field.
4..0	cexc	Indicate that one or more IEEE floating-point exceptions were generated by the most recently executed FPop instruction. The absence of an exception causes the corresponding bit to be cleared.

Trap Types

The *ftt* field can be read by the STFSR instruction. An LDFSR instruction does not affect *ftt field*.

Table 39. Trap Type Definition

TT	Name	Description
0	none	No trap.
1	IEEE_exception	An IEEE_754_exception floating-point trap type indicates that a floating-point exception occurred that conforms to the ANSI/IEEE Standard 754-1985. The exception type is encoded in the *cexc* field.
2	Unfinished_FPop	An unfinished_FPop indicates that an implementation's FPU was unable to generate correct results or exceptions
3	unimplemented_FPop	An unimplemented_FPop indicates that an implementation's FPU decoded an FPop that it does not implement. In this case, the *cexc* field is unchanged
4	sequence_error	A sequence_error indicates one of three abnormal error conditions in the FPU, all caused by erroneous supervisor software: - An attempt was made to execute a floating-point instruction when the FPU was not able to accept one. This type of sequence_error arises from a logic error in supervisor software that has caused a previous floating-point trap to be incompletely serviced (for example, the floating-point queue was not emptied after a previous floating-point exception). - An attempt was made to execute a STDFQ instruction when the floatingpoint deferred-trap queue (FQ) was empty, that is, when FSR.*qne* = 0. (Note that generation of sequence_error is recommended, but not required in this case)
5	hardware error	A hardware_error indicates that the FPU detected a catastrophic internal error, such as an illegal state or a parity error on an *f* register access. If a hardware_error occurs during execution of user code, it may not be possible to recover sufficient state to continue execution of the user application.
6	invalid register	An invalid_fp_register trap type indicates that one (or more) operands of an FPop are misaligned, that is, a double-precision register number is not 0 mod 2, or a quadruple-precision register number is not 0 mod 4. It is recommended that implementations generate an fp_exception trap with FSR.*ftt* = invalid_fp_register in this case, but an implementation may choose not to generate a trap.

Floating Point Condition Code

Table 40. FCC Field Definition

FCC	Description
0	$f_{rs1} = f_{rs2}$
1	$f_{rs1} < f_{rs2}$
2	$f_{rs1} > f_{rs2}$

FCC	Description
3	f_{rs1} ? f_{rs2} indicates an unordered relation, which is true if either f_{rs1} or f_{rs2} is a signaling NaN or quiet NaN

Note: *f rs1* and *f rs2* correspond to the single, double, or quad values in the *f* registers specified by an instruction's *rs1* and *rs2* fields. Note that *fcc* is unchanged if FCMP or FCMPE generates an IEEE_exception trap.

Floating Point Exception Fields The current and accrued exception fields and the trap enable mask assume the following definitions of the floating-point exception conditions.

Table 41. Exception Fields

Aexc Mnemonic	Cexc Mnemonic	Name	Description
nva	nvc	Invalid	An operand is improper for the operation to be performed. 1 = invalid operand, 0 = valid operand(s). Examples : 0 ÷ 0, ∞ – ∞ are invalid.
ofa	ofc	Overflow	The rounded result would be larger in magnitude than the largest normalized number in the specified format. 1 = overflow, 0 = no overflow.
ufa	ufc	Underflow	The rounded result is inexact and would be smaller in magnitude than the smallest normalized number in the indicated format. 1 = underflow, 0 = no underflow. Underflow is never indicated when the correct unrounded result is zero. if **UFM=0** : The *ufc* and *ufa* bits will be set if the correct unrounded result of an operation is less in magnitude than the smallest normalized number and the correctly-rounded result is inexact. These bits will be set if the correct unrounded result is less than the smallest normalized number, but the correct rounded result is the smallest normalized number. *nxc* and *nxa* are always set as well. if **UFM=1** : An IEEE_exception trap will occur if the correct unrounded result of an operation would be smaller than the smallest normalized number. A trap will occur if the correct unrounded result would be smaller than the smallest normalized number, but the correct rounded result would be the smallest normalized number.
dza	dzc	Div_by_zero	X÷0, where X is subnormal or normalized. Note that 0 ÷ 0 does **not** set the *dzc* bit. 1 = division-by-zero, 0 = no division-by-zero.
nxa	nxc	Inexact	The rounded result of an operation differs from the infinitely precise correct result. 1 = inexact result, 0 = exact result.

Table 42. f registers - fx (0 < x < 31)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
fx																															

Memory Interface

Registers

Table 43. Memory Configuration Register 1 - MCFG1

Address = 0x80000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved			iowdh		brdyn	bexcn	reserved	iows				iop	reserved	prbsz				reserved		prwen	reserved	prwdh		prwws				prrws			
r/w			r/w		r/w	r/w	r/w	r/w				r/w	r/w	r/w				r/w		r/w	r/w	r/w		r/w				r/w			
xxx			xx		x	x	x	xxx				x	x	xxxx				xx		x	x	xx		1111				1111			

Bit Number	Mnemonic	Description
28:27	iowdh	I/O bus width. Defines the data with of the I/O area (“00”=8, “01”=16, “10”=32).
26	brdyn	Bus ready enable for I/O area
25	bexcn	Bus error enable.
23:20	iows	I/O waitstates. Defines the number of waitstates during I/O accesses (“0000”=0, “0001”=1, “0010”=2,..., “1111”=15).
19	iop	I/O protection. ‘0’ : Read and write accesses to I/O area are disabled ‘1’ : Read and write accesses to I/O area are enabled.
17:14	prbsz	Prom bank size (*) Used when in 8 bit PROM mode Defines the size of PROM bank (“0000”=8 Kbyte, “0001”=16 Kbyte... “1111”=256 Mbyte).
11	prwen	Prom write enable. If set, enables write cycles to the prom area.
9:8	prwdh	Prom width. Defines the data with of the prom area (“00”=8, “01”=16, “10”=32).
7:4	prwws	Prom write waitstates. Defines the number of waitstates during prom write cycles (“0000”=0, “0001”=2,... “1111”=30).
3:0	prrws	Prom read waitstates. Defines the number of waitstates during prom read cycles (“0000”=0, “0001”=2,... “1111”=30).

During power-up, the prom width (bits [9:8]) are set with value on PIO[1:0] inputs. The prom waitstates fields are set to 15 (maximum). External bus error and bus ready are disabled. All other fields are undefined.

Note: The last 25% of the prom bank size are used to store EDAC checksums when EDAC is enabled in 8 bit mode.

Table 44. Memory Configuration Register 2 - MCFG2

Address = 0x80000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
sdrref	trp	trfc			*sdrcas*	*sdrbs*			sdrcls		sdrcmd		reserved				se	si	rambs				reserved	brdy	rmw	ramwdh		ramwws		ramrws	
r/w	r/w	r/w			r/w	r/w			r/w		r/w		r/w				r/w	r/w	r/w				r/w	r/w	r/w	r/w		r/w		r/w	

Table 44. Memory Configuration Register 2 - MCFG2
Address = 0x80000004

x	x	xxx	x	xxx	xx	xx	xxxx	x	x	xxxx	x	x	x	xx	xx	xx

Bit Number	Mnemonic	Description
31	sdrref	SDRAM refresh. If set, the SDRAM refresh will be enabled.
30	trp	SDRAM tRP timing. tRP will be equal to 2 or 3 system clocks (0/1).
29:27	trfc	SDRAM tRFC timing. tRFC will be equal to 3 + field-value system clocks.
26	sdrcas	SDRAM CAS delay. Selects 2 or 3 cycle CAS delay (0/1). When changed, a LOAD-COMMAND - REGISTER command must be issued at the same time. Also sets RAS/CAS delay (tRCD).
25:23	sdrbs	SDRAM banks size. Defines the banks size for SDRAM chip selects: “000”=4 Mbyte, “001”=8 Mbyte, “010”=16 Mbyte .... “111”=512 Mbyte.
22:21	sdrcls	SDRAM column size. “00”=256 when *sdrbs* = “111” “01”=512 when *sdrbs* = “111” “10”=1024 when *sdrbs* = “111” “11”=4096 when *sdrbs* = “111” “2048 otherwise“
20:19	sdrcmd	SDRAM command. Writing a non-zero value will generate an SDRAM command: “01”=PRECHARGE, “10”=AUTO-REFRESH, “11”=LOAD-COMMAND-REGISTER. The field is reset after command has been executed.
14	se	SDRAM enable. If set, the SDRAM controller will be enabled.
13	si	SRAM disable. If set together with bit 14 (SDRAM enable), the static ram access will be disabled.
12:9	rambs	SRAM bank size. Defines the size of each ram bank (“0000”=8 Kbyte, “0001”=16 Kbyte... “1111”=256 Mbyte).
7	brdy	Bus ready enable. If set, will enable BRDYN for ram area
6	rmw	Read-modify-write. Enable read-modify-write cycles on sub-word writes to 16- and 32-bit areas with common write strobe (no byte write strobe).
5:4	ramwdh	SRAM bus width. Defines the data with of the SRAMarea (“00”=8, “01”=16, “1X”= 32).
3:2	ramwws	SRAM write waitstates. Defines the number of waitstates during SRAM write cycles (“00”=0, “01”=1, “10”=2, “11”=3).
1:0	ramrws	SRAM read waitstates. Defines the number of waitstates during SRAM read cycles (“00”=0, “01”=1, “10”=2, “11”=3).

Table 45. Memory Configuration Register 3 - MCFG3
Address = 0x80000008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rfc		reserved		me	*srcrv*															wb	*rb*	re	pe	tcb							
r		r/w		r	r/w															r/w	r/w	r/w	r/w	r/w							
11		xx		1	xxx xxxx xxxx xxxx															x	x	x	x	xxxx xxxx							

Bit Number	Mnemonic	Description
31:30	rfc	Register file check bits. Indicates how many checkbits are used for the register file (11=7 (EDAC))
27	me	Memory EDAC Indicates if a memory EDAC is present
26:12	srcrv	SDRAM refresh counter reload value.
11	wb	EDAC diagnostic write bypass
10	rb	EDAC diagnostic read bypass
9	re	RAM EDAC enable. Enable EDAC checking of the RAM area
8	pe	PROM EDAC enable. Enable EDAC checking of the PROM area. At reset, this bit is initialised with the value of PIO[2]
7:0	tcb	Test checkbits. This field replaces the normal checkbits during store cycles when WB is set. TCB is also loaded with the memory checkbits during load cycles when RB is set.

The period between each AUTO-REFRESH command is calculated as follows:

tREFRESH = ((reload value) + 1) / SYSCLK

Table 46. Write Protection Register 1 - WPR1
Address = 0x8000001C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
en	bp	tag[14:0]															mask[14:0]														
r/w	r/w	r/w															r/w														
x	x	xx xxxx xxxx xxxx x															xxx xxxx xxxx xxxx														

Bit Number	Mnemonic	Description
31	en	Enable. If set, enables the write protect unit
30	bp	Block protect If set, selects block protect mode

Bit Number	Mnemonic	Description
29..15	tag	Address tag This field is compared against address(29:15)
14..0	mask	Address mask this field contains the address mask

Table 47. Write Protection Register 2 - WPR2
Address = 0x80000020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
en	bp	tag[14:0]															mask[14:0]														
r/w	r/w	r/w															r/w														
x	x	xx xxxx xxxx xxxx x															xxx xxxx xxxx xxxx														

Bit Number	Mnemonic	Description
31	en	Enable. If set, enables the write protect unit
30	bp	Block protect If set, selects block protect mode
29..15	tag	Address tag This field is compared against address(29:15)
14..0	mask	Address mask this field contains the address mask

System Registers

Table 48. Product Configuration Register - PCR
Address = 0x80000024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved	dsu	sdrctrl	wtpnb			imac	nwindows					icsz			ilsz		dcsz			dlsz		divinst	mulinst	reserved	memstat	fpu		pci		wprt	
r/w	r	r	r			r	r					r			r		r			r		r	r	r/w	r	r		r		r	
x	1	1	100			0	00111					100			11		100			11		1	1	x	1	01		01		01	

Bit Number	Mnemonic	Description
30	dsu	Debug support unit “0”=disabled “1”=present
29	sdrctrl	SDRAM controller present “0”=disabled “1”=present
28..26	wtpnt	Number of implemented watchpoints (0 - 4)
25	imac	UMAC/SMAC instruction implemented
24..20	nwindows	Number of register windows. The implemented number of SPARC register windows - 1
19..17	icsz	Instruction cache size. The size (in Kbytes) of the instruction cache. Cache size = 2ICSZ.
16..15	ilsz	Instruction cache line size. The line size (in 32-bit words) of each line. Line size = 2ILSZ.
14..12	dcsz	Data cache size. The size (in kbytes) of the data cache. Cache size = 2DCSZ.
11..10	dlsz	Data cache line size. The line size (in 32-bit words) of each line. Line size = 2DLSZ.
9	divinst	UDIV/SDIV instruction implemented
8	mulinst	UMUL/SMUL instruction implemented
6	memstat	Memory status and failing address register present
5..4	fpu	FPU type
3..2	pci	PCI core type
1..0	wprt	Write protection type

Table 49. Fail Address Register - FAILAR
Address = 0x8000000C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 49. Fail Address Register - FAILAR
Address = 0x8000000C

fa
r
xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx

Bit Number	Mnemonic	Description
31:0	fa	Failing Address This field contents the address of the access that triggered an error response. This register is updated each time an error occurs in the internal bus.

Table 50. Fail Status Register - FAILSR
Address = 0x80000010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																						ce	ne	rw	hmaster				hsize		
r/w																						r/w	r/w	r	r				r		
xxxxxxxxxxxxxxx																						0	0	0	0	0	0	0	0	0	0

Bit Number	Mnemonic	Description
9	ce	Correctable error detected by EDAC.
8	ne	New error. Set when a new error occurred. After an error, this bit has to be reset by software
7	rw	Read/Write. This bit is set if the failed access was a read cycle, otherwise it is cleared.
6...3	hmaster	AHB master. This field contains the HMASTER[3:0] of the failed access.
2..1	hsize	Transfer Size. This filed contains the HSIZE[2:0] of the failed transfer.

Caches Register

Table 51. Cache Control Register - CCR

Address = 0x80000014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
drepl		irepl		dsets		isets		ds	fd	fi	cpc		cpte		ib	ip	dp	ite		ide		dte		dde		df	if	dcs		ics	
r		r		r		r		r/w	r/w	r/w	r		r		r/w	r	r	r/w		r/w		r/w		r/w		r/w	r/w	r/w		r/w	
11		11		01		11		x	0	0	10		xx		x	x	x	00		00		00		00		x	x	xx		xx	

Bit Number	Mnemonic	Description
31.30	drepl	Data cache replacement policy ‘11’ - Least Recently Used (LRU)
29..28	irepl	Instruction cache replacement policy ‘11’ - Least Recently Used (LRU)
27..26	dsets	Data cache associativity Number of sets in the data cache ‘01’ - 2 way associative
25..24	isets	Instruction cache associativity Number of sets in the instruction cache ‘11’ - 4 way associative
23	ds	Data cache snoop enable If set, will enable data cache snooping.
22	fd	Flush data cache If set, will flush the instruction cache. Always reads as zero.
21	fi	Flush Instruction cache If set, will flush the instruction cache. Always reads as zero.
20..19	cpc	Cache parity bits Indicates how many parity bits are used to protect the caches ‘10’ =2 parity bits
18..17	cpte	Cache parity test bits These bits are XOR’ed to the data and tag parity bits during diagnostic writes.
16	ib	Instruction burst fetch This bit enables burst fill during instruction fetch.
15	ip	Instruction cache flush pending This bit is set when an instruction cache flush operation is in progress.
14	dp	Data cache flush pending This bit is set when an data cache flush operation is in progress.
13..12	ite	Instruction cache tag error counter This filed is incremented every time an instruction cache tag parity error is detected.
11.10	ide	Instruction cache data error counter This field is incremented each time an instruction cache data sub-block parity error is detected.
9..8	dte	Data cache tag error counter This filed is incremented every time a data cache tag parity error is detected.
7..6	dde	Data cache data error counter This field is incremented each time an instruction cache data sub-block parity error is detected

Bit Number	Mnemonic	Description
5	df	Data Cache Freeze on Interrupt If set, the data cache will automatically be frozen when an asynchronous interrupt is taken.
4	if	Instruction Cache Freeze on Interrupt If set, the instruction cache will automatically be frozen when an asynchronous interrupt is taken.
3..2	dcs	Data Cache state Set and Indicates the current data cache state ‘X0’ = disabled ‘01‘ = frozen ‘11‘ = enabled
1..0	ics	Instruction Cache state Set and Indicates the current data cache state ‘X0’ = disabled ‘01’ = frozen ‘11’ = enabled.

Power Down Register

Table 52. Idle Register - IDLE

Address = 0x80000018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
idle																															
w																															
xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx																															

Bit Number	Mnemonic	Description
31..0	idle	Write only with any data. A write to this register followed by a load access will cause the system to enter power down mode

Timers Registers

Table 53. Timer 1 Counter Register - TIMC1
Address = 0x80000040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								tim1val																							
r/w								r/w																							
xxxx xxxx								xxxx xxxx xxxx xxxx xxxx xxxx																							

Bit Number	Mnemonic	Description
23..0	tim1val	Timer 1 counter value A read access gives the decounting value of the scaler.

Table 54. Timer 1 Reload Register - TIMR1
Address = 0x80000044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								tim1rld																							
r/w								r/w																							
xxxx xxxx								xxxx xxxx xxxx xxxx xxxx xxxx																							

Bit Number	Mnemonic	Description
23..0	tim1rld	*Timer 1 reload value* A write access programs the reload value of Timer 1 counter.

Table 55. Timer 1 Control Register - TIMCTR1
Address = 0x80000048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																													ld1	rl1	en1
r/w																													r/w		
xxxx xxxx xxxx xxxx xxxx xxxx xxxx x																													x	x	x

Bit Number	Mnemonic	Description
2	ld1	Load counter when written with ‘one’, will load the timer reload register into the timer counter register. Always reads as a ‘zero’.
1	rl1	Reload counter If RL is set, then the counter will automatically be reloaded with the reload value after each underflow.
0	en1	Enable counter enables the timer when set.

Table 56. Watchdog Register - WDG
Address = 0x8000004C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								wdc																							
r/w								r/w																							
xxxx xxxx								xxxx xxxx xxxx xxxx xxxx xxxx																							

Bit Number	Mnemonic	Description
23..0	wdc	*Watchdog counter.* Fixes the watchdog 'Timeout'.

The 'Timeout' is the time between the loading (or re-loading) and the watchdog interrupt. 'ResetTimeout' is greater than 'Timeout'.

Note: Reading *wdc* field gives the loading (or re-loading) value, not the effective count value.

Table 57. Timer 2 Counter Register - TIMC2
Address = 0x80000050

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								tim2val																							
r/w								r/w																							
xxxx xxxx								xxxx xxxx xxxx xxxx xxxx xxxx																							

Bit Number	Mnemonic	Description
23..0	tim2val	Timer 2 counter value A read access gives the decounting value of the scaler.

Table 58. Timer 2 Reload Register - TIMR2
Address = 0x80000054

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								tim2rld																							
r/w								r/w																							
xxxx xxxx								xxxx xxxx xxxx xxxx xxxx xxxx																							

Bit Number	Mnemonic	Description
23..0	tim2rld	*Timer 2 reload value* A write access programs the reload value of Timer 1 counter.

Table 59. Timer 2 Control Register - TIMCTR2
Address = 0x80000058

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																													ld2	rl2	en2
r/w																													r/w		
xxxx xxxx xxxx xxxx xxxx xxxx xxxx x																													x	x	x

Bit Number	Mnemonic	Description
2	ld2	Load counter when written with ‘one’, will load the timer reload register into the timer counter register. Always reads as a ‘zero’.
1	rl2	Reload counter If RL is set, then the counter will automatically be reloaded with the reload value after each underflow.
0	en2	Enable counter enables the timer when set.

Table 60. Prescaler Counter Register - SCAC
Address = 0x80000060

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																						counter value									
r/w																						r/w									
xxxx xxxx xxxx xxxx xxxx xxx																						xx xxxx xxxx									

Bit Number	Mnemonic	Description
9..0	counter value	prescaler counter value

A read access gives the decounting value of the prescaler.

Table 61. Prescaler Reload Register - SCAR
Address = 0x80000064

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																						reload value									
r/w																						r/w									
xxxx xxxx xxxx xxxx xxxx xxx																						xx xxxx xxxx									

Bit Number	Mnemonic	Description
9..0	reload value	Prescaler reload value

A write access programs the reload value of the prescaler.

A read access gives the reload value of the prescaler.

UARTs Registers

Table 62. UART 1 Data Register - UAD1
Address = 0x80000070

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								rtd1							
r/w																								r/w							
xxxx xxxx xxxx xxxx xxxx xxxx																								xxxx xxxx							

Bit Number	Mnemonic	Description
7..0	rtd1	Received or Transmitted Data of UART1

rtd1 field has 2 meanings:

- A write access enables the sending of the written 8-bit data on UART 1.
- A read access provides the received 8-bit data on UART1.

Table 63. UART 1 Status Register - UAS1
Address = 0x80000074

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																									fe	pe	ov	br	th	ts	dr
r/w																									r/w						
xxxx xxxx xxxx xxxx xxxx xxxx x																									x	x	x	x	x	x	x

Bit Number	Mnemonic	Description
6	fe	Framing error Indicates that a framing error was detected.
5	pe	Parity error indicates that a parity error was detected.
4	ov	Overrun Indicates that one or more character have been lost due to overrun.
3	br	Break received Indicates that a BREAK has been received.
2	th	Transmitter hold register empty Indicates that the transmitter hold register is empty.
1	ts	Transmitter shift register empty Indicates that the transmitter shift register is empty.
0	dr	Data ready Indicates that new data is available in the receiver holding register.

Table 64. UART 1 Control Register - UAC1
Address = 0x80000078

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 64. UART 1 Control Register - UAC1
Address = 0x80000078

reserved	ec	lb	fl	pe	ps	ti	ri	te	re
r/w	r/w								
xxxx xxxx xxxx xxxx xxxx xxx	x	x	x	x	x	x	x	x	x

Bit Number	Mnemonic	Description
8	ec	External Clock if set, the UART scaler will be clocked by PIO[3]
7	lb	Loop back If set, loop back mode will be enabled.
6	fl	Flow control If set, enables flow control using CTS/RTS.
5	pe	Parity enable If set, enables parity generation and checking.
4	ps	Parity select Selects parity polarity “0” = even parity “1” = odd parity
3	ti	Transmitter interrupt enable If set, enables generation of transmitter interrupt.
2	ri	Receiver interrupt enable If set, enables generation of receiver interrupt.
1	te	Transmitter enable If set, enables the transmitter.
0	re	Receiver enable If set, enables the receiver.

Table 65. UART 1 Scaler Register - UASCA1
Address = 0x8000007C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																				scaler value											
r/w																				r/w											
xxxx xxxx xxxx xxxx xxxx																				xxxx xxxx xxxx											

Table 66. UART 2 Data Register - UAD2
Address = 0x80000080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								rtd2							
r/w																								r/w							

Table 66. UART 2 Data Register - UAD2
Address = 0x80000080

xxxx xxxx xxxx xxxx xxxx xxxx	xxxx xxxx

Bit Number	Mnemonic	Description
7..0	rtd2	Received or Transmitted Data of UART2

rtd1 field has 2 meanings :

A write access enables the sending of the written 8-bit data on UART 2.

A read access provides the received 8-bit data on UART2.

Table 67. UART 2 Status Register - UAS2
Address 0x80000084

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																									fe	pe	ov	br	th	ts	dr
r/w																									r/w						
xxxx xxxx xxxx xxxx xxxx xxxx x																									x	x	x	x	x	x	x

Bit Number	Mnemonic	Description
6	fe	Framing error Indicates that a framing error was detected.
5	pe	Parity error indicates that a parity error was detected.
4	ov	Overrun Indicates that one or more character have been lost due to overrun.
3	br	Break received Indicates that a BREAK has been received.
2	th	Transmitter hold register empty Indicates that the transmitter hold register is empty.
1	ts	Transmitter shift register empty Indicates that the transmitter shift register is empty.
0	dr	Data ready Indicates that new data is available in the receiver holding register.

Table 68. UART 2 Control Register - UAC2
Address = 0x80000088

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																							ec	lb	fl	pe	ps	ti	ri	te	re
r/w																							r/w								

Table 68. UART 2 Control Register - UAC2
Address = 0x80000088

xxxx xxxx xxxx xxxx xxxx xxx	x	x	x	x	x	x	x	x	x

Bit Number	Mnemonic	Description
8	ec	External Clock if set, the UART scaler will be clocked by PIO[3]
7	lb	Loop back If set, loop back mode will be enabled.
6	fl	Flow control If set, enables flow control using CTS/RTS.
5	pe	Parity enable If set, enables parity generation and checking.
4	ps	Parity select Selects parity polarity “0” = even parity “1” = odd parity
3	ti	Transmitter interrupt enable If set, enables generation of transmitter interrupt.
2	ri	Receiver interrupt enable If set, enables generation of receiver interrupt.
1	te	Transmitter enable If set, enables the transmitter.
0	re	Receiver enable If set, enables the receiver.

Table 69. UART 2 Scaler Register - UASCA2
Address = 0x8000008C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																				scaler value											
r/w																				r/w											
xxxx xxxx xxxx xxxx xxxx																				xxxx xxxx xxxx											

Interrupt Registers

Table 70. Interrupt Mask and Priority Register - ITMP
Address = 0x80000090

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ilevel[15:1]															reserved	imask[15:1]															reserved
																unused	PCI	unused	unused	DSU	unused	Timer2	Timer1	I/O3	I/O2	I/O1	I/O0	UART1	UART2	AMBA	
r/w															r/w	r/w															r/w
xxxx xxxx xxxx xxx															x	xxxx xxxx xxxx xxx															x

Bit Number	Mnemonic	Description
31..17	ilevel[15:1]	Interrupt level indicates whether an interrupt belongs to priority level 1 (ILEVEL[n]=1) or level 0 (ILEVEL[n]=0).
15..1	imask[15:1]	Interrupt mask indicates whether an interrupt is masked or enabled ‘0’ = masked ‘1’ = enabled

Table 71. Interrupt Pending Register - ITP
Address = 0x80000094

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																ipend[15:1]															reserved
																unused	PCI	unused	unused	DSU	unused	Timer2	Timer1	I/O3	I/O2	I/O1	I/O0	UART1	UART2	AMBA	
r/w																r															r/w
xxxx xxxx xxxx xxxx																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit Number	Mnemonic	Description
15..1	ipend[15:1]	Interrupt pending indicates whether an interrupt is pending “1” = interrupt pending “0” = interrupt not pending

When the IU acknowledges the interrupt, the corresponding pending bit is automatically cleared.

Table 72. Interrupt Force Register - ITF
Address = 0x80000098

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																iforce[15:1]															reserved
																unused	PCI	unused	unused	DSU	unused	Timer2	Timer1	I/O3	I/O2	I/O1	I/O0	UART1	UART2	AMBA	
r/w																r/w															r/w
xxxx xxxx xxxx xxxx																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit Number	Mnemonic	Description
15..1	iforce[15:1]	Interrupt force indicates whether an interrupt is being forced “1” = interrupt forced “0” = interrupt not forced

Interrupt can be forced by setting a bit in the interrupt force register. IU acknowledgement will clear the force bit.

Table 73. Interrupt Clear Register - ITC
Address = 0x8000009C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																iclear[15:1]															reserved
																unused	PCI	unused	unused	DSU	unused	Timer2	Timer1	I/O3	I/O2	I/O1	I/O0	UART1	UART2	AMBA	
r/w																r															r/w
xxxx xxxx xxxx xxxx																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit Number	Mnemonic	Description
	iclear[15:1]	Interrupt clear

If written with a ‘1’, will clear the corresponding bit(s) in the interrupt pending register.

A read returns zero.

General Purpose Interface Registers

Table 74. I/O Port Data Register - IODAT
Address = 0x800000A0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
meddat								lowdat								iodata															
r/w																r/w															
xxxx xxxx								xxxx xxxx								xxxx xxxx xxxx xxxx															

Bit Number	Mnemonic	Description
15..0	iodata	I/O port data

when read, returns the current value of the I/O port;

when written, value is driven on the I/O port signals (if enabled as Output)

Table 75. I/O Port Direction Register - IODIR
Address = 0x800000A4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved														meddir	lowddir	iodir[15:0]															
r/w														r/w	r/w	r/w															
xxxx xxxx xxxx xx														xx xxxx xxxx xxxx xxxx															

Bit Number	Mnemonic	Description
17	meddir	Defines the direction of D[15..8]
16	lowddir	Defines the direction of D[7..0]
15..0	iodir	I/O port direction Defines the direction of I/O ports 15 - 0. ‘1’ = output ‘0’ = input

Table 76. I/O Port Interrupt Register - IOIT
Address = 0x800000A8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
en3	le3	pl3	*isel3*					en2	le2	pl2	isel2					en1	le1	pl1	isel1					en0	le0	pl0	isel0				
r/w	r/w	r/w	r/w					r/w	r/w	r/w	r/w					r/w	r/w	r/w	r/w					r/w	r/w	r/w	r/w				
0	x	x	x xxxx					0	x	x	x xxxx					0	x	x	x xxxx					0	x	x	x xxxx				

Bit Number	Mnemonic	Description
31	en3	Enable. If set, the corresponding interrupt will be enabled, otherwise it will be masked.
30	le3	Level/edge triggered. If set, the interrupt will be edge-triggered, otherwise level sensitive.
29	pl3	Polarity If set, the corresponding interrupt will be active high (or edge-triggered on positive edge). Otherwise, it will be active low (or edge-triggered on negative edge).
28..24	isel3	I/O port select. The value of this field defines which I/O port (0 - 31) should generate parallel I/O port interrupt *3*.
23	en2	Enable. If set, the corresponding interrupt will be enabled, otherwise it will be masked.
22	le2	Level/edge triggered. If set, the interrupt will be edge-triggered, otherwise level sensitive.
21	pl2	Polarity If set, the corresponding interrupt will be active high (or edge-triggered on positive edge). Otherwise, it will be active low (or edge-triggered on negative edge).
20..16	isel2	I/O port select. The value of this field defines which I/O port (0 - 31) should generate parallel I/O port interrupt *2*.
15	en1	Enable. If set, the corresponding interrupt will be enabled, otherwise it will be masked.
14	le1	Level/edge triggered. If set, the interrupt will be edge-triggered, otherwise level sensitive.
13	pl1	Polarity If set, the corresponding interrupt will be active high (or edge-triggered on positive edge). Otherwise, it will be active low (or edge-triggered on negative edge).
12..8	isel1	I/O port select. The value of this field defines which I/O port (0 - 31) should generate parallel I/O port interrupt *3*.
7	en0	Enable. If set, the corresponding interrupt will be enabled, otherwise it will be masked.
6	le0	Level/edge triggered. If set, the interrupt will be edge-triggered, otherwise level sensitive.
5	pl0	Polarity If set, the corresponding interrupt will be active high (or edge-triggered on positive edge). Otherwise, it will be active low (or edge-triggered on negative edge).
4..0	isel0	I/O port select. The value of this field defines which I/O port (0 - 31) should generate parallel I/O port interrupt *2*.

PCI Registers

Table 77. PCI Device Identification Register 1 - PCIID1
Address = 0x80000100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
device id																vendor id															
r																r															
0x1202																0x1438															

Bit Number	Mnemonic	Description
31..16	device id	This field identifies the particular device. This identifier is allocated by the vendor.
15..0	vendor id	This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0FFFFh is an invalid value for Vendor ID.

Table 78. PCI Status - Command Register - PCISC
Address = 0x80000104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
stat15	stat14	stat13	*stat12*	stat11	*stat10..9*		stat8	stat7	stat6	stat5	stat4	stat3	reserved								*com10*	com9	com8	com7	com6	com5	com4	com3	com2	com1	com0
rr	rr	rr	rr	rr	r		rr	r	r	r	r	r	r								r/w	r/w	r/w	r	r/w	r	r/w	r	r/w	r/w	r/w
0	0	0	0	0	01		0	1	0	0	0	0	0x0000 0000								0	0	0	0	0	0	0	0	0	0	0

Note: 1. rr = Read and Reset by writing 1

Bit Number	Mnemonic	Description
31	stat15	Parity error detected. This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).
30	stat14	SERR asserted. This bit must be set whenever the device asserts **SERR*** . Devices who will never assert **SERR*** do not need to implement this bit.
29	stat13	Master has terminated master abort. This bit must be set by a master device whenever its transaction except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
28	stat12	Master has terminated target abort This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
27	stat11	Target signal target abort. This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
26..25	stat10_9	Devsel timing. These bits encode the timing of **DEVSEL*** . Three allowable timings for assertion of **DEVSEL*** are specified. These are encoded as 00 for fast, 01 for medium, and 10 for slow (11b is reserved). These bits are read-only and must indicate the slowest time that a device asserts **DEVSEL*** for any bus command except Configuration Read and Configuration Write.

Bit Number	Mnemonic	Description
24	stat8	Master received/asserted PERR This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted **PERR*** itself (on a read) or observed **PERR*** asserted (on a write); 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; 3) the Parity Error Response bit (Command register) is set.
23	stat7	Target supports fast back2back This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise.
22	stat6	User definable features
21	stat5	66 MHz capabality This optional read-only bit indicates whether or not this device is capable of running at 66 MHz as defined in Chapter 7. A value of zero indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable
20	stat4	Power management capability. This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
10	com10	Interrupt command. This bit disables the device/function from asserting **INTx***. A value of 0 enables the assertion of its **INTx*** signal. A value of 1 disables the assertion of its **INTx*** signal. This bit's state after **PCI_RST*** is 0.
9	com9	Master can generate fast back2back. This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means the master is allowed to generate fast back-to-back transactions to different agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent. This bit's state after **PCI_RST*** is 0.
8	com8	Enable SERR driver -This bit is an enable bit for the **SERR*** driver. A value of 0 disables the **SERR*** driver. A value of 1 enables the **SERR*** driver. This bit's state after **PCI_RST*** is 0. All devices that have an **SERR*** pin must implement this bit. Address parity errors are reported only if this bit and bit 6 are 1.
7	com7	Address/Data stepping on PCI bus
6	com6	Enable Parity Check This bit controls the device's response to parity errors. When the bitis set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error status bit (bit 15 in the Status register) when an error is detected, but does not assert **PERR*** and continues normal operation. This bit's state after **PCI_RST*** is 0. Devices that check parity must implement this bit. Devices are still required to generate parity even if parity checking is disabled.
5	com5	VGA palette snooping This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. When this bit is 1, palette snooping is enabled (i.e., the device does not respond to palette register writes and snoops the data). When the bit is 0, the device should treat palette write accesses like all other accesses. VGA compatible devices should implement this bit.
4	com4	Enable memory write and invalidate. This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, masters may generate the command. When it is 0, Memory Write must be used instead. State after **PCI_RST*** is 0. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.

Bit Number	Mnemonic	Description
3	com3	Enable special cycles Controls a device's action on Special Cycle operations. A value of 0 causes the device to ignore all Special Cycle operations. A value of 1 allows the device to monitor Special Cycle operations. State after **PCI_RST*** is 0.
2	com2	Enable PCI master Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. State after **PCI_RST*** is 0.
1	com1	Enable target memory command response Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after **PCI_RST*** is 0.
0	com1	Enable target IO command response Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after **PCI_RST*** is 0.

Table 79. PCI Device Identification 2 - PCIID2
Address = 0x80000108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
class code																								revision id							
r																								r							
0xB																								0x01							

Bit Number	Mnemonic	Description
31..8	class code	The Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register-level programming interface. The register is broken into three byte-size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device.
7..0	revision id	This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the *Device ID*.

Table 80. Bist, Header type, Latency, Cache line size Register - PCIBHLC
Address = 0x8000010C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
bist								header type								latency timer								cache line size							
r/w								r/w								r/w								r/w							
0x00								0x00								0x00								0x00							

Bit Number	Mnemonic	Description
31..24	bist	bist7 : Return 1 if device supports BIST. Return 0 if the device is not BIST capable. bist6 : Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds. bist[3..0] : A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.
23..16	header type	header 7 : multi-function device “0” : device is single function “1” : device is multi-function header[6..0] : header second part layout
15..8	latency timer	this field specifies the value for latency timer in PCI bus clock unit
7..0	cache line size	Specifies the cache line size

Table 81. Memory Base Address Register 1 - MBAR1
Address = 0x80000110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
base address																												pref	type		msi
r/w								r																				r	r	r	r
0x00								0x0000 0																				1	0	0	0

Bit Number	Mnemonic	Description
31..4	base address	
3	pref	Prefetchable indicates there are no side effects on reads. The device returns all bytes on reads regardless of the byte enables.
2..1	type	“00” Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space. “10” Base register is 64 bits wide and can be mapped anywhere in the 64-bit address space. “11” & “01” Reserved
0	msi	“0” : Indicates that base address mapes Memory Space

Table 82. Memory Base Address Register 2 - MBAR2
Address = 0x80000114

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
base address																												pref	type		msi
r/w								r																				r	r	r	r
0x00								0x0000 0																				1	0	0	0

Bit Number	Mnemonic	Description
31..4	base address	
3	pref	Prefetchable indicates there are no side effects on reads. The device returns all bytes on reads regardless of the byte enables.
2..1	type	“00” Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space. “10” Base register is 64 bits wide and can be mapped anywhere in the 64-bit address space. “11” & “01” Reserved
0	msi	“0” : Indicates that base address mapes Memory Space

Table 83. IO Base Address Register 3 - IOBAR3
Address = 0x80000118

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
io base address																														reserved	msi
r/w																						r								r	r
0x000000																						0x00								0	1

Bit Number	Mnemonic	Description
31..2	base address	
0	msi	“1” : Indicates that base address mapes I/O Space

Table 84. Subsystem Identification Register - PCISID
Address = 0x8000012C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
subsystem id																svi															
r																r															
0x1																0x1438															

Bit Number	Mnemonic	Description
31..16	sid	subsystem id
15..0	svi	subsystem vendor id

Table 85. PCI Capabilities Pointer Register - PCICP
Address = 0x80000134

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								pointer							
r																								r							
0x0000 00																								0xDC							

Bit Number	Mnemonic	Description
7..0	pointer	index for the extended capabilities registers

Table 86. PCI Latency Interrupt Register - PCILI
Address = 0x8000013C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
max_lat								min_gnt								int_pin								int_line							
r/w								r/w								r								r/w							
0								0								0								0							

Bit Number	Mnemonic	Description
31:24	maxlat	maxlat field specifies how often the processor need to gain access to the PCI bus. Units are 0.25 micosecond
23:16	mingnt	min_gnt identifies the length of burst period, assuming a 33MHz clock. Units are 0.25 micosecond
15:8	intpin	indicates which interrupt pin the processor uses - Always 0 due to absence of PCI interrupt management.
7:0	intlin	Indicates the interrupt line register to which the core is connected to. - Always 0 due to absence of PCI interrupt management.

Table 87. PCI Retry _trdy - PCIRT
Address = 0x80000140

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								reserved								retry								trdy							
																r/w								r/w							
0								0								0x80								0x80							

Bit Number	Mnemonic	Description
15:8	retry	Indicates the number of retry the core will performe when configured as master
7:0	trdy	Indicates the number of PCI clock the processor configured as master will wait for TRDY

Table 88. PCI Configuration Write Register - PCICW
Address = 0x80000144

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																												ben			
r/w																												r/w			
0x0000 000																												0x0			

Bit Number	Mnemonic	Description
3..0	ben	Byte enables for writes to the PCI core configuration space ‘0’ = enabled ‘1’ = disabled

Each of the 4 bits is assigned to one 8-bit lane.

- bit ben[3] is applied to Byte 3, the most significant byte (MSB)
- bit ben[2] is applied to Byte 2
- bit ben[1] is applied to Byte 1
- bit ben[0] is applied to Byte 0, the less significant byte (LSB)

Table 89. PCI Initiator Start Address - PCISA
Address = 0x80000148

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
start address																															
r/w																															
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit Number	Mnemonic	Description
31..0	start address	PCI start address for PCI initiator transactions in APB and DMA mode.

Table 90. PCI Initiator Write Register - PCIIW
Address = 0x8000014C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																												ben			
r/w																												r/w			
0x0000 000																												0x0			

Bit Number	Mnemonic	Description
3..0	ben	Byte enables for writes to the PCI core configuration space ‘0’ = enabled ‘1’ = disabled

Each of the 4 bits is assigned to one 8-bit lane.

- bit ben[3] is applied to Byte 3, the most significant byte (MSB)
- bit ben[2] is applied to Byte 2
- bit ben[1] is applied to Byte 1
- bit ben[0] is applied to Byte 0, the less significant byte (LSB)

Table 91. PCI DMA configuration Register - PCIDMA
address = 0x80000150

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																			b2b	com				wdcnt							
r/w																				r/w				r/w							
0x0000 0																			0	0x0				0x00							

Bit Number	Mnemonic	Description
12	b2b	Use back2back-mode. Can be written to 1, if this transaction is to the same target, as the last one. Note: works only, if the core is enabled for back2back mode.
11..8	com	PCI command to be used in DMA mode.
7..0	wdcnt	Word count. Minimum number of words for the burst.

Table 92. PCI Initiator Status Register - PCIIS
address = 0x8000015C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																				dmas				act	xff	xfe	rfe	ss			
r/w																				r				r	r	r	r	r			
0x0000 0																				0x0				0	0	1	1	0x0			

Bit Number	Mnemonic	Description
11..8	dmas	DMA state
7	act	PCI core active 1 = active 0 = inactive
6	ff	If set 1, the transmitter fifo is full
5	xfe	If set 1, the transmitter fifo is empty
4	rfe	If set 1, the receiver fifo is empty
3..0	ss	Slave status

Table 93. PCI Initiator Configuration - PCIIC
Address = 0x80000158

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								commsb		reserved		perr	dww	dwr	mod
r/w																								r/w		r/w		r/w	r/w	r/w	r/w
0x0000 00																								01		00		0	0	0	0

Bit Number	Mnemonic	Description
7.6	cmd	Specifies the two most significant bits of the command used by AHB slave interface. ‘00’ = IO write ‘01’ = memory read/write ‘10’ = configuration read/write ‘11’ = mem-read-line/write-invalidate
3	perr	Perr retry enable If set make target generate a retry on read with parity error
2	dww	Double word write ‘1’ = executes double word write as one 2 word burst ‘0’ = executes double word write as bursts of undefined length
1	dwr	Double word read ‘1’ = executes a 2 word burst read ‘0’ = executes two single reads

Bit Number	Mnemonic	Description
0	mod	PCI command source mode ‘1’ = AHB slave - DMA mode ‘0’ = APB mode

Table 94. PCI Target Page Address Register - PCITPA
Address = 0x8000015C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
tpa1								reserved								tpa2								reserved							
r/w								r/w								r/w								r/w							
0x40								0x00								0x90								0x00							

Bit Number	Mnemonic	Description
31..24	tpa1	Target page address defines the 8 most significant bits of the 16 MByte memory page on which PCI addresses are mapped
15..8	tpa2	Target page address defines the 8 most significant bits for the second memory BAR.

Table 95. PCI Target Status-Command Register - PCITSC
Address = 0x80000160

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								errmem	xff	xfe	rfe	tms			
r/w																															
0x0000 00																								0	0	1	1	0	0	0	0

Bit Number	Mnemonic	Description
7	errmem	Reception Fifo parity error ‘0’ = Do not save data with parity error ‘1’ = Data with parity error is saved to memory
6	xff	TXMT Fifo full ‘1’ = force transmistion to abort
5	xfe	TXMT Fifo empty ‘1’ = flushes TXMT Fifo
4	rfe	TRCV Fifo empty ‘1’ = flushes TRCV Fifo
3..0	tms	Target AHB master state ‘1111’ = reset the state machine

Table 96. PCI Interrupt Enable Register - PCIITE
Address = 0x80000164

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								dmaer	imier	cmfer	imper	tier	tbeer	tper	syser
r/w																								r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
0x0000 00																								0	0	0	0	0	0	0	0

Bit Number	Mnemonic	Description
7	dmaer	DMA end of transfer ‘0’ = disable ‘1’ = enable
6	imier	Initiator error ‘0’ = disable ‘1’ = enable
5	cmfer	PCI core error ‘0’ = disable ‘1’ = enable
4	imper	Initiator Parity error ‘0’ = disable ‘1’ = enable
3	tier	Target error ‘0’ = disable ‘1’ = enable
2	tbeer	Target byte enable error ‘0’ = disable ‘1’ = enable
1	tper	Target parity error ‘0’ = disable ‘1’ = enable
0	syser	System error asserted on PCI bus ‘0’ = disable ‘1’ = enable

Table 97. PCI Interrupt Pending Register - PCIITP(1)
Address = 0x80000168

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								dmaer	imier	cmfer	imper	tier	tbeer	tper	syser
r/w																								r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
0x0000 00																								0	0	0	0	0	0	0	0

Bit Number	Mnemonic	Description
7	dmaer	DMA end of transfer ‘0’ = not pending ‘1’ = pending
6	imier	Initiator error ‘0’ = not pending ‘1’ = pending
5	cmfer	PCI core error ‘0’ = not pending ‘1’ = pending
4	imper	Initiator Parity error ‘0’ = not pending ‘1’ = pending
3	tier	Target error ‘0’ = not pending ‘1’ = pending
2	tbeer	Target byte enable error ‘0’ = not pending ‘1’ = pending
1	tper	Target parity error ‘0’ = not pending ‘1’ = pending
0	syser	System error asserted on PCI bus ‘0’ = not pending ‘1’ = pending

Note: 1. Bits are cleared when written with a 1. Writing a 0 to the register has no effect.

Table 98. PCI Interrupt Force Register - PCIITF
Address = 0x8000016C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								dmaer	imier	cmfer	imper	tier	tbeer	tper	syser
r/w																								r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
0x0000 00																								0	0	0	0	0	0	0	0

Bit Number	Mnemonic	Description
7	dmaer	DMA end of transfer ‘0’ = not forced ‘1’ = forced
6	imier	Initiator error ‘0’ = not forced ‘1’ = forced
5	cmfer	PCI core error ‘0’ = not forced ‘1’ = forced

Bit Number	Mnemonic	Description
4	imper	Initiator Parity error ‘0’ = not forced ‘1’ = forced
3	tier	Target error ‘0’ = not forced ‘1’ = forced
2	tbeer	Target byte enable error ‘0’ = not forced ‘1’ = forced
1	tper	Target parity error ‘0’ = not forced ‘1’ = forced
0	syser	System error asserted on PCI bus ‘0’ = not forced ‘1’ = forced

Table 99. PCI Data Register - PCID
Address = 0x80000170

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
dat																															
r/w																															
xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx																															

Bit Number	Mnemonic	Description
31..0	dat	data writen/read to/from Fifo

Table 100. PCI Burst End Register - PCIBE
Address = 0x80000174

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
dat																															
r/w																															
xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx																															

Bit Number	Mnemonic	Description
31..0	dat	Last data of a burst in APB mode

Table 101. PCI DMA Address Register - PCIDMAA
Address = 0x80000178

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
addr																															
r/w																															
xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx																															

Bit Number	Mnemonic	Description
31..0	addr	Defines the start address of a DMA transaction

Table 102. PCI Arbiter Register - PCIA
Address = 0x80000280

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																												p3	p2	p1	p0
r																												r	r/w	r/w	r/w
0x0000 000																												1	1	1	1

Bit Number	Mnemonic	Description
3	p3	Round robin level for agent 3
2	p2	Round robin level for agent 2
1	p1	Round robin level for agent 1
0	p0	Round robin level for agent 0

DSU Registers

Table 103. Trace Buffer Control Register - TBC
Address = 0x9000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved						*ta*	*ti*	*reserved*			*AHB index*									*reserved*			*Inst Index*								
r/w						r/w	r/w	r/w			r/w									r/w			r/w								
000000								000												000											

Bit Number	Mnemonic	Description
25	ta	Trace AHB enable
24	ti	Trace instruction enable
20..12	AHB Index	AHB trace index counter

Bit Number	Mnemonic	Description
8..0	Inst Index	Instruction trace index counter

Table 104. DSU Control Register - DSUC
Address = 0x90000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved			*dcnt*									*re*	*dr*	*lr*	*ss*	*pe*	*ee*	*eb*	*dm*	*de*	*bz*	*bx*	*bd*	*bn*	*bs*	*bw*	*be*	*ft*	*bt*	*dm*	*te*
																	read only														

Bit Number	Mnemonic	Description
28..20	dcnt	Trace buffer delay counter
19	re	Reset error mode if set, will clear the error mode in the processor.
18	dr	Debug mode response If set, the DSU communication link will send a response word when the processor enters debug mode
17	lr	Link response If set, the DSU communication link will send a response word after AHB transfer.
16	ss	Single step If set, the processor will execute one instruction and the return to debug mode
15	pe	Processor error mode returns ‘1’ on read when processor is in error mode else return ‘0’.
14	ee	value of the external DSUEN signal (read-only)
13	eb	value of the external DSUBRE signal (read-only)
12	dm	Debug mode Indicates when the processor has entered debug mode (read-only).
11	de	Delay counter enable If set, the trace buffer delay counter will decrement for each stored trace. This bit is set automatically when an DSU breakpoint is hit and the delay counter is not equal to zero.
10	bz	Break on error traps If set, will force the processor into debug mode on all *except* the following traps: priviledged_instruction, fpu_disabled, window_overflow, window_underflow, asynchronous_interrupt, ticc_trap.
9	bx	Break on trap If set, will force the processor into debug mode when any trap occurs.

Bit Number	Mnemonic	Description
8	bd	Break on DSU breakpoint If set, will force the processor to debug mode when an DSU breakpoint is hit.
7	bn	Break now Force processor into debug mode. If cleared, the processor will resume execution.
6	bs	Break on S/W breakpoint If set, debug mode will be forced when an breakpoint instruction (ta 1) is executed
5	bw	Break on IU watchpoint If set, debug mode will be forced on a IU watchpoint (trap 0xb).
4	be	Break on error (BE) - if set, will force the processor to debug mode when the processor would have entered error condition (trap in trap).
3	ft	Freeze timers If set, the scaler in the LEON timer unit will be stopped during debug mode to preserve the time for the software application.
2	bt	Break on trace If set, will generate a DSU break condition on trace freeze.
1	dm	Delay counter mode (DM). In mixed tracing mode, setting this bit will cause the delay counter to decrement on AHB traces. If reset, the delay counter will decrement on instruction traces
0	te	Trace enable. Enables the trace buffer.

Table 105. DSU UART Status Register - DSUUS
Address = 0x800000C4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																									fe	reserved	ov	reserved	th	ts	dr
r/w																									r	r/w	r	r/w	r	r	r
xxxx xxxx xxxx xxxx xxxx xxxx x																									0	x	0	x	0	0	0

Bit Number	Mnemonic	Description
6	fe	Framing error Indicates that a framing error was detected.
4	ov	Overrun Indicates that one or more character have been lost due to overrun.
2	th	Transmitter hold register empty Indicates that the transmitter hold register is empty.
1	ts	Transmitter shift register empty Indicates that the transmitter shift register is empty.
0	dr	Data ready Indicates that new data is available in the receiver holding register.

Table 106. DSU Trap Register - DTR
Address = 0x9008001C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																			*em*	*trap type*								*0000*			

Bit Mnemonic	Description
em	Error Mode. Set if the trap would have cause the processor to enter error mode
trap type	8_bit Sparc trap type

Table 107. Break Address Register 1 - BAD1
Address = 0x90000010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BADD																														*reserved*	*ex*

Bit mnemonic	Description
ex	Enables break on executed instruction

Table 108. Break Mask Register 1 - BMA1
Address = 0x90000014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMA																														*ld*	*st*

Bit mnemonic	Description
ex	Enables break on executed instruction
ld	Enables break on AHB load
st	Enables break on AHB write

Table 109. Break Address Register 2- BAD2
Address = 0x90000018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BADD																														*reserved*	*ex*

Bit mnemonic	Description
ex	Enables break on executed instruction

Table 110. Break Mask Register - BMA2
Address = 0x9000001C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMA																														*ld*	*st*

Bit mnemonic	Description
ex	Enables break on executed instruction
ld	Enables break on AHB load
st	Enables break on AHB write

Table 111. DSU UART Control Register - DSUUC
Address = 0x800000C8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																														bl	re
r/w																														r	r/w
xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx																														0	x

Bit Number	Mnemonic	Description
1	bl	Baud rate locked Is automatically set when the baud rate is locked.
0	re	Receiver enable If set, enables both the transmitter and receiver.

Table 112. DSU UART Scaler Reload Register - DSUUS
Address = 0x800000CC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																		scaler reload value													
r/w																		r/w													
xxxx xxxx xxxx xxxx xx																		xx xxxx xxxx xxxx													

Note: 1. The best scaler value for manually programming the baudrate can be calculated as follows:

$$scaler = \frac{\frac{sysclk \times 10}{baudrate \times 8} - 5}{10}$$

Electrical Characteristics

Electrical Characteristics for this product have not yet been finalized. Please consider all values listed here as preliminary and non contractual

Absolute Maximum Ratings

Operating Temperature .....-55 °C to +125 °C

Storage Temperature .....-65 °C to +150 °C

Voltage on VDD with respect to Ground .....-0.5 V to + 2.0 V

Voltage on VCC with respect to Ground .....-0.5 V to + 4.0 V

DC current VCC (VDD) and VSS Pins .....200 mA

Input Voltage on I/O pins with respect to Ground .....-0.5 V to +4 V

DC current per I/O pins.....40 mA

ESD ..... 250 V

Notes: 1. Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 113. DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VDD	Core Power Supply	1.65	1.8	1.95	V	
VCC	I/O Power Supply Voltage	3	3.3	3.6	V	
IILpu	Low Level Input Pull-up Current	100		500	uA	Vin = VSS
IIHpd	High Level Input Pull-downCurrent	100		500	uA	Vin = VCC (max)
IIL	Low Level Input Leakage Current	-1		1	uA	Vin = VSS
IIH	High Level Input Leakage Current	-1		1	uA	Vin = VCC (max)
IOZ	High Impedance Current	100		500	uA	Vin = VSS or VCC (max)
VIL TTL	Low Level Input Voltage			0.8	V	
VIL CMOS				30%VCC	V	
VIH TTL	High Level Input Voltage	2			V	
VIH CMOS		70%VCC			V	
VOL	Low Level Output Voltage			0.4	V	VCC = VCC(min) IOL = 2, 4, 8, 16mA
VOL pci	Low Level Output Voltage for PCI buffers			0.1 VCC	V	VCC = VCC(min) IOL = 1.5mA
VOH	High Level Output Voltage	VCC - 0.4			V	VCC = VCC(min) IOH = 2, 4, 8, 16mA

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VOH pci	High Level Output Voltage for PCI buffers	0.9 VCC			V	VCC = VCC(min) IOH = 0.5mA
ICCSb	Standby Current			5	mA	VCC = VCC(max) no clock active

Power "On/Off" Sequence

The AT697E is based on the Atmel 0.18 µm CMOS process. As VDD (1.8V) and VCC (3.3V) power supplies are electrically isolated, there is no specified sequence in which the power rails may be activated or deactivated.

Power Consumption

The power dissipation is the sum of three basic contributions : P = Pcore + Pio + Ppci

- Pcore represents the contribute due to the internal activity.
- Pio represents the contribute due to the IO pads and output load current, except the PCI bus.
- Ppci represents the contribute due to the PCI pads and output load current.

The following table gives the estimated current consumption for different conditions. The values are coming from estimation and calculation and not from real measurement.

Table 114. Power Dissipation

Mode	Typical conditions			Worst Conditions		
	P Core (1.8V) in W	P I/O (3.3V) in W	P PCI (3.3V) in W	P Core (1.8V) in W	P I/O (3.3V) in W	P PCI (3.3V) in W
Operating (100MHz)	0.6	0.2	0.1	0.8	0.3	0.2

Typical conditions : 25°C, 1.8V core, 3.3V I/O, High I/O and core activity

Worst conditions : 125°C, 1.95 V core, 3.6V I/O; High I/O and core activity

In idle mode (100 MHz external clock), the core power consumption is 0.5W in typical conditions and 0.7W in worst case conditions.

Decoupling capacitance

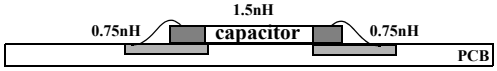
Two main frequencies are involved in the AT697 processor environment :

- 33MHz from the PCI interface
- 100MHz from the master clock of the processor (either from PLL or directly from resonator input)

The following hypothesis is taken for the calculation of the decoupling capacitance :

- 1.5nH is issued from the connection of the capacitor to the PCB
- 1.5nH is issued from the capacitor intrinsic inductance

Figure 53. Capacitor description



This hypothesis corresponds to a capacitor connected to two micro-vias on a PCB.

The filter defined by the self and the decoupling capacitor shall be able to filter the characteristic frequencies of the application. Each frequency to filtre is defined by :

$$fc = \frac{1}{\dot{2}\pi\sqrt{\dot{L}C}}$$

- L : the inductance equivalent to the global inductance on the VSS/VDD (VSS/VCC) line.
- C : the decoupling capacitance.

For a processor running at 100MHz with a PCI interface at a characteristic frequency of 33MHz and considering that power supply pins ar grouped by multiple of four, the decoupling capacitance to set are :

- 33nF for 33MHz decoupling
- 3nF for 100MHz decoupling

Capacitance Rating

Parameter	Description	MAX
C_{IN}	Standard Input Capacitance	5pF
C_{IO}	Standard Input/Output Capacitance	5pF
C_{INp}	PCI Input Capacitance	7pF
C_{IOp}	PCI Input/Output Capacitance	7pF

AC Characteristics

The AT697 processor implements a single event transient protection mechanism. The influence of this protection is reflected by the timing figures presented in the following tables.

The following tables show the timing figures for the skew condition natural and maximum.

Natural Skew

Test Conditions

- Natural Skew
- Temperature range : -55°C to 125°C
- Voltage range :
  - I/O: 3,3V +/- 0,30V
  - Core: 1,8V +/- 0,15V
- Clock frequency : 100MHz
- Output load : 30pF

Table 115. AC Characteristics - Natural Skew

Parameter	Min (ns)	Max (ns)	Comment	Reference edge ('+' for rising edge)
t1	10		CLK Period with PLL disable	
t1_p	40	50	CLK Period with PLL enable	
t2	4.5		CLK Low and High pulse width - PLL disabled	
t2_p	18		CLK Low and High pulse width - PLL enabled	
t3	10		SDCLK Period	
t4	2	7	SDCLK output delay - PLL disabled	CLK
t5		1.10^7	PLL setup time	
t6	1*t3		Reset Pulse Width	
t10	1.5	7	A[27:0] output delay	SDCLK +
t11	2	9	D[31:0] and CB[7:0] output delay	SDCLK +
t12	4.5		D[31:0] and CB[7:0] setup time	SDCLK +
t13	0		D[31:0] and CB[7:0] hold time during load/fetch	SDCLK +
t14	2	9	D[31:0] and CB[7:0] hold time during write	SDCLK +
t15	2	7	OE*, READ and WRITE* output delay	SDCLK +
t16	2	6.5	ROMS*[1:0] output delay	SDCLK +
t17	2	9,5	RAMS*[4:0], RAMOE*[4:0] and RWE*[3:0] output delay	SDCLK +
t18	2	6	IOS* output delay	SDCLK +
t19	4		BRDY* setup time	SDCLK +
t20	0		BRDY* hold time	SDCLK +
t21	3	9	SDCAS* output delay	SDCLK +

Parameter	Min (ns)	Max (ns)	Comment	Reference edge ('+' for rising edge)
t22	2	8,5	SDCS*[1:0], SDRAS*, SDWE* and SDDQM*[3:0] output delay	SDCLK +
t23	4		BEXC* setup time	SDCLK +
t24	0		BEXC* hold time	SDCLK +
t25	2.5	10	PIO[15:0] output delay	SDCLK +
t26	4.5		PIO[15:0] setup time	SDCLK +
t27	0		PIO[15:0] hold time during load	SDCLK +
t28	2.5		PIO[15:0] hold time during write	SDCLK +
t101	33		PCI_CLK Period	
t102	14.5		PCI_CLK Low and High pulse width	
t110	4	12	A/D[31:0] and C/BE[3:0] output delay	PCI_CLK +
t111	6		A/D[31:0] and C/BE[3:0] setup time	PCI_CLK +
t112	0		A/D[31:0] and C/BE[3:0] hold time	PCI_CLK +
t113	4	11	FRAME*, PAR, PERR*, SERR*, STOP* and DEVSEL* output delay	PCI_CLK +
t114	4	11	IRDY* and TRDY* output delay	PCI_CLK +
t115	4	12	REQ* output delay	PCI_CLK +
t116	7		FRAME*, LOCK*, PAR, PERR*, SERR*, IDSEL*, STOP* and DEVSEL* setup time	PCI_CLK +
t117	7		IRDY* and TRDY* setup time	PCI_CLK +
t118	6		GNT* setup time	PCI_CLK +
t119	0		FRAME*, LOCK*, PAR, PERR*, SERR*, IDSEL*, STOP* and DEVSEL* hold time	PCI_CLK +
t120	0		IRDY* and TRDY* hold time	PCI_CLK +
t121	0		GNT* hold time	PCI_CLK +

Maximum Skew

Test Conditions

- Maximum Skew Programmed
- Temperature range : -55°C to 125°C
- Voltage range :
  - I/O: 3,3V +/- 0,30V
  - Core: 1,8V +/- 0,15V
- Clock frequency : 83MHz
- Output load : 30pF

Table 116. AC Characteristics - Maximum Skew

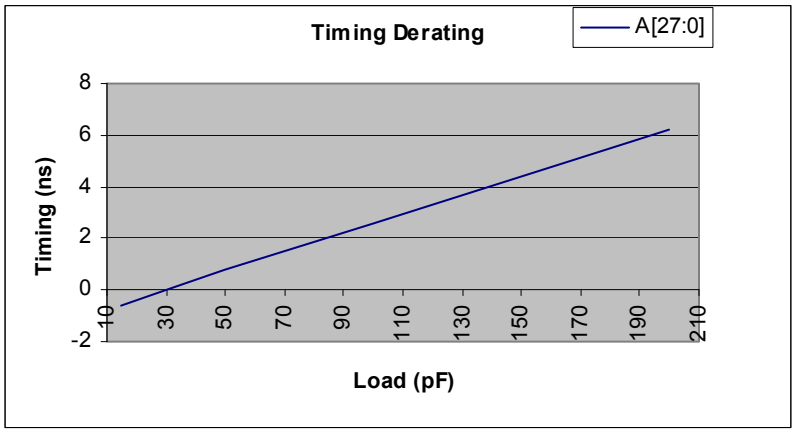
Parameter	Min (ns)	Max (ns)	Comment	Reference edge ('+' for rising edge)
t1	12		CLK Period with PLL disable	
t1_p	48	50	CLK Period with PLL enable	
t2	5.4		CLK Low and High pulse width - PLL disabled	
t2_p	21		CLK Low and High pulse width - PLL enabled	
t3	12		SDCLK Period	
t4	2	7	SDCLK output delay - PLL disabled	CLK
t5		1.10^7	PLL setup time	
t6	1* t3		Reset Pulse Width	
t10	1.5	8	A[27:0] output delay	SDCLK +
t11	2	11	D[31:0] and CB[7:0] output delay	SDCLK +
t12	4.5		D[31:0] and CB[7:0] setup time	SDCLK +
t13	0		D[31:0] and CB[7:0] hold time	SDCLK +
t14	2	11	D[31:0] and CB[7:0] hold time during write	SDCLK +
t15	2	8.5	OE*, READ and WRITE* output delay	SDCLK +
t16	2	8	ROMS*[1:0] output delay	SDCLK +
t17	2	10	RAMS*[4:0], RAMOE*[4:0] and RWE*[3:0] output delay	SDCLK +
t18	2	8	IOS* output delay	SDCLK +
t19	3		BRDY* setup time	SDCLK +
t20	0		BRDY* hold time	SDCLK +
t21	3	10	SDCAS* output delay	SDCLK +
t22	2	9.5	SDCS*[1:0], SDRAS*, SDWE* and SDDQM*[3:0] output delay	SDCLK +
t23	4		BEXC* setup time	SDCLK +
t24	0		BEXC* hold time	SDCLK +
t25	2.5	11	PIO[15:0] output delay	SDCLK +
t26	4.5		PIO[15:0] setup time	SDCLK +

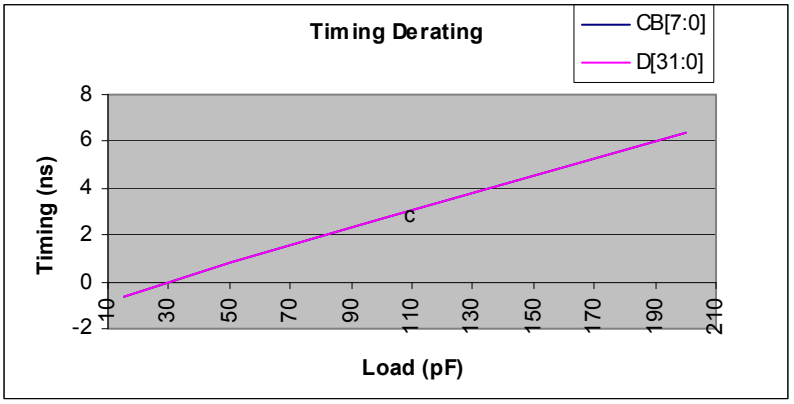
Parameter	Min (ns)	Max (ns)	Comment	Reference edge ('+' for rising edge)
t27	0		PIO[15:0] hold time	SDCLK +
t28	2.5		PIO[15:0] hold time during write	SDCLK +
t101	33		PCI_CLK period	
t102	14.5		PCI_CLK low and high pulse width	
t110	4	13	A/D[31:0] and C/BE[3:0] output delay	PCI_CLK +
t111	6		A/D[31:0] and C/BE[3:0] setup time	PCI_CLK +
t112	1		A/D[31:0] and C/BE[3:0] hold time	PCI_CLK +
t113	4	12	FRAME*, PAR, PERR*, SERR*, STOP* and DEVSEL* output delay	PCI_CLK +
t114	4	12.5	IRDY* and TRDY* output delay	PCI_CLK +
t115	4	13	REQ* output delay	PCI_CLK +
t116	7.5		FRAME*, LOCK*, PAR, PERR*, SERR*, IDSEL*, STOP* and DEVSEL* setup time	PCI_CLK +
t117	7.5		IRDY* and TRDY* setup time	PCI_CLK +
t118	6		GNT* setup time	PCI_CLK +
t119	0.5		FRAME*, LOCK*, PAR, PERR*, SERR*, IDSEL*, STOP* and DEVSEL* hold time	PCI_CLK +
t120	0.5		IRDY* and TRDY* hold time	PCI_CLK +
t121	0.5		GNT* hold time	PCI_CLK +

Timing Derating

Depending on the capacitance load on each pin, the timing figures change. The following figures summarize the timing derating versus the load capacitance.

Figure 54. Timing derating (1/2)





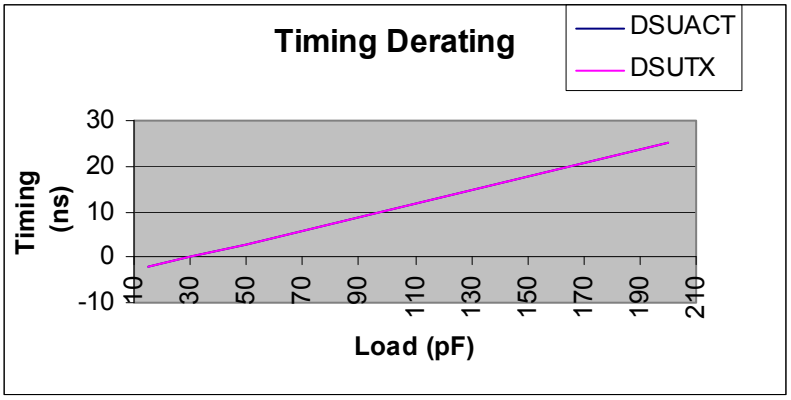
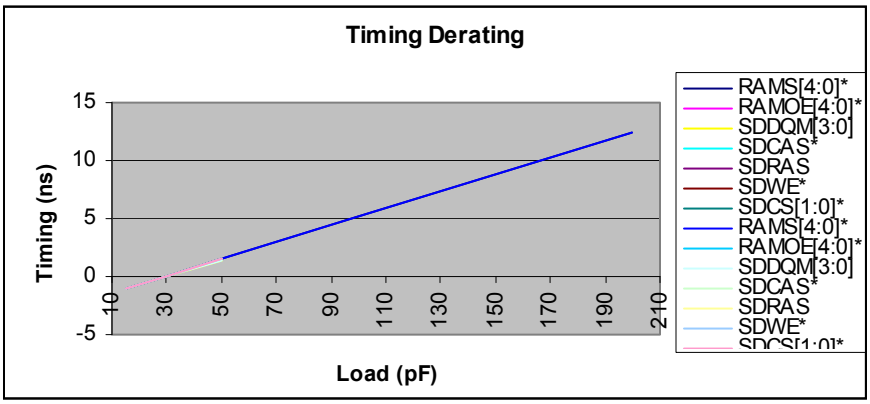
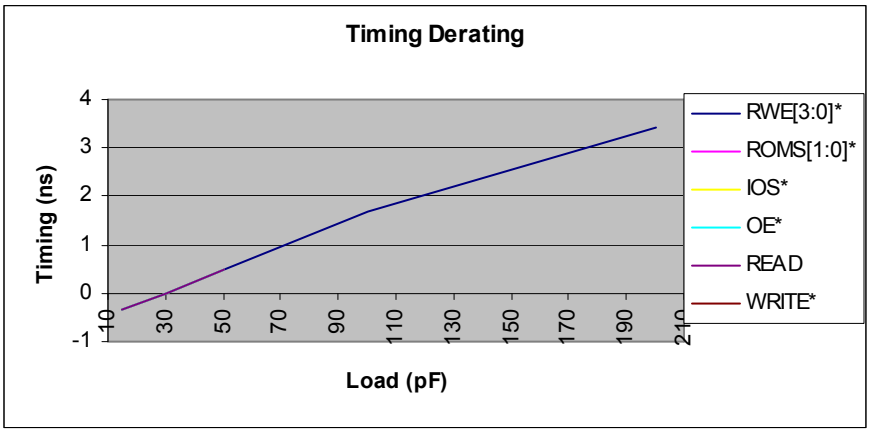
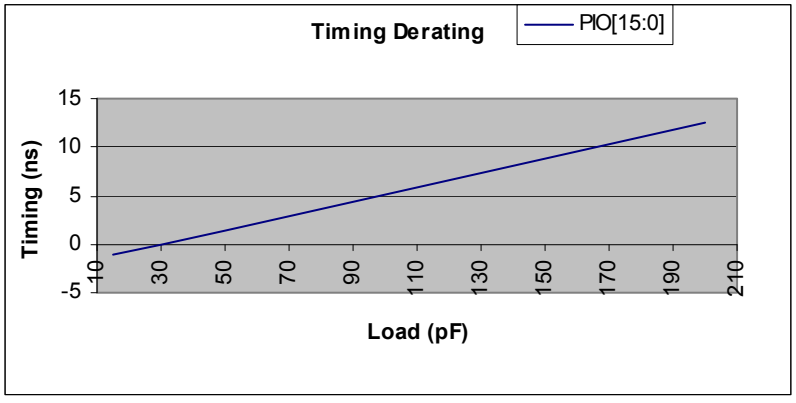


Figure 55. Timing derating (2/2)







Timing Diagrams

Diagram List

- Reset Sequence
- Clock Input without PLL
- Clock Input with PLL

- Fetch, Read and Write from/to 32-bit PROM - 0 Waitstate
- Fetch, Read and Write from/to 32-bit PROM - n Waitstates
- Fetch, Read and Write from/to 32-bit PROM - n Waitstates + BRDY*

- Fetch from 8-bit PROM with EDAC disabled - n Waitstates
- Word Write to 8-bit PROM with EDAC disabled - n Waitstates
- Byte and Half Word Write to 8-bit PROM with EDAC disabled - n Waitstates
- Fetch from 8-bit PROM with EDAC enabled - n Waitstates
- Fetch from 16-bit PROM - n Waitstates

- Fetch, Read and Write from/to 32-bit SRAM - 0 Waitstate
- Fetch, Read and Write from/to 32-bit SRAM - n Waitstates

- Burst of fetches and Write from/to 32-bit SRAM - 0 Waitstate
- Burst of fetches and Write from/to 32-bit SRAM - n Waitstates

- SDRAM Read (or Fetch) with Precharge ; CL = 3
- SDRAM Write with Precharge ; CL = 3

- Fetch from ROM, Read and Write from/to 32-bit I/O - 0 Waitstate
- Fetch from ROM, Read and Write from/to 32-bit I/O - n Waitstates
- Fetch from ROM, Read and Write from/to 32-bit I/O - n Waitstates + BRDY*

Figure 56. Reset Sequence

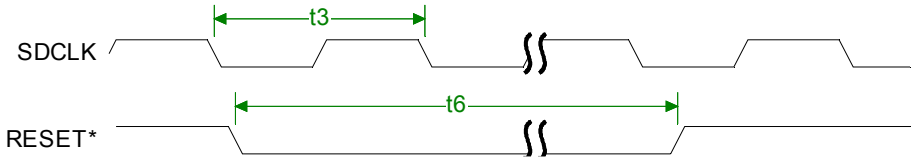


Figure 57. Clock Input without PLL

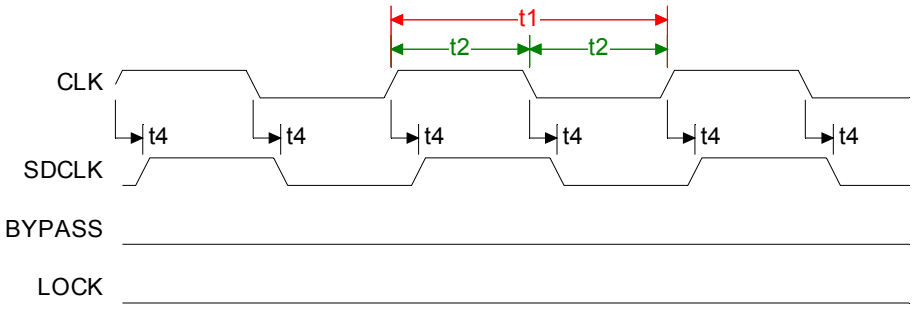


Figure 58. Clock Input with PLL

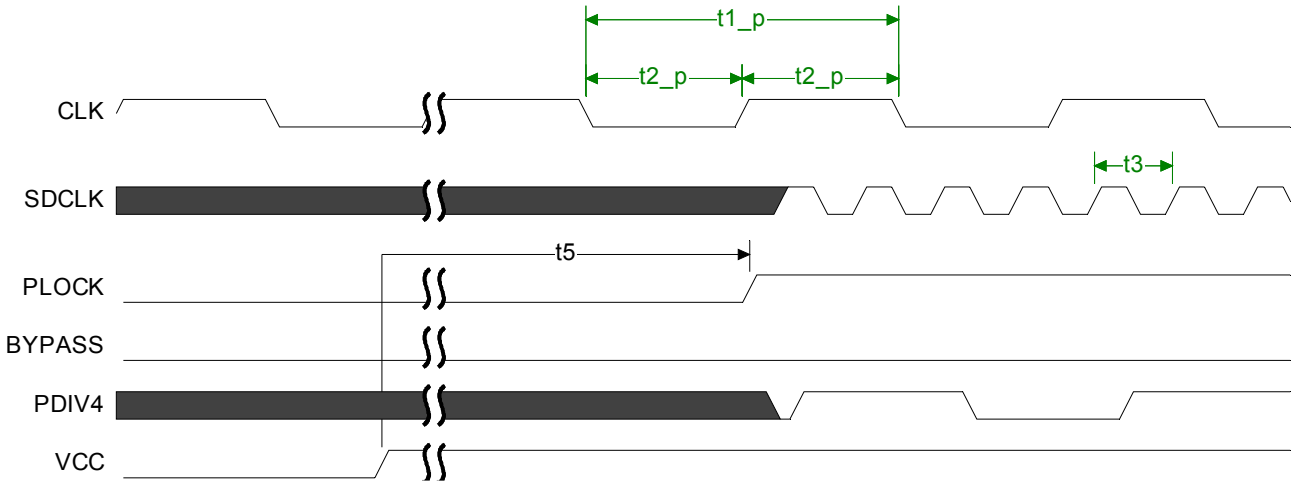


Figure 59. Fetch, Read and Write from 32-bit PROM - 0 Waitstate

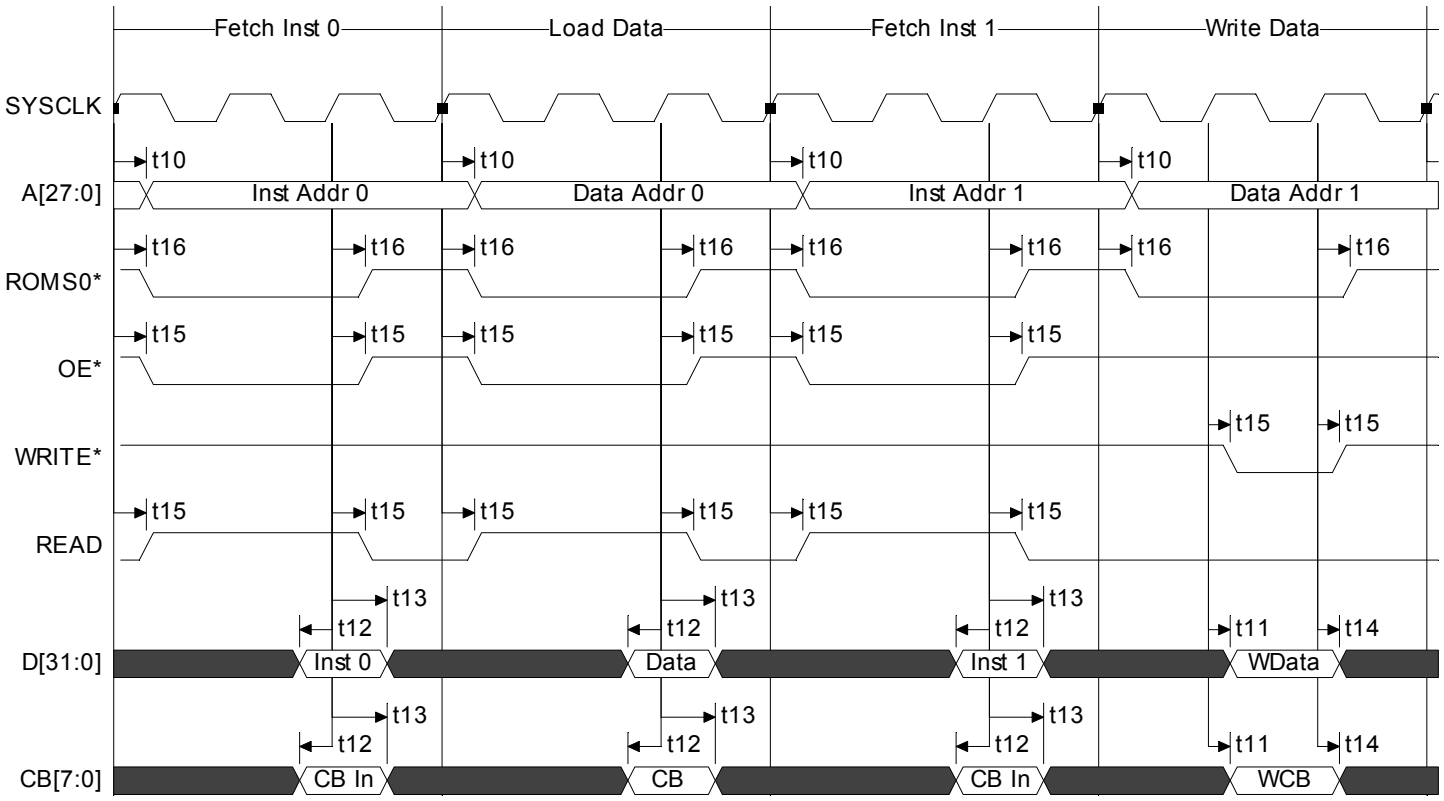


Figure 60. Fetch, Read and Write from 32-bit PROM - n Waitstates

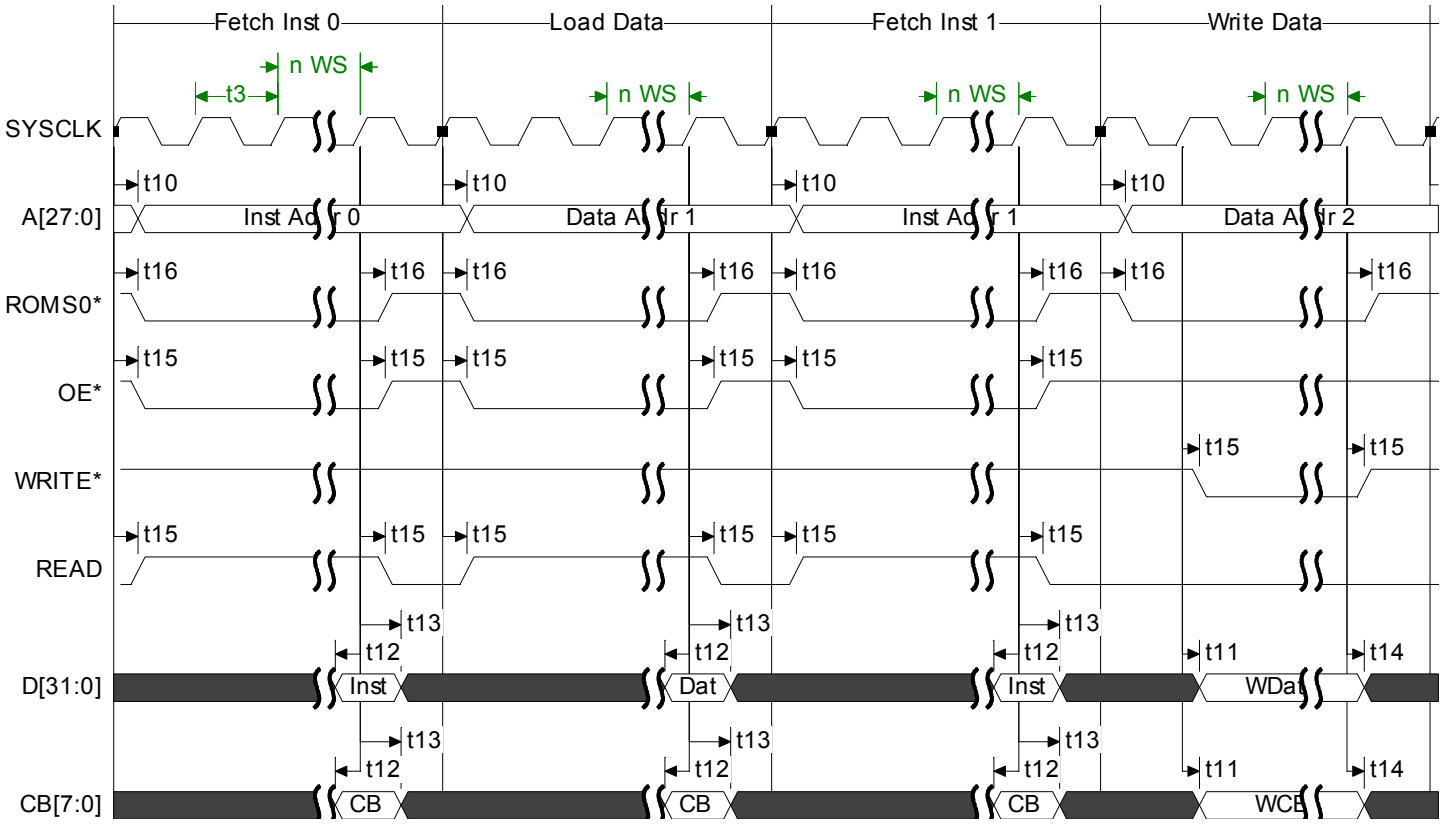


Figure 61. Fetch, Read and Write from 32-bit PROM - n Waitstates + BRDY*

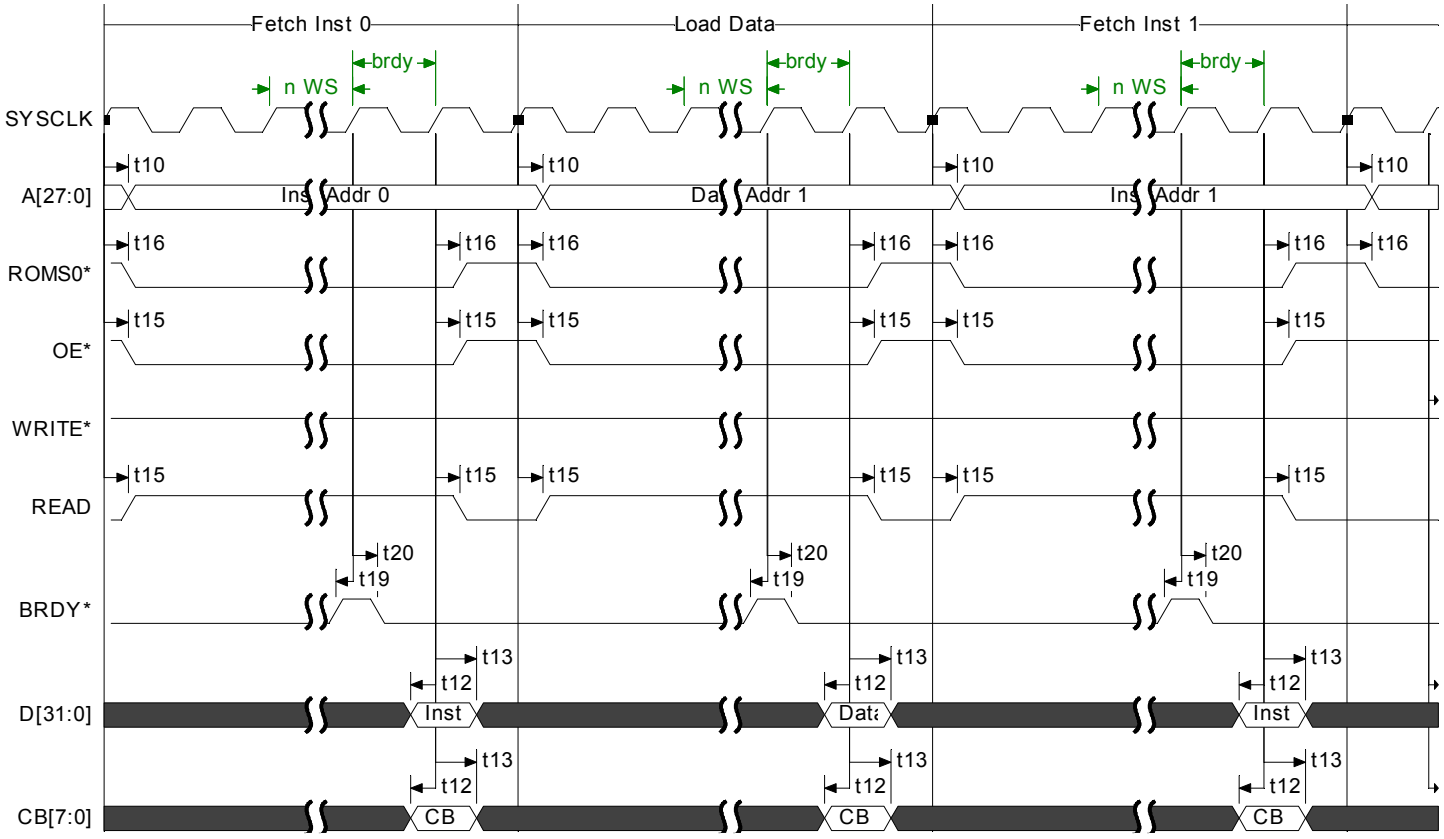


Figure 62. Fetch from 8-bit PROM with EDAC disabled - n Waitstates

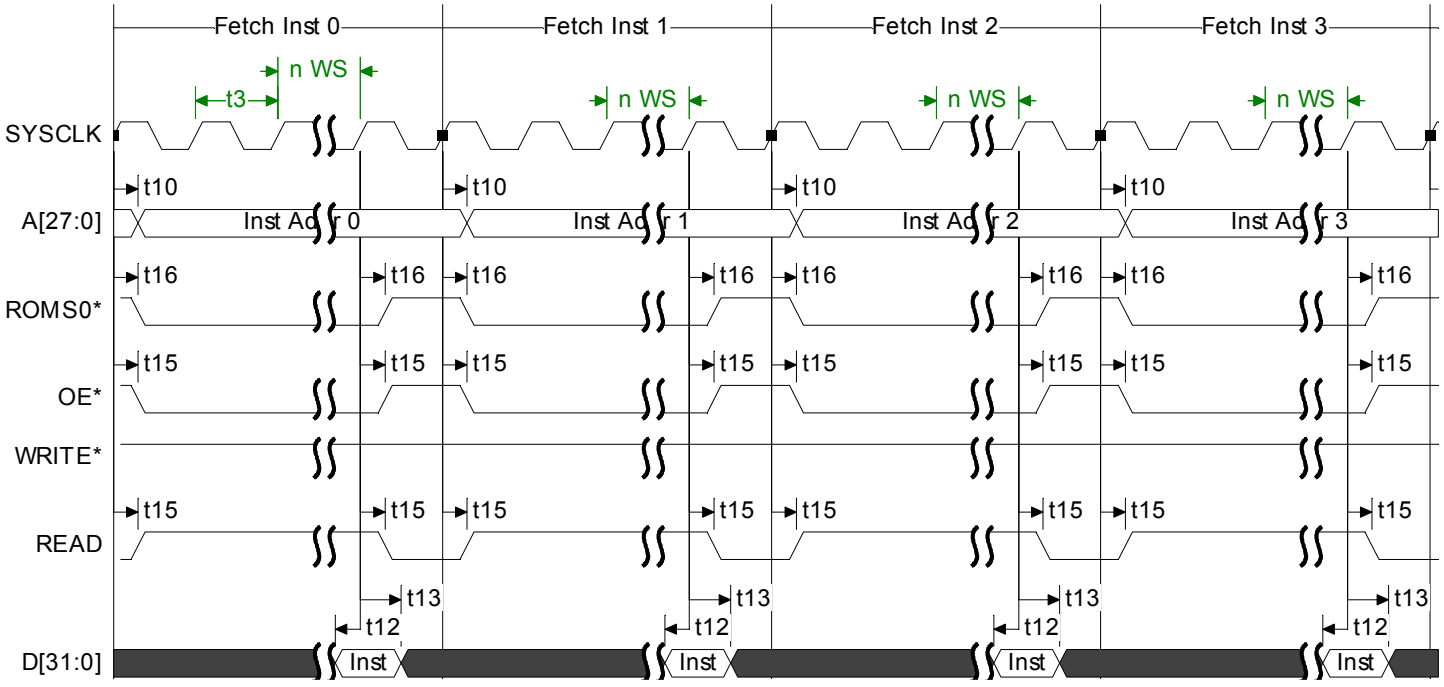


Figure 63. Word Write to 8-bit PROM with EDAC disabled - n Waitstates

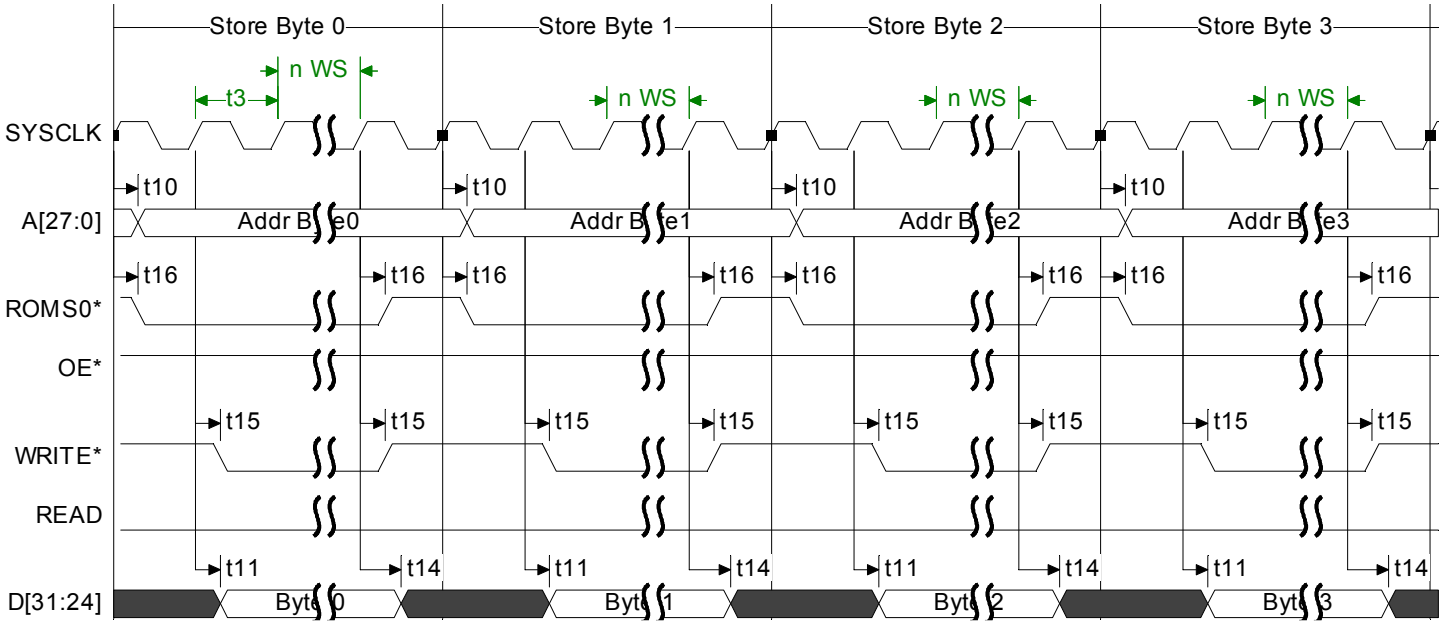


Figure 64. Byte and Half Word Write to 8-bit PROM with EDAC disabled - n Waitstates

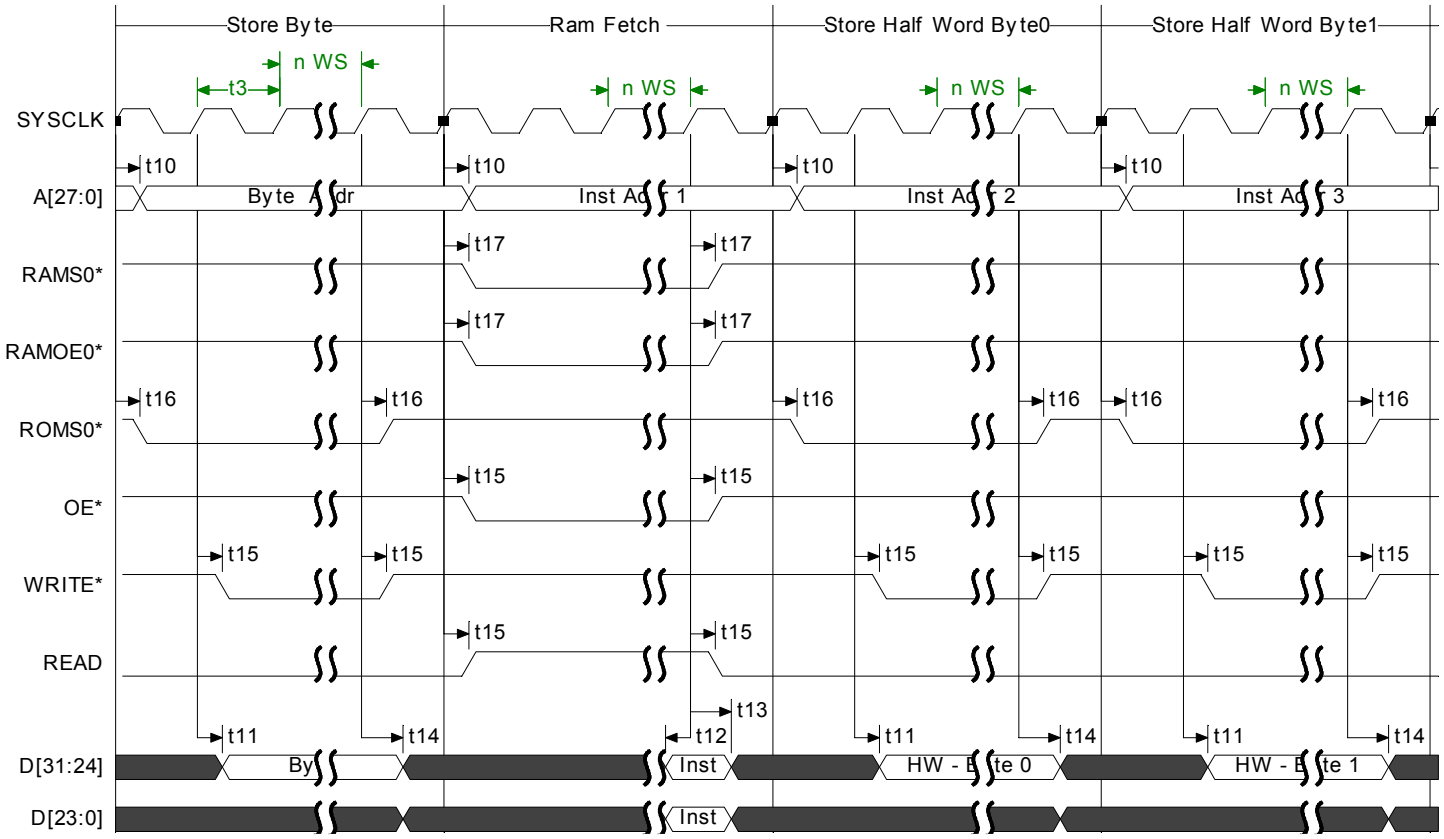


Figure 65. Fetch from 8-bit PROM with EDAC enabled - n Waitstates

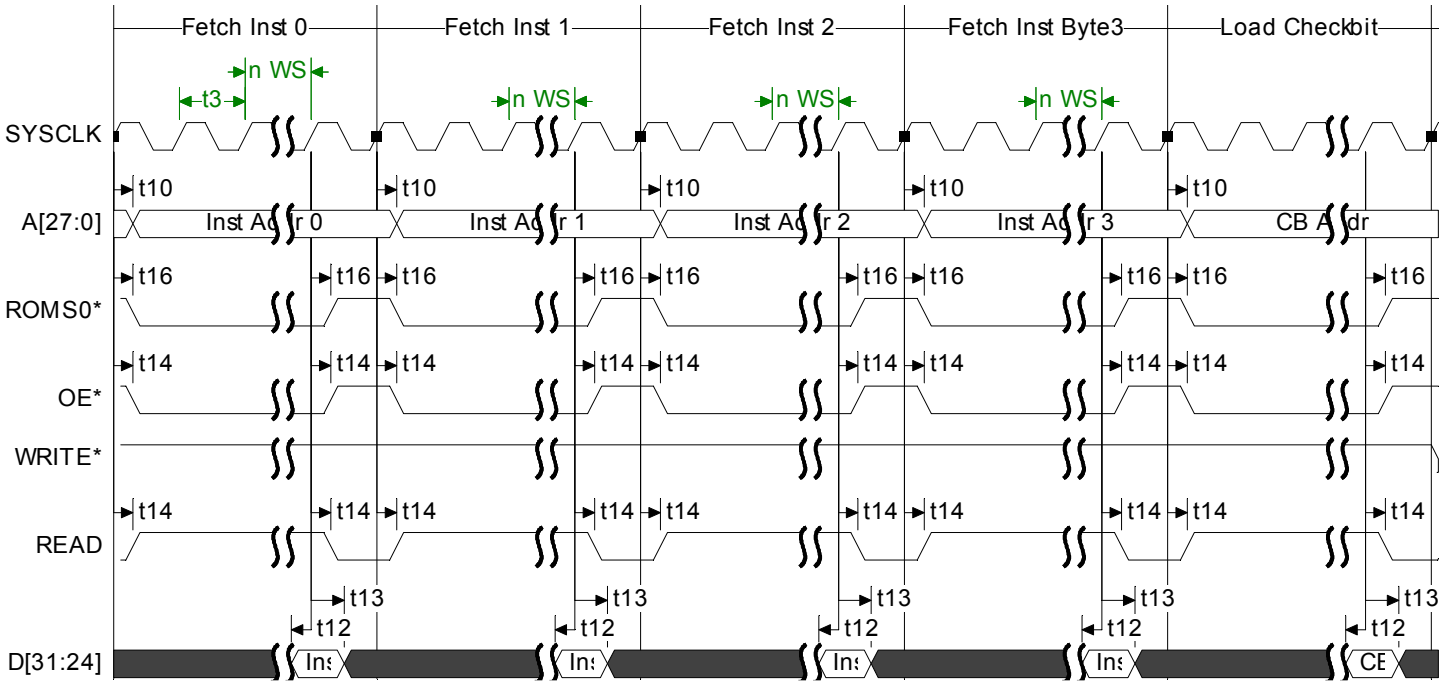


Figure 66. Fetch from 16-bit PROM - n Waitstates

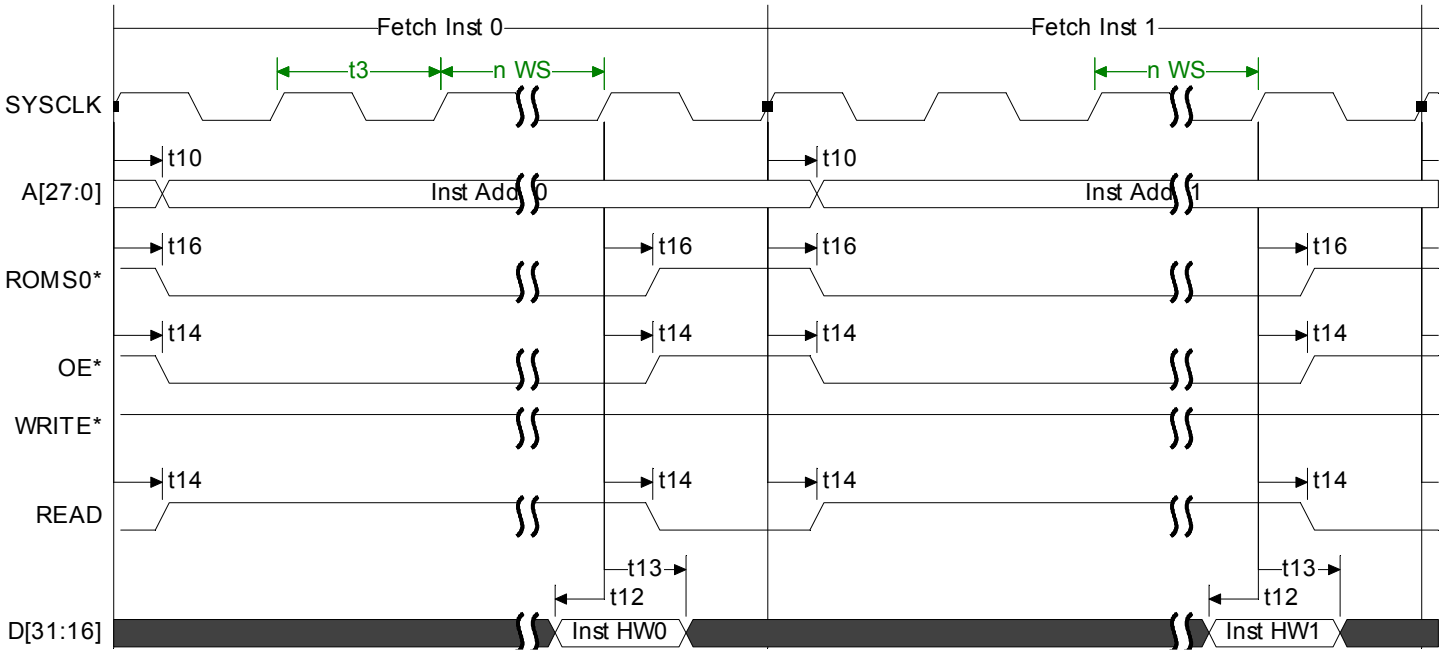


Figure 67. Fetch, Read and Write from/to 32-bit SRAM - 0 Waitstate

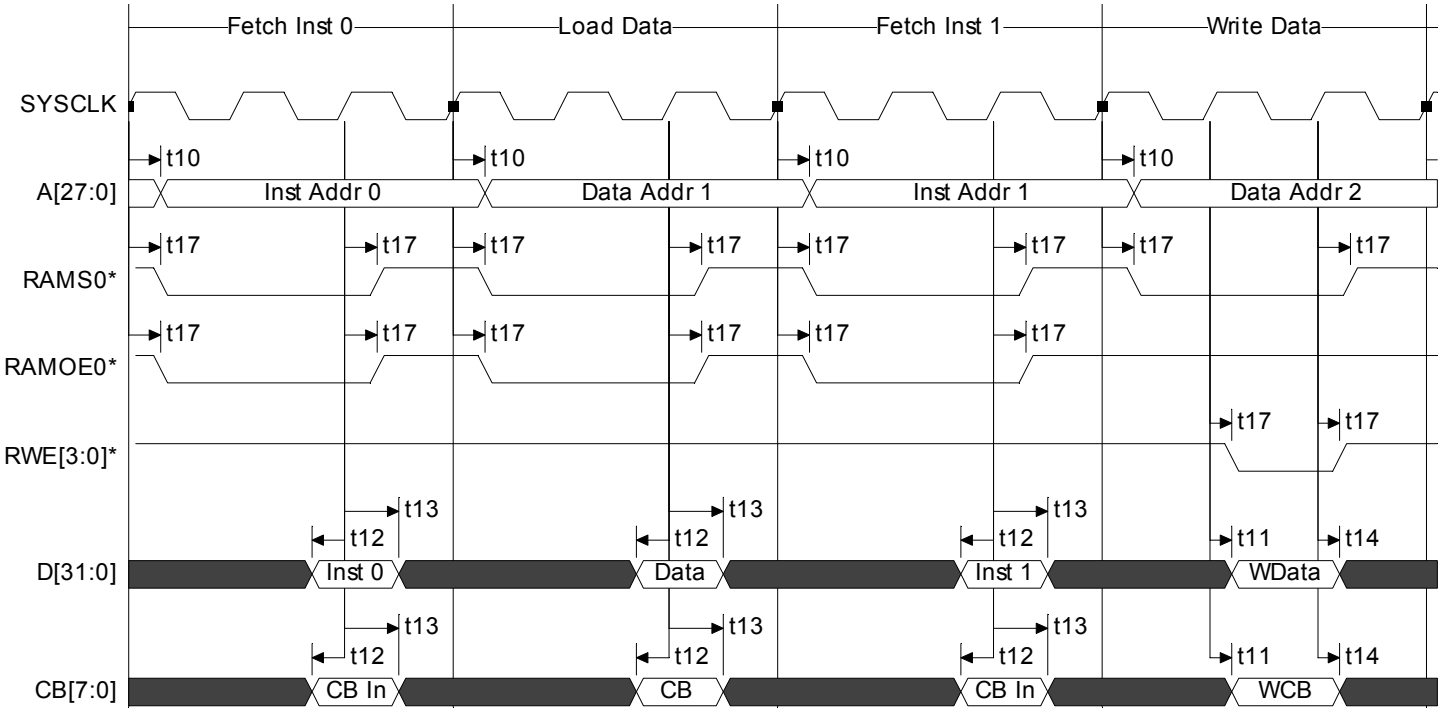


Figure 68. Fetch, Read and Write from/to 32-bit SRAM - n Waitstates

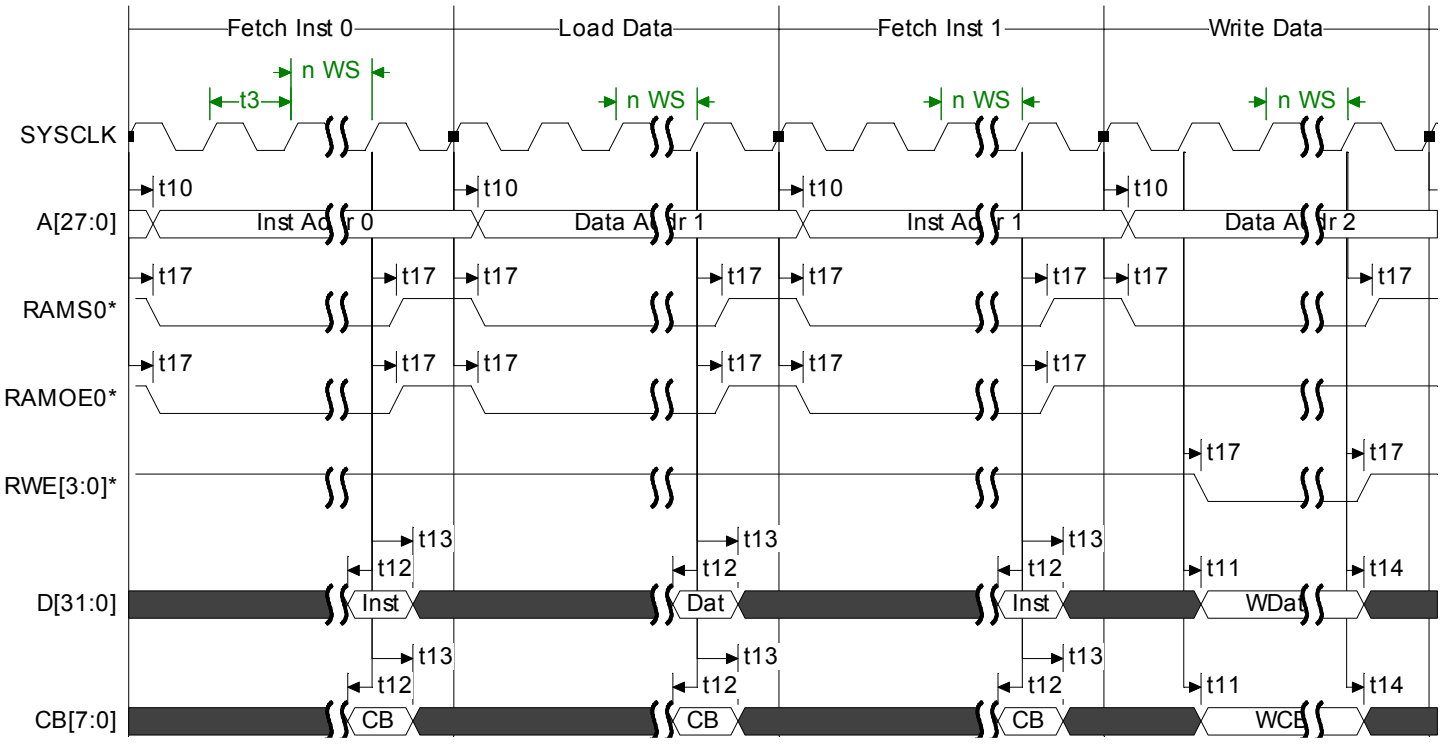


Figure 69. Burst of RAM Fetches and RAM Write Sequence - 0 Waitstate

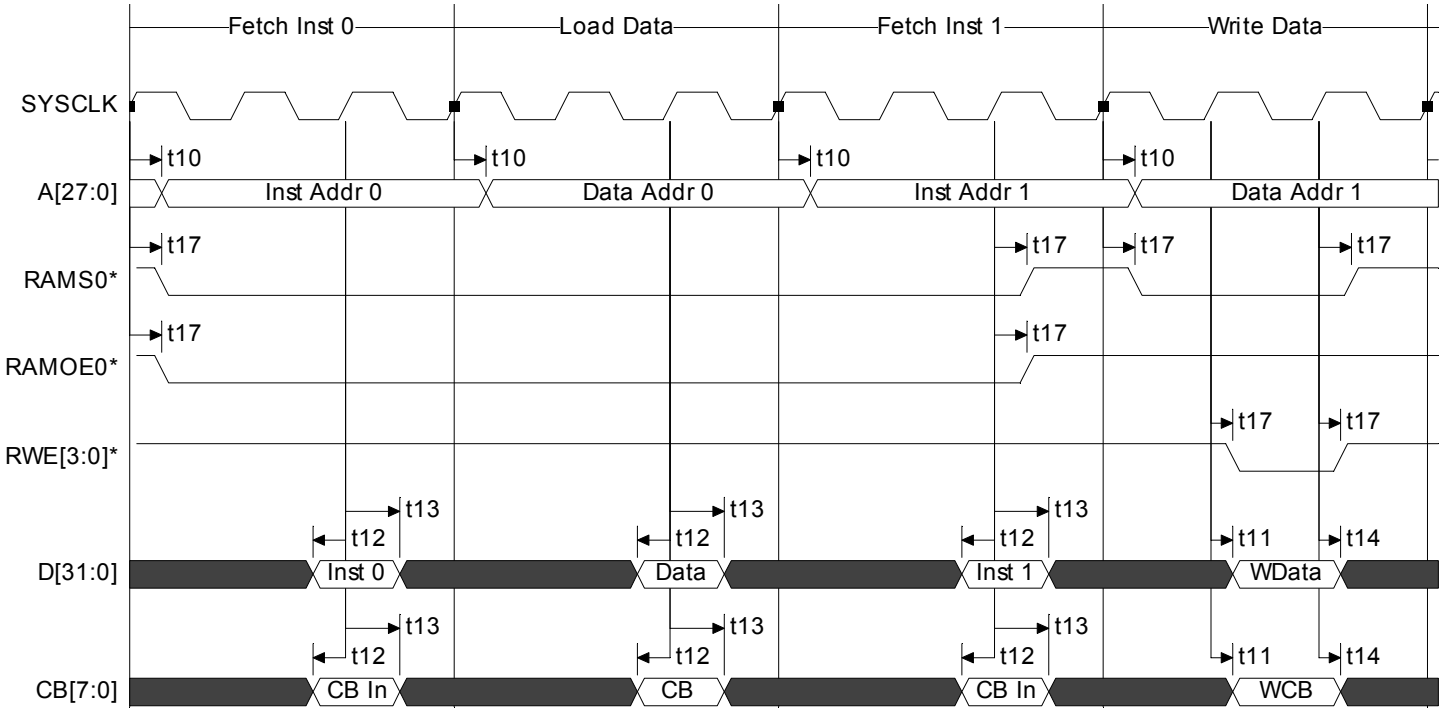


Figure 70. Burst of RAM Fetches and RAM Write Sequence - n Waitstates

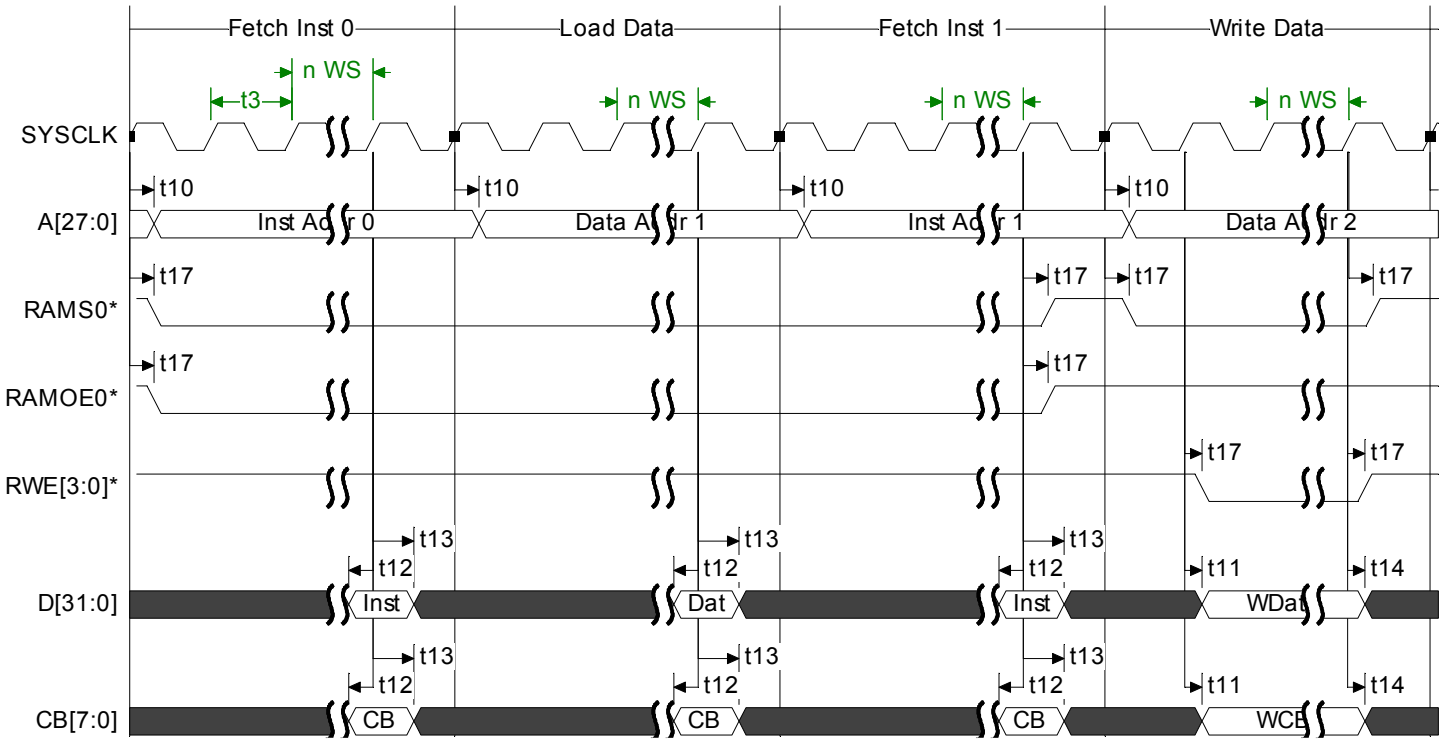


Figure 71. SDRAM Read (or Fetch) with Precharge - Burst length = 1; CL = 3

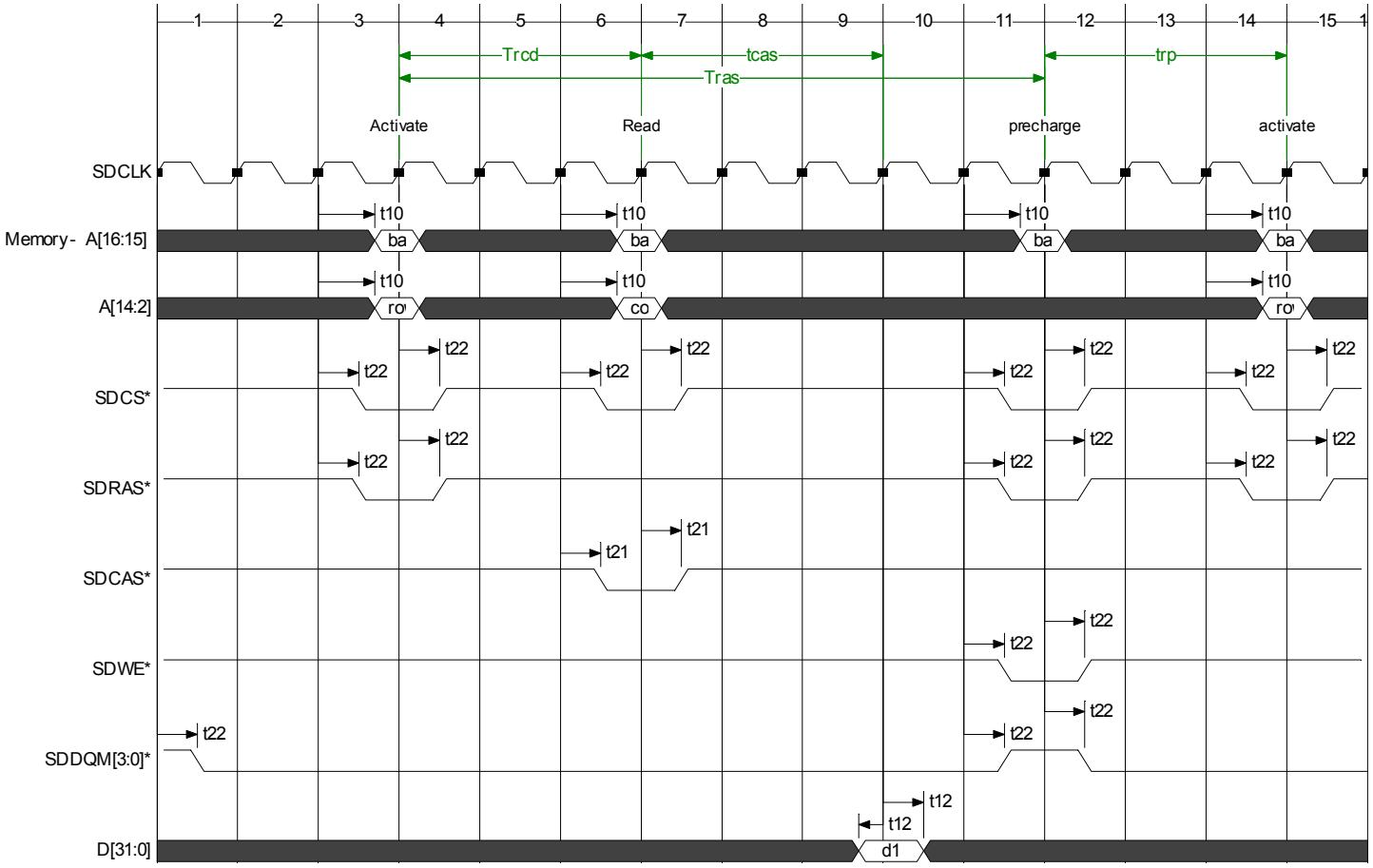


Figure 72. SDRAM Write with Precharge - Burst length = 1; CL = 3

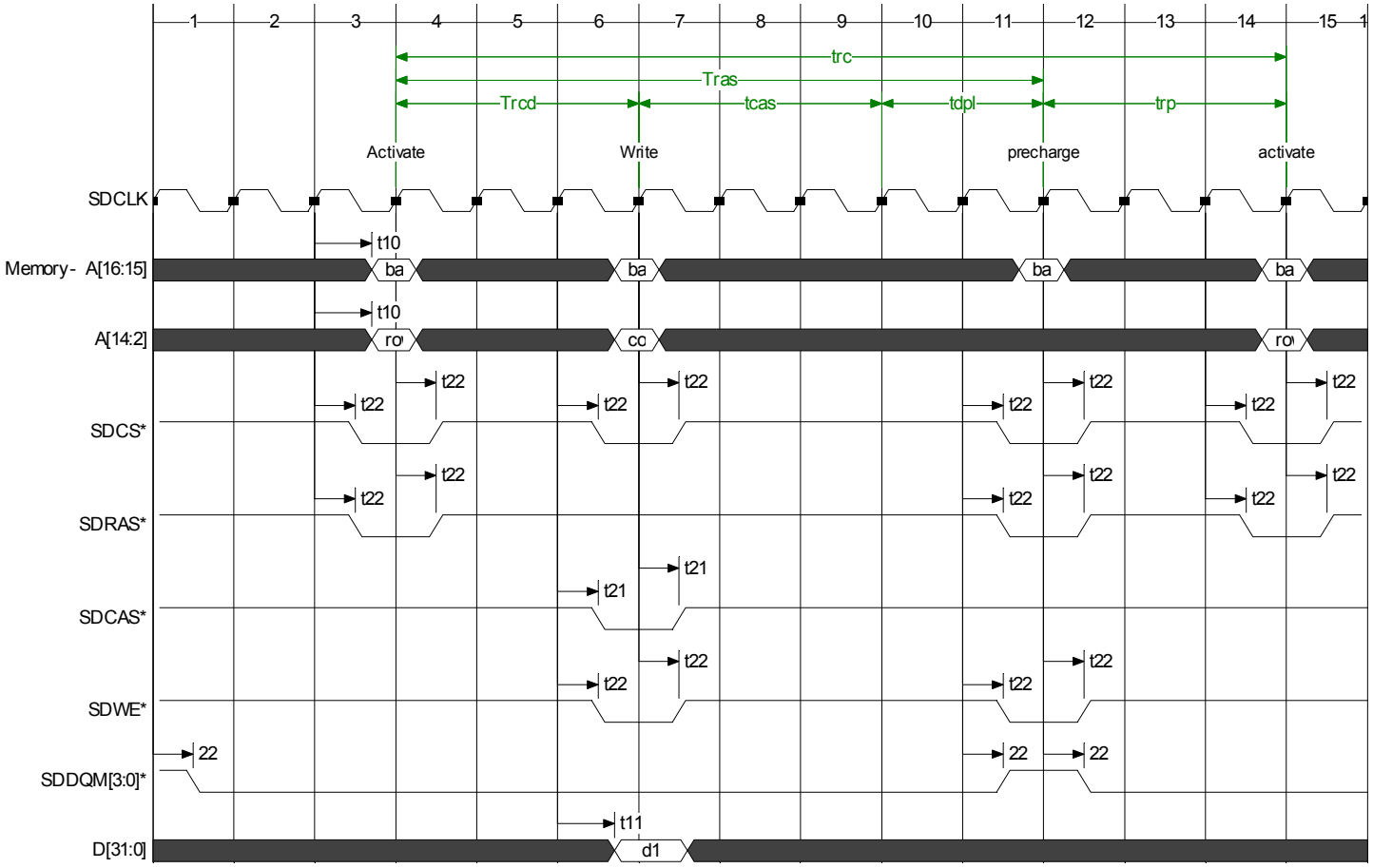


Figure 73. Fetch from ROM, Read and Write from/to 32-bit I/O - 0 Waitstate

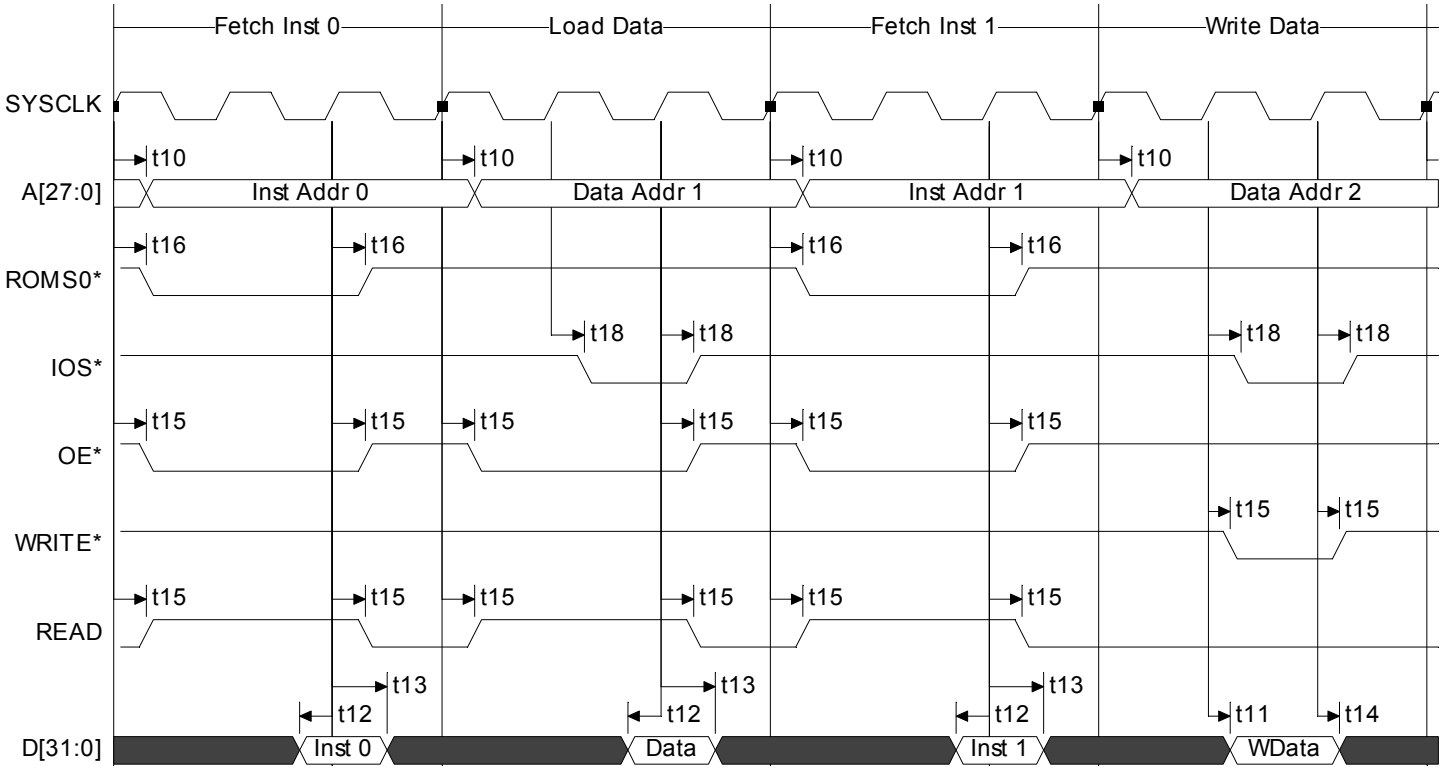


Figure 74. Fetch from ROM, Read and Write from/to 32-bit I/O - n Waitstates

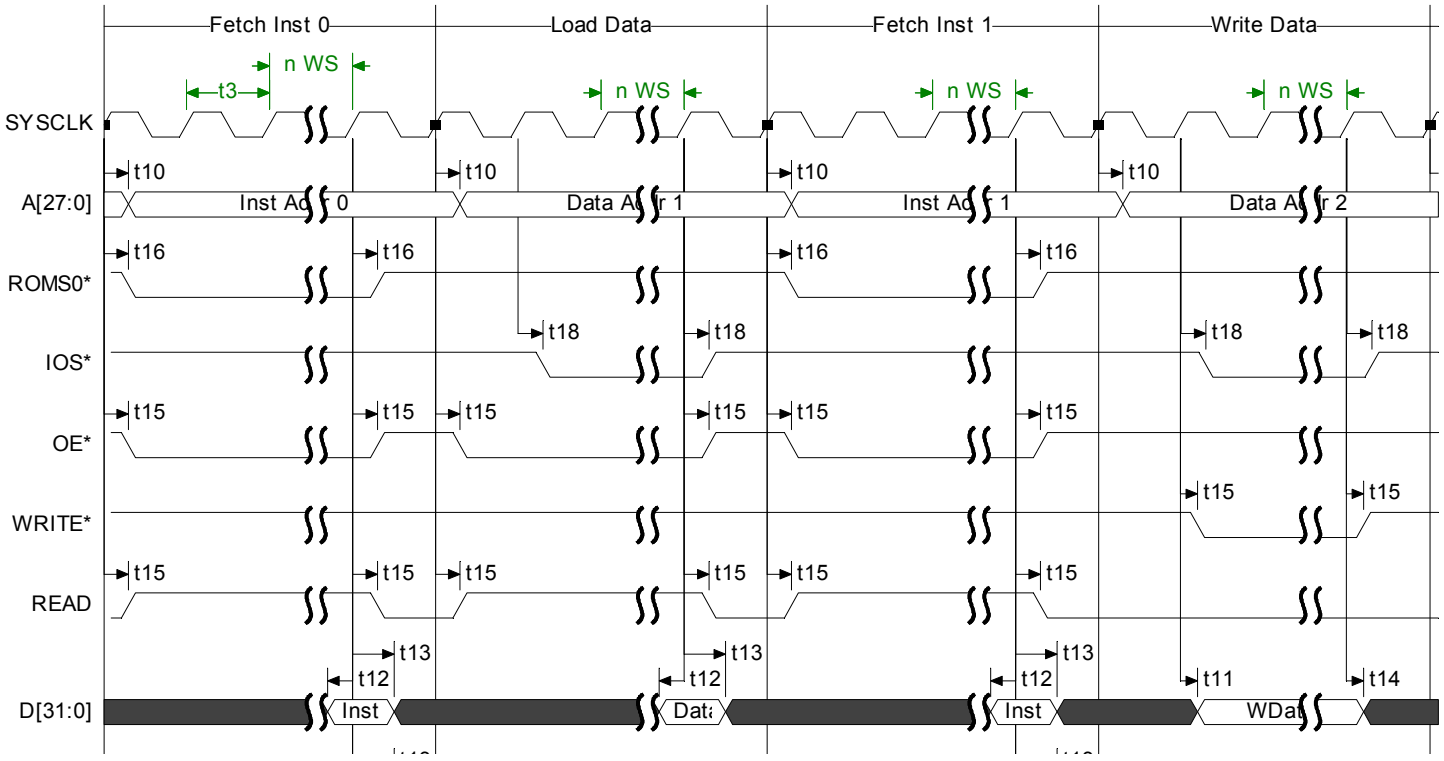
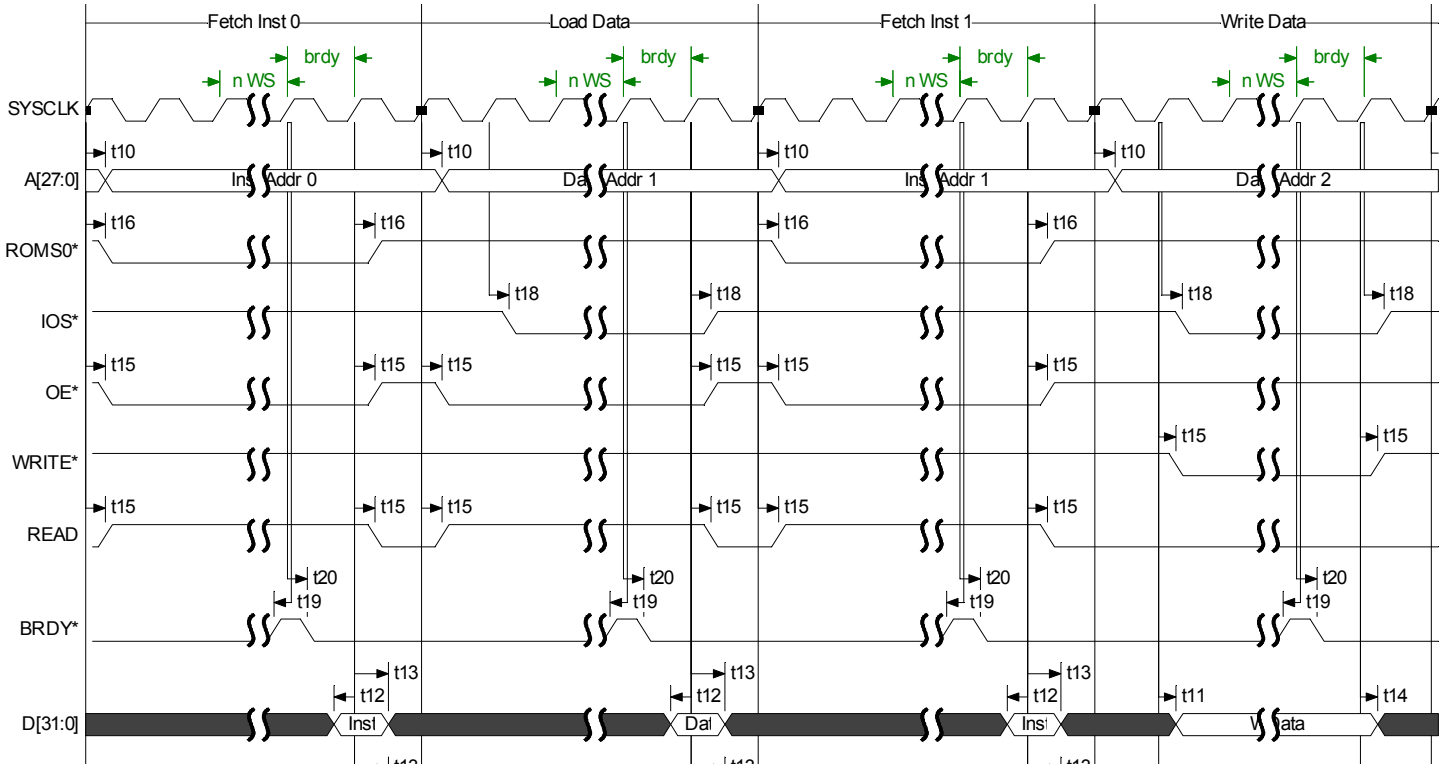


Figure 75. Fetch from ROM, Read and Write from/to 32-bit I/O - n Waitstates + BRDY*



Ordering Information

Table 117. Possible Order Entries

Part-Number	Supply Voltage (core / IOs)	Temperature Range	Maximum Speed (MHz)	Packaging	Quality Flow
AT697E-2H-E	1.8V / 3.3V	+25°C	100	MCGA349	Engineering Samples
5962-0722401QXB	1.8V / 3.3V	-55°C ; +125°C	100	MCGA349	QMLQ
AT697E-2H-SV	1.8V / 3.3V	-55°C ; +125°C	100	MCGA349	Space level B
AT697E-KG-E	1.8V / 3.3V	+25°C	100	MQFP256	Engineering Samples
AT697E-KG-MQ	1.8V / 3.3V	-55°C ; +125°C	100	MQFP256	Military Level B
AT697E-KG-SV	1.8V / 3.3V	-55°C ; +125°C	100	MQFP256	Space level B

Datasheet Revision History

Changes from Rev. C 08/05 to Rev. D 02/06

1. Update of electrical characteristics and timing diagrams.

Rev. D 02/06 to Rev. E 09/06

1. Timing chronograms review for IO space and ROM space.
2. Update of electrical characteristics and timing diagrams.

Rev. F 02/09

1. Add MQFP256 pinout
2. Part number modification

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