May 9, 2012

TEXAS INSTRUMENTS

LP5907

Ultra Low-Noise, 250 mA Linear Regulator for RF/Analog Circuits - Requires No Bypass Capacitor

General Description

The LP5907 is a linear regulator capable of supplying 250 mA output current. Designed to meet the requirements of RF/Analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current, and low line/load transient response figures. Using new innovative design techniques the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

The device is designed to work with a 1.0 µF input and a 1.0 µF output ceramic capacitor. (No Bypass Capacitor is required.)

The device is available in an ultra-thin micro SMD package. This device is available between 1.2V and 4.5V in 25 mV steps. Please contact Texas Instruments Sales for specific voltage option needs.

Features

- Stable with 1.0 µF Ceramic Input and Output Capacitors
- No Noise Bypass Capacitor Required
- Remote Output Capacitor Placement
- Thermal-overload and short-circuit protection
- −40°C to +125°C junction temperature range for operation

Key Specifications

Input voltage range	2.2V to 5.5V
Output voltage range	1.2V to 4.5V
Output current	250 mA
Low output voltage noise	<10 μV_{RMS}
PSRR	82 dB at 1kHz
Output voltage tolerance	± 2%
Virtually zero I_Q (disabled)	<1µA
Very low I_Q (enabled)	12 µA
Startup time	80 µs
Low dropout	120 mV typ.

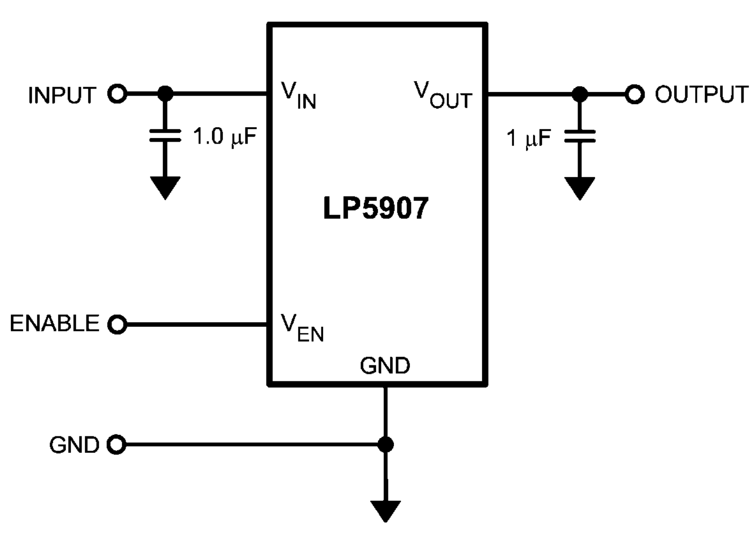
Package

4-Bump ultra-thin micro SMD (lead free)	0.35 mm pitch 0.65 mm x 0.65 mm x 0.40 mm

Applications

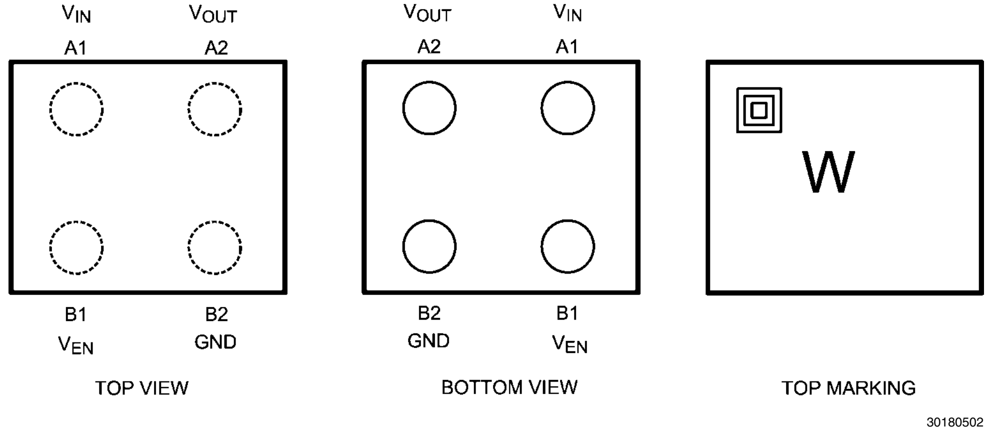
- Cellular phones
- PDA handsets
- Wireless LAN devices

Typical Application Circuit



Connection Diagrams

4-Bump Ultra-Thin micro SMD Package
Package Number UVK04AAA



The actual physical placement of the package marking will vary from part to part.

Pin Descriptions

micro SMD Pin No.	Symbol	Name and Function
A1	VIN	Input voltage supply. A 1.0 µF capacitor should be connected at this input.
A2	VOUT	Output voltage. A 1.0 µF Low ESR capacitor should be connected to this pin. Connect this output to the load circuit. An internal 280Ω discharge resistor prevents a charge remaining on V_{OUT} when disabled, only active when EN = high.
B1	VEN	Enable input; disables the regulator when ≤ 0.4V. Enables the regulator when ≥ 1.2V. An internal 1MΩ pulldown resistor connects this input to ground.
B2	GND	Common ground.

Ordering Information

micro SMD Package (Lead Free)

Output Voltage (V)	Supplied As	
	250 tape and reel	3000 tape and reel
1.2	LP5907UVE-1.2/NOPB	LP5907UVX-1.2/NOPB
1.8	LP5907UVE-1.8/NOPB	LP5907UVX-1.8/NOPB
2.7	LP5907UVE-2.7/NOPB	LP5907UVX-2.7/NOPB
2.8	LP5907UVE-2.8/NOPB	LP5907UVX-2.8/NOPB
2.85	LP5907UVE-2.85/NOPB	LP5907UVX-2.85/NOPB
3.0	LP5907UVE-3.0/NOPB	LP5907UVX-3.0/NOPB
3.1	LP5907UVE-3.1/NOPB	LP5907UVX-3.1/NOPB
3.2	LP5907UVE-3.2/NOPB	LP5907UVX-3.2/NOPB
3.3	LP5907UVE-3.3/NOPB	LP5907UVX-3.3/NOPB
4.5	LP5907UVE-4.5/NOPB	LP5907UVX-4.5/NOPB

Contact your local TI Sales Office for availability of other voltage options.

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

V_{IN} Pin: Input Voltage	−0.3 to 6.0V
V_{OUT} Pin: Output Voltage	−0.3 to (V_{IN} + 0.3V) to 6.0V (max)
V_{EN} Pin: Enable Input Voltage	−0.3 to (V_{IN} + 0.3V) to 6.0V (max)
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65 to 150°C
Maximum Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating (Note 4)	
Human Body Model	2kV
Machine Model	200V

Operating Ratings (Note 1, Note 2)

V_{IN}: Input Voltage Range	2.2V to 5.5V
V_{EN}: Enable Voltage Range	0 to (V_{IN} + 0.3V) to 5.5V (max)
Recommended Load Current (Note 5)	0 to 250 mA
Junction Temperature Range (T_J)	−40°C to +125°C
Ambient Temperature Range (T_A) (Note 5)	−40°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance θ_{JA} (Note 6)

JEDEC Board (micro SMD) (Note 16)	119.6°C/W
4L Cellphone Board (micro SMD)	186.5°C/W

Electrical Characteristics

Limits in standard typeface are for T_A = 25ºC. Limits in **boldface** type apply over the full operating junction temperature range (−40ºC ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP5907 Typical Application Circuit (pg. 1) with: V_{IN} = $V_{OUT (NOM)}$ + 1.0V, V_{EN} = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, I_{OUT} = 1.0 mA. (Note 2, Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.2		5.5	V
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V, I_{OUT} = 1mA to 250 mA	**−2**		**2**	%
	Line Regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V, I_{OUT} = 1 mA		0.02		%/V
	Load Regulation	I_{OUT} = 1mA to 250 mA		0.001		%/mA
I_{LOAD}	Load Current	(Note 9)				mA
	Maximum Output Current		**250**			
I_Q	Quiescent Current (Note 11)	V_{EN} = 1.2V, I_{OUT} = 0 mA		12	**25**	µA
		V_{EN} = 1.2V, I_{OUT} = 250 mA		250	**425**	
		V_{EN} = 0.3V (Disabled)		0.2	**1**	
I_G	Ground Current (Note 13)	I_{OUT} = 0 mA (V_{EN} = 1.2V)		14		µA
V_{DO}	Dropout Voltage (Note 10)	V_{OUT} = 2.8V; I_{OUT} = 100 mA		50		mV
		V_{OUT} = 2.8V; I_{OUT} = 250 mA		120	**200**	
I_{SC}	Short Circuit Current Limit	(Note 12)	250	500		mA
PSRR	Power Supply Rejection Ratio (Note 15)	f = 100 Hz, I_{OUT} = 20 mA		90		dB
		f = 1 kHz, I_{OUT} = 20 mA		82		
		f = 10 kHz, I_{OUT} = 20 mA		65		
		f = 100 kHz, I_{OUT} = 20 mA		60		
e_N	Output Noise Voltage (Note 15)	BW = 10 Hz to 100 kHz, I_{OUT} = 1 mA		10		$µV_{RMS}$
		BW = 10 Hz to 100 kHz, I_{OUT} = 250 mA		6.5		
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		160		°C
		Hysteresis		15		

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIN INPUT THRESHOLDS						
V_{IL}	Low Input Threshold (V_{EN})	V_{IN} = 2.2V to 5.5V			**0.4**	V
V_{IH}	High Input Threshold (V_{EN})	V_{IN} = 2.2V to 5.5V	**1.2**			V
I_{EN}	Input Current at V_{EN} Pin (Note 14)	V_{EN} = 5.5V and V_{IN} = 5.5V		5.5		µA
		V_{EN} = 0.0V and V_{IN} = 5.5V		0.001		
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line Transient (Note 15)	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to ($V_{OUT(NOM)}$ + 1.6V) in 30 µs, I_{OUT} = 1mA	**-1**			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6V) to ($V_{OUT(NOM)}$ + 1.0V) in 30 µs, I_{OUT} = 1mA			**+1**	
	Load Transient (Note 15)	I_{OUT} = 1mA to 250 mA in 10 µs	**−40**			mV
		I_{OUT} = 250 mA to 1mA in 10 µs			**40**	
	Overshoot on Startup (Note 15)	Stated as a percentage of nominal VOUT			**5**	%
	Turn on Time	To 95% of $V_{OUT(NOM)}$		80	150	µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage.

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$. See applications section.

Note 6: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 9: The device maintains a stable, regulated output voltage without a load current.

Note 10: Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Note 11: Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.

Note 12: Short Circuit Current is measured with V_{OUT} pulled to 0V and V_{IN} worst case = 6.0V.

Note 13: Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.

Note 14: There is a 1MΩ resistor between V_{EN} and ground on the device.

Note 15: This specification is guaranteed by design.

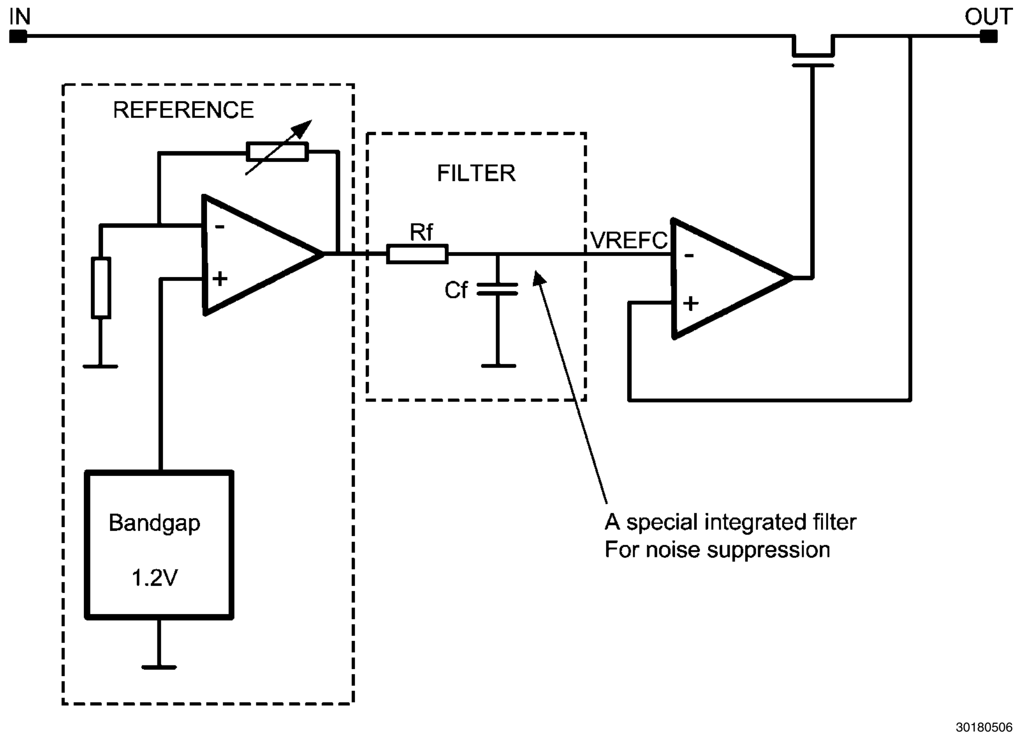
Note 16: Detailed description of the board can be found in JESD51-7.

Output & Input Capacitors

Symbol	Parameter	Conditions	Min	Nom	Max	Units
C_{IN}	Input Capacitance (Note 15)	Capacitance for stability	**0.7**	1.0		µF
C_{OUT}	Output Capacitance (Note 15)		**0.7**	1.0	**10**	
ESR	Output/Input Capacitance (Note 15)		5		500	mΩ

Note: The minimum capacitance should be > 0.5 µF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.

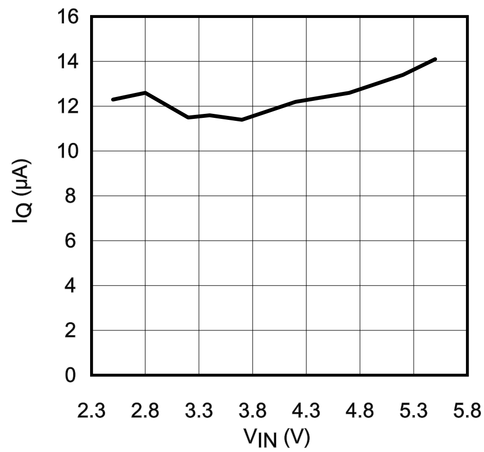
Block Diagram



Typical Performance Curves

Unless otherwise, V_{OUT} = 2.8V, V_{IN} = 3.7V, EN = 1.2V, C_{IN} = 1.0µF, C_{OUT} = 1.0µF, T_A = 25°C.

I_q vs. V_{IN}



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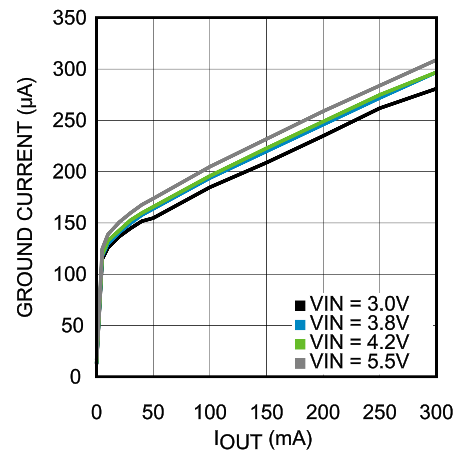
Ground Current vs. Output Current



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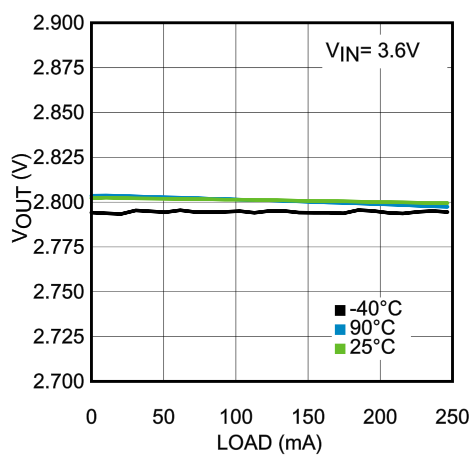
Load Regulation



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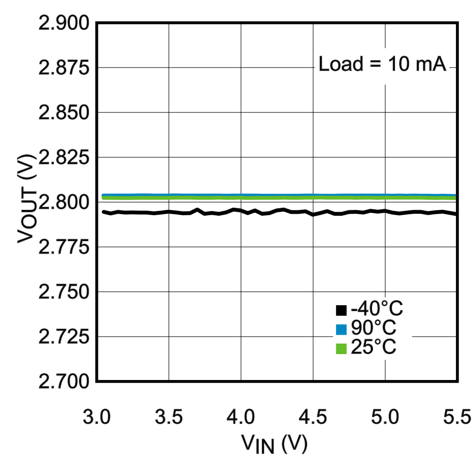
Line Regulation



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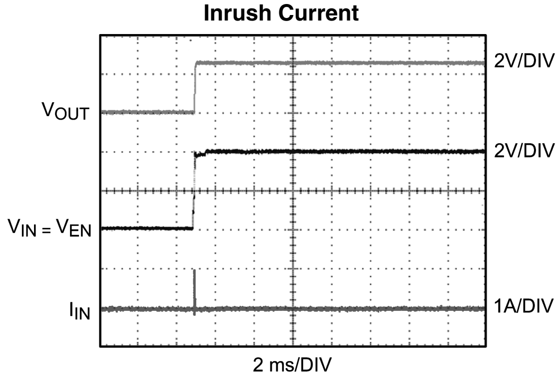
Inrush Current



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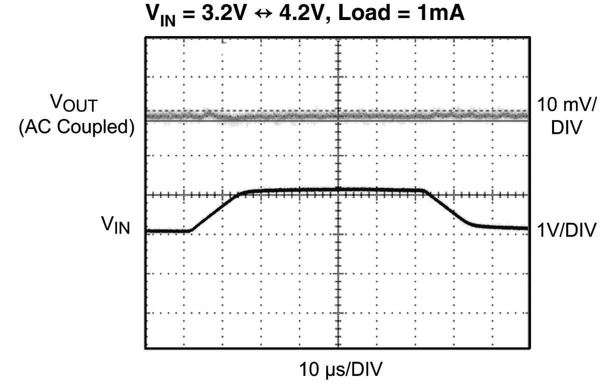
Line Transient
V_{IN} = 3.2V ↔ 4.2V, Load = 1mA



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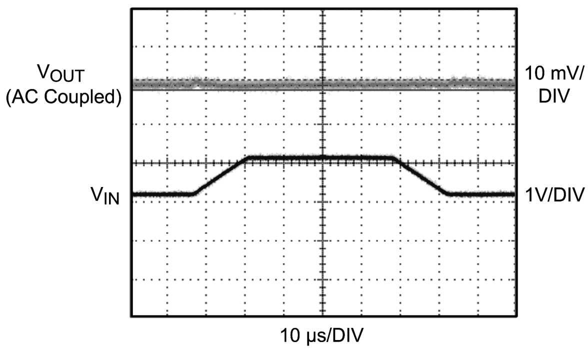
Line Transient
V_{IN} = 3.2V ↔ 4.2V, Load = 250mA



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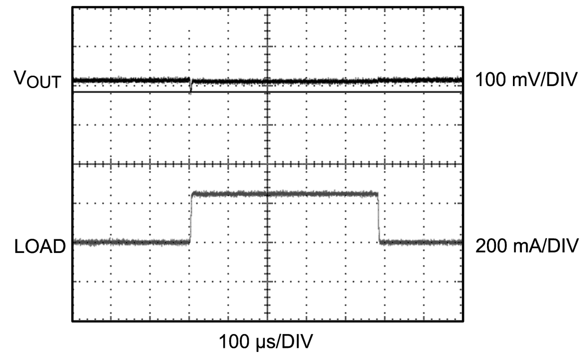
Load Transient
Load = 0mA ↔ 250mA, −40°C



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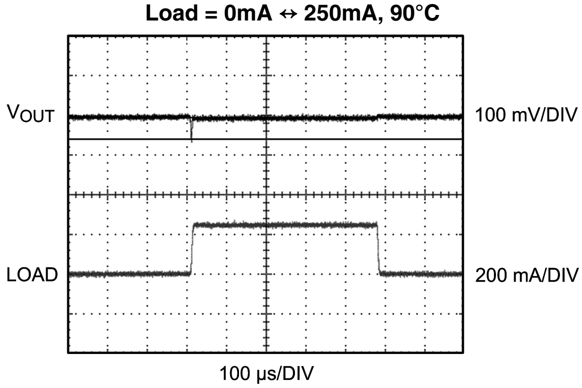
Load Transient
Load = 0mA ↔ 250mA, 90°C



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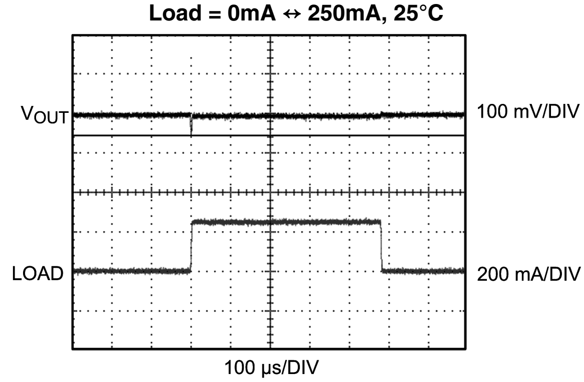
Load Transient
Load = 0mA ↔ 250mA, 25°C



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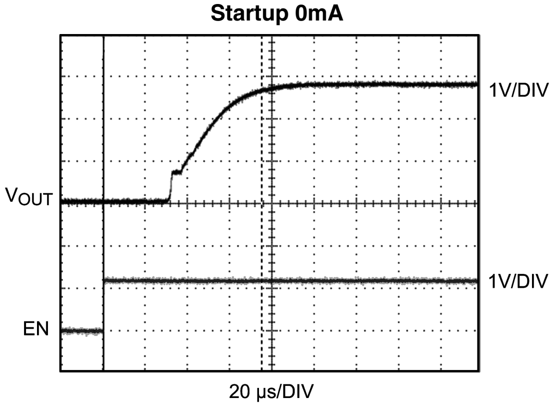
Startup 0mA



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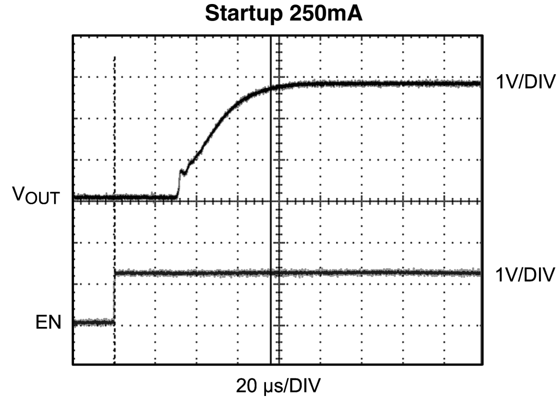
Startup 250mA



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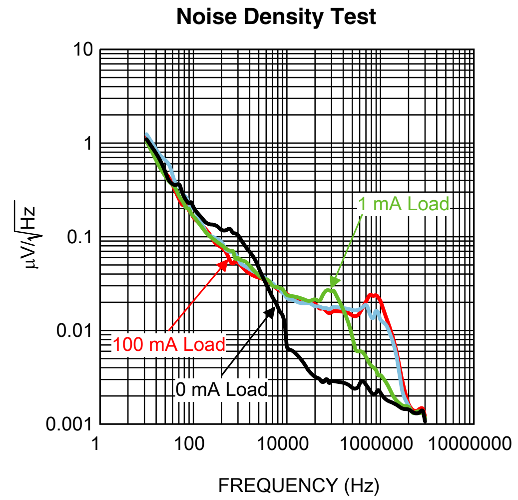

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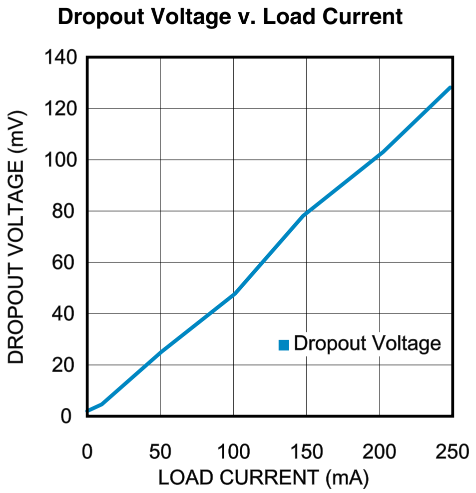

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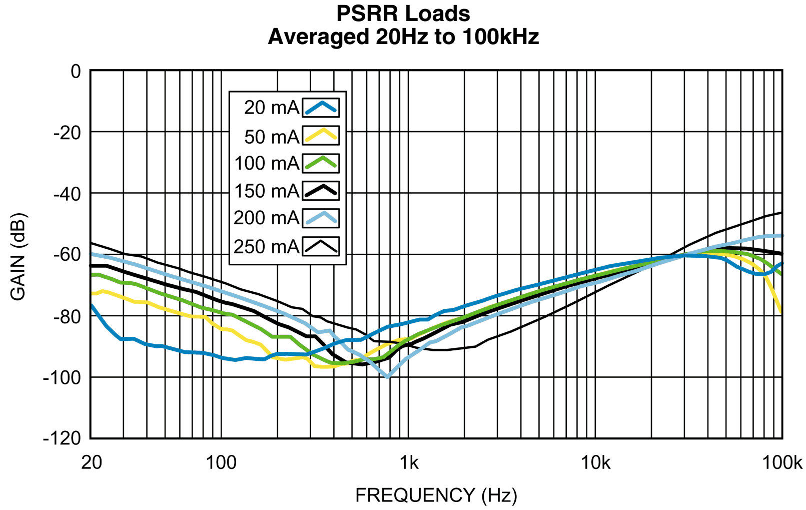

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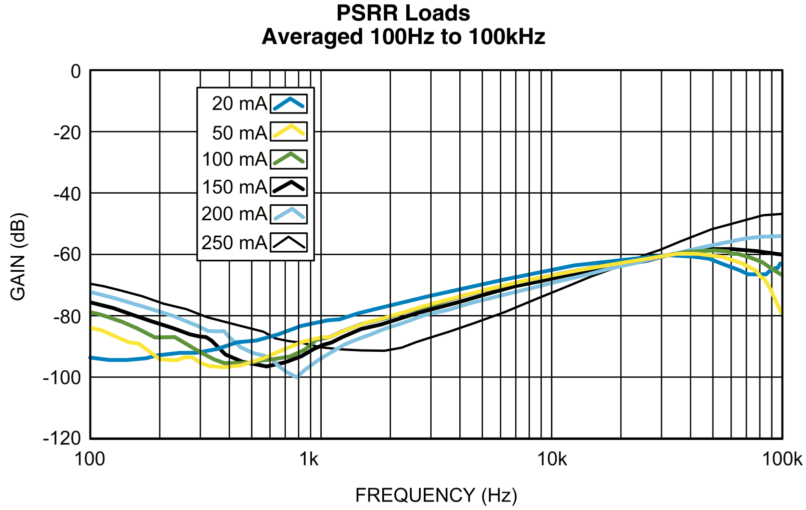

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Application Hints

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air. As stated in (*Note 5*) of the electrical characteristics, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{JMAX} - T_A)}{\theta_{JA}}$$

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP5907 requires external capacitors for regulator stability. The LP5907 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1.0 µF capacitor has to be connected between the LP5907 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1.0 uF

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907, then it is recommended to increase the input capacitor to at least 10 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 1.0 µF ±30% over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1.0 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 1.0 µF to 10 µF range, and with ESR between 5mΩ to 500 mΩ, is suitable in the LP5907 application circuit. For this device the output capacitor should be connected between the V_{OUT} pin and a good ground connection.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *CAPACITOR CHARACTERISTICS* below).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5mΩ to 500 mΩ for stability.

CAPACITOR CHARACTERISTICS

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1.0 µF to 10 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5907.

The temperature performance of ceramic capacitors varies by type and manufacturer. Most large value ceramic capacitors (≥2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1.0 µF to 10 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

REMOTE CAPACITOR OPERATION

The LP5907 requires at least a 1µF capacitor at output pin, but there is no strict requirements about the location of the capacitor in regards the LDO output pin. In practical designs the output capacitor may be located some 5-10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitor(s) in the system (like a capacitor at the input of supplied part). The Remote Capacitor feature helps user to minimize the number of capacitors in the system. As a good design practice, it is good to keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitor(s), keeping the LDO trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

NO-LOAD STABILITY

The LP5907 will remain stable and in regulation with no external load.

ENABLE CONTROL

The LP5907 may be switched ON or OFF by a logic input at the ENABLE pin. A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3nA. However if the application does not require the shutdown feature, the V_{EN} pin can be tied to V_{IN} to keep the regulator output permanently on.

A 1MΩ pulldown resistor ties the V_{EN} input to ground, this ensures that the device will remain off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

MICRO SMD MOUNTING

The micro SMD package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112.

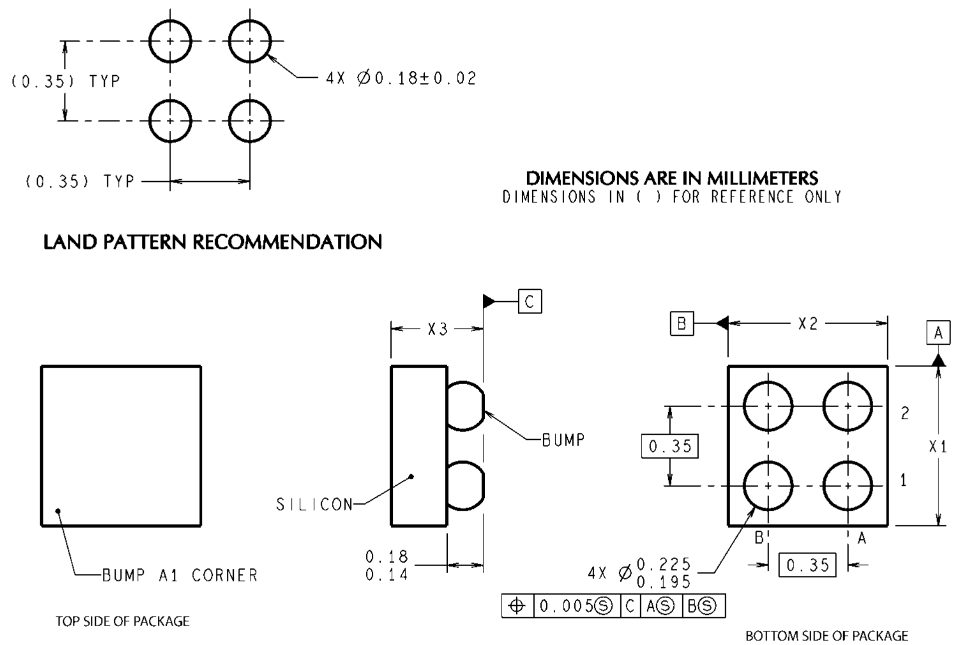
For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

MICRO SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

Physical Dimensions inches (millimeters) unless otherwise noted



UVK04XXX (Rev B)

4-Bump Ultra-Thin micro SMD Package (0.35 mm Pitch)
Package Number UVK04AAA
The dimensions for X1, X2 and X3 are given as:
X1 = 0.65 mm ± 0.030 mm
X2 = 0.65 mm ± 0.030 mm
X3 = 0.40 mm ± 0.045 mm

Notes

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