SLG46140

GreenPAK
Programmable Mixed-signal Matrix

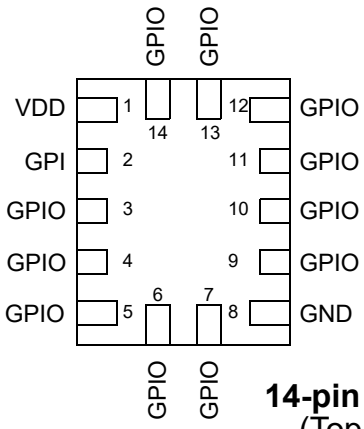
General Description

The SLG46140 GreenPAK is a one-time non-volatile memory (NVM) Programmable Mixed-Signal Matrix designed to implement a wide variety of mixed-signal functions in a single, small, low-power device by integrating a number of common discrete ICs and passive components.

Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- 1.8V (±5%) to 5V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free: 1.6 x 2.0 x 0.55 mm, 0.4 mm pitch

Pin Configuration



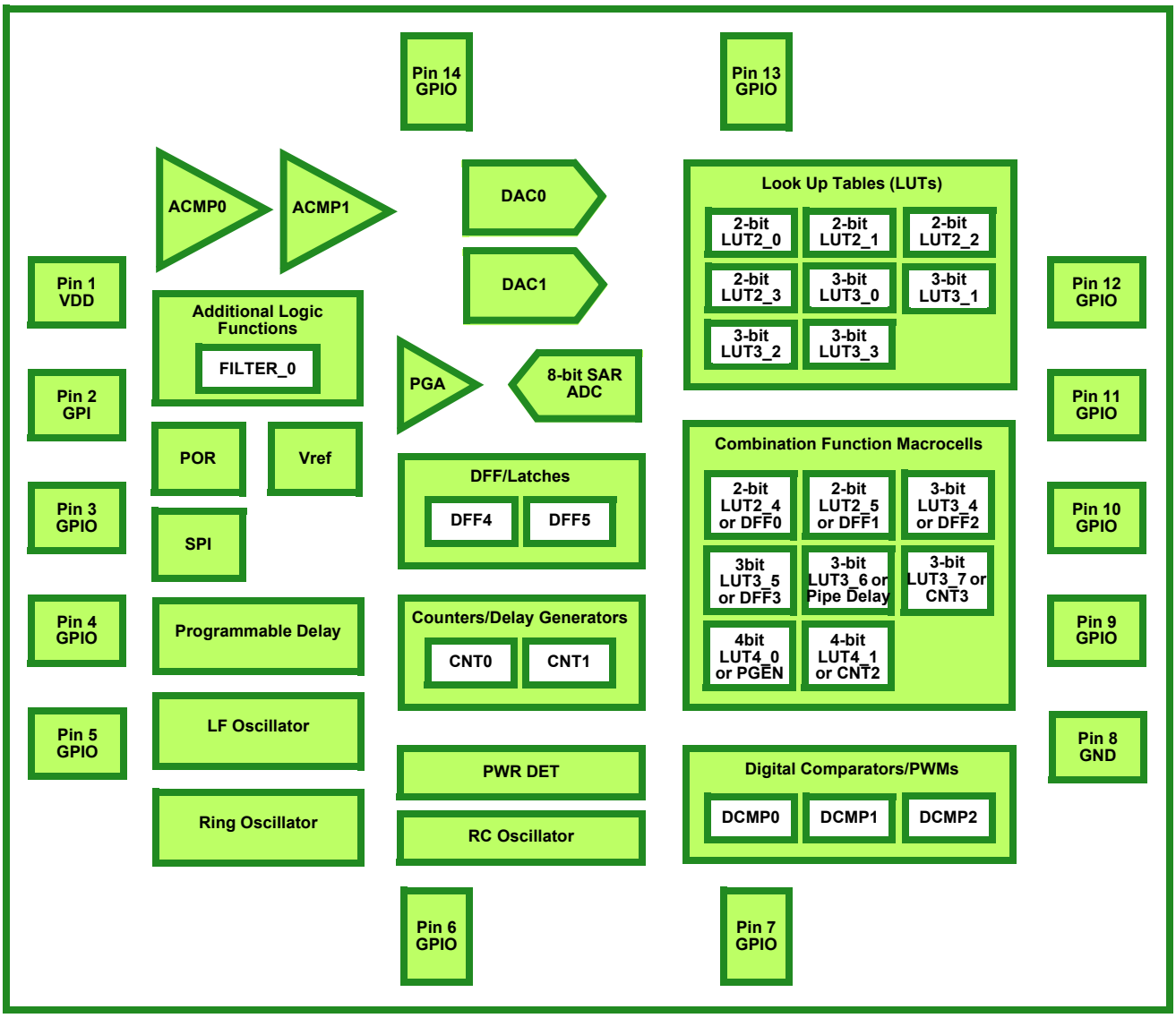
14-pin STQFN
(Top View)

Applications

The extensive list of integrated components included in the SLG46140 can be used to implement these and many other functions, often in combination.

- Ambient Light Detect
- Battery Charge Control
- Fan Control
- Hall Effect Drive
- LED Control
- Level Shift
- One-Shot Detect
- Optical Encode
- Over Voltage Protect
- Port Detection
- Power Sequencing
- Sensor Interface
- Signal De-Glitch
- Signal Delay
- System Reset
- Thermal Management
- Voltage Level Detect

Block Diagram



1.0 Overview

In addition to the integrated analog and digital components, the SLG46140 comprises an internal connection matrix and one-time programmable NVM. By programming the NVM, using the easy-to-use GreenPAK development tools, the designer configures the connection matrix, I/O Pins, and integrated components of the SLG46140. The SLG46140 includes the following analog and digital resources:

- 8-bit Successive Approximation Register Analog-to-Digital Converter (SAR ADC)
- ADC 3-bit Programmable Gain Amplifier (PGA)
- Two Digital-to-Analog Converters (DAC)
- Two Analog Comparators (ACMP)
- Voltage Reference (VREF)
- Eight Combinatorial Lookup Tables (LUTs)
  - Four 2-bit LUTs
  - Four 3-bit LUTs
- Nine Combination Function Macrocells
  - One 14-bit Delay/Counter (Wake-Sleep Control)
  - Two Selectable DFF/Latch or 2-bit LUTs
  - Two Selectable DFF/Latch or 3-bit LUTs
  - One Selectable 16-Stage / 3-Output Pipe Delay or 3-bit LUT
  - One 8-bit Delay/Counter/Finite State Machine
  - One 14-bit Delay/Counter/Finite State Machine
  - One Selectable Pattern Generator or 4-bit LUT
- Three Digital Comparators/Pulse Width Modulators (DCMPs /PWMs) w/ Selectable Deadband
- Three Counters/Delays (CNT/DLY)
  - One 14-bit Delay/Counter/Finite State Machine
  - One 14-bit Delay/Counter
  - One 8-bit Delay/Counter
- Two D Flip-flops/Latches
- Programmable Delay w/ Edge Detection
- Three Internal Oscillators
  - Low-Frequency
  - Ring
  - RC 25 kHz and 2 MHz
- Power-On-Reset (POR)
- Slave SPI
- One Bandgap

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply
2	GPI	General Purpose Input
3	GPIO	General Purpose I/O or ADC Vref_IO
4	GPIO	General Purpose I/O or Analog Comparator 0 (-) / PGA_OUT
5	GPIO	General Purpose I/O or Analog Comparator 1 (-)
6	GPIO	General Purpose I/O or PGA(+)
7	GPIO	General Purpose I/O or PGA(-)
8	GND	GND
9	GPIO	General Purpose I/O or ACMP1(+)
10	GPIO	General Purpose I/O or ACMP0(+)
11	GPIO	General Purpose I/O or AIN MUX
12	GPIO	General Purpose I/O
13	GPIO	General Purpose I/O
14	GPIO	General Purpose I/O

3.0 User Programmability

The SLG46140 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the I/O Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Silego to integrate into a production process.

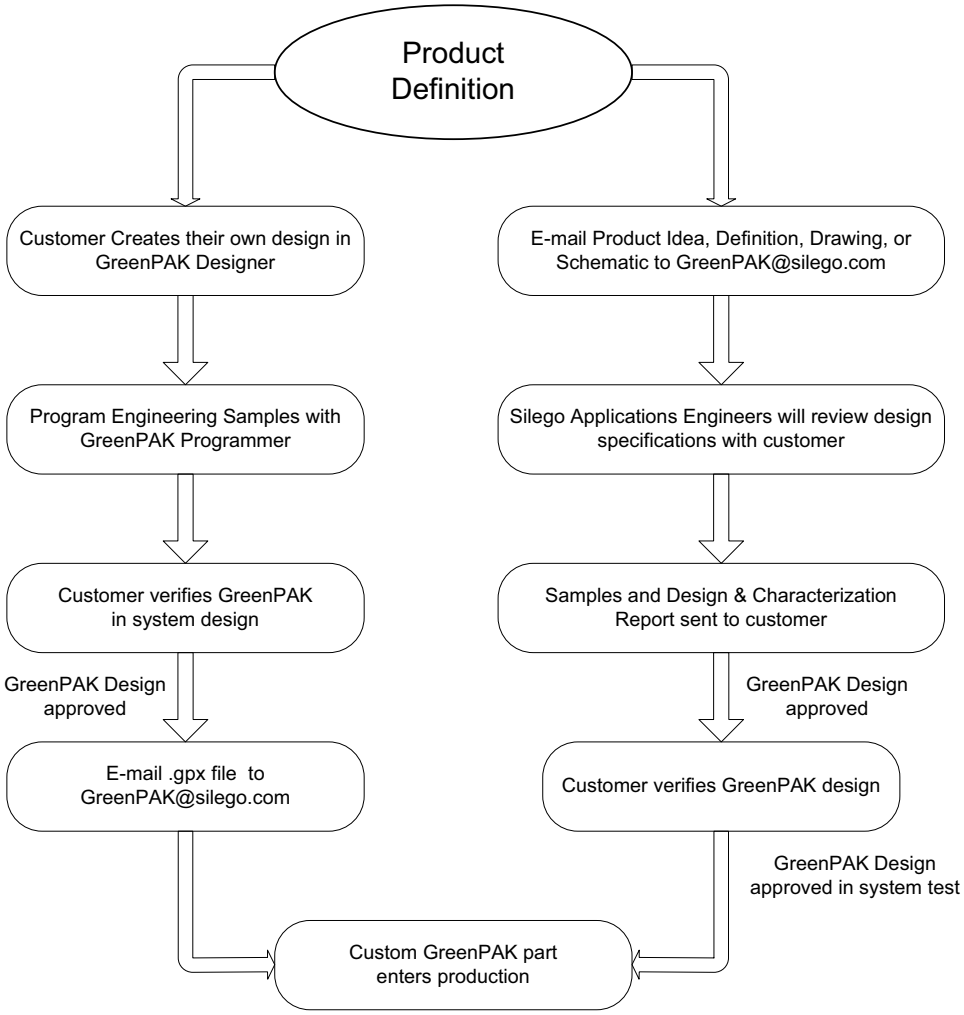


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46140V	14-pin STQFN
SLG46140VTR	14-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
	Push-Pull 2x	--	21	
	Push-Pull 4x	--	43	
	OD 1x	--	18	
	OD 2x	--	45	
	OD 4x	--	72	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.08	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD}	V
		Low-Level Logic Input	0.980	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	0.690	V
		Logic Input with Schmitt Trigger	0	--	0.440	V
		Low-Level Logic Input	0	--	0.520	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.273	0.413	0.553	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.39	2.39	nA
		Vin = VDD	--	0.26	1.29	nA
	PGA Input Leakage	Vin = 0 V	--	0.04	0.18	nA
		Vin = VDD	--	0.12	0.65	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.04	0.34	nA
		Vin = VDD	--	1.55	71.77	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.04	0.39	nA
		Vin = VDD	--	1.55	72.26	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.04	0.33	nA
		Vin = VDD	--	1.55	72.39	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.670	1.788	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.679	1.792	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 100 µA	1.700	1.798	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.007	0.010	V
		Push-Pull 4X, I_{OL}= 100 µA	--	0.004	0.009	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.007	0.010	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.002	0.010	V
		Open Drain NMOS 4X, I_{OL}= 100 µA	--	0.001	0.004	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.053	1.690	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.069	3.390	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, $V_{OH} = V_{DD}$ - 0.2	4.007	7.070	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.420	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.840	--	mA
		Push-Pull 4X, V_{OL} = 0.15 V	4.430	6.122	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.840	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.680	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.15 V	10.504	14.987	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.671	1.179	4.999	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.961	1.310	1.657	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.875	1.109	1.287	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	896.67	1075.81	1337.85	kΩ
		100 k Pull Up	93.13	111.06	132.78	kΩ
		10 k Pull Up	11.10	12.95	15.30	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	660.68	1074.06	1287.58	kΩ
		100 k Pull Down	93.29	111.06	132.78	kΩ
		10 k Pull Down	10.90	12.75	15.51	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6 and 7 are connected to one side, pins 9,10, 11, 12, 13 and 14 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs (when all macrocells that require internal RC OSC or bandgap are inactive)	--	0.16	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V_{DD}	V
		Low-Level Logic Input	1.130	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.210	V
		Logic Input with Schmitt Trigger	0	--	0.950	V
		Low-Level Logic Input	0	--	0.690	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.346	0.486	0.625	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.42	2.49	nA
		Vin = VDD	--	0.30	1.48	nA
	PGA Input Leakage	Vin = 0 V	--	0.05	0.21	nA
		Vin = VDD	--	0.13	0.73	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.05	0.39	nA
		Vin = VDD	--	1.47	67.45	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.05	0.40	nA
		Vin = VDD	--	1.47	67.80	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.05	0.39	nA
		Vin = VDD	--	1.47	67.84	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 3 mA	2.722	3.102	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.861	3.201	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 3 mA	2.927	3.248	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.151	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.079	0.130	V
		Push-Pull 4X, I_{OL}= 3 mA	--	0.055	0.104	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.070	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.040	0.070	V
		Open Drain NMOS 4X, I_{OL}= 3 mA	--	0.018	0.023	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.770	11.151	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.278	21.750	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	21.458	40.903	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.060	6.920	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	8.130	13.840	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	19.628	28.240	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	8.130	13.850	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	16.260	23.700	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	45.976	66.769	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				VDD	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.504	0.927	3.092	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.962	1.312	1.658	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.876	1.109	1.287	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	888.18	1075.30	1316.50	kΩ
		100 k Pull Up	92.15	110.40	132.16	kΩ
		10 k Pull Up	9.83	11.99	14.49	kΩ

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
R_{PDWN}	Pull Down Resistance	1 M Pull Down	662.60	1074.47	1285.21	kΩ
		100 k Pull Down	92.42	110.60	132.48	kΩ
		10 k Pull Down	10.00	11.88	14.25	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6 and 7 are connected to one side, pins 9,10, 11, 12, 13 and 14 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs (when all macrocells that require internal RC OSC or bandgap are inactive)	--	0.25	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.901	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.254	--	V_{DD}	V
		Low-Level Logic Input	1.209	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.840	V
		Logic Input with Schmitt Trigger	0	--	1.510	V
		Low-Level Logic Input	0	--	0.780	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.443	0.618	0.792	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.70	3.30	nA
		Vin = VDD	--	0.38	1.84	nA
	PGA Input Leakage	Vin = 0 V	--	0.25	1.05	nA
		Vin = VDD	--	0.17	0.91	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.29	1.40	nA
		Vin = VDD	--	1.46	64.99	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.29	1.40	nA
		Vin = VDD	--	1.45	65.16	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.29	1.40	nA
		Vin = VDD	--	1.45	66.16	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 5 mA	4.168	4.759	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.330	4.878	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 5 mA	4.405	4.932	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.193	0.330	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.101	0.160	V
		Push-Pull 4X, I_{OL}= 5 mA	--	0.071	0.135	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.090	0.160	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.050	0.080	V
		Open Drain NMOS 4X, I_{OL}= 5 mA	--	0.021	0.030	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	20.716	30.759	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	40.059	59.691	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	76.137	112.724	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	6.010	9.730	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	12.020	19.460	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	26.150	37.191	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	12.030	19.460	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	24.060	38.920	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	60.071	86.737	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				VDD	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.462	0.848	2.693	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.963	1.314	1.659	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.877	1.109	1.288	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	884.96	1074.96	1306.99	kΩ
		100 k Pull Up	91.90	110.17	131.96	kΩ
		10 k Pull Up	8.98	11.64	14.55	kΩ

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
R_{PDWN}	Pull Down Resistance	1 M Pull Down	667.10	1074.89	1287.81	kΩ
		100 k Pull Down	92.03	110.34	132.21	kΩ
		10 k Pull Down	9.45	11.55	14.05	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6 and 7 are connected to one side, pins 9,10, 11, 12, 13 and 14 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.5 Typical Delay Estimated for Each Macrocell

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	LUT 2-bit	17.43	15.33	6.31	6.09	4.20	4.31	ns
tpd	Delay	LUT 2-bit (Shared with DFF/Latch)	21.53	20.67	8.13	8.33	5.45	6.01	ns
tpd	Delay	LUT 3-bit	18.49	15.69	6.74	6.31	4.49	4.52	ns
tpd	Delay	LUT 3-bit (Shared with DFF/Latch)	23.04	21.51	8.74	8.75	5.86	6.37	ns
tpd	Delay	LUT 3-bit (Shared with Pipe Delay)	25.65	24.01	9.37	9.47	6.67	7.32	ns
tpd	Delay	LUT 3-bit (Shared with CNT/DLY)	23.17	20.67	8.62	8.32	5.73	6.05	ns
tpd	Delay	LUT 4-bit (Shared with PGEN)	21.13	22.27	9.07	8.97	6.04	6.46	ns
tpd	Delay	LUT 4-bit (Shared with CNT/DLY)	25.42	22.29	9.54	9.02	6.41	6.59	ns
tpd	Delay	DFF (Shared with 2-bit LUT)	27.25	28.68	10.67	10.78	7.30	7.51	ns
tpd	Delay	DFF (Shared with 3-bit LUT)	27.87	28.96	10.87	10.93	7.44	7.61	ns
tpd	Delay	DFF (Shared with 3-bit LUT) nReset	--	29.84	--	12.41	--	8.95	ns
tpd	Delay	DFF (Shared with 3-bit LUT) nSet	--	36.73	--	14.00	--	9.42	ns
tpd	Delay	DFF	23.01	23.77	8.91	8.73	5.95	6.15	ns
tpd	Delay	DFF nReset	--	23.64	--	9.71	--	7.11	ns
tpd	Delay	DFF nSet	--	31.5	--	11.4	--	7.68	ns
tpd	Delay	CNT/DLY opposite to selected edge delay	46.61	36.87	18.56	15.62	12.53	11.23	ns
tpd	Delay	CNT/DLY (Shared) opposite to selected edge delay	47.30	37.16	18.78	15.78	12.68	11.77	ns
tpd	Delay	CNT/DLY Both edge detect	49.5	52.9	20.07	20.84	13.81	14.32	ns
tpd	Delay	CNT/DLY Rising edge detect	52.39	--	21.32	--	14.67	--	ns
tpd	Delay	CNT/DLY Falling edge detect	--	55.94	--	22.15	--	15.27	ns
tw	Width	CNT/DLY Both edge detect	25.17	24.93	11.98	12.01	8.76	8.83	ns
tw	Width	CNT/DLY Rising edge detect	25.76	--	12.14	--	8.86	--	ns
tw	Width	CNT/DLY Falling edge detect	--	24.51	--	11.79	--	8.57	ns
tpd	Delay	Latch (Shared with 2-bit LUT)	26.25	25.43	10.2	10.43	6.99	7.58	ns
tpd	Delay	Latch (Shared with 3-bit LUT)	26.93	25.72	10.42	10.6	7.11	7.72	ns
tpd	Delay	Latch (Shared with 3-bit LUT) nReset	--	31.8	--	13.17	--	9.61	ns
tpd	Delay	Latch (Shared with 3-bit LUT) nSet	--	34.23	--	12.97	--	8.76	ns
tpd	Delay	Latch	21.28	19.87	8.17	8.13	5.51	5.92	ns
tpd	Delay	Latch nReset	--	25.45	--	10.52	--	7.74	ns
tpd	Delay	Latch nSet	--	28.36	--	10.37	--	6.76	ns
tpd	Delay	Pipe Delay (Shared)	33.44	34.93	13.39	13.21	9.40	9.17	ns
tpd	Delay	Pipe Delay (Shared) nReset	--	35.42	--	15.07	--	11.24	ns
tpd	Delay	PGEN (Shared)	22.44	23.52	8.69	9.00	5.77	6.01	ns
tpd	Delay	PGEN (Shared) nReset to 0	--	21.73	--	8.88	--	6.60	ns
tpd	Delay	PGEN (Shared) nReset to 1	22.81	--	9.75	--	6.99	--	ns
tpd	Delay	PDLY 1Cells Both edge detect	30.71	35.23	12.00	13.45	8.42	9.26	ns
tpd	Delay	PDLY 1Cells delayed output Both edge detect	191.41	195.73	75.44	76.67	48.41	49.32	ns

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	PDLY 1Cells delayed output Rising edge detect	192.15	--	75.71	--	48.65	--	ns
tpd	Delay	PDLY 1Cells delayed output Falling edge detect	--	195.73	--	76.60	--	49.42	ns
tpd	Delay	PDLY 1Cells Rising edge detect	31.32	--	12.33	--	8.65	--	ns
tpd	Delay	PDLY 1Cells Falling edge detect	--	35.52	--	13.63	--	9.36	ns
tpd	Delay	PDLY 2Cells Both edge detect	30.68	35.23	12.04	13.47	8.44	9.25	ns
tpd	Delay	PDLY 2Cells delayed output Both edge detect	358.75	362.80	139.97	141.13	88.68	89.64	ns
tpd	Delay	PDLY 2Cells delayed output Rising edge detect	359.61	--	140.37	--	88.92	--	ns
tpd	Delay	PDLY 2Cells delayed output Falling edge detect	--	362.93	--	141.33	--	89.66	ns
tpd	Delay	PDLY 2Cells Rising edge detect	31.35	--	12.33	--	8.65	--	ns
tpd	Delay	PDLY 2Cells Falling edge detect	--	35.49	--	13.60	--	9.37	ns
tpd	Delay	PDLY 3Cells Both edge detect	30.65	35.25	12.04	13.51	8.43	9.26	ns
tpd	Delay	PDLY 3Cells delayed output Both edge detect	517.41	521.47	202.97	204.20	128.17	129.08	ns
tpd	Delay	PDLY 3Cells delayed output Rising edge detect	518.35	--	203.44	--	128.36	--	ns
tpd	Delay	PDLY 3Cells delayed output Falling edge detect	--	522.00	--	204.27	--	129.16	ns
tpd	Delay	PDLY 3Cells Rising edge detect	31.35	--	12.33	--	8.68	--	ns
tpd	Delay	PDLY 3Cells Falling edge detect	--	35.60	--	13.65	--	9.37	ns
tpd	Delay	PDLY 4Cells Both edge detect	30.76	35.23	12.03	13.53	8.42	9.25	ns
tpd	Delay	PDLY 4Cells delayed output Both edge detect	684.15	688.20	267.31	268.47	168.33	169.41	ns
tpd	Delay	PDLY 4Cells delayed output Rising edge detect	685.08	--	267.57	--	168.46	--	ns
tpd	Delay	PDLY 4Cells delayed output Falling edge detect	--	688.67	--	268.47	--	169.54	ns
tpd	Delay	PDLY 4Cells Rising edge detect	31.37	--	12.35	--	8.66	--	ns
tpd	Delay	PDLY 4Cells Falling edge detect	--	35.73	--	13.63	--	9.35	ns
tpd	Delay	PDLY Both edge delay Delayed output 1CELLs Rising	382.08	382.60	166.57	167.53	121.00	122.74	ns
tpd	Delay	PDLY Both edge delay Delayed output 2CELLs Rising	730.35	730.80	319.84	321.13	232.80	234.41	ns
tpd	Delay	PDLY Both edge delay Delayed output 3CELLs Rising	1074.28	1075.93	471.71	473.47	343.46	345.28	ns
tpd	Delay	PDLY Both edge delay Delayed output 4CELLs Rising	1421.41	1422.60	624.77	626.47	455.13	456.94	ns
tw	Width	PDLY 1Cells Both edge detect	344.67	346.13	153.20	153.73	111.89	112.43	ns
tw	Width	PDLY 1Cells delayed output Both edge detect	348.67	350.20	152.07	152.73	110.93	111.13	ns
tw	Width	PDLY 1Cells delayed output Rising edge detect	348.80	--	152.20	--	110.80	--	ns
tw	Width	PDLY 1Cells delayed output Falling edge detect	--	349.93	--	152.87	--	111.39	ns

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tw	Width	PDLY 1Cells Rising edge detect	344.67	--	153.27	--	111.95	--	ns
tw	Width	PDLY 1Cells Falling edge detect	--	345.80	--	153.73	--	112.43	ns
tw	Width	PDLY 2Cells Both edge detect	692.87	694.27	306.80	307.33	223.53	224.33	ns
tw	Width	PDLY 2Cells delayed output Both edge detect	687.40	688.73	301.60	302.27	220.20	220.80	ns
tw	Width	PDLY 2Cells delayed output Rising edge detect	687.33	--	301.93	--	219.93	--	ns
tw	Width	PDLY 2Cells delayed output Falling edge detect	--	688.60	--	302.47	--	220.47	ns
tw	Width	PDLY 2Cells Rising edge detect	693.00	--	306.87	--	223.87	--	ns
tw	Width	PDLY 2Cells Falling edge detect	--	693.73	--	307.33	--	224.13	ns
tw	Width	PDLY 3Cells Both edge detect	1036.87	1039.20	458.53	459.93	334.20	335.27	ns
tw	Width	PDLY 3Cells delayed output Both edge detect	1034.47	1036.87	452.07	453.20	329.47	330.27	ns
tw	Width	PDLY 3Cells delayed output Rising edge detect	1034.33	--	452.27	--	329.20	--	ns
tw	Width	PDLY 3Cells delayed output Falling edge detect	--	1036.80	--	453.27	--	330.00	ns
tw	Width	PDLY 3Cells Rising edge detect	1036.73	--	458.73	--	334.47	--	ns
tw	Width	PDLY 3Cells Falling edge detect	--	1038.73	--	459.73	--	335.13	ns
tw	Width	PDLY 4Cells Both edge detect	1383.47	1385.73	611.73	612.67	445.93	446.80	ns
tw	Width	PDLY 4Cells delayed output Both edge detect	1371.27	1373.67	600.93	602.07	439.00	439.93	ns
tw	Width	PDLY 4Cells delayed output Rising edge detect	1371.47	--	601.13	--	438.73	--	ns
tw	Width	PDLY 4Cells delayed output Falling edge detect	--	1373.80	--	602.20	--	439.73	ns
tw	Width	PDLY 4Cells Rising edge detect	1383.40	--	611.67	--	446.07	--	ns
tw	Width	PDLY 4Cells Falling edge detect	--	1385.13	--	612.60	--	446.53	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS	--	34.18	--	13.60	--	9.47	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS 2x	--	31.88	--	12.85	--	8.97	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS 4x	--	31.80	--	12.51	--	8.80	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS	41.12	--	15.24	--	10.58	--	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS 2x	40.29	--	14.93	--	10.38	--	ns
tpd	Delay	Digital Input with Schmitt Trigger -- Push Pull	41.10	35.59	15.64	15.03	10.89	10.69	ns
tpd	Delay	Low Voltage Digital Input -- Push Pull	41.67	476.4	15.39	--	10.49	120.93	ns
tpd	Delay	Digital Input without Schmitt trigger -- 3-state	40.28	34.33	15.11	14.38	10.46	10.23	ns
tpd	Delay	Digital Input without Schmitt trigger -- 3-state 2x	38.65	33.95	14.50	13.95	10.11	9.94	ns

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input without Schmitt trigger -- 3-state 4x	37.83	33.03	14.14	13.54	9.93	9.67	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull Z to 1	42.03	--	15.61	--	10.78	--	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull Z to 0	--	36.09	--	13.83	--	9.51	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 1x	40.92	35.45	15.32	14.79	10.60	10.52	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 2x	39.61	34.98	14.8	14.37	10.31	10.17	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 4x	37.84	33.40	14.11	13.80	9.93	9.92	ns

5.6 Typical Current Consumption

Table 2. Typical Current Consumption

Note	VDD = 1.8V	VDD = 3.3V	VDD = 5.0V	Unit
Quiescent current	0.08	0.16	0.25	uA
Low frequency OSC; Clock predivider by 1	0.37	0.48	0.67	uA
Low frequency OSC; Clock predivider by 16	0.36	0.46	0.64	uA
RC OSC 25kHz; First Clock predivider by 1	4.85	5.24	6.07	uA
RC OSC 25kHz; First Clock predivider by 8	4.77	5.08	5.81	uA
RC OSC 2MHz; First Clock predivider by 1	23.94	35.78	51.44	uA
RC OSC 2MHz; First Clock predivider by 8	16.70	21.17	27.94	uA
Ring OSC; First Clock predivider by 1	70.80	83.81	116.94	uA
Ring OSC; First Clock predivider by 16	57.82	57.31	71.86	uA
ACMP; Hysteresis 0mv/25mV; Low bandwidth Disable; Input PIN10; Gain 0.25x - 1x	47.49	39.65	43.72	uA
ACMP; Hysteresis 0mV/25mV; Low bandwidth Enable; Input PIN10; Gain 1x	42.50	34.64	38.71	uA
Bandgap	37.06	29.18	33.26	uA
VREF	79.08	71.38	75.46	uA
PGA; Single-end mode; Gain 0.25x;	97.58	119.37	132.18	uA
PGA; Single-end mode; Gain 0.5x;	103.04	119.59	131.32	uA
PGA; Single-end mode; Gain 1x	69.44	73.44	77.36	uA
PGA; Single-end mode; Gain 2x	116.42	91.50	111.10	uA
PGA; Single-end mode; Gain 4x	117.87	97.20	114.72	uA
DAC0; Power on	48.24	40.40	44.47	uA
DAC1; DCMP1 Input	62.83	55.04	59.11	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25 kHz; First Clock predivider by 1; Sample rate 1.56 kHz	172.24	166.10	171.01	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25 kHz; First Clock predivider by 16; Sample rate 97.66 Hz	172.58	166.00	170.76	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2 MHz; First Clock predivider by 16; Sample rate 7.81 kHz	190.91	196.84	216.93	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2 MHz; First Clock predivider by 1; Sample rate 125.00 kHz	195.71	208.71	255.56	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 16; Sample rate 106.45 kHz	224.60	297.64	380.98	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 1; Sample rate 1.70 MHz	260.15	342.27	697.94	uA

5.7 OSC Specifications

5.7.1 25 kHz RC Oscillator

Table 3. 25 kHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	24.599	25.444	23.979	25.859	23.571	26.960
3.3 V ±10%	24.894	25.101	23.973	25.664	23.813	26.605
5 V ±10%	24.739	25.428	23.976	25.714	23.689	26.550
2.5 V - 4.5 V	24.842	25.147	23.937	25.691	23.803	26.642
1.71 V….5.5 V	24.380	25.701	23.891	25.989	23.429	27.036

Table 4. 25 kHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-1.60%	1.78%	-4.08%	3.43%	-5.72%	7.84%
3.3 V ±10%	-0.43%	0.41%	-4.11%	2.66%	-4.75	6.42%
5 V ±10%	-1.04%	1.71%	-4.10%	2.85%	-5.25%	6.20%
2.5 V - 4.5 V	-0.63%	0.59%	-4.25%	2.76%	-4.79%	6.57%
1.71 V….5.5 V	-2.48%	2.80%	-4.44%	3.95%	-6.29%	8.14%

5.7.2 2 MHz RC Oscillator

Table 5. 2 MHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.953	2.028	1.894	2.060	1.866	2.121
3.3 V ±10%	1.972	2.031	1.928	2.075	1.832	2.095
5 V ±10%	1.944	2.173	1.905	2.200	1.802	2.200
2.5 V - 4.5 V	1.924	2.069	1.884	2.106	1.783	2.106
1.71 V….5.5 V	1.832	2.180	1.782	2.191	1.782	2.209

Table 6. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-2.36%	1.38%	-5.29%	3.02%	-6.69%	6.04%
3.3 V ±10%	-1.40%	1.57%	-3.59%	3.76%	-8.38%	4.76%
5 V ±10%	-2.82%	8.64%	-4.77%	10.00%	-9.88%	10.00%
2.5 V - 4.5 V	-3.82%	3.46%	-5.80%	5.30%	-10.86%	5.30%
1.71 V….5.5 V	-8.43%	9.02%	-10.89%	9.56%	-10.89%	10.45%

5.7.3 25 MHz Ring Oscillator

Table 7. 25 MHz Ring OSC Frequency Limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	22.482	28.084	21.855	28.084	21.855	28.084
3.3 V ±10%	23.647	28.092	23.330	28.092	22.561	28.092
5 V ±10%	23.312	28.167	22.992	28.176	22.224	28.176
2.5 V - 4.5 V	23.617	28.095	23.299	28.095	22.528	28.095
1.71 V….5.5 V	22.482	28.167	21.855	28.176	21.855	28.176

Table 8. 25 MHz Ring OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-11.83%	10.13%	-14.30%	10.13%	-14.30%	10.13%
3.3 V ±10%	-7.27%	10.16%	-8.51%	10.16%	-11.52%	10.16%
5 V ±10%	-8.58%	10.46%	-9.84%	10.49%	-12.85%	10.49%
2.5 V - 4.5 V	-7.38%	10.18%	-8.63%	10.18%	-11.66%	10.18%
1.71 V….5.5 V	-11.83%	10.46%	-14.30%	10.49%	-14.30%	10.49%

5.7.4 1.9 kHz LF Oscillator

Table 9. 1.9 kHz LF OSC Frequency Limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	1.619	2.264	1.606	2.273	1.537	2.289
3.3 V ±10%	1.604	2.251	1.592	2.260	1.525	2.272
5 V ±10%	1.602	2.277	1.590	2.285	1.525	2.291
2.5 V - 4.5 V	1.601	2.258	1.588	2.266	1.522	2.281
1.71 V….5.5 V	1.601	2.277	1.588	2.285	1.522	2.291

Table 10. 1.9 kHz LF OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-14.80%	19.18%	-15.48%	19.64%	-19.13	20.46%
3.3 V ±10%	-15.58%	18.46%	-16.23%	18.91%	-19.74%	19.56%
5 V ±10%	-15.69%	19.84%	-16.33%	20.27%	-19.75%	20.57%
2.5 V - 4.5 V	-15.74%	18.82%	-16.43%	19.25%	-19.88%	20.03%
1.71 V….5.5 V	-15.74%	19.84%	-16.43%	20.27%	-19.88%	20.57%

5.7.5 OSC Power On Delay

Table 11. Oscillators Power On Delay at Room Temperature, RC OSC Power Setting: "Auto Power On", RC OSC Clock to Matrix Input: "Enable"

Power Supply Range (VDD) V	LF OSC		RC OSC 2 MHz		RC OSC 25 kHz		RING OSC	
	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, µs
1.71	496.70	691.9	717.73	1290.3	40.72	41.79	126	69.8
1.80	494.51	690.6	697.27	1172.2	40.77	41.87	109	62.6
1.89	492.70	687.3	680.73	1080.7	40.77	41.75	102	51.1
2.50	482.97	681.5	621.87	1228.4	40.94	41.84	77	19.1
2.70	480.31	680.1	613.00	989.0	41.01	42.04	72	17.2
3.00	476.72	677.1	604.33	924.5	41.15	42.13	70	15.3
3.30	473.21	675.9	598.27	878.4	41.28	42.36	66	8.4
3.60	469.91	674.1	594.67	845.8	41.38	42.30	65	7.0
4.20	463.03	665.7	589.20	803.0	41.62	42.92	61	5.4
4.50	459.00	661.3	586.67	790.2	41.72	42.90	60	5.7
5.00	451.72	641.8	579.60	773.9	41.66	42.78	57	4.5
5.50	442.70	609.03	564.07	1165.3	41.30	42.46	56	3.8

5.8 ACMP Specifications

Table 12. ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input	VDD = 1.8 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	1.1	V
		Positive Input	VDD = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	VDD = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-10.2	--	9.0	mV
			T = (-40..85)°C	-15.3	--	13.4	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-6.8	--	6.3	mV
			T = (-40..85)°C	-7.2	--	6.6	mV
t_{start}	ACMP Start Time	ACMP Power On delay, Minimal required wake time for the “Wake and Sleep function”, Regulator and Charge Pump set to automatic ON/OFF	BG = 550 µs, T = 25°C VDD = (1.71..5.5) V	--	406.7	1735.7	µS
			BG = 550 µs, T = (-40..85)°C VDD = (1.71..5.5) V	--	468.3	4411.9	µS
			BG = 100 µs, T = 25°C VDD = 2.7..5.5 V	--	157.3	507.5	µS
			BG = 100 µs, T = (-40..85)°C VDD = 2.7..5.5 V	--	171.2	1402.1	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = 25°C	2.7	--	28.6	mV
			LB - Disabled, T = 25°C	13.8	--	33.2	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25°C	43.5	--	58.5	mV
			LB - Disabled, T = 25°C	44.8	--	54.1	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25°C	192.8	--	210.5	mV
			LB - Disabled, T = 25°C	192.6	--	205.8	mV
		V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = (-40…+85)°C	2.7	--	28.6	mV
			LB - Disabled, T = (-40…+85)°C	7.4	--	44.4	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = (-40…+85)°C	35.1	--	72.4	mV
			LB - Disabled, T = (-40…+85)°C	43.8	--	55.6	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = (-40…+85)°C	184.8	--	224.2	mV
			LB - Disabled, T = (-40…+85)°C	189.7	--	207.9	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
PROP	Propagation Delay, Response Time	Low Bandwidth - Enable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	124.90	776.40	µS
			High to Low, T = (-40…+85)°C	--	136.80	862.10	µS
		Low Bandwidth - Disable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	3.70	5.10	µS
			High to Low, T = (-40…+85)°C	--	3.00	6.30	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
G	Gain error (including threshold and internal Vref error), T = (-40…+85)°C	G = 1, VDD = 1.71 V	Vref = 50…1200 mV	--	1	--	
		G = 1, VDD = 3.3 V	Vref = 50…1200 mV	--	1	--	
		G = 1, VDD = 5.5 V	Vref = 50…1200 mV	--	1	--	
		G = 0.5, VDD = 1.71 V	Vref = 50…1200 mV	-1.09%	--	0.55%	
		G = 0.5, VDD = 3.3 V	Vref = 50…1200 mV	-0.83%	--	0.73%	
		G = 0.5, VDD = 5.5 V	Vref = 50…1200 mV	-0.70%	--	0.79%	
		G = 0.33, VDD = 1.71V	Vref = 50…1200 mV	-0.58%	--	0.95%	
		G = 0.33, VDD = 3.3 V	Vref = 50…1200 mV	-0.70%	--	0.82%	
		G = 0.33, VDD = 5.5 V	Vref = 50…1200 mV	-0.54%	--	0.88%	
		G = 0.25, VDD = 1.71V	Vref = 50…1200 mV	-0.49%	--	1.21%	
		G = 0.25, VDD = 3.3 V	Vref = 50…1200 mV	-0.65%	--	1.00%	
		G = 0.25, VDD = 5.5 V	Vref = 50…1200 mV	-0.41%	--	1.18%	
Vref	Internal Vref error, Vref = 1200 mV	VDD = 1.8 V ± 5 %	T = 25°C	-0.96%	--	0.95%	
			T = (-40…+85)°C	-1.30%	--	1.12%	
		VDD = 3.3 V ± 10 %	T = 25°C	-1.02%	--	1.03%	
			T = (-40…+85)°C	-1.34%	--	1.14%	
		VDD = 5.0 V ± 10 %	T = 25°C	-1.20%	--	1.15%	
			T = (-40…+85)°C	-1.58%	--	1.48%	

5.9 ADC Specifications (Including PGA)

Table 13. Single-Ended ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
V_{inp}	Input Voltage Range (bit 0 to bit 255), relative to GND	G = 0.25	VDD = 5V ±10%	120	4120	mV
		G = 0.5	VDD = 2.5 to 5.5 V	60	2060	mV
		G = 1		30	1030	mV
		G = 2		20	520	mV
		G = 4		15	265	mV
		G = 8		12	137	mV
ZE	Offset Zero Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±1.7	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±2.6	LSB
		G = 1	T = 25°C	--	±3	LSB
		G = 2		--	±2.6	LSB
		G = 4		--	±3.3	LSB
		G = 8		--	±4.6	LSB
dZE/dT	Offset Zero Error Temperature Drift	G = 0.25	VDD = 5V ±10%	--	±0.008	%/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.009	%/°C
		G = 1		--	±0.01	%/°C
		G = 2		--	±0.014	%/°C
		G = 4		--	±0.025	%/°C
		G = 8		--	±0.048	%/°C
GE	Gain Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±1.5	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±1.3	LSB
		G = 1	T = 25°C	--	±1.5	LSB
		G = 2		--	±1.7	LSB
		G = 4		--	±1.3	LSB
		G = 8		--	±1.2	LSB
dGE/dT	Gain Error Temperature Coefficient	G = 0.25	VDD = 5V ±10%	--	±0.007	%/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.008	%/°C
		G = 1		--	±0.007	%/°C
		G = 2		--	±0.009	%/°C
		G = 4		--	±0.008	%/°C
		G = 8		--	±0.008	%/°C

Table 13. Single-Ended ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
INL	Integral Non-Linearity Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±2.1	LSB
			VDD = 5V ±10%	--	±3.2	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±1.9	LSB
			VDD = 2.5 to 5.5 V	--	±3.4	LSB
		G = 1	T = 25°C	--	±1.7	LSB
				--	±3.2	LSB
		G = 2	T = 25°C	--	±1.8	LSB
				--	±2.9	LSB
		G = 4	T = 25°C	--	±1.8	LSB
				--	±2.7	LSB
		G = 8	T = 25°C	--	±1.6	LSB
				--	±2.6	LSB
DNL	Differential Non-Linearity	G = 0.25, 0.5, 1, 2, 4, 8		--	±0.5	LSB
NOISE				--	±0.5	LSB

Note: To ensure linear operation, absolute input voltage on each pin should not exceed VDD-0.5.

Table 14. Differential ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
V_{ind}	Input Voltage Range (bit 0 to bit 255), Differential	G = 1		-500	500	mV
		G = 2		-250	250	mV
		G = 4		-125	125	mV
		G = 8		-62.5	62.5	mV
		G = 16		-31.25	31.25	mV
V_{cm}	Input Common Voltage (see Note 1)	G = 1, 2, 4, 8, 16	VDD = 1.8 V ±5%	400	550	mV
			VDD = 3.3 V ±10%	400	950	mV
			VDD = 5 V ±10%	400	950	mV
ZE	Offset Zero Error	G = 1	T = 25°C	--	±2.5	LSB
		G = 2		--	±2.7	LSB
		G = 4		--	±3.3	LSB
		G = 8		--	±4.6	LSB
		G = 16		--	±6.8	LSB
dZE/dT	Offset Zero Error Temperature Drift	G = 1		--	±0.014	%/°C
		G = 2		--	±0.015	%/°C
		G = 4		--	±0.02	%/°C
		G = 8		--	±0.032	%/°C
		G = 16		--	±0.1	%/°C
GE	Gain Error	G = 1	T = 25°C	--	±0.8	LSB
		G = 2		--	±0.8	LSB
		G = 4		--	±0.5	LSB
		G = 8		--	±1	LSB
		G = 16		--	±1	LSB
dGE/dT	Gain Error Temperature Drift	G = 1		--	±0.007	%/°C
		G = 2		--	±0.007	%/°C
		G = 4		--	±0.006	%/°C
		G = 8		--	±0.006	%/°C
		G = 16		--	±0.005	%/°C
INL	Integral Non-Linearity Error	G = 1	T = 25°C	--	±1.6	LSB
				--	±3.2	LSB
		G = 2	T = 25°C	--	±1.3	LSB
				--	±3	LSB
		G = 4	T = 25°C	--	±1.2	LSB
				--	±3.1	LSB
		G = 8	T = 25°C	--	±1.3	LSB
				--	±3.4	LSB
		G = 16	T = 25°C	--	±1.6	LSB
				--	±3.2	LSB

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
DNL	Differential Non-Linearity	G = 1, 2, 4, 8, 16		--	±0.5	LSB
NOISE				--	±0.5	LSB

Note 1: V_{cm} range is given for stable CMRR > 34 dB.

Note 2: To ensure linear operation, absolute input voltage on each pin should not exceed VDD-0.5.

Table 15. Pseudo-Differential ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
V_{ind}	Input Voltage Range (bit 0 to bit 255), Differential	G = 1		0	980	mV
		G = 2		0	490	mV
		G = 4		0	245	mV
V_{inn}	Negative input voltage range	G = 1, 2, 4	VDD = 1.8 V ±5%	500	500	mV
			VDD = 3.3 V ±10%	500	1250	mV
			VDD = 5 V ±10%	500	1250	mV
ZE	Offset Zero Error	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±2.6	LSB
		G = 2	T = 25°C	--	±2.7	LSB
		G = 4		--	±3.3	LSB
dZE/dT	Offset Zero Error Temperature Drift	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±0.012	%/°C
		G = 2	T = 25°C	--	±0.013	%/°C
		G = 4		--	±0.018	%/°C
GE	Gain Error	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±1.9	LSB
		G = 2	T = 25°C	--	±2.4	LSB
		G = 4		--	±1.4	LSB
dGE/dT	Gain Error Temperature Drift	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±0.009	%/°C
		G = 2	T = 25°C	--	±0.013	%/°C
		G = 4		--	±0.007	%/°C
INL	Integral Non-Linearity Error	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±1.4	LSB
			VDD = 2.0 to 5.5 V	--	±2	LSB
		G = 2	T = 25°C	--	±1.7	LSB
				--	±2.4	LSB
		G = 4	T = 25°C	--	±1.8	LSB
				--	±2.1	LSB
DNL	Differential Non-Linearity	G = 1, 2, 4		--	±0.5	LSB
NOISE				--	±0.5	LSB

Note 1: V_{inn} is given for convenience instead of V_{cm}.

Note 2: V_{inn} range is given for stable CMRR > 34 dB.

Note 3: To ensure linear operation, absolute input voltage on each pin should not exceed VDD-0.5.

5.10 PGA Specifications

Table 16. Single-Ended PGA Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTI, see Note 1)	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±8.5	±50.3	mV
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±5.3	±28.3	mV
		G = 1	T = 25°C	--	±2.2	±12.1	mV
		G = 2	T = 25°C	--	±3.4	±13.7	mV
		G = 4	T = 25°C	--	±3.2	±12.0	mV
		G = 8	T = 25°C	--	±3.2	±11.6	mV
dV_{os}/dT	V_{os} (RTI) Temperature Drift	G = 0.25	VDD = 5V ±10%	--	±0.0097	±0.0584	mV/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.0058	±0.0345	mV/°C
		G = 1		--	±0.0018	±0.0111	mV/°C
		G = 2		--	±0.0031	±0.0186	mV/°C
		G = 4		--	±0.0028	±0.0167	mV/°C
		G = 8		--	±0.0026	±0.0158	mV/°C
ΔG	Gain Error	G = 0.25	VDD = 5V ±10%	-0.822	0.562	1.945	%
		G = 0.5	VDD = 2.5 to 5.5 V	-0.877	0.196	1.260	%
		G = 1		-0.118	-0.012	0.093	%
		G = 2		-1.361	-0.213	0.935	%
		G = 4		-2.169	-0.554	1.060	%
		G = 8		-3.616	-1.299	1.018	%
V_{ind}(lin)	Linear Differential Input Voltage Range	G = 0.25	VDD = 5V ±10%	273	--	4167	mV
		G = 0.5	VDD = 2.5 to 5.5 V	126	--	2153	mV
		G = 1		59	--	1145	mV
		G = 2		39	--	572	mV
		G = 4		23	--	286	mV
		G = 8		15	--	144	mV
V_{sw}	Output Voltage Swing			--	GND to 1380	--	mV

Note 1: RTI - referred to input.

Table 17. Differential PGA Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTO, see Note 1)	All gains	V_{id} = 0	--	550	--	mV
ΔV_{os}	Offset Voltage Error (RTO)	G = 1	T = 25°C	--	±1.4	±5.4	mV
		G = 2	T = 25°C	--	±1.1	±4.5	mV
		G = 4	T = 25°C	--	±1.1	±6.5	mV
		G = 8	T = 25°C	--	±2.2	±10.1	mV
		G = 16	T = 25°C	--	±4.0	±20.4	mV
dV_{os}/dT	V_{os} (RTO) Temperature Drift	G = 1		--	±0.0124	±0.0551	mV/°C
		G = 2		--	±0.0118	±0.0658	mV/°C
		G = 4		--	±0.0148	±0.0884	mV/°C
		G = 8		--	±0.0240	±0.1416	mV/°C
		G = 16		--	±0.0432	±0.256	mV/°C
ΔG	Gain Error	G = 1		-1.080	-0.194	0.664	%
		G = 2		-1.761	-0.568	0.629	%
		G = 4		-2.573	-0.929	0.656	%
		G = 8		-3.553	-1.620	0.225	%
		G = 16		-3.720	-1.808	0.106	%
V_{ind} (lin)	Linear Differential Input Voltage Range	G = 1		-452	--	578	mV
		G = 2		-229	--	289	mV
		G = 4		-115	--	145	mV
		G = 8		-57	--	72	mV
		G = 16		-29	--	32	mV
CMRR	Common-Mode Rejection Rate	G = 1		32	--	--	dB
		G = 2		38	--	--	dB
		G = 4		44	--	--	dB
		G = 8		50	--	--	dB
		G = 16		56	--	--	dB
ICMR	Input Common Mode Range	All gains	VDD = 1.8 V, Vind=(-500 to 500) mV/G	400	--	550	mV
			VDD = 3.3 V, Vind=(-500 to 500) mV/G	400	--	900	mV
			VDD = 5.0 V, Vind=(-500 to 500) mV/G	450	--	900	mV
V_{sw}	Output Voltage Swing			--	GND to 1380	--	mV

Note 1: RTO - referred to output.

Table 18. Pseudo-Differential PGA operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vinn = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTO, see Note 1)	All gains	V_{id} = 0	--	180	--	mV
ΔV_{os}	Offset Voltage Error (RTO)	G = 1	T = 25°C, VDD = 2.0 V to 5.5 V	--	±1.2	±3.6	mV
		G = 2	T = 25°C	--	±1.5	±5.5	mV
		G = 4	T = 25°C	--	±2.1	±6.4	mV
dV_{os}/dT	V_{os} (RTO) Temperature Drift	G = 1		--	±0.0088	±0.0493	mV/°C
		G = 2		--	±0.0098	±0.0588	mV/°C
		G = 4		--	±0.0128	±0.0772	mV/°C
ΔG	Gain Error	G = 1		-0.916	-0.455	0.549	%
		G = 2		-1.855	-0.567	0.685	%
		G = 4		-2.559	-0.918	0.735	%
V_{ind} (lin)	Linear Differential Input Voltage Range	G = 1		0	--	834	mV
		G = 2		0	--	394	mV
		G = 4		0	--	239	mV
CMRR	Common-Mode Rejection Rate	G = 1		32	--	--	dB
		G = 2		38	--	--	dB
		G = 4		44	--	--	dB
V_{inn}	Negative Input Voltage Range	All gains	VDD = 1.8 V, Vind=(0 to 1000) mV/G	500	--	500	mV
			VDD = 3.3 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
			VDD = 5.0 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
V_{sw}	Output Voltage Swing			--	180 to 1380	--	mV

Note 1: RTO - referred to output.

Table 19. Differential or Pseudo-Differential PGA Operation, ADC - Power Down, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTI, see Note 1)	All gains	T = 25°C, VDD = 3.3 V	--	±1.9	±11.2	mV
ΔG	Gain Error	G = 1		-1.080	-0.194	0.664	%
		G = 2		-1.761	-0.568	0.629	
		G = 4		-2.573	-0.929	0.656	
		G = 8		-3.553	-1.620	0.225	%
		G = 16		-3.720	-1.808	0.106	%
CMRR	Common-Mode Rejection Rate	G = 1		32	--	--	dB
		G = 2		38	--	--	dB
		G = 4		44	--	--	dB
		G = 8		50	--	--	dB
		G = 16		56	--	--	dB
V_{inn}	Negative Input Voltage Range	All gains	VDD = 1.8 V, Vind=(0 to 1000) mV/G	500	--	500	mV
			VDD = 3.3 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
			VDD = 5.0 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
V_{sw}	Output Voltage Swing			--	GND to 1380	--	mV

Note 1: RTI - referred to input.

Note 2: When ADC is powered down, PGA operation in Differential or Pseudo-Differential mode is not recommended. Parameters in Table 19. are for reference only.

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs (x1, x2, x4)
- Push Pull Outputs (x1, x2, x4)
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- 40 mA Open Drain 4X Drive output, Pin 9 and Pin 10 (depending on VDD)
- Pins 3, 5, 7, 9, 10, 13, 14, 16, 18, 19 can be configured as bidirectional IO

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog-to-Digital Converter

- 8-bit, 100 kHz, Successive Approximation Register ADC
- DNL < ± 0.5 LSB, INL < ± 3.4 LSB
- VIN Range: (0..1)/G V
- 3-bit Programmable Gain Amplifier with gain values of (1, 2, 4, 8,16X in differential mode, 1, 2, 4X in Pseudo-Differential mode and 0.25, 0.5, 1, 2, 4, 8x in single-ended mode)
- SPI output format

6.4 Digital-to-Analog Converter

- Two 8-bit Digital-to-Analog Converters 0 to 1 V

6.5 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV
- Internal or external Vref
- Selectable gain (1x, 0.5x, 0.33x, 0.25x)
- Low bandwidth

6.6 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins
- 50 mV to 1.2 V, with 50 mV resolution
- Chopper stabilized output amplifier

6.7 Combinational Logic Look Up Tables (LUTs – 8 total)

- Four 2-bit Lookup Tables
- Four 3-bit Lookup Tables

6.8 Combination Function Macrocells (8 total)

- Two Selectable DFF/Latch or 2-bit LUTs
- Two Selectable DFF/Latch or 3-bit LUTs
- One Selectable 16-Stage / 3-Output Pipe Delay or 3-bit LUT
- One Selectable CNT/DLY or 3-bit LUT
- One Selectable CNT/DLY or 4-bit LUT
- One Selectable Pattern Generator or 4-bit LUT

6.9 Digital Comparators or PWM (3 total)

- Three 8-bit 100 kHz PWMs or 10 MHz Digital Comparators Delays/Counters (2 total)
- One 14-bit Delay/Counter: Range 1 – 16383 clock cycles
- One 8-bit Delay/Counter: Range 1 – 255 clock cycles
- Clock cycles can be sourced from External Clock Input or LF, Ring, or RC Oscillator
- Two counters can function as FSM counters

6.10 Programmable Delay

- 150 ns/300 ns/450 ns/600 ns @ 3.3 V
- Includes Edge Detection function

6.11 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- Pre-divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Output to Matrix: OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, OSC/64
- Output to CNT/DLY/FSM/PWM_ramp: OSC/1, OSC/4, OSC/12, OSC/24, OSC/64
- Output to ADC: OSC/1, OSC/16

6.12 Low Frequency (LF) Oscillator

- 1.9 kHz
- OSC/1, OSC/2, OSC/4, OSC/16 dividers

6.13 Ring Oscillator

- 25 MHz
- Post divider: OSC/1, OSC/4, OSC/8, OSC/16
- Output to Matrix: OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, OSC/64
- Output to CNT/DLY/FSM/PWM_ramp: OSC/1, OSC/256
- Output to ADC: OSC/1, OSC/16

6.14 Digital Storage Elements

- DFFs/Latches

6.15 Slave SPI

- Serial-to-Parallel: 8 and 16-bit modes
- Parallel-to-Serial: 8 and 16-bit modes
- Can be used as ADC buffer

7.0 I/O Pins

The SLG46140 has a total of 12 general purpose I/O pins (GPIO) which can be configured as either Input or Output, some with special functions (such as outputting the Vref), or serving as a signal for programming of the on-chip NVM.

Normal Mode pin definitions are as follows:

- Pin 1: VDD Power Supply
- Pin 2: General Purpose Input (GPI)
- Pin 3: GPIO with Output Enable (OE)
- Pin 4: GPIO with OE, ACMP0(-) Input, PGA Output
- Pin 5: GPIO with OE, ACMP1(-) Input
- Pin 6: GPIO without OE, PGA(+)
- Pin 7: GPIO with OE, PGA(-)
- Pin 8: GND
- Pin 9: GPIO with OE, 4x Drive Output, ACMP1(+) Input
- Pin 10: GPIO, 4x Drive Output, ACMP0(+) Input
- Pin 11: GPIO, ADC Channel Select
- Pin 12: GPIO with OE
- Pin 13: GPIO with OE
- Pin 14: GPIO with OE

Programming Mode pin definitions are as follows:

- Pin 1: VDD Power Supply
- Pin 2: VPP Programming Voltage
- Pin 3: RTSB
- Pin 10: Programming Mode Control
- Pin 11: Programming ID
- Pin 12: Programming SDIO
- Pin 13: Programming SRDWB
- Pin 14: Programming SCL

7.1 Input Modes

Digital Input

Each GPI, GPIO pin can be configured as a:

- Digital input with/without buffered Schmitt Trigger
- Low Voltage Digital Input (LVDI)

Pin 2 can function as a RESET pin

Analog Input

- Pin 3 can function as an analog input for the ADC Vref
- Pins 4, 5, 9, 10 can function as analog inputs for the ACMPs
- Pins 6 and 7 can function as analog input for PGA(+) and PGA(-), respectively

7.2 Output Modes

Pins 3, 4, 5, 9, 12, 13, and 14 can be configured as a digital output with 1x/2x push pull, 1x/2x Open Drain NMOS, or 1x/2x 3-state output with output enable.

7.3 Pull Up/Down Resistors

All GPIO pins can be configured with pull up/pull down resistors with selectable values or left floating (no resistor):

- Floating
- 10 kΩ
- 100 kΩ
- 1 MΩ

The GPI pin (PIN2) can only be configured with pull down resistors with the same values.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 20. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Input Mode Control	reg <762:761>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	reg <764:763>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 2 Pull Up/Down Resistor Selection	reg <765>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.2 PIN 3 Register Settings

Table 21. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Input Mode Control	reg <767:766>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Analog IO
PIN 3 Output Mode Control	reg <769:768>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 3 Pull Up/Down Resistor Value Selection	reg <771:770>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <772>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.3 PIN 4 Register Settings

Table 22. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Input Mode Control	reg <774:773>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 4 Output Mode Control	reg <776:775>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 4 Pull Up/Down Resistor Value Selection	reg <778:777>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	reg <779>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.4 PIN 5 Register Settings

Table 23. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Input Mode Control	reg <781:780>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 5 Output Mode Control	reg <783:782>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 5 Pull Up/Down Resistor Value Selection	reg <785:784>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	reg <786>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.5 PIN 6 Register Settings

Table 24. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Input Mode Control	reg <790:788>	000: Digital in without Schmitt Trigger 001: Digital in with Schmitt Trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull Mode 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO and NMOS Open-Drain Mode
PIN 6 Pull Up/Down Resistor Value Selection	reg <792:791>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	reg <793>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 6 Output Driver Current x2 Enable.	reg <794>	0: Disable 1: Enable

7.4.6 PIN 7 Register Settings

Table 25. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Input Mode Control	reg <796:795>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 7 Output Mode Control	reg <798:797>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 7 Pull Up/Down Resistor Value Selection	reg <800:799>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 7 Pull Up/Down Resistor Selection	reg <801>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.7 PIN 9 Register Settings

Table 26. PIN 9 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 9 Input Mode Control	reg <803:802>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 9 Output Mode Control	reg <805:804>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 9 Pull Up/Down Resistor Value Selection	reg <807:806>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 9 Pull Up/Down Resistor Selection	reg <808>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 9 4x Driver Enable.	reg <809>	0: Disable 1: Enable

7.4.8 PIN 10 Register Settings

Table 27. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Input Mode Control	reg <813:811>	000: Digital in without Schmitt Trigger 001: Digital in with Schmitt Trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull Mode 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO and NMOS Open-Drain Mode
PIN 10 Pull Up/Down Resistor Value Selection	reg <815:814>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	reg <816>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 10 Output Driver Current x2 Enable	reg <817>	0: Disable 1: Enable
PIN 10 4x Drive Enable	reg <818>	0: Disable 1: Enable

7.4.9 PIN 11 Register Settings

Table 28. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Input Mode Control	reg <822:820>	000: Digital in without Schmitt Trigger 001: Digital in with Schmitt Trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull Mode 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO and NMOS Open-Drain Mode
PIN 11 Pull Up/Down Resistor Value Selection	reg <824:823>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 11 Pull Up/Down Resistor Selection	reg <825>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 11 Output Driver Current x2 Enable.	reg <826>	0: Disable 1: Enable

7.4.10 PIN 12 Register Settings

Table 29. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Input Mode Control	reg <828:827>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 12 Output Mode Control	reg <830:829>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 12 Pull Up/Down Resistor Value Selection	reg <832:831>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	reg <833>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.11 PIN 13 Register Settings

Table 30. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Input Mode Control	reg <835:834>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 13 Output Mode Control	reg <837:836>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 13 Pull Up/Down Resistor Value Selection	reg <839:838>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 13 Pull Up/Down Resistor Selection	reg <840>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.12 PIN 14 Register Settings

Table 31. PIN 14 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 14 Input Mode Control	reg <842:841>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 14 Output Mode Control	reg <844:843>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 14 Pull Up/Down Resistor Value Selection	reg <846:845>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 14 Pull Up/Down Resistor Selection	reg <847>	0: Pull Down Resistor 1: Pull Up Resistor

7.5 GPI Structure (for Pin 2)

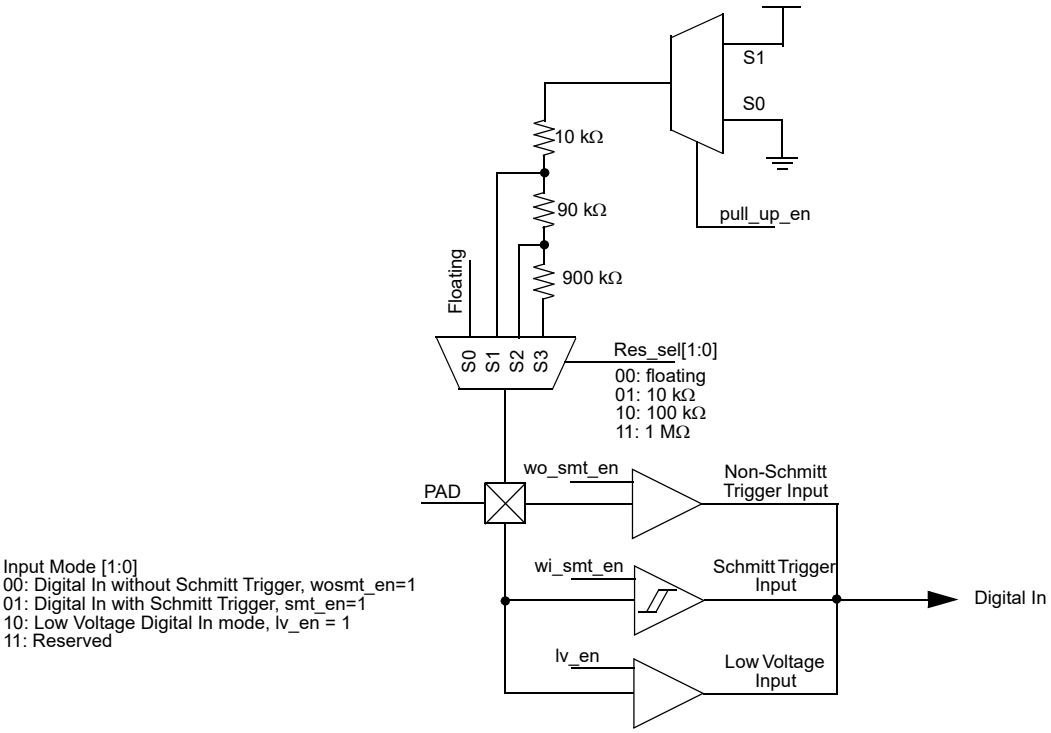


Figure 2. PIN 2 GPI IO Structure Diagram

7.6 Matrix OE IO Structure

7.6.1 Matrix OE IO Structure (for Pins 3, 4, 5, 7, 12, 13, 14)

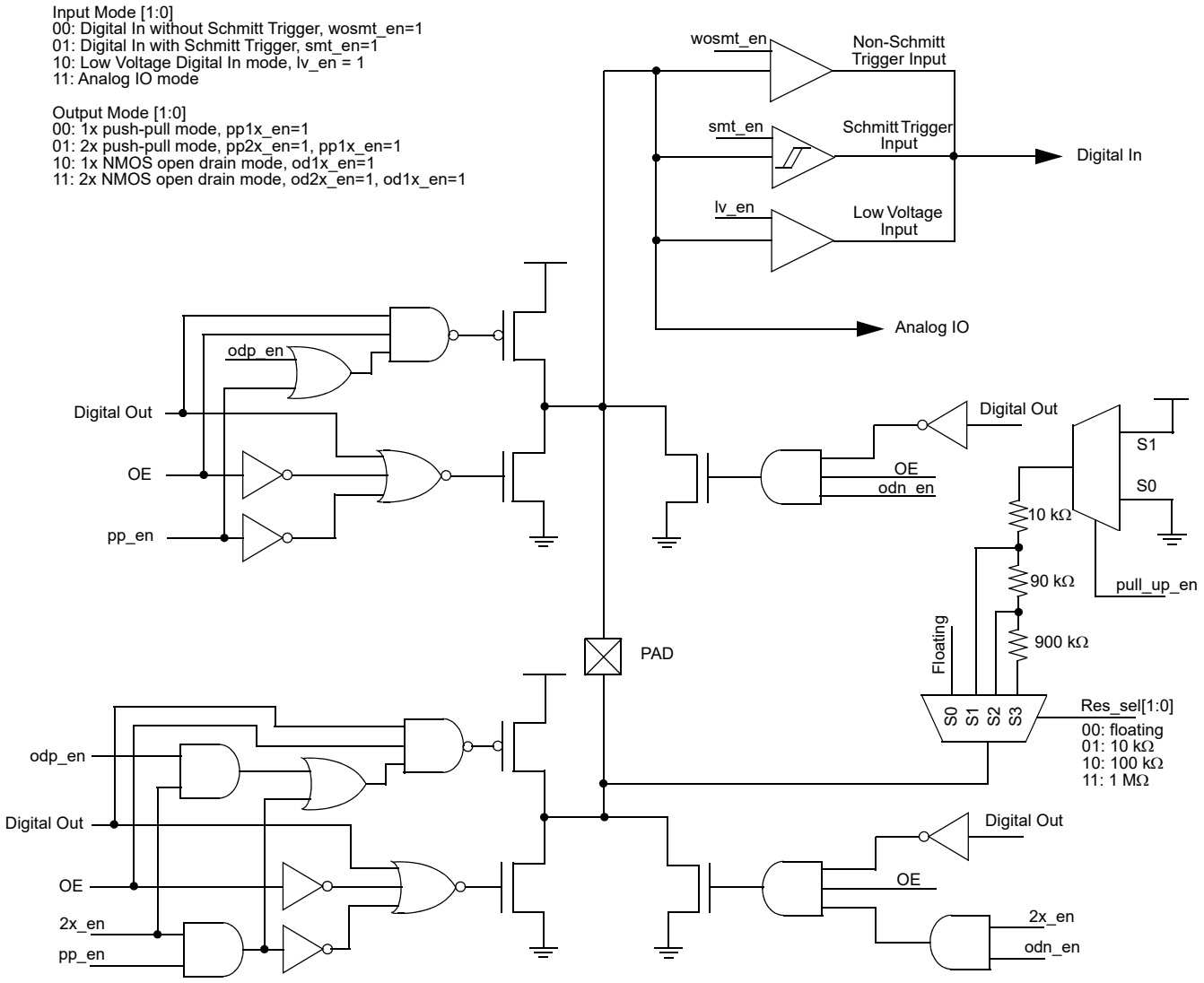


Figure 3. Matrix OE IO Structure Diagram

7.6.2 Matrix OE 4x Drive Structure (for Pin 9)

The Matrix OE 4x Drive Structure consists of two Matrix OE IO structures (see above section)

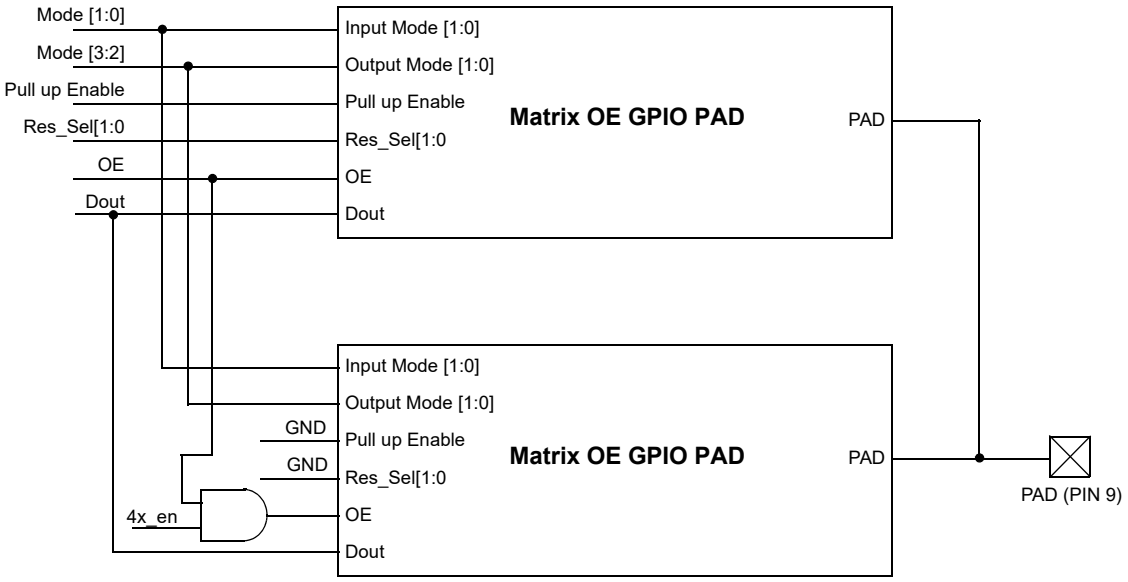


Figure 4. Matrix OE IO 4x Drive Structure Diagram

7.7 Register OE IO Structure

7.7.1 Register OE IO Structure (for Pins 6, 11)

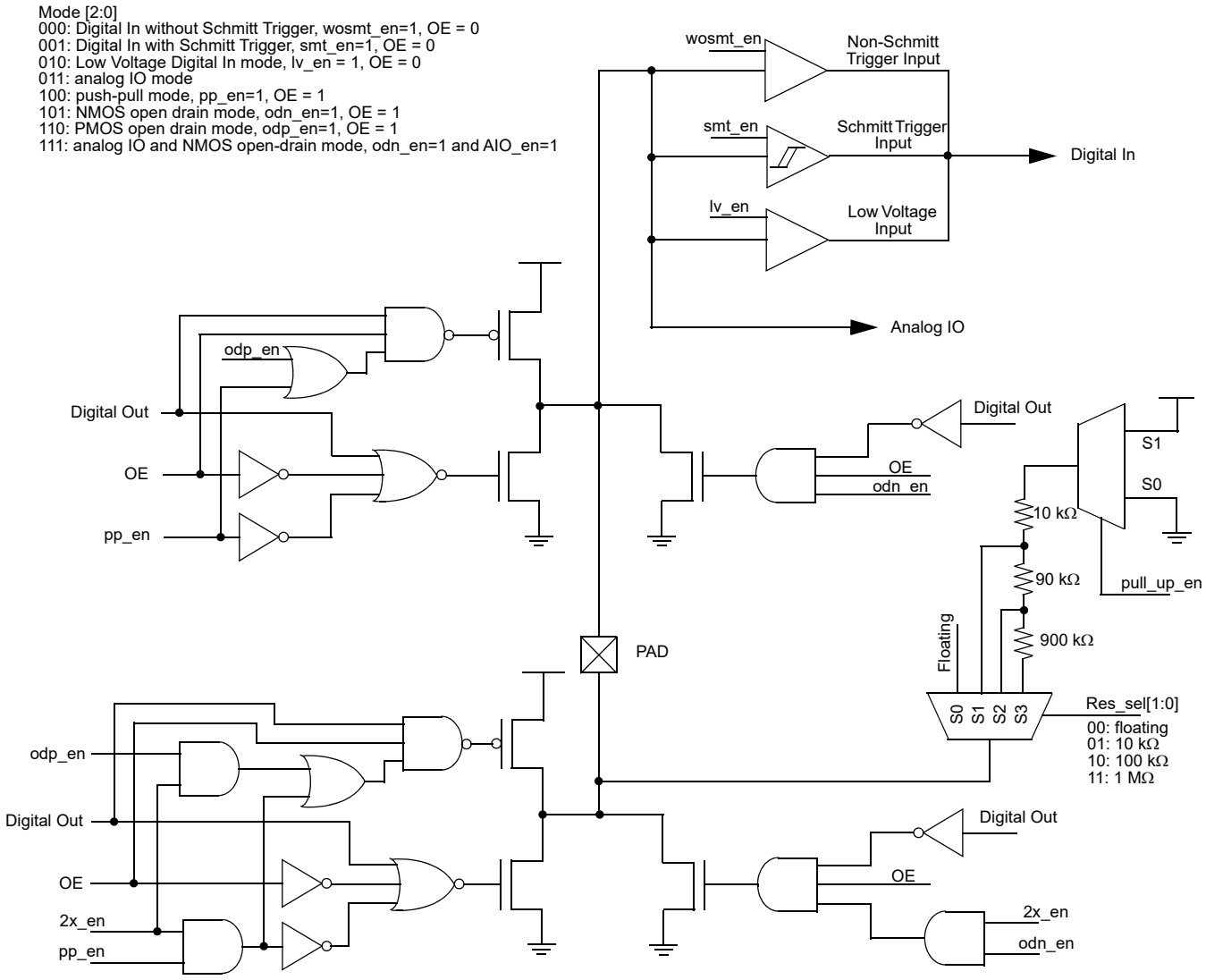


Figure 5. Register OE IO Structure Diagram

7.7.2 Register OE 4x Drive Structure (for Pin 10)

The Register OE 4x Drive Structure consists of two Register OE IO structures (see above section)

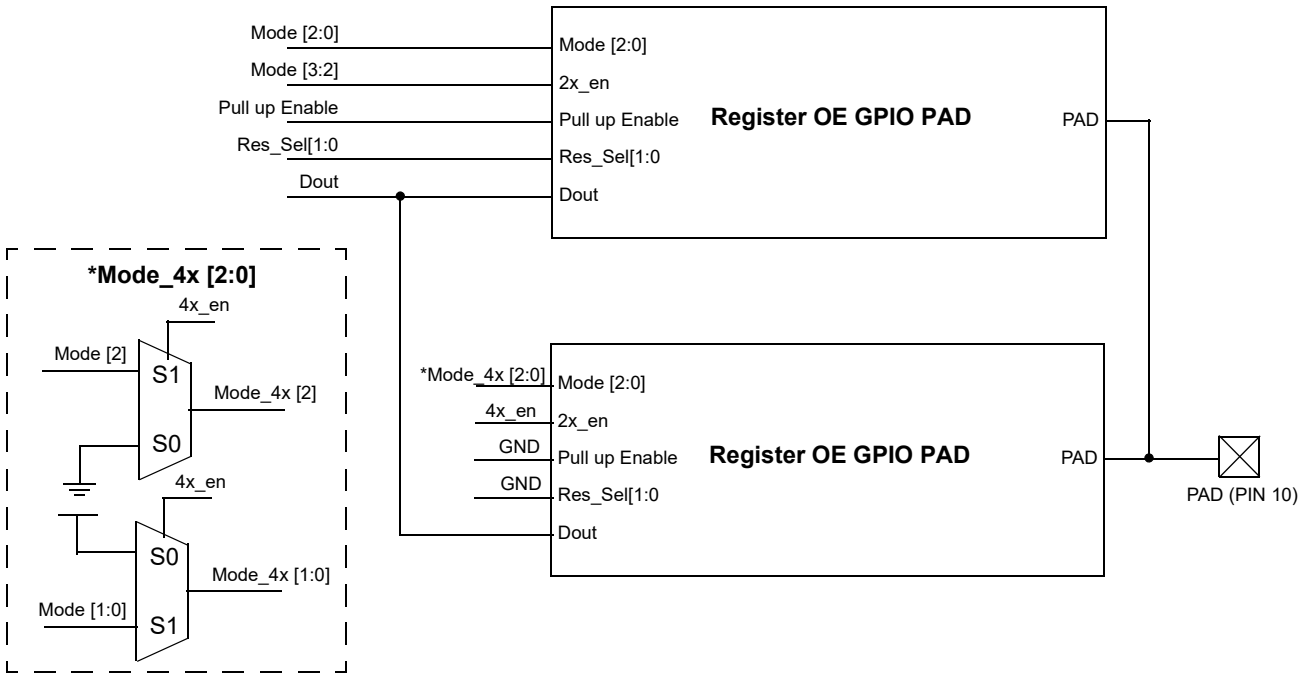


Figure 6. Register OE IO 4x Drive Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46140 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection points for each logic cell within the SLG46140 have a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 1024 register bits within the SLG46140 are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 81 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, analog comparators, other resources and VDD. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46140’s register table, see Section *23.0 Appendix A - SLG46140 Register Definition*.

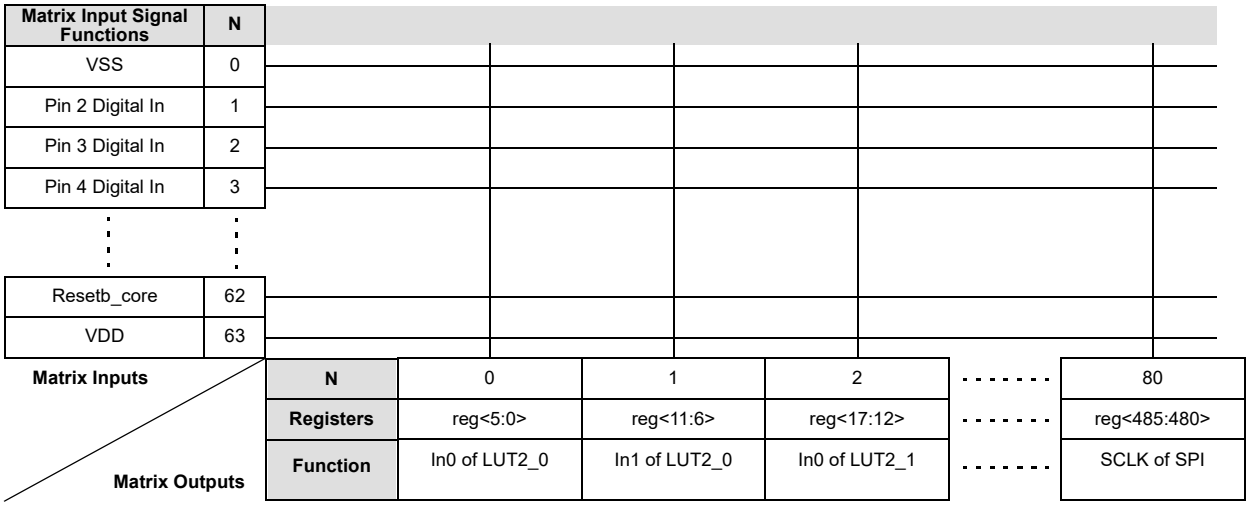


Figure 7. Connection Matrix

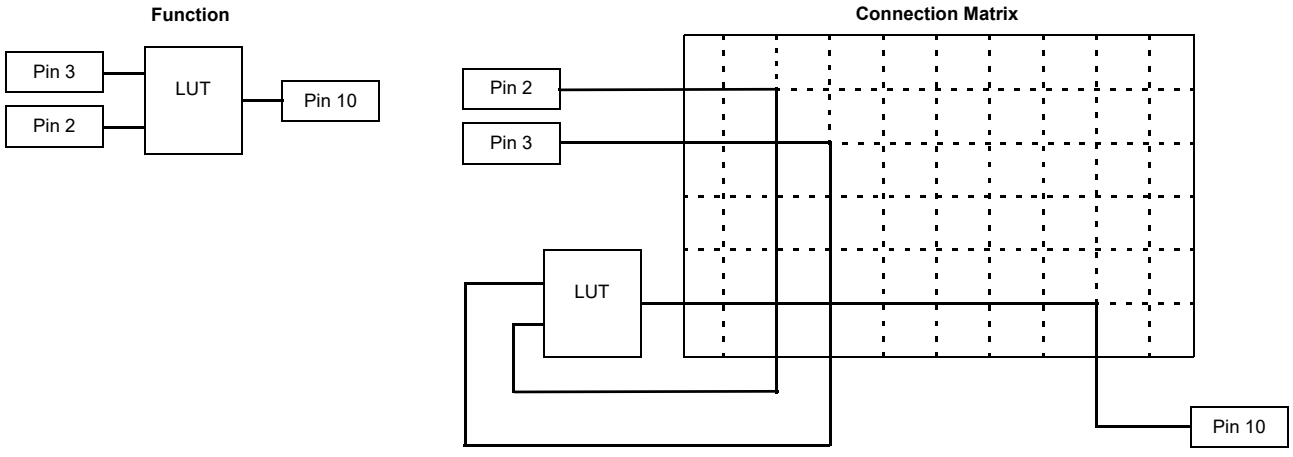


Figure 8. Connection Matrix Example

8.1 Matrix Input Table

Table 32. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GROUND	0	0	0	0	0	0
1	LUT2_0 output	0	0	0	0	0	1
2	LUT2_1 output	0	0	0	0	1	0
3	LUT2_2 output	0	0	0	0	1	1
4	LUT2_3 output	0	0	0	1	0	0
5	LUT2_4 / DFF0/Latch0 output	0	0	0	1	0	1
6	LUT2_5 / DFF1/Latch1 output	0	0	0	1	1	0
7	LUT3_0 output	0	0	0	1	1	1
8	LUT3_1 output	0	0	1	0	0	0
9	LUT3_2 output	0	0	1	0	0	1
10	LUT3_3 output	0	0	1	0	1	0
11	LUT3_4 / DFF2/Latch2 output	0	0	1	0	1	1
12	LUT3_5 / DFF3/Latch3 output	0	0	1	1	0	0
13	LUT4_0 output/PGEN output	0	0	1	1	0	1
14	DFF4/Latch4 Q output with resetb or setb	0	0	1	1	1	0
15	DFF4/Latch4 QB output with resetb or setb	0	0	1	1	1	1
16	DFF5/Latch5 Q output with resetb or setb	0	1	0	0	0	0
17	DFF5/Latch5 QB output with resetb or setb	0	1	0	0	0	1
18	1 PIPE OUT of pipe delay / LUT3_6 output	0	1	0	0	1	0
19	OUT0 of pipe delay	0	1	0	0	1	1
20	OUT1 of pipe delay	0	1	0	1	0	0
21	edgedet progdly output	0	1	0	1	0	1
22	PIN2 output	0	1	0	1	1	0
23	PIN3 output	0	1	0	1	1	1
24	PIN4 output	0	1	1	0	0	0
25	PIN5 output	0	1	1	0	0	1
26	PIN6 output	0	1	1	0	1	0
27	PIN7 output	0	1	1	0	1	1
28	PIN9 output	0	1	1	1	0	0
29	PIN10 output	0	1	1	1	0	1
30	PIN11 output	0	1	1	1	1	0
31	PIN12 output	0	1	1	1	1	1
32	PIN13 output	1	0	0	0	0	0
33	PIN14 output	1	0	0	0	0	1
34	ring oscillator output	1	0	0	0	1	0
35	RC oscillator output	1	0	0	0	1	1
36	low frequency oscillator output	1	0	0	1	0	0
37	CNT0/DLY0 output	1	0	0	1	0	1

Table 32. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	CNT1/DLY1 output	1	0	0	1	1	0
39	CNT2/DLY2 / LUT4_1 output	1	0	0	1	1	1
40	CNT3/DLY3 / LUT3_7 output	1	0	1	0	0	0
41	PWM0_DCMP0_Out_positive	1	0	1	0	0	1
42	PWM0_DCMP0_Out_negative	1	0	1	0	1	0
43	PWM1_DCMP1_Out_positive	1	0	1	0	1	1
44	PWM1_DCMP1_Out_negative	1	0	1	1	0	0
45	PWM2_DCMP2_Out_positive	1	0	1	1	0	1
46	PWM2_DCMP2_Out_negative	1	0	1	1	1	0
47	SPI interrupt	1	0	1	1	1	1
48	ACMP0 output	1	1	0	0	0	0
49	ACMP1 output	1	1	0	0	0	1
50	ADC interrupt	1	1	0	0	1	0
51	bg_ok signal (delay 200ns)	1	1	0	0	1	1
52	power detector output	1	1	0	1	0	0
53	no divider RC oscillator output	1	1	0	1	0	1
54	GROUND	1	1	0	1	1	0
55	GROUND	1	1	0	1	1	1
56	GROUND	1	1	1	0	0	0
57	GROUND	1	1	1	0	0	1
58	GROUND	1	1	1	0	1	0
59	GROUND	1	1	1	0	1	1
60	GROUND	1	1	1	1	0	0
61	GROUND	1	1	1	1	0	1
62	POR output	1	1	1	1	1	0
63	VDD	1	1	1	1	1	1

8.2 Matrix Output Table

Table 33. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<5:0>	In0 of LUT2_0	0
reg<11:6>	In1 of LUT2_0	1
reg<17:12>	In0 of LUT2_1	2
reg<23:18>	In1 of LUT2_1	3
reg<29:24>	In0 of LUT2_2	4
reg<35:30>	In1 of LUT2_2	5
reg<41:36>	In0 of LUT2_3	6
reg<47:42>	In1 of LUT2_3	7
reg<53:48>	In0 of LUT2_4 / Data of DFF/Latch 0	8
reg<59:54>	In1 of LUT2_4 / Clock of DFF/Latch 0	9
reg<65:60>	In0 of LUT2_5 / Data of DFF/Latch 1	10
reg<71:66>	In1 of LUT2_5 / Clock of DFF/Latch 1	11
reg<77:72>	In0 of LUT3_0	12
reg<83:78>	In1 of LUT3_0	13
reg<89:84>	In2 of LUT3_0	14
reg<95:90>	In0 of LUT3_1	15
reg<101:96>	In1 of LUT3_1	16
reg<107:102>	In2 of LUT3_1	17
reg<113:108>	In0 of LUT3_2	18
reg<119:114>	In1 of LUT3_2	19
reg<125:120>	In2 of LUT3_2	20
reg<131:126>	In0 of LUT3_3	21
reg<137:132>	In1 of LUT3_3	22
reg<143:138>	In2 of LUT3_3	23
reg<149:144>	In0 of LUT3_4 / Resetb of DFF/Latch 2	24
reg<155:150>	In1 of LUT3_4 / Data of DFF/Latch 2	25
reg<161:156>	In2 of LUT3_4 / Clock of DFF/Latch 2	26
reg<167:162>	In0 of LUT3_5 / Resetb of DFF/Latch 3	27
reg<173:168>	In1 of LUT3_5 / Data of DFF/Latch 3	28
reg<179:174>	In2 of LUT3_5 / Clock of DFF/Latch 3	29
reg<185:180>	In0 of LUT4_0	30
reg<191:186>	In1 of LUT4_0	31
reg<197:192>	In2 of LUT4_0 or PGEN	32
reg<203:198>	In3 of LUT4_0 or PGEN	33
reg<209:204>	Resetb of DFF/Latch 4	34
reg<215:210>	Data of DFF/Latch 4	35
reg<221:216>	Clock of DFF/Latch 4	36
reg<227:222>	Resetb of DFF/Latch 5	37

Table 33. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<233:228>	Data of DFF/Latch 5	38
reg<239:234>	Clock of DFF/Latch 5	39
reg<245:240>	Clock of Pipe Delay / In0 of LUT3_6	40
reg<251:246>	In of Pipe Delay / In1 of LUT3_6	41
reg<257:252>	PORB of Pipe Delay / In2 of LUT3_6	42
reg<263:258>	Input of Edge Detector and Programmable Delay	43
reg<269:264>	Digital Output of PIN3	44
reg<275:270>	OE of PIN3	45
reg<281:276>	Digital Output of PIN4	46
reg<287:282>	OE of PIN4	47
reg<293:288>	Digital Output of PIN5	48
reg<299:294>	OE of PIN5	49
reg<305:300>	Digital Output of PIN6	50
reg<311:306>	Digital Output of PIN7	51
reg<317:312>	OE of PIN7	52
reg<323:318>	Digital Output of PIN9	53
reg<329:324>	OE of PIN9	54
reg<335:330>	Digital Output of PIN10	55
reg<341:336>	Digital Output of PIN11	56
reg<347:342>	Digital Output of PIN12	57
reg<353:348>	OE of PIN12	58
reg<359:354>	Digital Output of PIN13	59
reg<365:360>	OE of PIN13	60
reg<371:366>	Digital Output of PIN14	61
reg<377:372>	OE of PIN14	62
reg<383:378>	ADC Power Down (1: Power Down)	63
reg<389:384>	PDB (Power Down) for ACMP0 (0: Power Down)	64
reg<395:390>	PDB (Power Down) for ACMP1 (0: Power Down)	65
reg<401:396>	Oscillator Power Down (1: Power Down)	66
reg<407:402>	counter external Clock In3 of LUT4_1	67
reg<413:408>	Input of DLY/CNT0	68
reg<419:414>	Input of DLY/CNT1	69
reg<425:420>	Input of DLY/CNT2 In0 of LUT4_1	70
reg<431:426>	Keep of DLY/CNT2 (FSM0) In1 of LUT4_1	71
reg<437:432>	Up of DLY/CNT2 (FSM0) In2 of LUT4_1	72
reg<443:438>	Input of DLY/CNT3 In0 of LUT3_7	73

Table 33. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<449:444>	Keep of DLY/CNT3 (FSM1) In1 of LUT3_7	74
reg<455:450>	Up of DLY/CNT3 (FSM1) In2 of LUT3_7	75
reg<461:456>	PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 0	76
reg<467:462>	PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 1	77
reg<473:468>	PWM Power Down (1: Power Down)	78
reg<479:474>	CSB of SPI	79
reg<485:480>	SCLK of SPI	80

9.0 8-bit SAR ADC Analog-to-Digital Converter (ADC)

The Analog to Digital Converter in the SLG46140 is an 8-bit Successive Approximation Register Analog to Digital Converter (SAR ADC) which operates at a sampling speed of 100 kHz. The ADC's DNL < ± 0.5 LSB and INL < ± 3.4 LSB and has a ADC V_{REF} accuracy of ± 50 mV. The ADC consists of two parts: PGA which provides signal amplification and conditioning and SAR ADC which handles analog to digital conversion. PGA can be used as amplifier when ADC is disabled. Please see section *9.3.2 PGA Output* for more details. User controlled inputs and outputs of the ADC are listed below:

Inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input Mux Control Signal (PIN 11, VDD)
- IN+: Single-Ended Mode Input (PIN6 or PIN7) and Differential Mode Positive Input (PIN6)
- IN-: Differential Mode Negative Input (PIN 7 or DAC0)
- VREF: ADC Voltage Reference Input (ADC V_{REF}, VDD/4, none)
- CLK or CLK/16: ADC Clock Input (Ring OSC, Ext. CLK2 (matrix_out67), RC OSC, SPI SCLK)
- Wake/Sleep

Outputs:

- PGA_Out: Output of the PGA to PIN4
- PGA_Out: Output of the PGA to ACMP1
- SER DATA: ADC serial output (SPI)
- PAR DATA: 8-bit ADC parallel data to either the SPI, PWM, or DCMP
- INT_ OUT: ADC Interrupt Output (matrix_in50)

9.1 ADC Functional Diagram

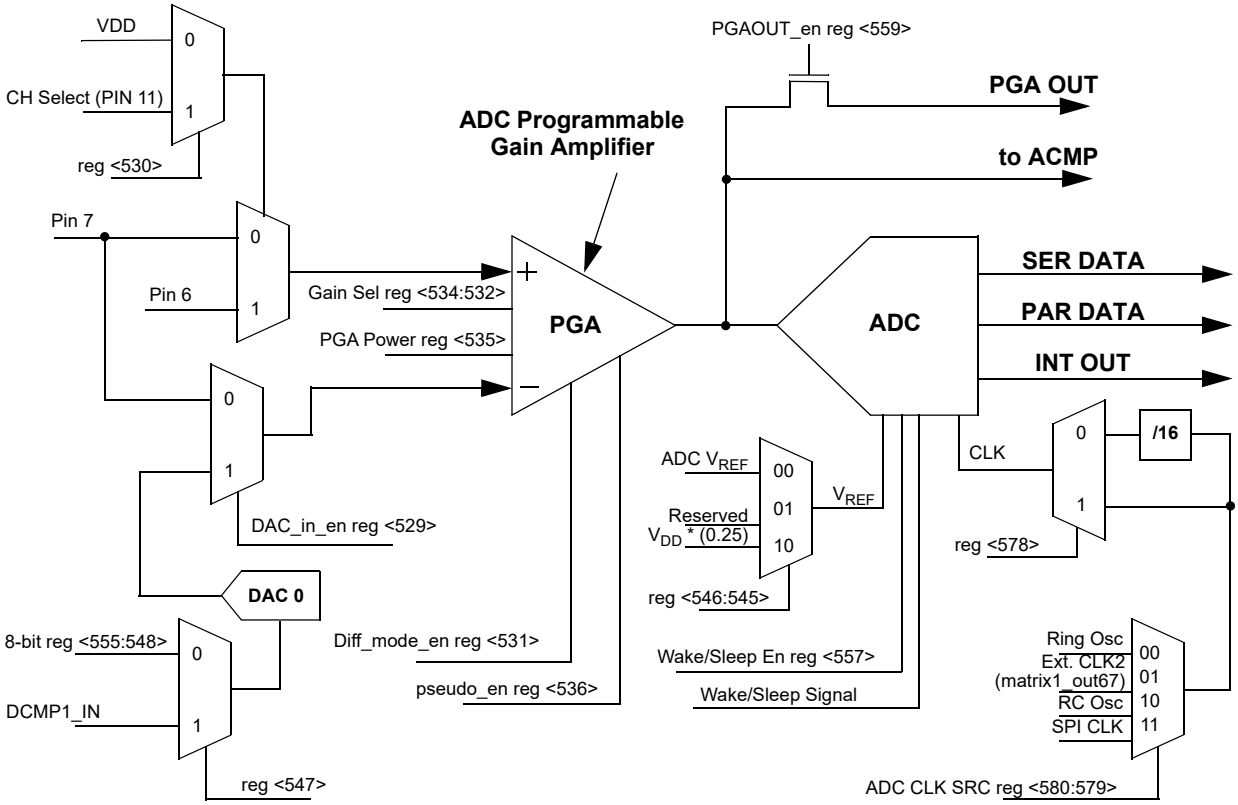


Figure 9. ADC Functional Diagram

9.2 ADC Operation Modes

The ADC has three operating modes:

- Single-Ended ADC operation using IN+ from PIN 6 or 7, when *ADC_sel* (reg <531>) is “0”
- Differential ADC operation using IN+ from PIN 6 and IN- from PIN 7, when *ADC_sel* (reg <531>) is “1”
- Pseudo-Differential ADC operation using IN+ from PIN 6 and IN- from PIN 7, when *ADC_sel* (reg <531>) and

ADC_pseudo-diff_en (reg <536>) bits are both set to “1”.

9.3 ADC 3-bit Programmable Gain Amplifier (PGA)

The front end of the ADC is a PGA with 3 bits for setting gain. The PGA buffers the ADC in all cases. The PGA gain is set by the ADC_gain_control (reg<534:532>). See ADC Register Settings Table.

Available gain settings depending on PGA mode selected (when used as ADC front-end):

- Single-ended: 0.25x, 0.5x, 1x, 2x, 4x, 8x;
- Differential: 1x, 2x, 4x, 8x, 16x;
- Pseudo-Differential: 1x, 2x, 4x.

PGA inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input Mux Control Signal (PIN 11, VDD)
- IN+: Single-Ended Mode Input (PIN6 or PIN7) and Differential Mode Positive Input (PIN6)
- IN-: Differential Mode Negative Input (PIN7 or DAC0)

PGA output is connected directly to ADC input. Also, it is possible to connect PIN7 to PGA output (reg<886>), when ADC is not in use only. The output of PGA has an offset when used as ADC front-end. Please see section *9.3.2 PGA Output* for more details.

9.3.1 PGA 2-Channel Selection

When *ADC_channel_sel* (reg <530>) is set to “1”, the PGA of the ADC will sample either PIN 6 or PIN 7 on the IN+ input, where the selection is controlled by PIN 11.

- When PIN 11 is set to “0”, the ADC will sample PIN 7
- When PIN 11 is set to “1”, the ADC will sample PIN 6

When *ADC_channel_sel* (reg <530>) is set to “0”, the PGA of the ADC will sample PIN 6 on the IN+ input.

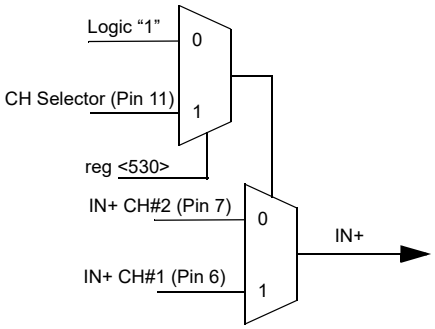


Figure 10. ADC 2-Channel Selection

9.3.2 PGA Output

PGA can be used either in standalone mode or as ADC font-end / ACMP input buffer.

In PGA standalone mode (ADC in POWER DOWN mode) PGA output is always referenced to GND. When ADC is powered on, it powers also the PGA output reference macrocell, so that the output voltage is referenced to one of predefined output offset voltages Vos(RTO) which can be found in PGA specifications. This offset is required for correct ADC operation and it does not affect output code calculation.

PGA output reference (when ADC is on):

- Single-ended mode: Vos(RTO) = GND
- Differential mode: Vos(RTO) = 550 mV
- Pseudo-Differential mode: Vos(RTO) = 180 mV

Note that the reference voltage macrocell is controlled by ADC, therefore if ADC is in POWER DOWN mode, the reference macrocell is OFF and PGA output is referenced to GND. In this case both Differential and Pseudo-Differential modes provide the same output. Typical PGA specifications in Differential/Pseudo-Differential mode with ADC in POWER DOWN state are given in specifications section for information only.

Note 1: PGA operation in Differential/Pseudo-Differential mode with ADC in POWER DOWN state is not recommended to use.

Note 2: Toggling ADC POWER DOWN mode will also toggle the PGA output reference macrocell, that will influence the ACMP input voltage.

PGA has a few output connection possibilities: to ACMP1 and/or ADC, and to external output on PIN4. Connection to external output is possible only when ADC is powered down.

PGA output connection options:

- Single-Ended mode:
  - ADC
  - ACMP
  - External output
- Differential mode:
  - ADC
  - ACMP (See Note 2)
  - External output (Operation in this mode is not recommended)
- Pseudo-Differential mode:
  - ADC
  - ACMP (See Note 2)
  - External output (Operation in this mode is not recommended)

9.3.3 PGA Power On Signal

Whenever ADC is enabled, PGA is powered on automatically. However, it is possible to use PGA separately. In this case, Power On function must be enabled, reg <535> = 1.

9.3.4 PGA Register Settings

Table 34. PGA Register Settings

Signal Function	Register Bit Address	Register Definition
PGA Native Input From Internal DAC0	<529>	0: Disable 1: Enable

Table 34. PGA Register Settings

Signal Function	Register Bit Address	Register Definition
Multichannel Input MUX Enable (Controlled By Pin11)	<530>	0: Disable (PIN11 can not control) 1: Enable
PGA Input Mode Control	<531>	0: Single ended 1: Differential input
PGA Gain Selection	<534:532>	000: 0.25x (For single-ended operation only) 001: 0.5x (For single-ended operation only) 010: 1x 011: 2x 100: 4x 101: 8x (For single-ended and differential operation) 110: 16x (For differential operation only) 111: Reserved
PGA power on signal	<535>	0: power down 1: power on Note: in ADC wake/sleep dynamic on/off mode, must be set to 0
PGA Pseudo-Differential Mode Enable	<536>	0: Disable 1: Enable
DAC0 Input Selection	<547>	0: From register 1: From DCMP1's input
DAC0 8 Bit Register Control	<855:548>	00: DAC0 output Is 0 FF: DAC0's output Is 1 V
Force ADC Analog Part On	<558>	0: Disable 1: Enable
PGA Output Enable	<559>	0: Disable 1: Enable

9.3.5 PGA Typical Performance

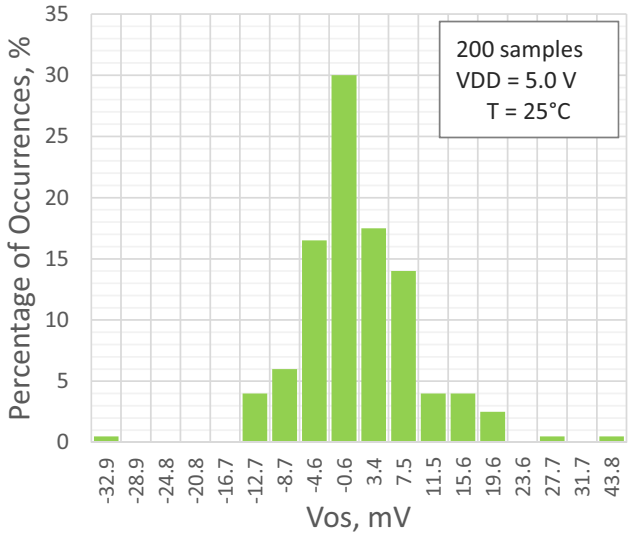


Figure 11. PGA Input Offset Distribution, Single-Ended Mode, G = 0.25

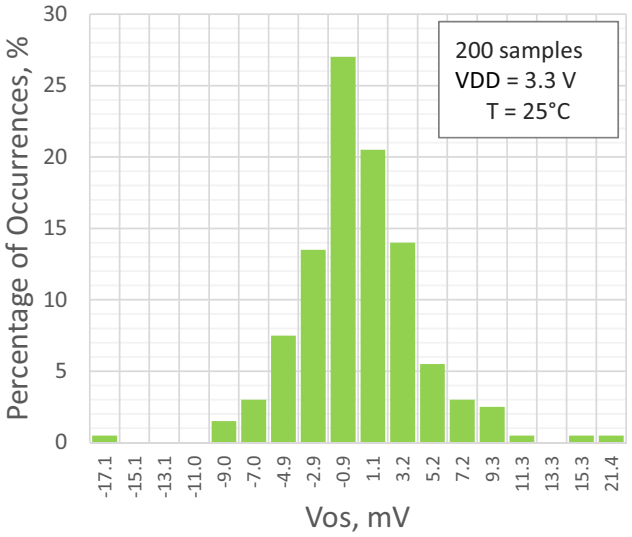


Figure 12. PGA Input Offset Distribution, Single-Ended Mode, G = 0.5

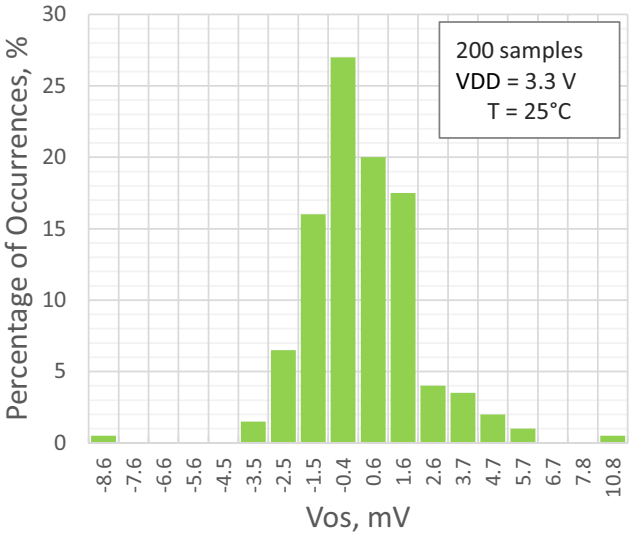


Figure 13. PGA Input Offset Distribution, Single-Ended Mode, G = 1

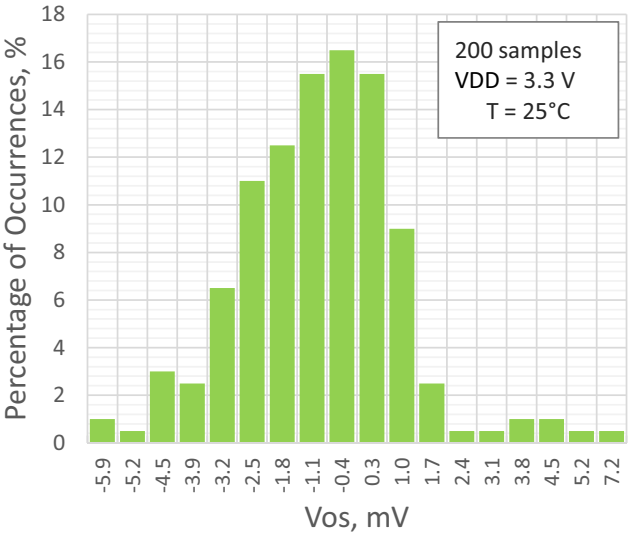


Figure 14. PGA Input Offset Distribution, Single-Ended Mode, G = 2

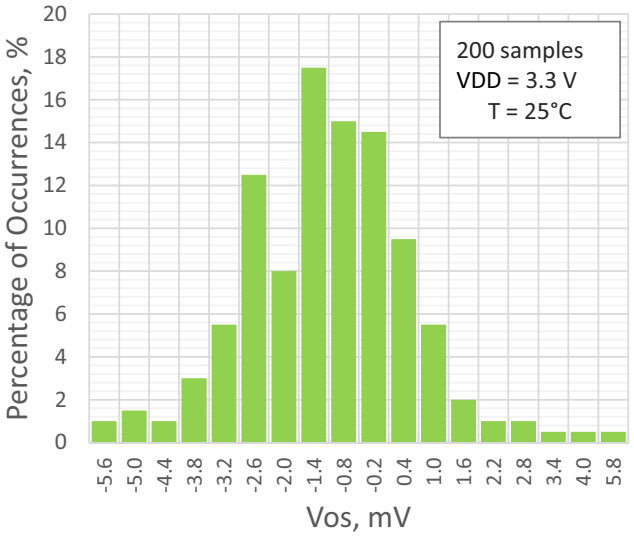


Figure 15. PGA Input Offset Distribution, Single-Ended Mode, G = 4

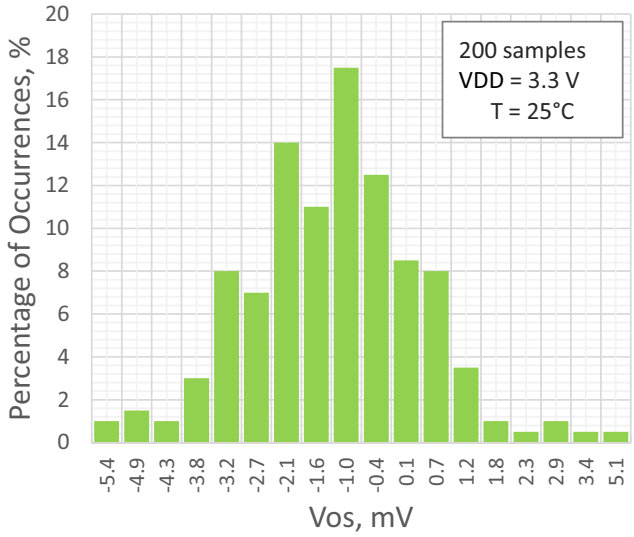


Figure 16. PGA Input Offset Distribution, Single-Ended Mode, G = 8

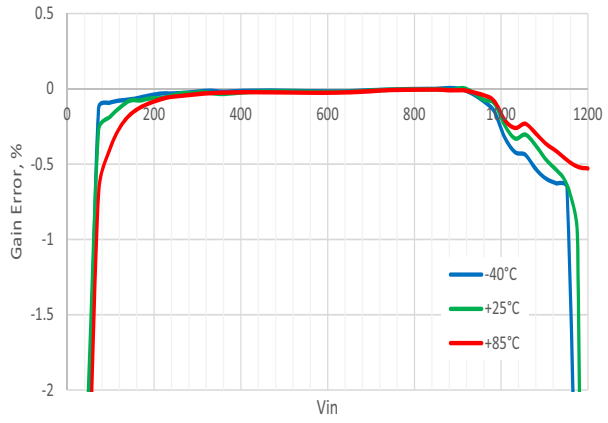


Figure 17. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 1, VDD = 1.71 V

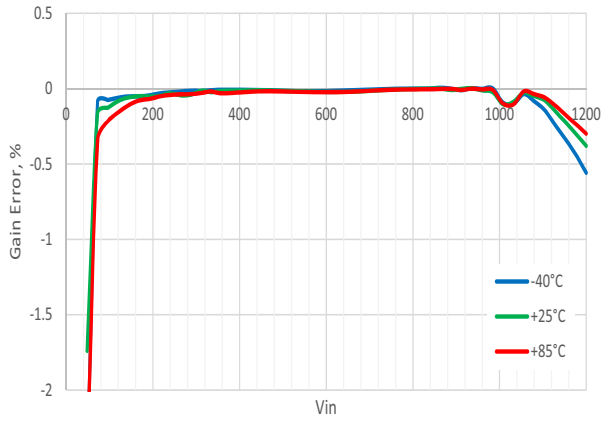


Figure 18. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 1, VDD = 5.5 V

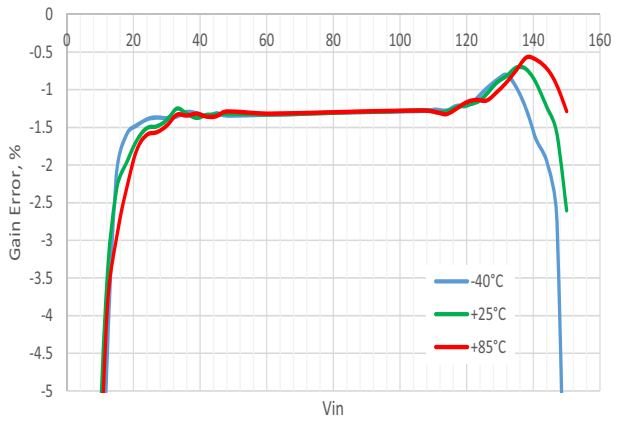


Figure 19. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 8, VDD = 1.71 V

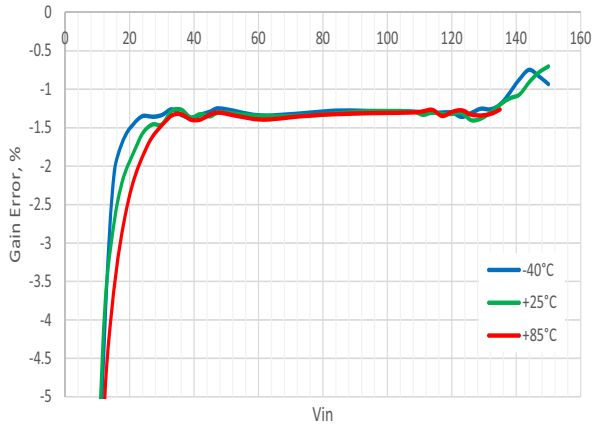


Figure 20. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 8, VDD = 5.5 V

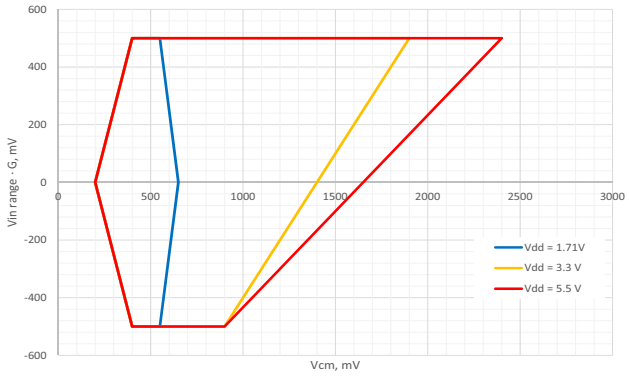


Figure 21. PGA Input Vind Range Multiplied by Gain vs. Vcm, Differential Mode

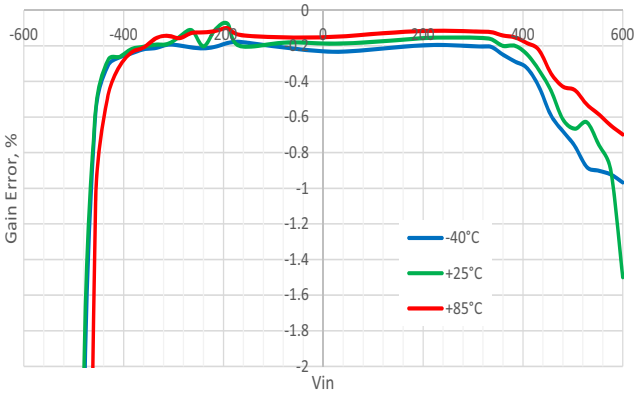


Figure 22. Typical PGA Gain Error vs. Vin, Differential Mode, G = 1, VDD = 1.71 V

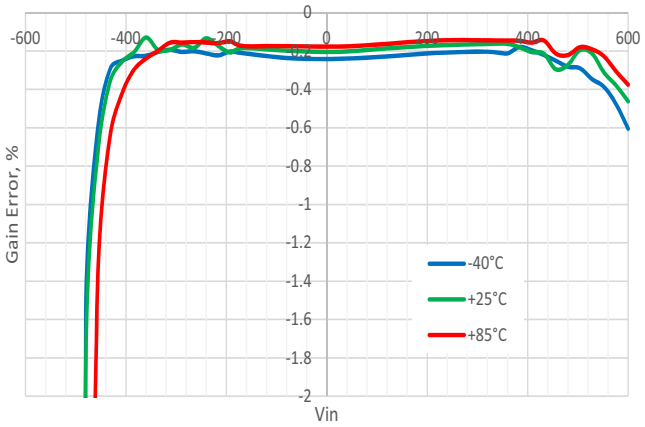


Figure 23. Typical PGA Gain Error vs. Vin, Differential Mode, G = 1, VDD = 5.5 V

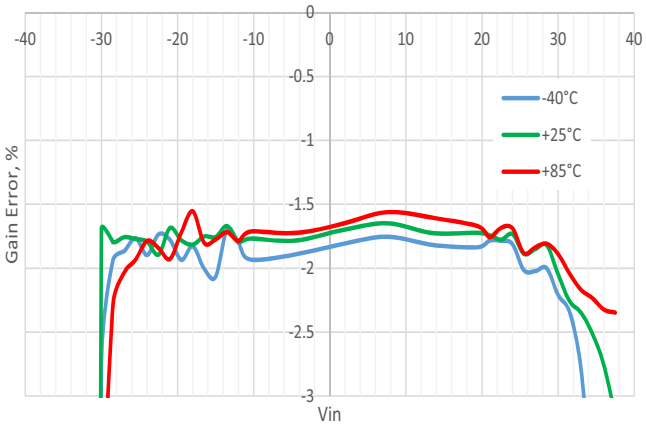


Figure 24. Typical PGA Gain Error vs. Vin, Differential Mode, G = 16, VDD = 1.71 V

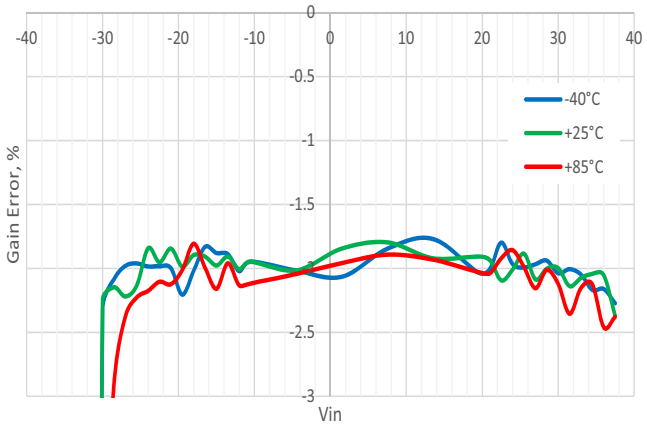


Figure 25. Typical PGA Gain Error vs. Vin, Differential Mode, G = 16, VDD = 5.5 V

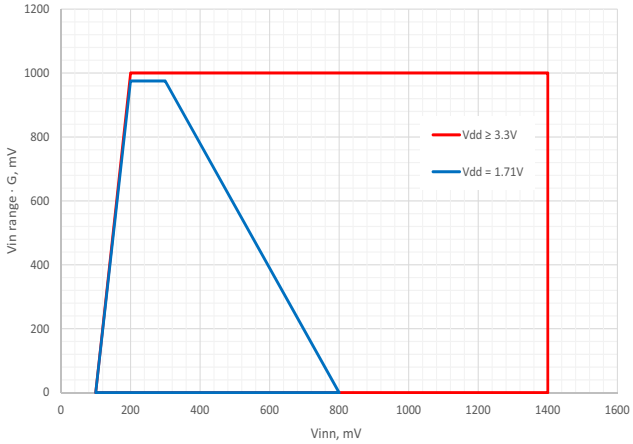


Figure 26. PGA Input Vind Range Multiplied by Gain vs. Vinn, Pseudo-Differential Mode, G = 1

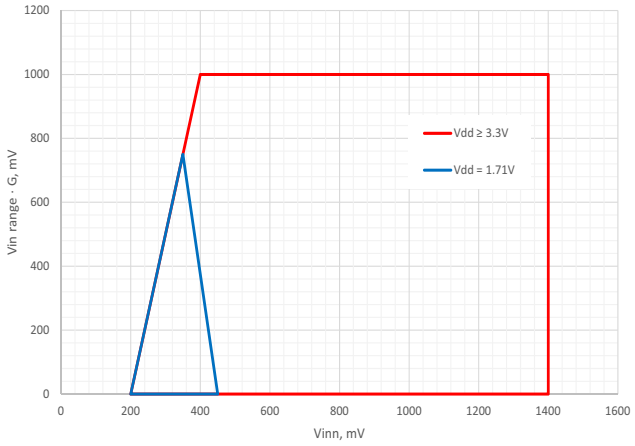


Figure 27. PGA Input Vind Range Multiplied by Gain vs. Vinn, Pseudo-Differential Mode, G = 2

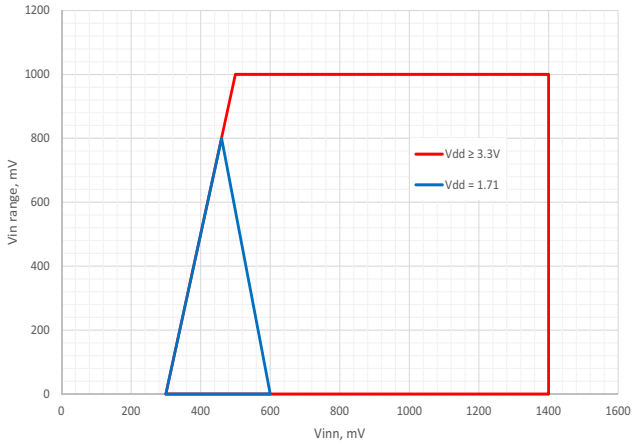


Figure 28. PGA Input Vind Range Multiplied by Gain vs. Vinn, Pseudo-Differential Mode, G = 4

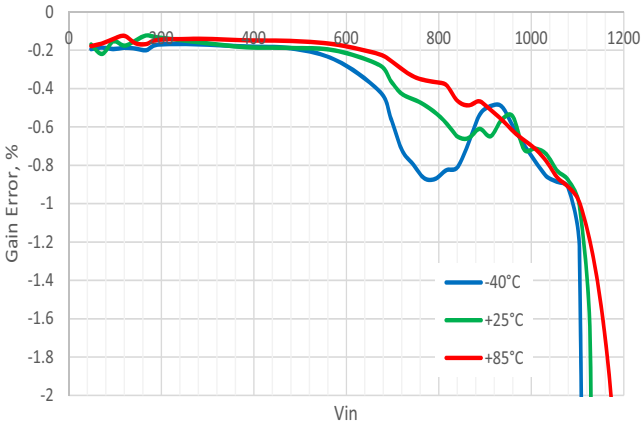


Figure 29. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G = 1, VDD = 2.0 V

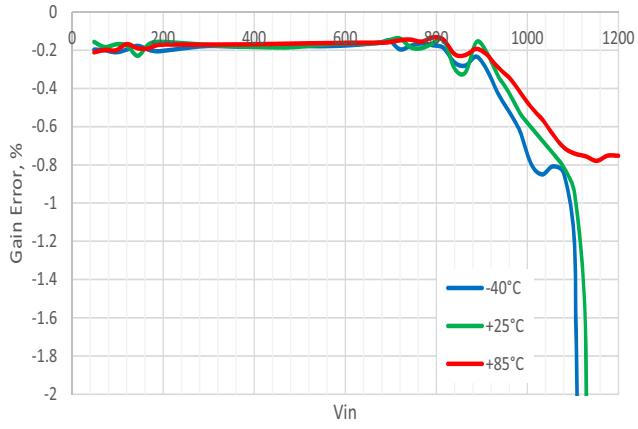


Figure 30. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G = 1, VDD = 5.5 V

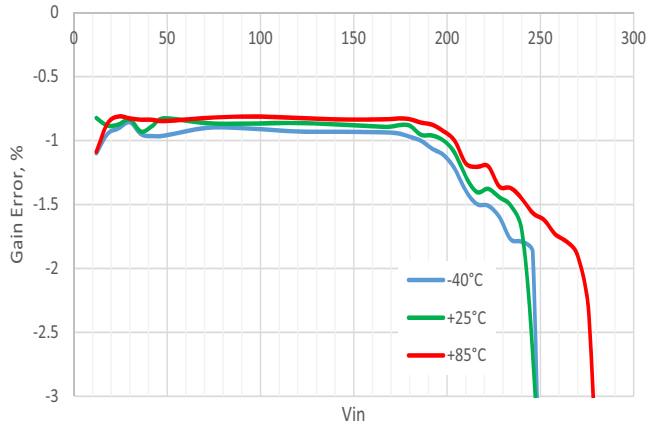


Figure 31. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G= 4, VDD = 1.71 V

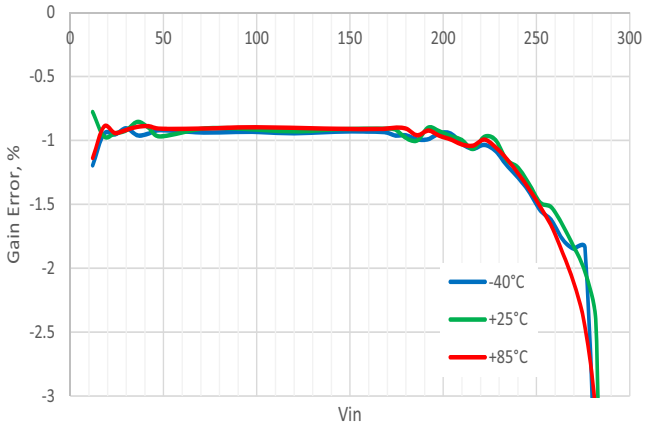


Figure 32. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G= 4, VDD = 5.5 V

9.4 ADC Input Voltage Definition

The ADC's input voltage (V_{IN_ADC}) is calculated based on either the single-ended or differential operation modes the logic cell is set to. In single-ended mode V_{IN_ADC} is the positive input voltage multiplied by the gain of the PGA. While in differential mode the V_{IN_ADC} is the difference between the positive and negative input voltages multiplied by the gain of the PGA plus one half of the reference voltage.

$$V_{OUT(PGA)} = V_{IN(ADC)} = G \cdot (V_{inp} + V_{os(RTI)}) \text{ - for SE mode}$$

$$V_{OUT(PGA)} = V_{IN(ADC)} = G \cdot V_{ind} + V_{os(RTO)} \text{ - for DI and PD mode}$$

V_{os} - PGA offset voltage. RTI and RTO denotes referred to input and referred to output V_{os}.

$$V_{os(RTI)} = \frac{V_{os(RTO)}}{G}$$

G - PGA nominal gain

V_{ind} - PGA input voltage (differential):

$$V_{ind} = V_{inp} - V_{inn}$$

$$V_{inp} = V_{cm} + \frac{V_{ind}}{2}$$

$$V_{inn} = V_{cm} - \frac{V_{ind}}{2}$$

V_{inn} and V_{inp} - absolute voltage at negative and positive PGA input correspondingly

V_{cm} - common mode PGA voltage:

$$V_{cm} = \frac{V_{inn} + V_{inp}}{2}$$

Note: In Pseudo-Differential mode V_{cm} is replaced by V_{inn} voltage for convenience

ADC code for PGA differential input voltage V_{ind} can be calculated as follows:

- Single-ended mode:

$$V_{ind} = V_{inp}$$

$$ADC_{code} = \frac{255}{V_{inp[max]} - V_{inp[min]}}(V_{inp} - V_{inp[min]})$$

Vinp[min] and Vinp[max] - positive input voltage for bit0 and bit255 correspondingly (can be found in ADC specifications)

- Differential and Pseudo-Differential mode:

$$ADC_{code} = \frac{255}{V_{ind[max]} - V_{ind[min]}}(Vind - Vind[min])$$

$V_{ind[min]}$ and $V_{ind[max]}$ - differential input voltage for bit0 and bit255 correspondingly (can be found in ADC specifications)

Least significant bit size (LSB) calculates as follows:

$$LSB = \frac{FS}{255}$$

where FS is full-scale range:

$$FS = V_{ind[max]} - V_{ind[min]}$$

9.5 ADC Reference Voltage

The ADC's reference voltage (V_{REF}) is controlled by ADC_Vref_sel (reg <546:545>). The two reference inputs are chosen from the following:

- ADC V_{REF} from Internal Source (ADC V_{REF} = 1.2 V)
- Power Divider of (0.25) * V_{DD}
-

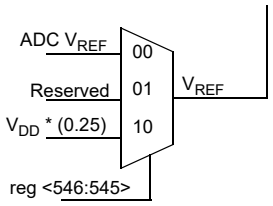


Figure 33. ADC Reference Voltage

9.6 ADC Power Down Select Mode

The ADC's power down source is selected by Matrix_Out63 reg<383:378>. A value of "1" will drive the ADC and the PGA to power down mode. The SLG46140 also has a slow/fast power on mode feature controlled by reg<558>. When reg<558> = 0, the ADC is in slow power on mode and the entire analog macrocell is controlled by *connection matrix output 63*. When reg<558> = 1, ADC is in fast power on mode, where only the ADC will be controlled by *connection matrix output 63* and the analog macrocell will remain on. With this feature, the first ADC power on (with the rest of the analog macrocell) will be approximately 500μs; the next power cycle the ADC power on (ADC only) time is <5 μs.

9.7 ADC Clock Source

The ADC clock source comes from either the internal RC Oscillator, Matrix1_Out73, Ring Oscillator, or SPI CLK. The ADC requires 16 clock cycles to sample the analog voltage and output the sampled data.

Note: sampling rate should not exceed approximately 100 kbps.

The selection is made from the *ADC_clk_sel* signal via reg <580:579> where:

- 00: Ring Oscillator
- 01: Matrix1_Out 73
- 10: RC Oscillator
- 11: SPI CLK

Note: It is not recommended to design in high frequency signals (input our output) on pins adjacent to the following pins: Pin7, Pin8, PIn9 as this may affect ADC performance.

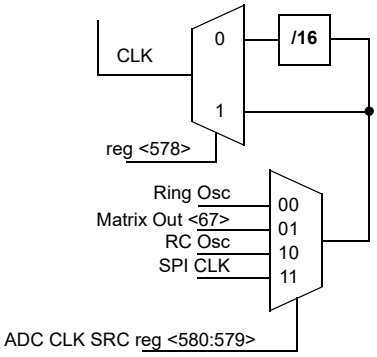


Figure 34. ADC Clock Source

9.8 ADC Outputs

The ADC's output can be shifted out through the SPI logic cell. Both SER DATA and PAR DATA produce an 8-bit data string over 16 clock cycles. See *Figure 35.*

9.8.1 ADC Serial Output

The 8-bit serial data can be output from the SLG46140 device on PIN 6. The individual 8 serial data bits can be read into an external device within the larger system design.

To initialize the *SER DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After 3 ADC_CLK cycles the ADC will start to output the 8-Bit Serial Data. This PD signal needs to be held for at least 16 ADC_CLK cycles. The ADC_CLK is determined by either the RC Osc, Ring Osc, Matrix_Out67, or SPI CLK.

9.8.2 ADC Parallel Output

The 16-bit parallel data can be output from the ADC logic cell to either the DCMP/PWM or FSM logic cells within the SLG46140 device.

To initialize the *PAR DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After ten ADC_CLK cycles the ADC will start to output the 16-Bit Parallel Data. This PD signal needs to be held for at least 32 ADC_CLK cycles. The ADC_CLK is determined by either the RC Osc, Ring Osc, Matrix_Out67, or SPI CLK.

9.9 ADC Interrupt Output Timing Diagram

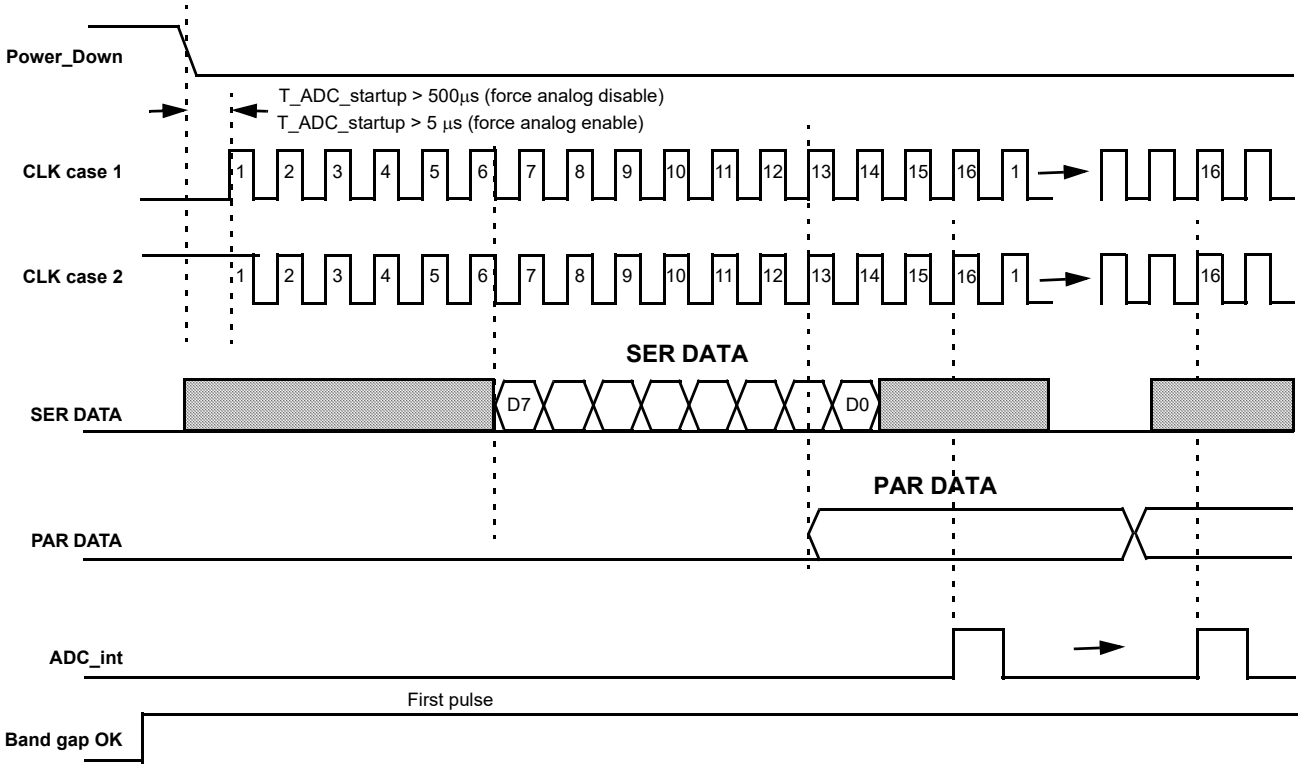


Figure 35. ADC Interrupt Output Timing Diagram

9.10 ADC Register Settings

Table 35. ADC Register Settings

Signal Function	Register Bit Address	Register Definition
ADC Speed Selection	<543:542>	00: Reserved 01: Reserved 10: 100 kHz 11: Reserved
ADC Vref Source Select	<546:545>	00: ADC V_{REF} 01: Reserved 10: 1/4 Vdd 11: None
ADC Wake Sleep Enable	<557>	0: Disable 1: Enable

Note: For PGA Register settings refer to Table 34.

10.0 8-bit Digital-to-Analog Converter (DAC)

There are two DACs in the SLG46140 (DAC0 and DAC1), they are 8-bit Digital to Analog Converters which operate at a maximum sampling speed of 100 ksps. The DAC's DNL is less than 1LSB and INL is less than 1LSB. DAC output to PIN resistance is 1 kΩ. Load resistance is recommended to be no less than 10 kΩ; load capacitance is recommended to be no more than 100 pF.

User controlled inputs and outputs of the DAC are listed below:

DAC0 Inputs:

- Registers
- 8LSBs SPI
- FSM0<7:0>
- FSM1<7:0>

DAC0 Outputs:

- PIN3
- PGA negative input (00: 0 V; FF: 1 V)
- ACMP0 negative input
- ACMP1 negative input

DAC1 Inputs:

- Registers
- 8LSBs SPI
- FSM0<7:0>
- FSM1<7:0>

DAC1 Outputs:

- ACMP0 negative input
- ACMP1 negative input

If a DAC0 output is connected to external Pin3 of SLG46140's, it is necessary to enable this external pin as analog input/output. reg <544>: 0 - DAC0 power off, 1 - DAC0 power on. reg <538>: 0 - DAC1 power off, 1 - DAC1 power on.

Please note that DAC1 is shared with ADC macrocell. Therefore it is impossible to use DAC1, when ADC is used. Also to activate DAC1, DAC0 must be enabled (reg <544> = 1 and reg <538> = 1). In addition, DAC0 is used as a part of pseudo-differential mode of PGA macrocell. Therefore DAC0 is not available when PGA is in pseudo-differential mode.

10.1 DAC0 Functional Diagram

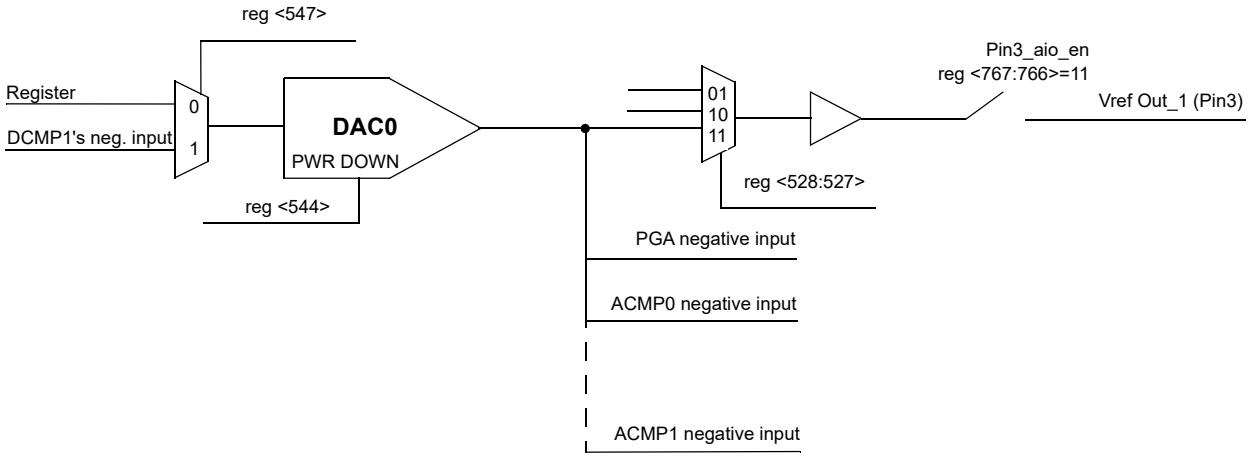


Figure 36. DAC0 Functional Diagram

10.2 DAC1 Functional Diagram

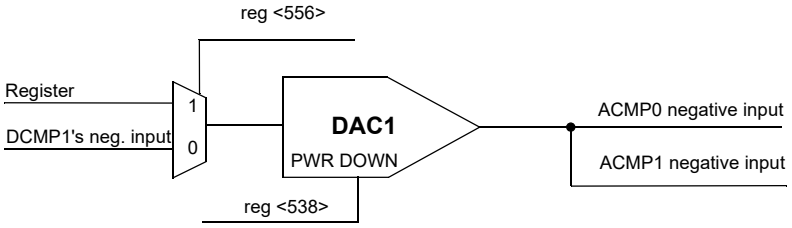


Figure 37. DAC1 Functional Diagram

10.3 DAC Register Settings

Table 36. DAC Register Settings

Register Bit Address	Signal Function	Register Definition
reg<529>	ADC native input from internal DAC0	0: disable 1: enable
reg<538>	DAC1 power on signal	0: power down 1: power on
reg<544>	DAC0 power on signal	0: power down 1: power on When DAC0 used only, need set this bit
reg<547>	DAC0 input selection	0: from register 1: from DCMP1's input
reg<555:548>	DAC0 8 bit register control	00: DAC0 output is 0 FF: DAC0's output is 1 V
reg<556>	DAC1 input selection	0: from DCMP1's Negative input 1: from register
reg<558>	Force ADC analog part on	0: disable 1: enable

11.0 Combinatorial Logic

Combinatorial logic is supported via nine Lookup Tables (LUTs) within the SLG46140. There are four 2-bit LUTs and four 3-bit LUTs. The device also includes eight Combination Function Macrocells that can be used as LUTs. For more details, please see Section *12.0 Combination Function Macrocells*.

Inputs/Outputs for the eight LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

11.1 2-Bit LUT

The four 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

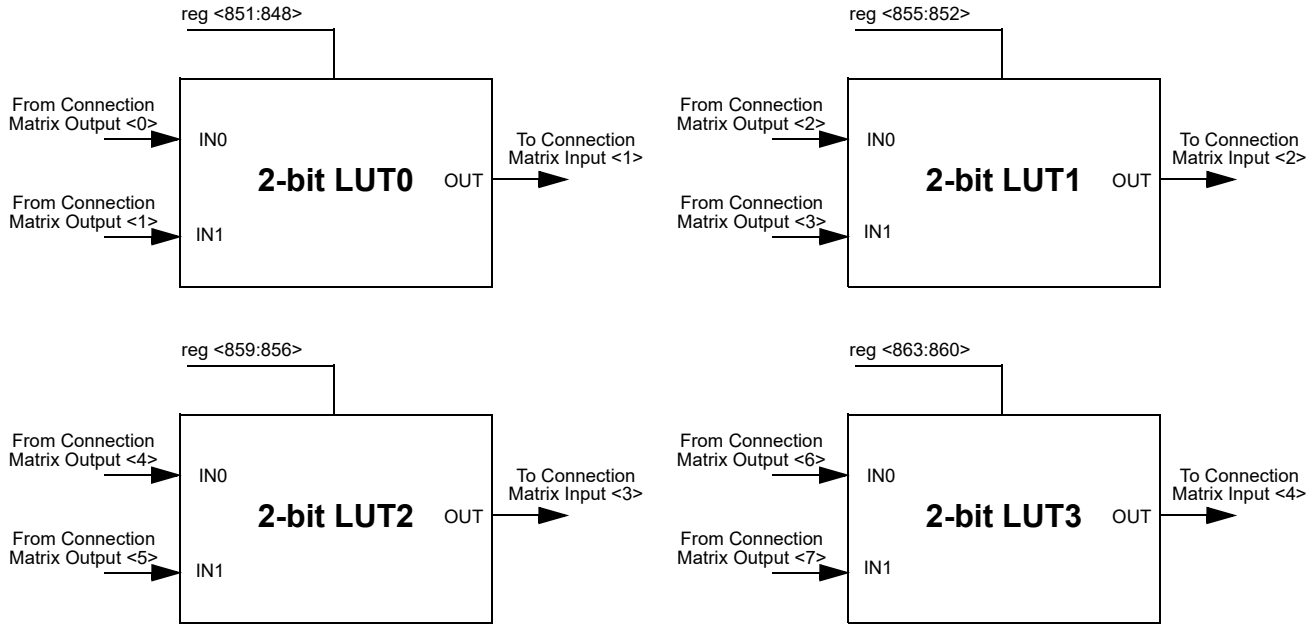


Figure 38. 2-bit LUTs

Table 37. 2-bit LUT0 Truth Table

IN1	IN0	OUT
0	0	reg <848>
0	1	reg <849>
1	0	reg <850>
1	1	reg <851>

Table 38. 2-bit LUT1 Truth Table

IN1	IN0	OUT
0	0	reg <852>
0	1	reg <853>
1	0	reg <854>
1	1	reg <855>

Table 39. 2-bit LUT2 Truth Table

IN1	IN0	OUT
0	0	reg <856>
0	1	reg <857>
1	0	reg <858>
1	1	reg <859>

Table 40. 2-bit LUT3 Truth Table

IN1	IN0	OUT
0	0	reg <860>
0	1	reg <861>
1	0	reg <862>
1	1	reg <863>

Table 41. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

11.2 3-Bit LUT

The seven 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

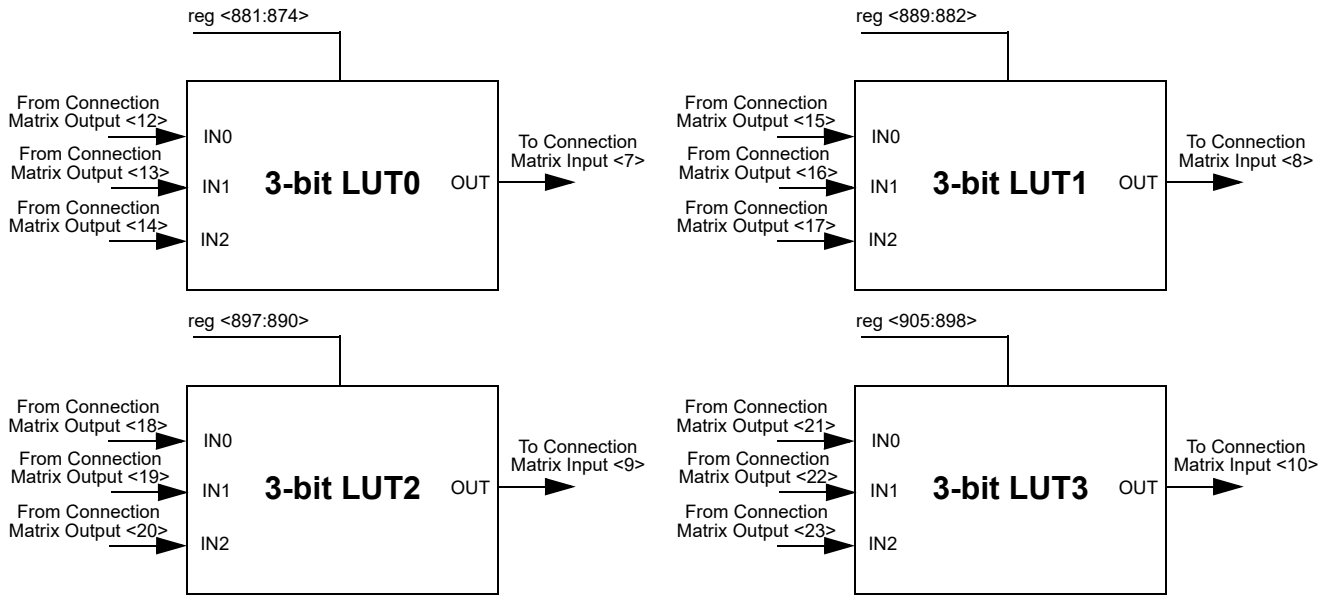


Figure 39. 3-bit LUTs

Table 42. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <874>
0	0	1	reg <875>
0	1	0	reg <876>
0	1	1	reg <877>
1	0	0	reg <878>
1	0	1	reg <879>
1	1	0	reg <880>
1	1	1	reg <881>

Table 43. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <882>
0	0	1	reg <883>
0	1	0	reg <884>
0	1	1	reg <885>
1	0	0	reg <886>
1	0	1	reg <887>
1	1	0	reg <888>
1	1	1	reg <889>

Table 44. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <890>
0	0	1	reg <891>
0	1	0	reg <892>
0	1	1	reg <893>
1	0	0	reg <894>
1	0	1	reg <895>
1	1	0	reg <896>
1	1	1	reg <897>

Table 45. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <898>
0	0	1	reg <899>
0	1	0	reg <900>
0	1	1	reg <901>
1	0	0	reg <902>
1	0	1	reg <903>
1	1	0	reg <904>
1	1	1	reg <905>

Table 46. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

12.0 Combination Function Macrocells

The SLG46140 has eight combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Two macrocells that can serve as either 2-bit LUTs or as D Flip Flops
- Two macrocells that can serve as either 3-bit LUTs or as D Flip Flops
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- One macrocell that can serve as either 3-bit LUT or as 8-Bit Counter / Delay
- One macrocell that can serve as either 4-bit LUT or 16-bit Pattern Generator
- One macrocell that can serve as either 4-bit LUT or as 14-Bit Counter / Delay

Inputs/Outputs for the eight combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

When used as a D Flip Flop / Latch, the source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state, and all have the option to connect both the Q and Q Bar outputs to the connection matrix. The macrocells DFF2 and DFF3 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

Latch: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

12.1 2-Bit LUT or D Flip Flop Macrocells

There are two macrocells that can serve as either 2-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip Flop, with the output going back to the connection matrix.

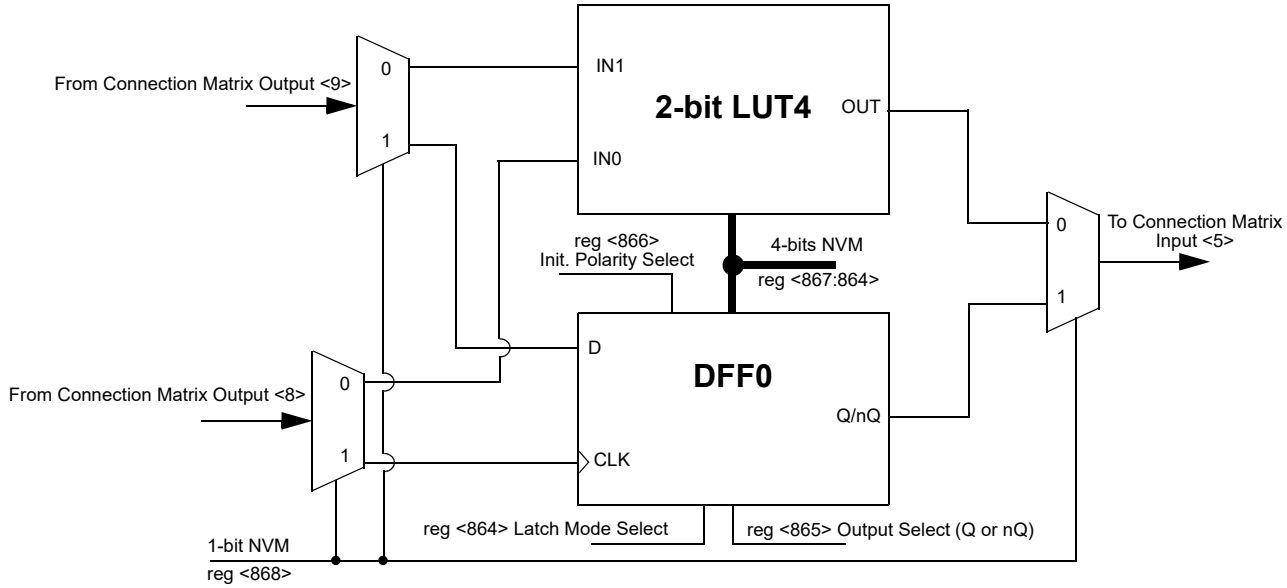


Figure 40. 2-bit LUT4 or DFF0

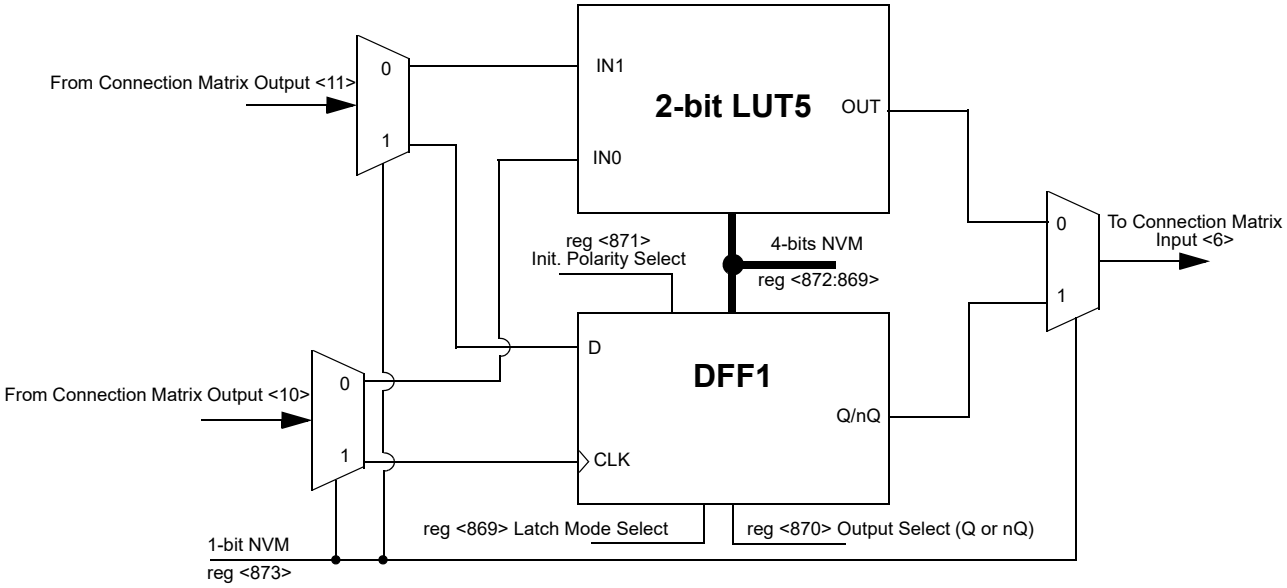


Figure 41. 2-bit LUT5 or DFF1

12.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Table 47. 2-bit LUT4 Truth Table.

IN1	IN0	OUT
0	0	reg <864>
0	1	reg <865>
1	0	reg <866>
1	1	reg <867>

Table 48. 2-bit LUT5 Truth Table.

IN1	IN0	OUT
0	0	reg <869>
0	1	reg <870>
1	0	reg <871>
1	1	reg <872>

12.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 49. LUT2_4 or DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF0 or Latch Select	<864>	0: DFF function 1: Latch function
DFF0 Output Select	<865>	0: Q output 1: nQ output
DFF0 Initial Polarity Select	<866>	0: Low 1: High
LUT2_4 or DFF0 Select	<868>	0: LUT2_4 1: DFF0

Table 50. LUT2_5 or DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF1 or Latch Select	<869>	0: DFF function 1: Latch function
DFF1 Output Select	<870>	0: Q output 1: nQ output
DFF1 Initial Polarity Select	<871>	0: Low 1: High
LUT2_5 or DFF1 Select	<873>	0: LUT2_5 1: DFF1

12.2 3-Bit LUT or D Flip Flop with Set/Reset Macrocells

There are two macrocells that can serve as either 3-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (rRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix.

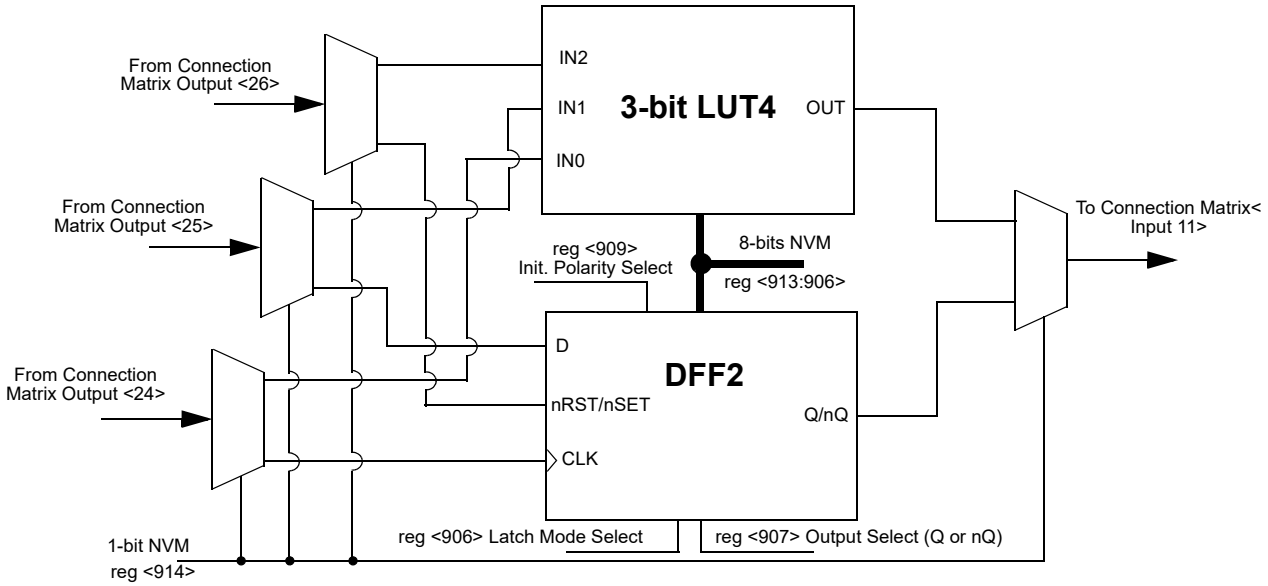


Figure 42. 3-bit LUT4 or DFF2

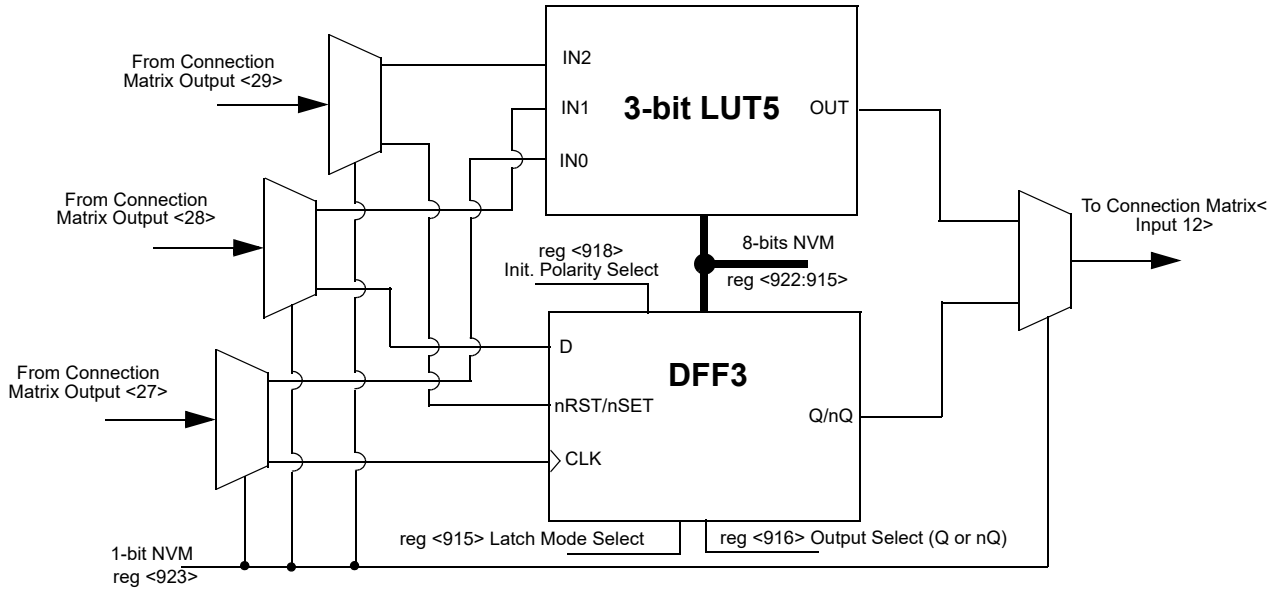


Figure 43. 3-bit LUT5 or DFF3

12.2.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

Table 51. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <906>
0	0	1	reg <907>
0	1	0	reg <908>
0	1	1	reg <909>
1	0	0	reg <910>
1	0	1	reg <911>
1	1	0	reg <912>
1	1	1	reg <913>

Table 52. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <916>
0	0	1	reg <917>
0	1	0	reg <918>
0	1	1	reg <919>
1	0	0	reg <920>
1	0	1	reg <921>
1	1	0	reg <922>
1	1	1	reg <923>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT4 is defined by reg<906:913>

3-Bit LUT5 is defined by reg<916:923>

12.2.2 3-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 53. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF2 or Latch Select	reg<906>	0: DFF function 1: Latch function
DFF2 Output Select	reg<907>	0: Q output 1: nQ output
DFF2 nRST/nSET Select	reg<908>	1: nSET from matrix out 0: nRST from matrix out
DFF2 Initial Polarity Select	reg<909>	0: Low 1: High
LUT3_4 or DFF2 Select	reg<914>	0: LUT3_4 1: DFF2

Table 54. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF3 or Latch Select	reg<915>	0: DFF function 1: Latch function
DFF3 Output Select	reg<916>	0: Q output 1: nQ output
DFF3 nRST/nSET Select	reg<917>	1: nSET from matrix out 0: nRST from matrix out
DFF3 Initial Polarity Select	reg<918>	0: Low 1: High
LUT3_5 or DFF3 Select	reg<923>	0: LUT3_5 1: DFF3

12.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three input signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (OUT2) is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by reg <753:750> for OUT0 and reg <757:754> for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46140 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46140). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

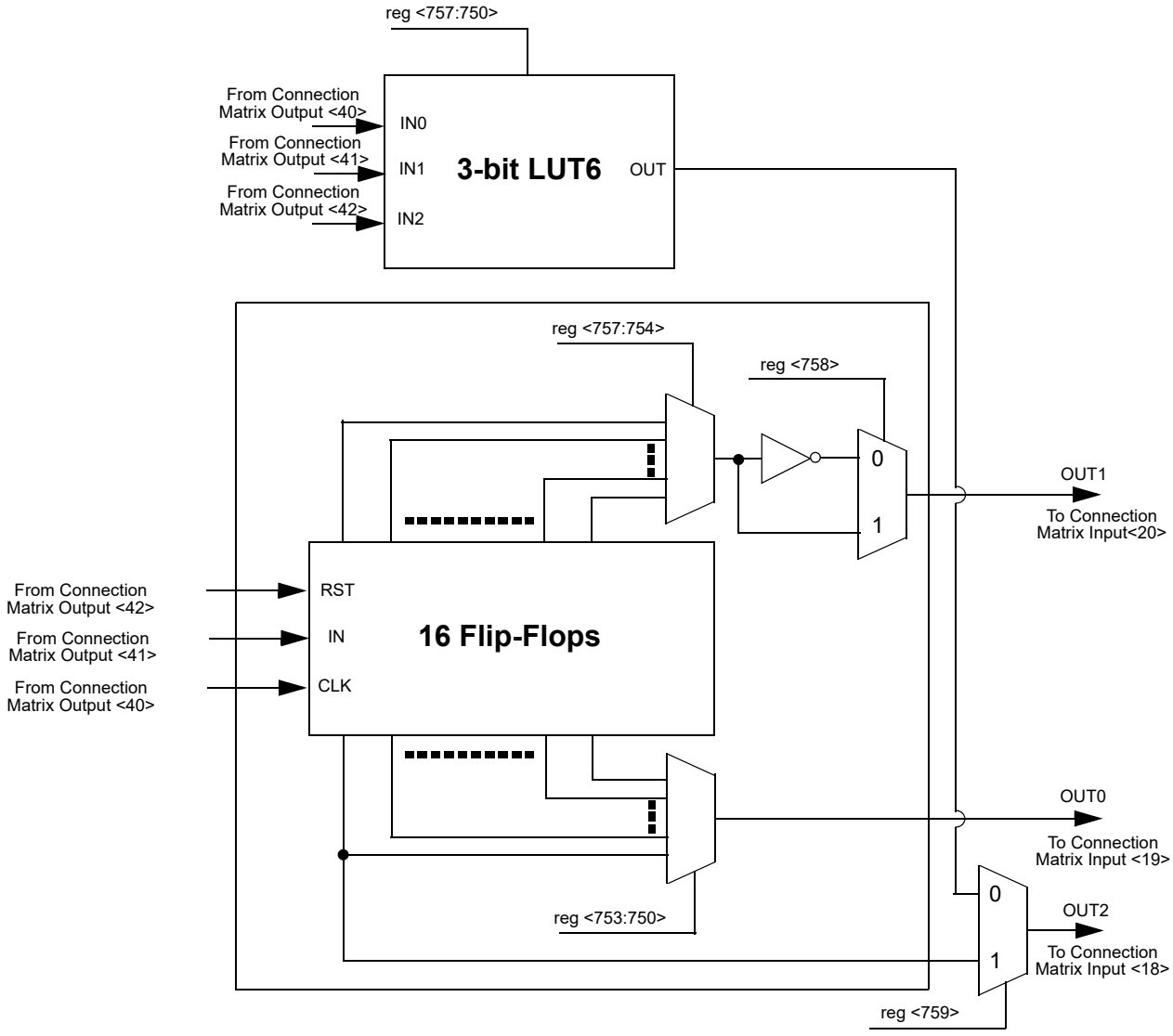


Figure 44. 3-bit LUT6 or Pipe Delay

12.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 55. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <750>
0	0	1	reg <751>
0	1	0	reg <752>
0	1	1	reg <753>
1	0	0	reg <754>
1	0	1	reg <755>
1	1	0	reg <756>
1	1	1	reg <757>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT6 is defined by reg<757:750>

12.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 56. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 select	reg<753:750>	
OUT1 select	reg<757:754>	
Pipe delay OUT1 Polarity Select Bit	reg<758>	0: Non-inverted 1: Inverted
LUT3_6 or Pipe Delay Output Select	reg<759>	0: LUT3_6 1: 1 Pipe Delay Output

12.4 3-bit LUT or 8-Bit Counter / Delay Macrocells

There is one macrocell that can serve as either a 3-bit LUT or as a Counter / Delay. When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delay function, three input signals from the connection matrix go to the Delay Input (DLY In), Up and Keep of the counter/delay, with the output going back to the connection matrix. It is possible to reverse counting of the CNT (by default, CNT is counting down) using UP input. Also, it is possible to stop and resume counting using KEEP input.

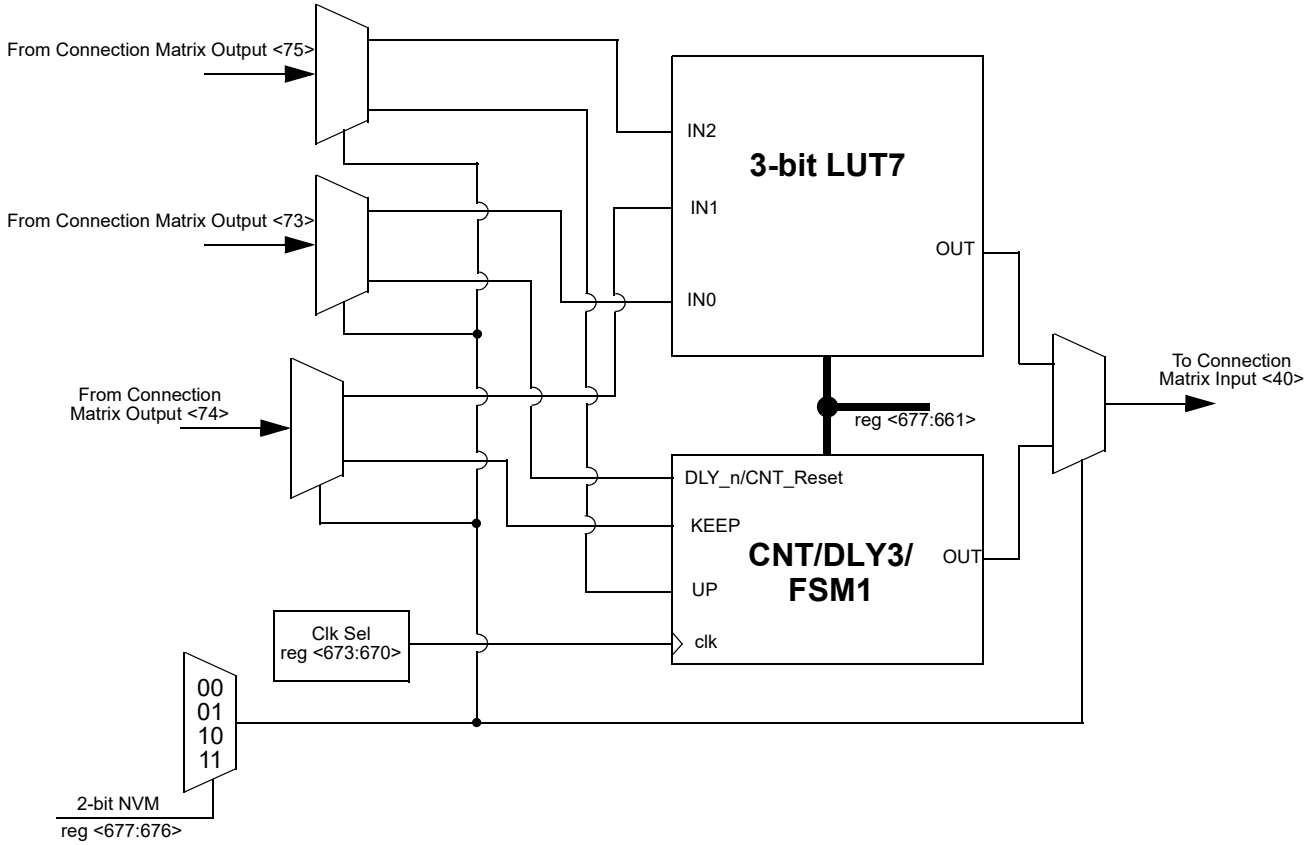


Figure 45. 3-bit LUT7 or CNT/DLY3/FSM1

12.4.1 3-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 3-Bit LUT

Table 57. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <661>
0	0	1	reg <662>
0	1	0	reg <663>
0	1	1	reg <664>
1	0	0	reg <665>
1	0	1	reg <666>
1	1	0	reg <667>
1	1	1	reg <668>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT7 is defined by reg<668:661>

12.4.2 3-Bit LUT or as 8-Bit Counter / Delay Register Settings

Table 58. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay/FSM Control Data	reg <668:661>	1 – 256 (delay time = (counter control data +2.5) /freq)
Counter/delay/FSMQ mode	reg <669>	0: Reset to 0s 1: Set to Data
Counter/delay/FSM Clock Source Select	reg <673:670>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END2 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
Delay Mode Select or asynchronous counter reset	reg <675:674>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset Delay) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
Counter/delay/FSM or LUT3_7 Macrocell Function Select	reg <677:676>	00: Delay mode 01: Counter/FSM mode 10: Edge Detect mode 11: LUT3_7

Table 58. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
FSM Input Data Source Select	reg <679:678>	00: 8 bits counter data 01: 8bits ADC data 10: no Data 11: 8MSBs SPI parallel data

12.5 4-bit LUT or Programmable Pattern Generator (PGEN)

The SLG46140 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGEN).

When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix 0 and produce a single output, which goes back into the connection matrix 0. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.See *Figure 47.*

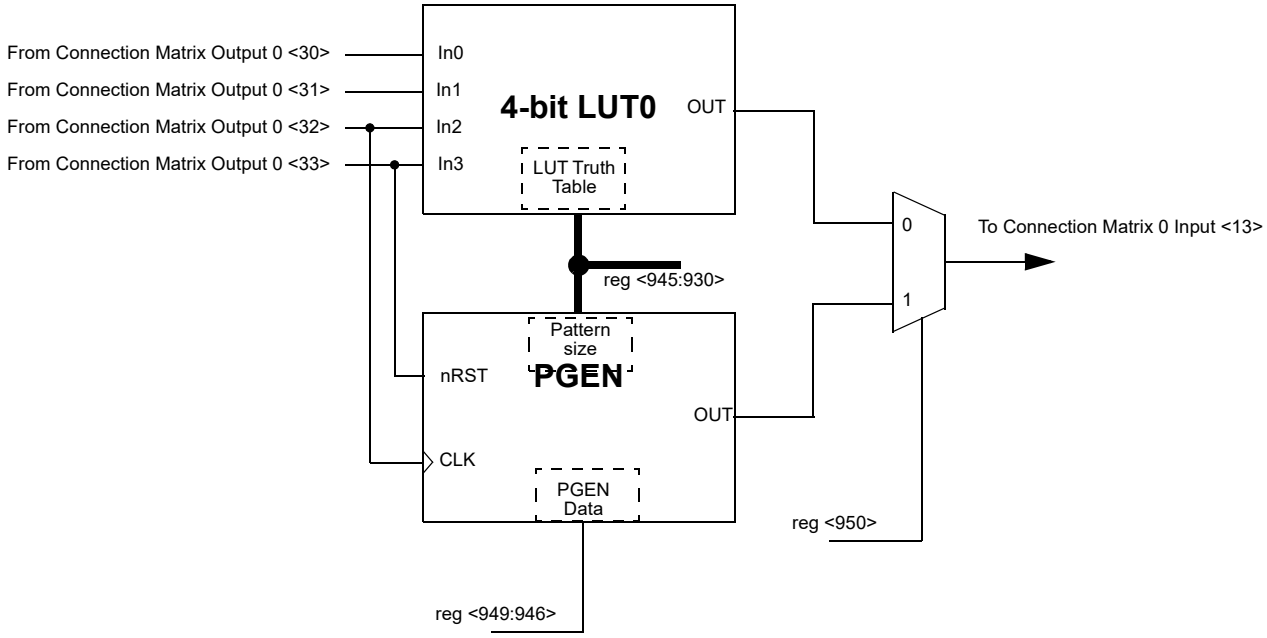


Figure 46. 4-bit LUT0 or PGEN

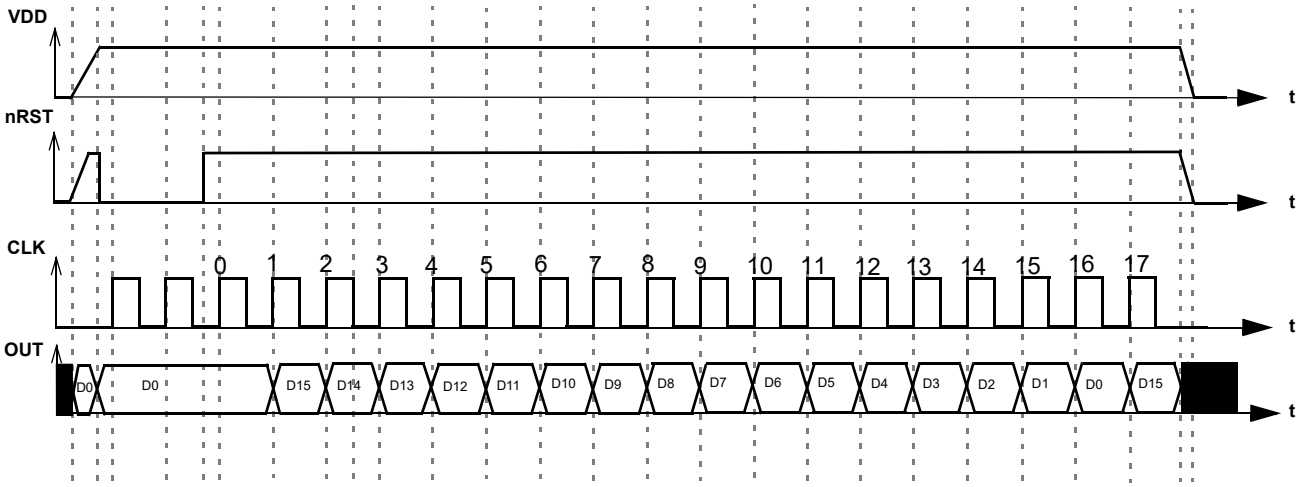


Figure 47. PGEN Timing Diagram

When this macrocell is used to implement LUT function, the 4-bit LUT uses a 16-bit register signal to define its output function;

4-Bit LUT0 is defined by reg<945:930>.

Table 59. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <930>
0	0	0	1	reg <931>
0	0	1	0	reg <932>
0	0	1	1	reg <933>
0	1	0	0	reg <934>
0	1	0	1	reg <935>
0	1	1	0	reg <936>
0	1	1	1	reg <937>
1	0	0	0	reg <938>
1	0	0	1	reg <939>
1	0	1	0	reg <940>
1	0	1	1	reg <941>
1	1	0	0	reg <942>
1	1	0	1	reg <943>
1	1	1	0	reg <944>
1	1	1	1	reg <945>

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by reg<945:930>

Table 60. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

12.5.1 4-Bit LUT0 or Programmable Pattern Generator Register Settings

Table 61. 4-Bit LUT0 or Programmable Pattern Generator Register Settings

Signal Function	Register Bit Address	Register Definition
LUT4_0 & PGEN data	<945:930>	Data
4-bit counter data in PGEN	<949:946>	Data
PGEN Enable Signal	<950>	0: LUT4 Function 1: PGEN Function

12.6 4-Bit LUT or 14-Bit Counter / Delay Macrocells

There is one macrocell that can serve as a 4-bit LUT or as Counter / Delay. When used to implement LUT functions, the 4-bit LUTs each take in four input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement 14-Bit Counter / Delays function, two of the four input signals from the connection matrix go to the external clock (ext_CLK) and reset (DLY_In/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

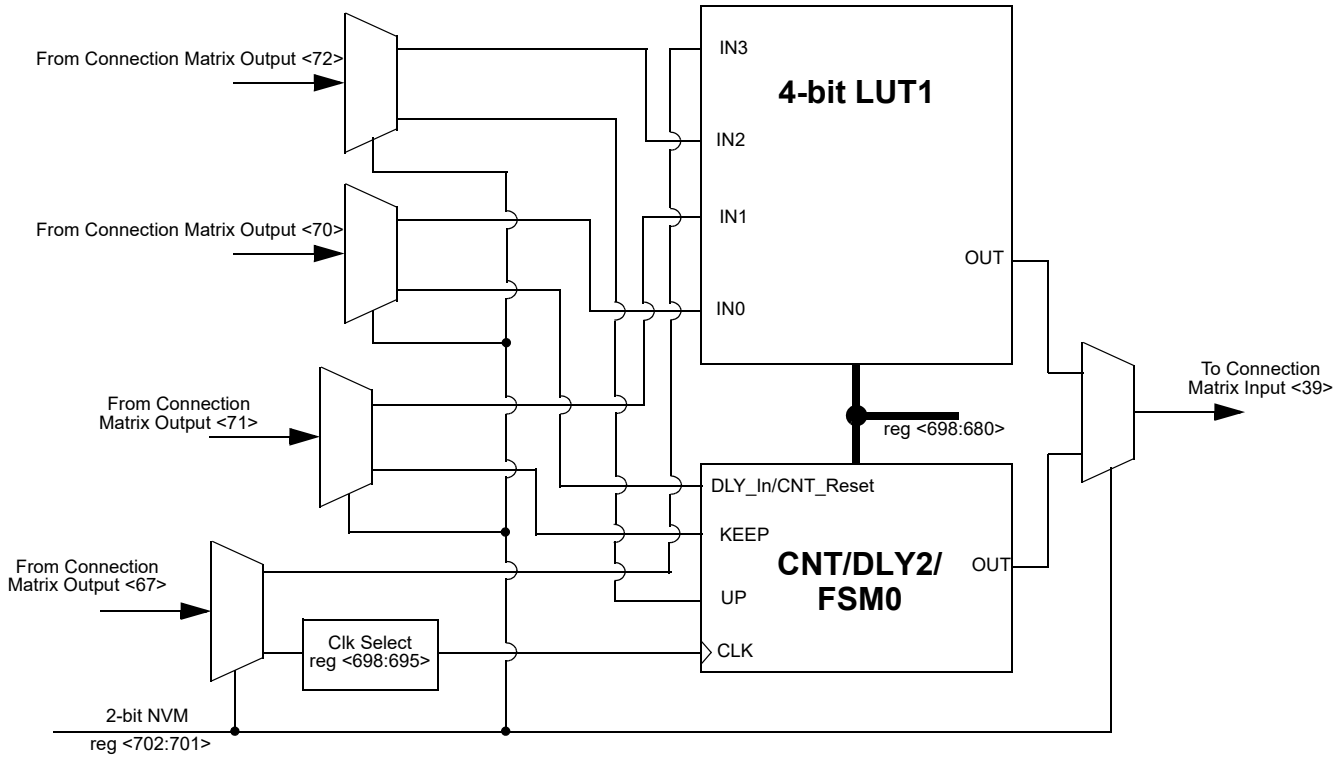


Figure 48. 4-bit LUT1 or CNT/DLY2/FSM0

12.6.1 4-Bit LUT or 14-Bit Counter / Delay Macrocell Used as 4-Bit LUT

Table 62. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <680>
0	0	0	1	reg <681>
0	0	1	0	reg <682>
0	0	1	1	reg <683>
0	1	0	0	reg <684>
0	1	0	1	reg <685>
0	1	1	0	reg <686>
0	1	1	1	reg <687>
1	0	0	0	reg <688>
1	0	0	1	reg <689>
1	0	1	0	reg <690>
1	0	1	1	reg <691>
1	1	0	0	reg <692>
1	1	0	1	reg <693>
1	1	1	0	reg <694>
1	1	1	1	reg <695>

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT1 is defined by reg<695:680>

Table 63. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

12.6.2 4-Bit LUT or as 14-Bit Counter / Delay Register Settings

Table 64. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT4_1 data [bits 13:0] (if reg<702:701>=11) or DLY2/CNT2/FSM0 data	reg<693:680>	data
LUT4_1 data [bit 14] (if reg<702:701>=11) or CNT2/FSM0's Q are set to 1s or reset 0s selection	reg<694>	0: reset to 0s 1: set to Data.
Counter/delay2 Clock Source Select	reg<698:695>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END1 0110: Matrix0_out67 0111: Matrix0_out67 divide by 8 1000: CK_RINGOSC 1001: Matrix0_out80(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
Delay2 Edge Mode Select	reg<700:699>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY2 Macrocell Function Select	reg<702:701>	00: DLY 01: CNT/FSM 10: edge detect 11: 4bit LUT4_1
FSM0 Input Data Source Select	reg<704:703>	00: 8 bits NVM data 01: 8 bits ADC data 10: 0 11: 8MSBs SPI parallel data.

13.0 Analog Comparators (ACMP)

There are two Analog Comparator (ACMP) macrocells in the SLG46140. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMPx_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on always on, always off, or power cycled based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

PWR UP = 1 => ACMP is powered up

PWR UP = 0 => ACMP is powered down

During ACMP power up, its output will remain low, and then becomes valid 4.42 ms (max) after ACMP power up signal goes high, see *Figure 49*. If VDD is greater or equal to 2.7 V, it is possible to decrease turn-on time by setting the BG ok delay to 100 µs, see *Figure 50*. The ACMP cells have an input "Low bandwidth" signal selection, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the VDD signal.

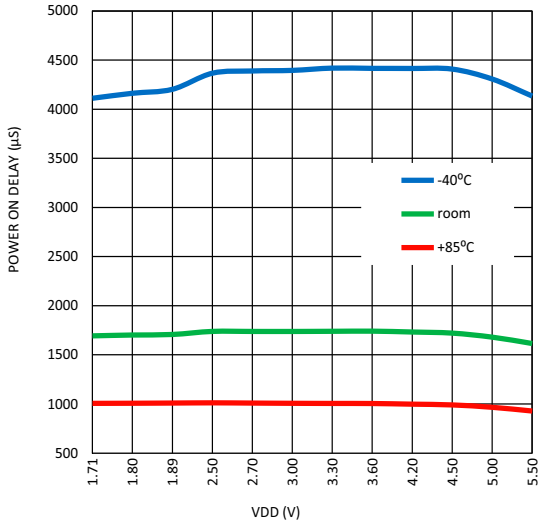


Figure 49. Maximum Power On Delay vs. VDD, BG = 550 µs, Regulator and Charge Pump set to automatic ON/OFF

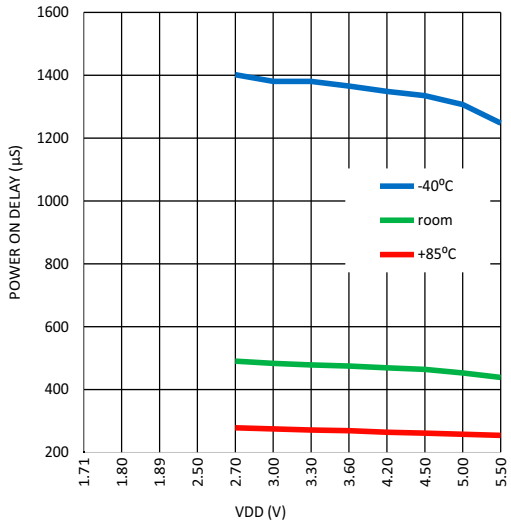


Figure 50. Maximum Power On Delay vs. VDD, BG = 100 µs, Regulator and Charge Pump set to automatic ON/OFF

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 KΩ (typ.) resistors, see *Table 65*. For gain divider accuracy refer to *Table 66.* IN- voltage range: 0 - 1.2 V. Can use Vref selection VDD/4 and VDD/3 to maintain this input range.

Input bias current < 1 nA (typ).

Table 65. Gain Divider Input Resistance (typical)

Gain	x1	x0.5	x0.33	x0.25
Input Resistance	100 GΩ	1 MΩ	0.75 MΩ	1 MΩ

Table 66. Gain Divider Accuracy

Gain	x0.5	x0.33	x0.25
Accuracy	-0.83% +0.73%	-0.83% +0.96%	-0.78% +1.14%

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only. While 25 mV hysteresis option can be used with both internal and external voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be Vref (high threshold) and Vref - hysteresis (low threshold). The ACMP output will retain its previous value, if the input voltage is within thresholds window (between Vref and Vref - hysteresis). Please note for the 25 mV hysteresis option threshold levels will be Vref + hysteresis/2 (high threshold) and Vref - hysteresis/2 (low threshold).

Note: Any ACMP powered on enables the Bandgap internal circuit as well. An analog voltage will appear on Vref even when the Force Bandgap option is set as Disabled.

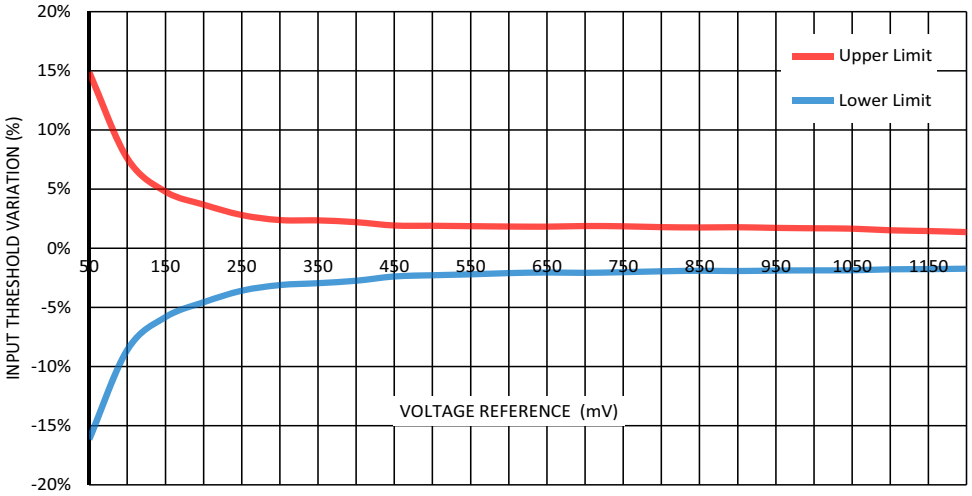


Figure 51. Input Threshold Variation (including Vref variation, ACMP offset) vs. Voltage reference at T=(-40 … +85)°C, LBW Mode - Disable, Vhys=0 mV.

Note: when VDD < 1.8V voltage reference should not exceed 1100 mV.

Table 67. Built-in Hysteresis Tolerance.

Vhys (mV)	VDD=1.7 V		VDD=3.3 V		VDD=5.5 V	
	min (mV)	max (mV)	min (mV)	max (mV)	min (mV)	max (mV)
25	7.8	34.0	7.9	34.1	4.9	34.2
50	43.8	55.3	43.8	55.2	43.8	55.6
200	193.4	206.3	188.3	207.6	189.7	207.9

13.1 ACMP0 Block Diagram

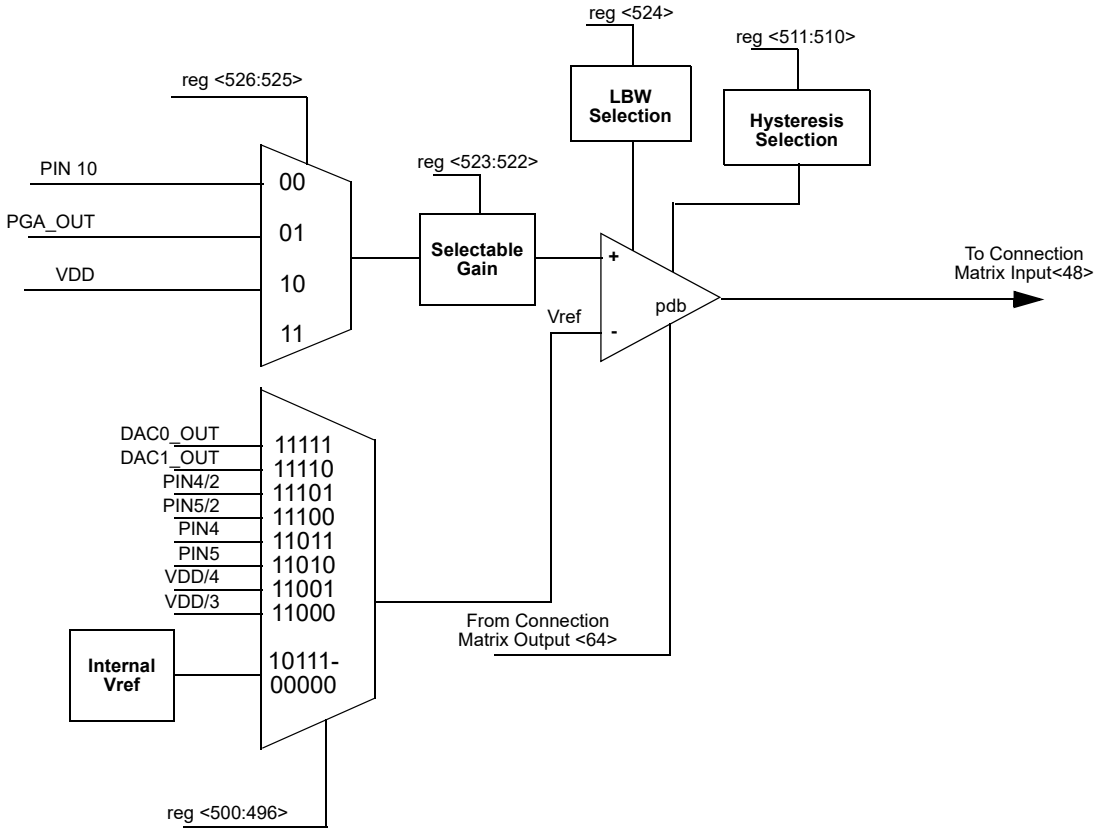


Figure 52. ACMP0 Block Diagram

13.2 ACMP0 Register Settings

Table 68. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 In Voltage Select	reg<500:496>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: vref_ext_acmp1 11011: vref_ext_acmp0 11100: vref_ext_acmp1 / 2 11101: vref_ext_acmp0 / 2 11100: DAC1_out 11111: DAC0_out
ACMP0 Hysteresis Enable	reg<511:510>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP0 Positive Input Divider	reg<523:522>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg<524>	1: On 0: Off
ACMP0 Positive Input Source Select	reg<526:525>	00: Pin10 input 01: ADC PGA out 10: VDD 11: None
ACMP0 input 100u Current Source Enable	reg<540>	0: Disable 1: Enable

13.3 ACMP1 Block Diagram

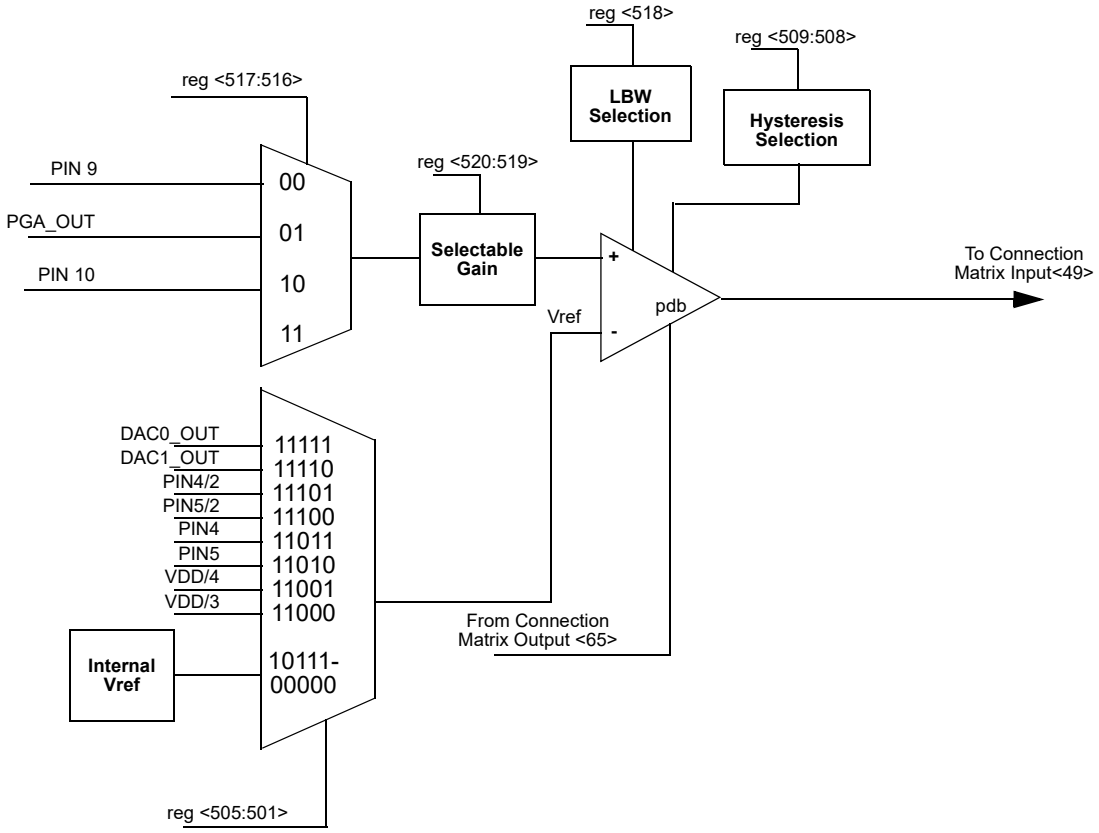


Figure 53. ACMP1 Block Diagram

13.4 ACMP1 Register Settings

Table 69. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 In Voltage Select	reg<505:501>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: vref_ext_acmp1 11011: vref_ext_acmp0 11100: vref_ext_acmp1 / 2 11101: vref_ext_acmp0 / 2 11100: DAC1_out 11111: DAC0_out
ACMP1 Hysteresis Enable	reg<509:508>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP1 Positive Input Source Select	reg<517:516>	00: Pin9 input 01: ADC PGA out 10: Pin10 input 11: None
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg<518>	0: Off 1: On
ACMP1 Positive Input Divider	reg<520:519>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP1 input 100u Current Source Enable	reg<541>	0: Disable 1: Enable

14.0 Digital Storage Elements (DFFs/Latches)

There are six Combination Function macrocells that can be used to implement D-Flip Flop or Latch functions. Please see Section *12.1 2-Bit LUT or D Flip Flop Macrocells* and Section *12.2 3-Bit LUT or D Flip Flop with Set/Reset Macrocells* for the description of this Combination Function macrocell.

14.1 Initial Polarity Operations

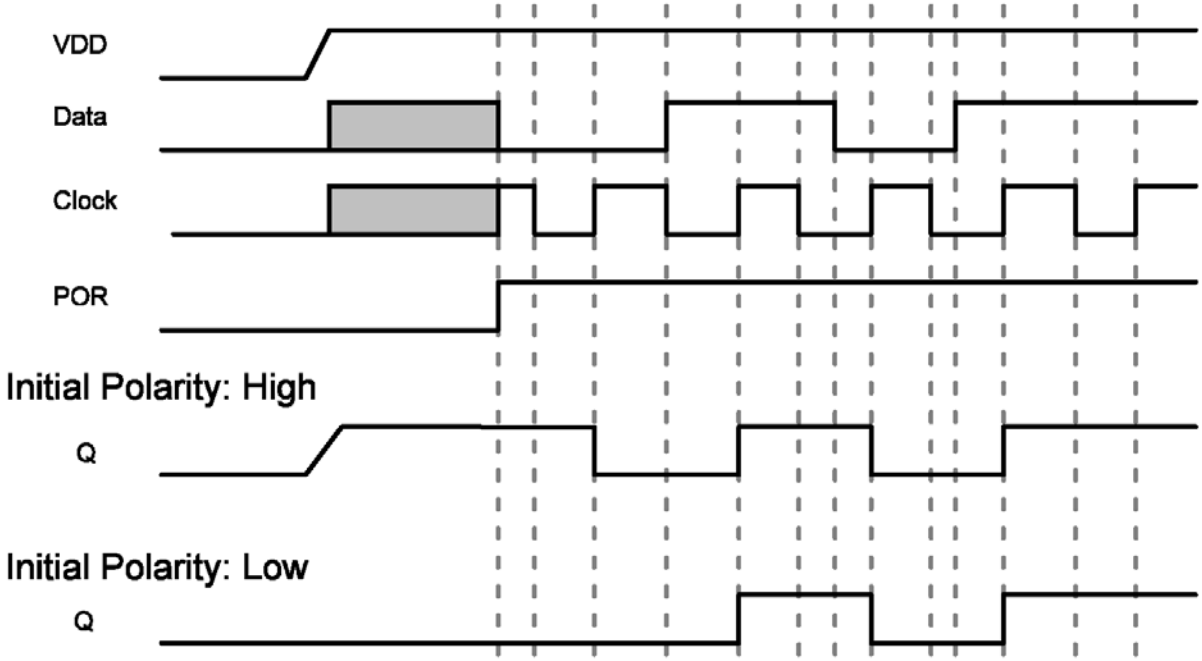


Figure 54. DFF Polarity Operations

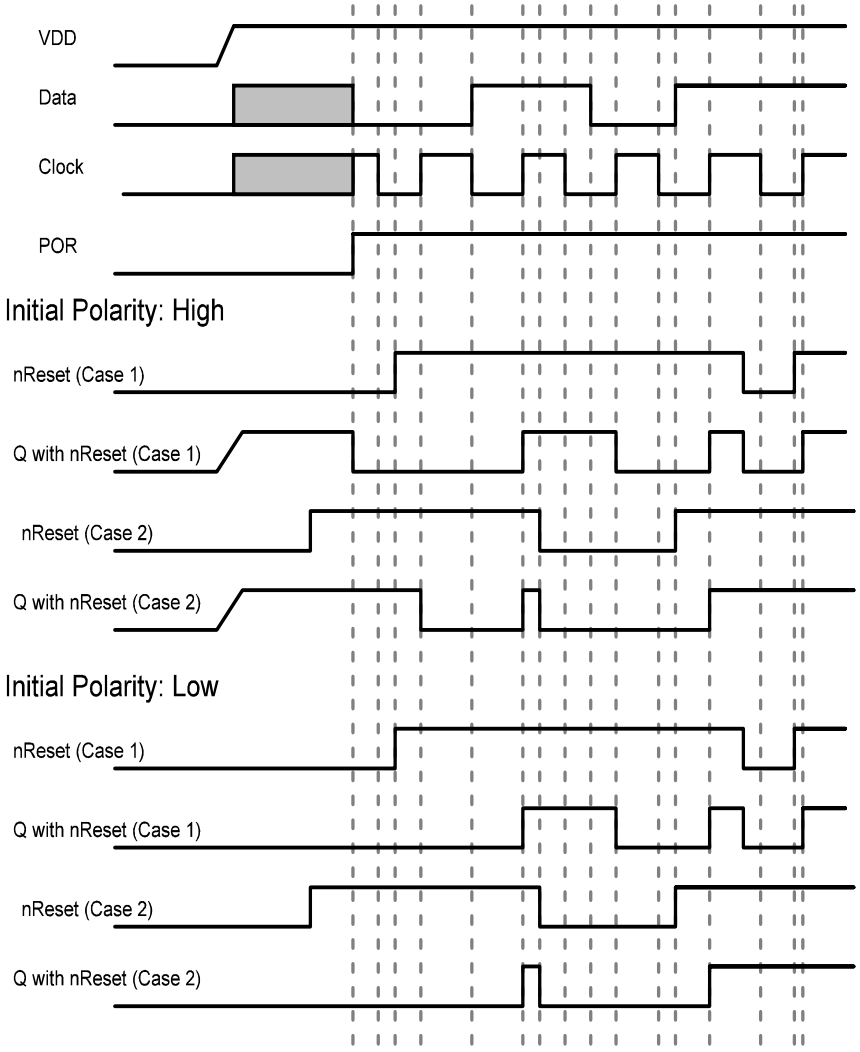


Figure 55. DFF Polarity Operations with nReset

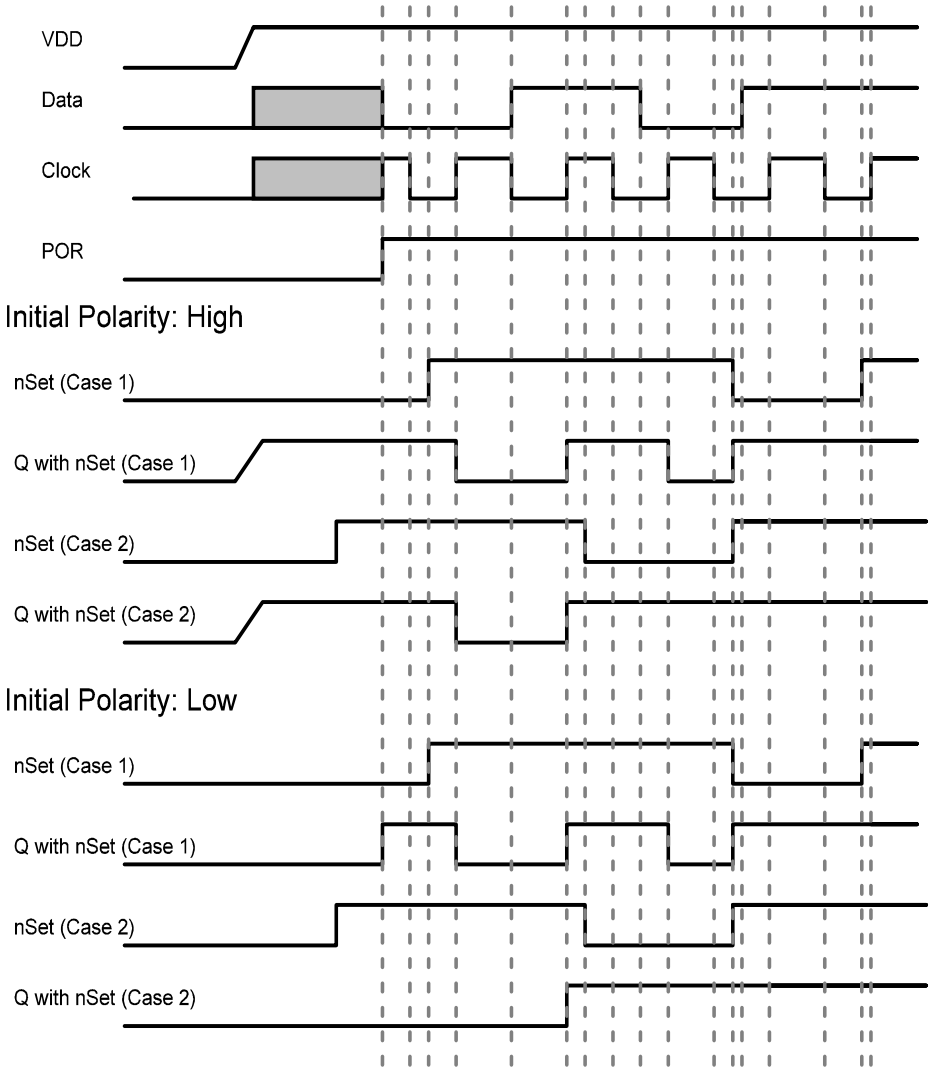


Figure 56. DFF Polarity Operations with nSet

15.0 Counters/Delay Generators (CNT/DLY)

There are two configurable counters/delay generators in the SLG46140. One of the counter/delay generators (CNT/DLY 0) is 14-bit, and the other counter/delay generator (CNT/DLY 1) is 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

One of the counter/delay generator macrocells (CNT/DLY 0) has two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. The other counter/delay generator macrocell (CNT/DLY 1) has one input from the connection matrix, which has a shared function of either a Delay Input or an external clock input.

The delay time and counter output equation is as follows:

Delay time = ((counter data + 1) + variable) / Clock
*Variable = (0 or 1) * period*
Counter period = (counter data + 1) / Clock

Note: variable can be negative, since OSC can operate while Delay input changes. In this case it might be possible that we will not see first period, if OSC rising edge appears immediately after input change.

Note that there are also two Combination Function Macrocells that can implement either 3-bit LUT or 8-bit counter / delay or 4-bit LUT or 14-bit counter / delay. For more information please see Section *12.4 3-bit LUT or 8-Bit Counter / Delay Macrocells* and *12.6 4-Bit LUT or 14-Bit Counter / Delay Macrocells*.

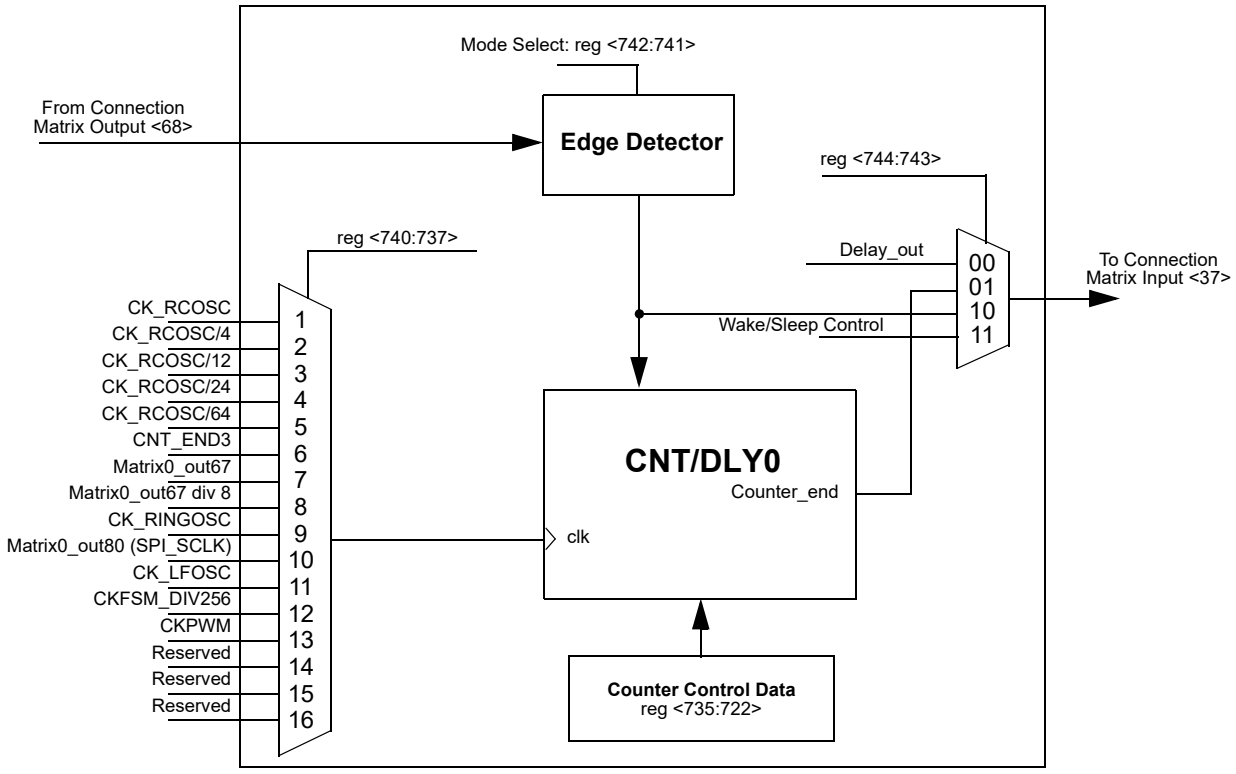


Figure 57. CNT/DLY0

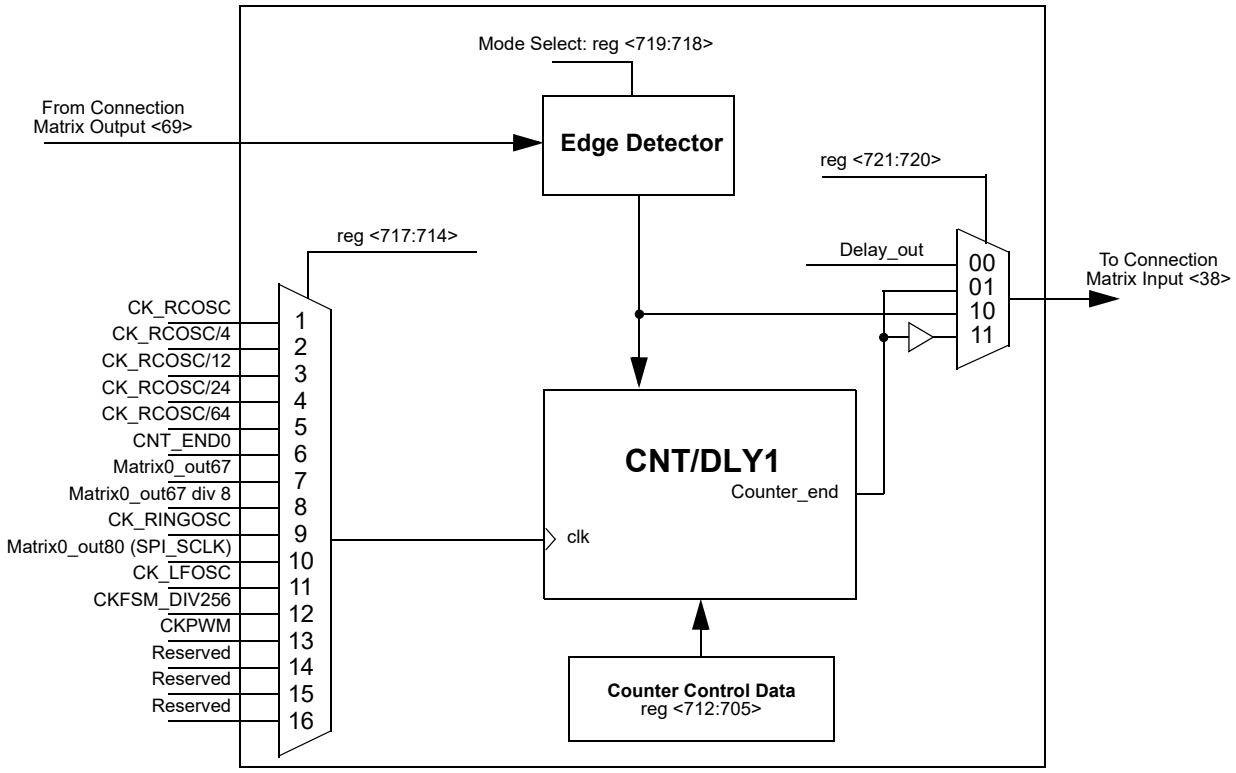


Figure 58. CNT/DLY1

15.1 CNT/DLY Timing Diagrams

15.1.1 Delay Mode (counter data: 3) CNT/DLY0...CNT/DLY9

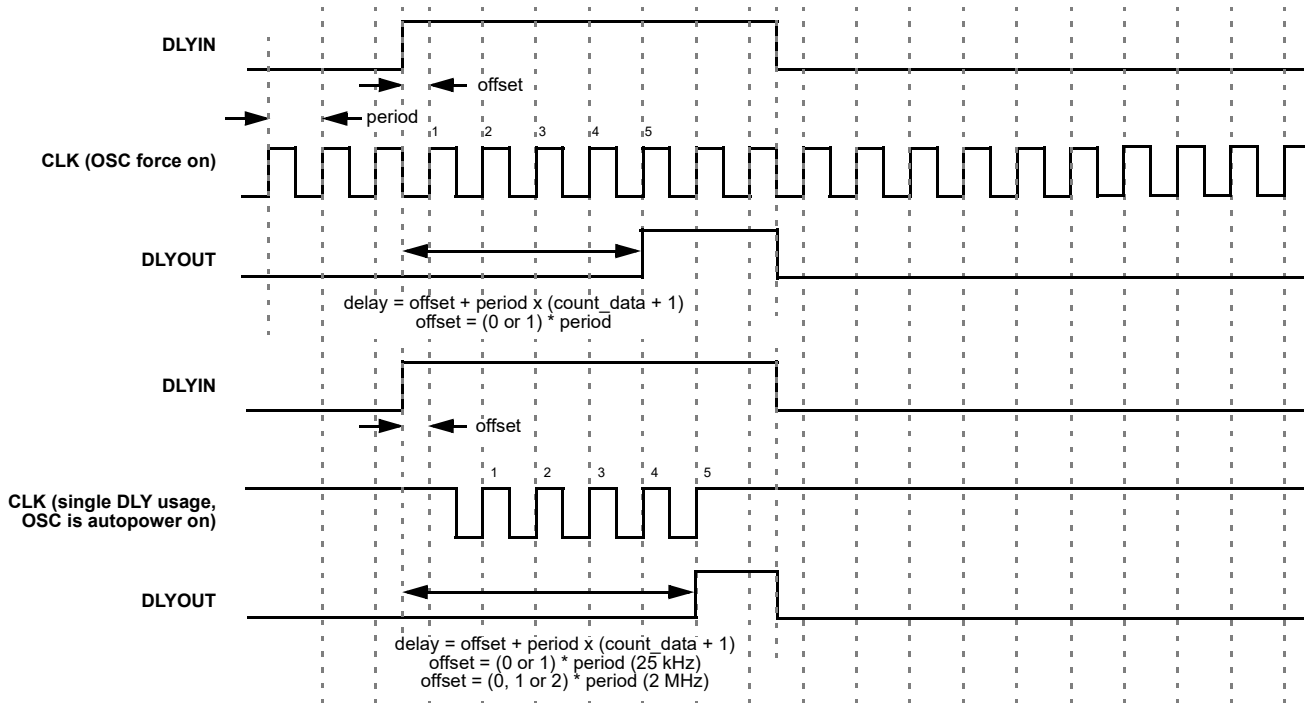


Figure 59. Timing (rising edge) for count data = 3

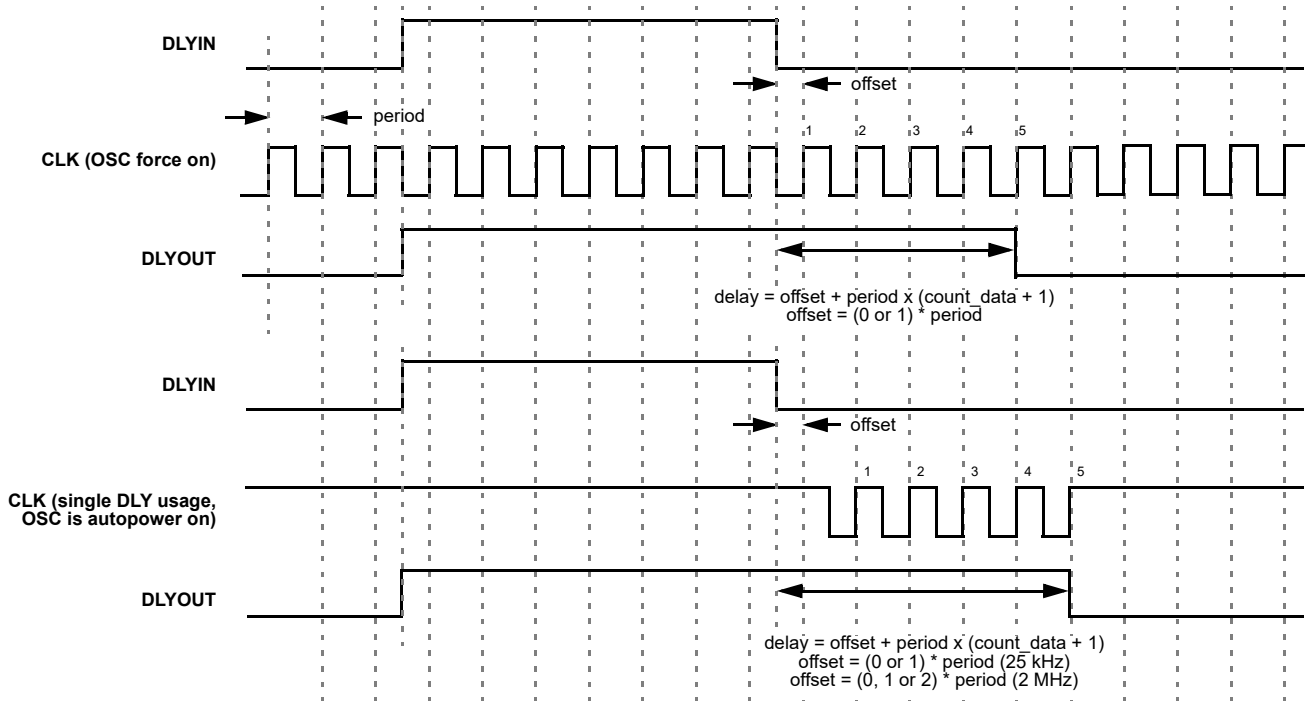


Figure 60. Timing (falling edge) for count data = 3

15.1.2 Counter Mode (counter data: 3) CNT/DLY0...CNT/DLY9

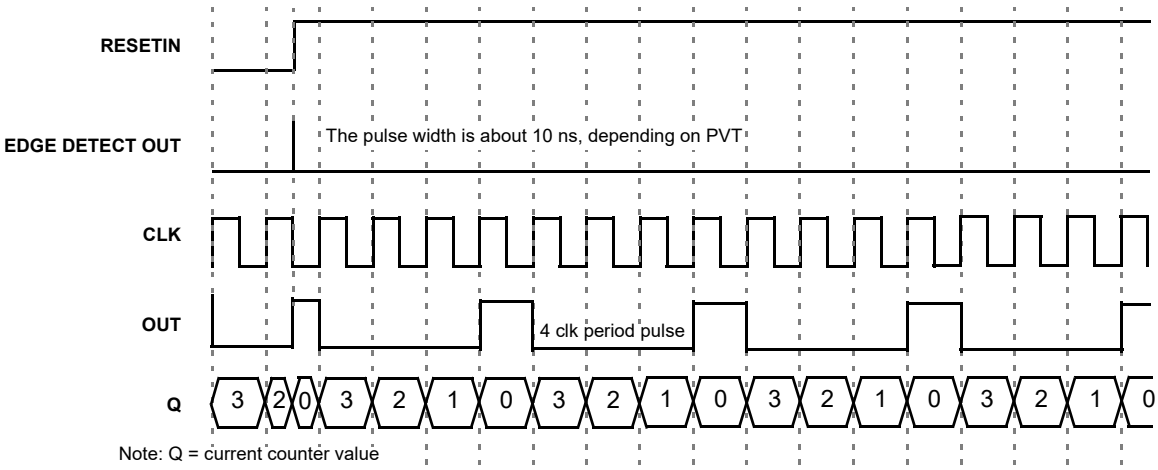


Figure 61. Timing (reset rising edge mode, oscillator is forced on) for count data = 3

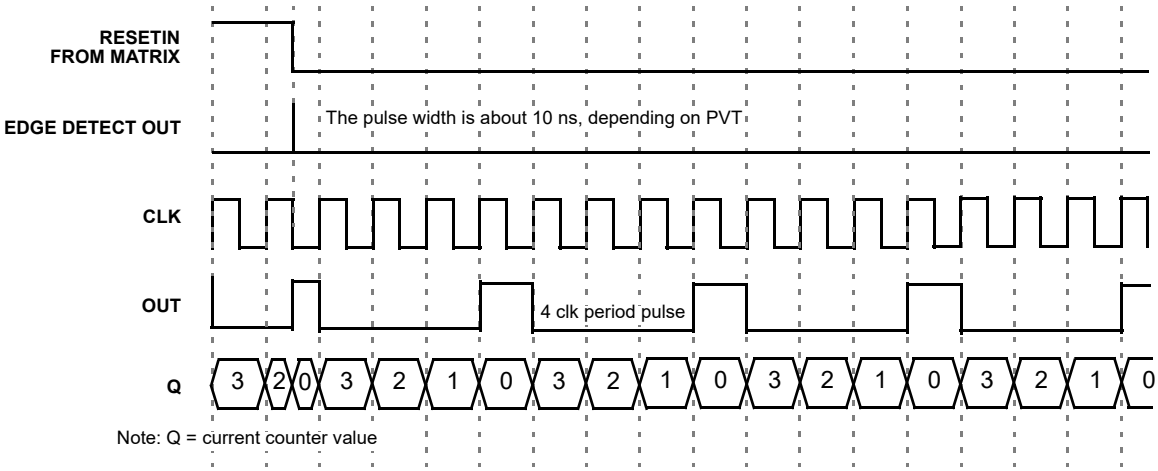


Figure 62. Timing (reset falling edge mode, oscillator is forced on) for count data = 3

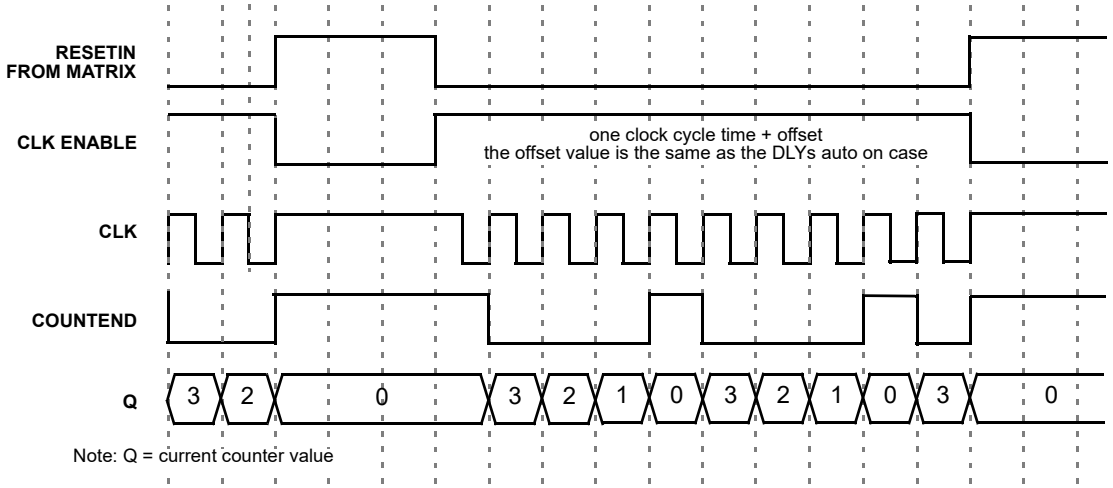


Figure 63. Timing (reset high level mode, oscillator is autopowered on (controlled by reset)) for count data = 3

15.1.3 CNT/FSM Mode CNT/DLY2, CNT/DLY4

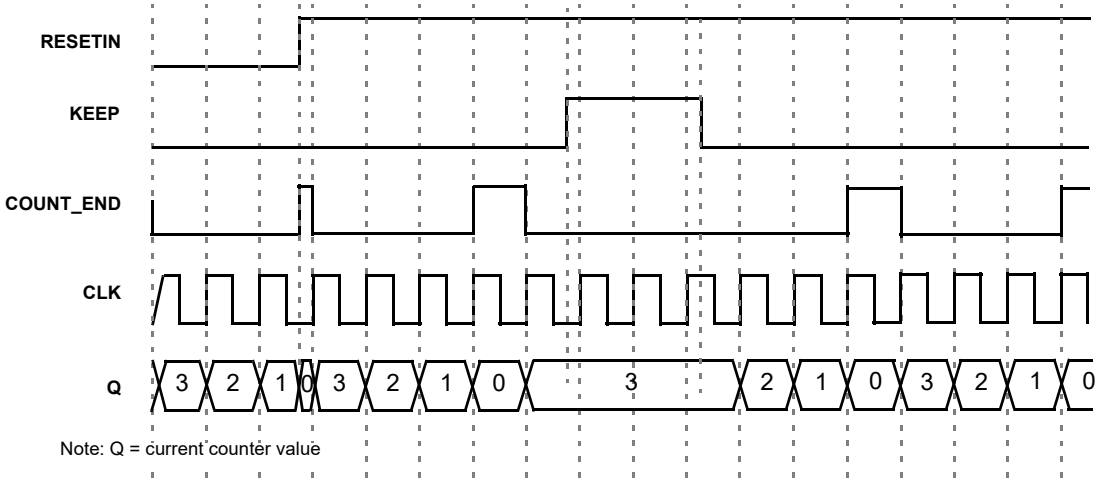


Figure 64. CNT/FSM Timing Diagram (reset rising edge mode, oscillator is forced on, UP=0) for counter data = 3

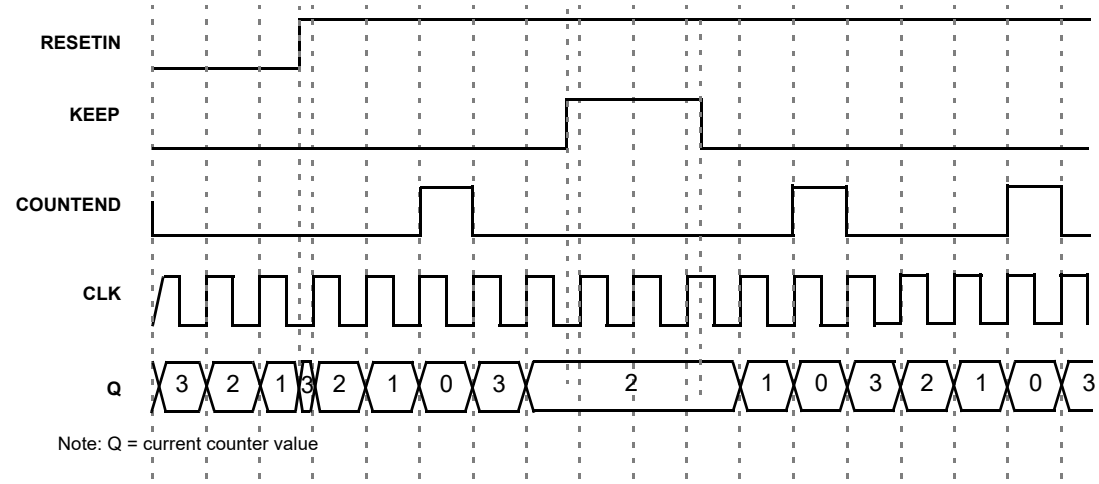


Figure 65. CNT/FSM Timing Diagram (set rising edge mode, oscillator is forced on, UP=0) for counter data = 3

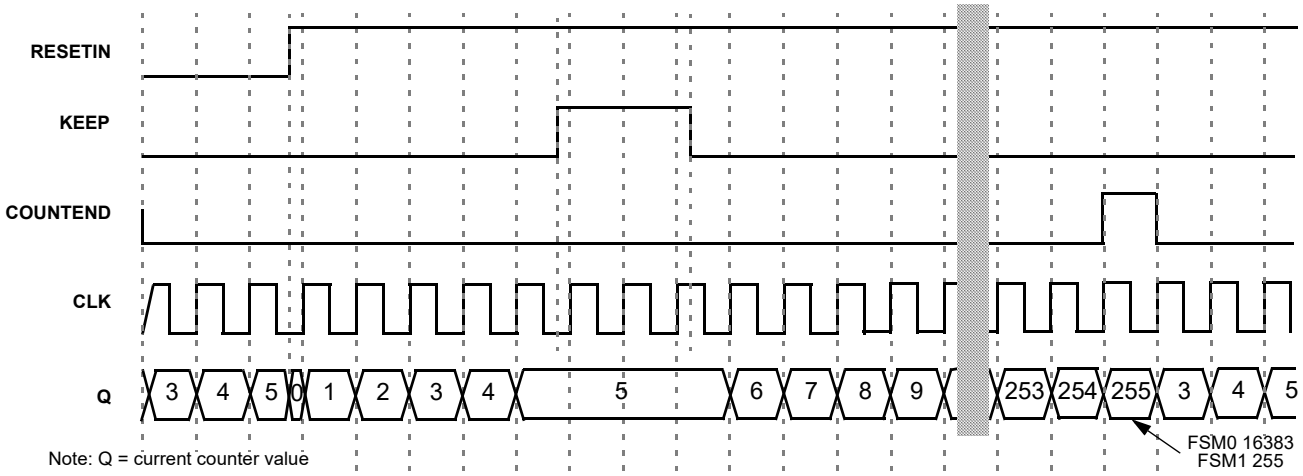


Figure 66. CNT/FSM Timing Diagram (reset rising edge mode, oscillator is forced on, UP=1) for counter data = 3

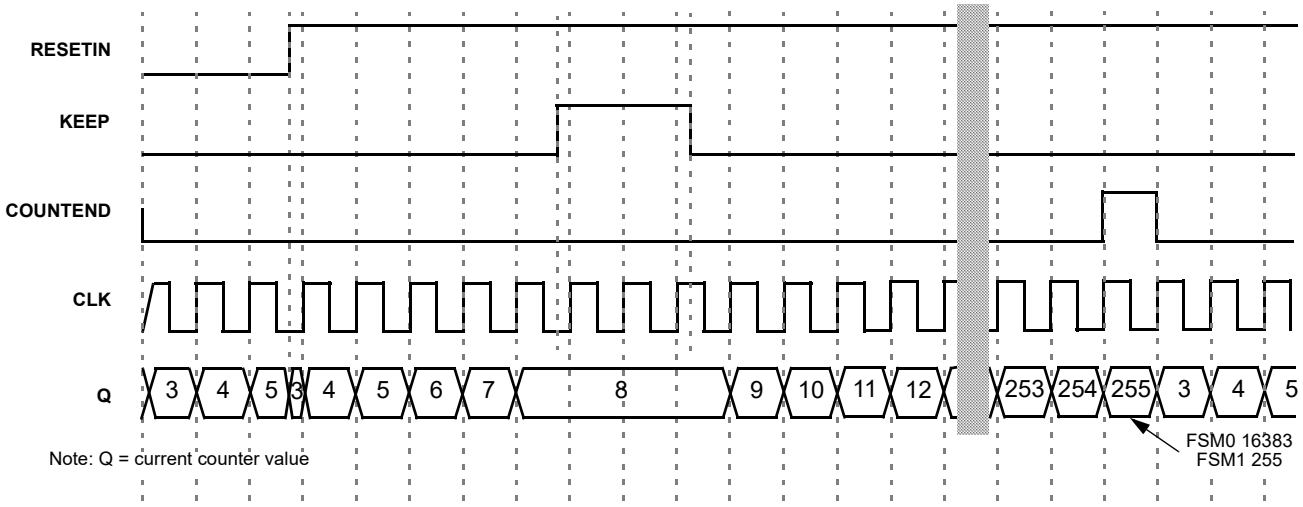


Figure 67. CNT/FSM Timing Diagram (set rising edge mode, oscillator is forced on, UP=1) for counter data = 3

15.2 CNT/DLY0 Register Settings

Table 70. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter0 Control Data/Delay0 Time Control	reg<735:722>	1-16384: (delay time = (counter control data +2) /freq)
Counter/Delay0 Clock Source Select	reg<740:737>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END3 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80 (SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
Delay0 Mode Select	reg<742:741>	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
Counter/Delay0 Macrocell Function Select	reg<744:743>	00: DLY 01: CNT/FSM 10: edge detect 11: wake sleep ratio control

15.3 CNT/DLY1 Register Settings

Table 71. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter1 Control Data/Delay1 Time Control	reg<712:705>	1-255: (delay time = (counter control data +2) /freq)
Counter/Delay1 Clock Source select	reg<717:714>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END0 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80 (SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
Delay1 Mode Select	reg<719:718>	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
Counter/Delay1 Macrocell Function Select	reg<721:720>	00: DLY 01: CNT/FSM 10: edge detect 11: CNT/FSM

15.4 CNT/DLY2 Register Settings

Table 72. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter2 Control Data/Delay2 Time Control	reg<693:680>	1-16384: (delay time = (counter control data +2) /freq)
Counter/Delay2 Clock Source Select	reg<698:695>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END1 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80 (SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
Delay2 Mode Select	reg<700:699>	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
Counter/Delay2 Macrocell Function Select	reg<702:701>	00: DLY 01: CNT/FSM 10: edge detect 11: 4bit LUT4_1

15.5 CNT/DLY3 Register Settings

Table 73. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter3 Control Data/Delay3 Time Control	reg<668:661>	1-255: (delay time = (counter control data +2) /freq)
Counter/Delay3 Clock Source Select	reg<673:670>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END2 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80 (SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
Delay3 Mode Select	reg<675:674>	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
Counter/Delay3 Macrocell Function Select	reg<677:676>	00: DLY 01: CNT/FSM 10: edge detect 11: 3bit LUT3_7

16.0 Digital Comparator (DCMP) / Pulse Width Modulator (PWM)

The SLG46140 has three 8-bit digital comparator / pulse width modulator logic cells. Each of these three logic cells can be either a digital comparator (DCMP) or a pulse width modulator (PWM) independently of how the other two logic cells are defined.

Both the DCMP and PWM logic can operate at up to a frequency of 10MHz. The input power for the three logic cells is controlled independently by reg<612> for DCMP0/PWM0, reg<601> for DCMP1/PWM1 and reg<590> for DCMP2/PWM2.

PWM power down control is configured by reg <653> which is also shared with the ADC and OSC.

16.1 DCMP Input Modes

The three DCMP logic cells have a positive (IN+) and a negative (IN-) input that are compared within the logic cell. The *inp* signal (connected to the IN+ input) takes the value from a 4:1 mux selection between the following signals:

- 8-bit signal from the ADC Parallel Output
- 8-bit signal from the SPI logic cell output (SPI<15:8> for DCMP0 and DCMP2 or SPI<7:0> for DCMP1)
- 8-bit signal from the FSM0<7:0>
- 8-bit user defined signal value

The inn signal (connected to the IN- input) takes the value from a 4:1 mux selection between the following signals:

- 8-bit signal from the SPI logic cell output (SPI<7:0> for DCMP0 and DCMP2 or SPI<15:8> for DCMP1)
- 8-bit signal from the FSM0<7:0>
- 8-bit signal from the FSM1<7:0> (for DCMP0 and DCMP1) or CNT1'Q<7:0> (for DCMP2)
- 8-bit user defined signal value

16.2 DCMP Output Modes

The two 8-bit data inputs from IN+ and IN- are compared within the DCMP logic cells to produce the output and a *match* signal.

- If *inp* > *inn*, both *OUT*+ and *OUT* signals are equal to “1”, and *EQ* signal is equal to “0”
- If *inp* < *inn*, both *OUT*+ and *OUT* signals are equal to “0”, and *EQ* signal is equal to “0”
- If *inp* = *inn*, both *OUT*+ and *OUT* signals are equal to “0”, and *EQ* signal is equal to “1”

Both the *OUT*+ and *EQ* signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit reg <580:579>).

There are two cases for the OUT signal controlled by reg <614>, reg <603>, reg <592>.

If these registers = 0, then

- if *inp* > *inn*, OUT = 1, EQ = 0
- if *inp* < *inn*, OUT = 0, EQ = 0
- if *inp* = *inn*, OUT = 0, EQ = 1

If these registers = 1, then

- if *inp* > *inn*, OUT = 1, EQ = 0
- if *inp* < *inn*, OUT = 0, EQ = 0
- if *inp* = *inn*, OUT = 1, EQ = 1

16.3 PWM Input Modes

IN+ for the PWM is an 8-bit data string that can be selected from one of four sources:

- 8-bit signal from the ADC Parallel Output

- 8-bit signal from the SPI logic cell output (SPI<15:8> for DCMP0 and DCMP1 or SPI<7:0> for DCMP2)
- 8-bit signal from the FSM0<7:0>
- 8-bit user defined signal value

IN-'s 8-bit data string for all PWMs is sourced from an 8-bit signal from CNT/DLY.

16.4 PWM Output Modes

The output (*OUT+*) duty cycle can be set to either count down to 0% or count up to 100% and each PWM is independently controlled by the value of reg<614> (PWM0), reg<603> (PWM1), and reg<592> (PWM2). When both inputs are equal the output signal (*EQ*) will go high. The outputs (*OUT-* and *OUT+*) are non-overlapping.

When reg<614/603/592> = “0”

- PWM output duty cycle ranges from 0% to 99.61% and is determined by: Output Duty Cycle = IN+/256
- (IN+ = 0: output duty cycle = 0/256 = 0%; IN+ = 255: output duty cycle = 255/256 = 99.61%)
- Output signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit reg <580:579>)

When reg<614/603/592> = “1”

- PWM output duty cycle ranges from 0.39% to 100% and is determined by Output Duty Cycle = (IN+ + 1)/256
- (IN+ = 0: output duty cycle = 1/256 = 0.39%; IN+ = 255: output duty cycle = 256/256 = 100%)
- Output signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit reg <580:579>)

When IN+ = IN- then EQ = “1”

16.5 DCMP0/PWM0 Functional Diagram

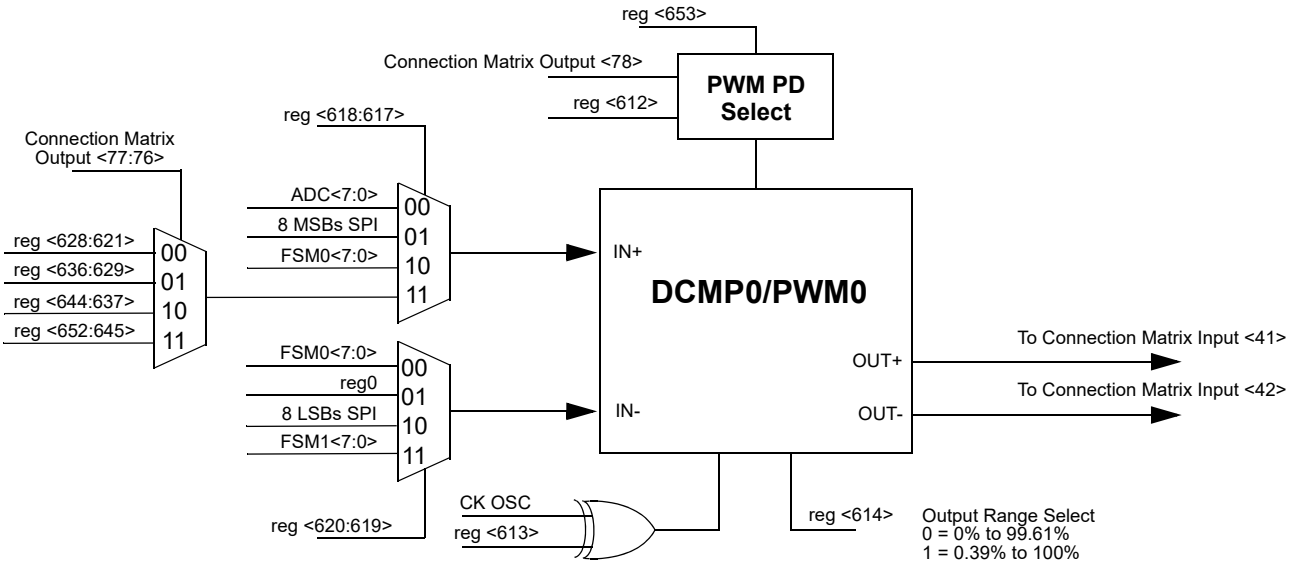


Figure 68. DCMP0/PWM0 Functional Diagram

16.6 DCMP1/PWM1 Functional Diagram

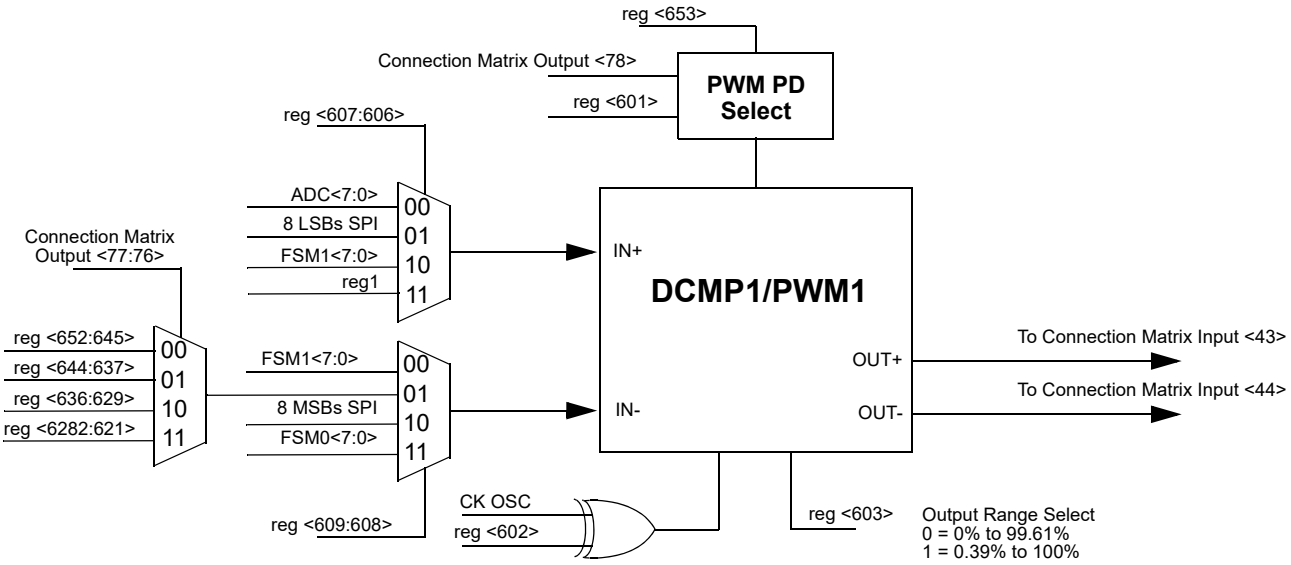


Figure 69. DCMP1/PWM1 Functional Diagram

16.7 DCMP2/PWM2 Functional Diagram

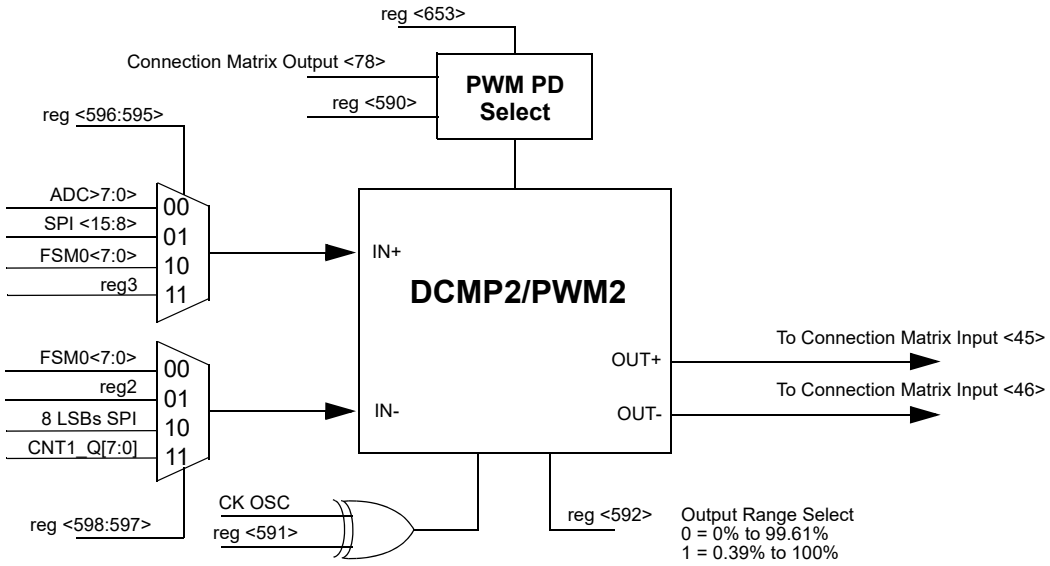


Figure 70. DCMP2/PWM2 Functional Diagram

16.8 PWM Dead Band Control

The dead band interval can be controlled with NVM bits from PWM0 reg<616:615>, from PWM1 reg<605:604>, from PWM2 reg<594:593>. The typical dead band time starts at 8 ns and can go to 64 ns, increasing by 8 ns intervals.

For the Delay dead band control, the dead time control range is:

$$T_D = (PWM\ Register\ bits + 1) \times 8ns$$

16.9 PWM Dead Band Control Timing Diagram

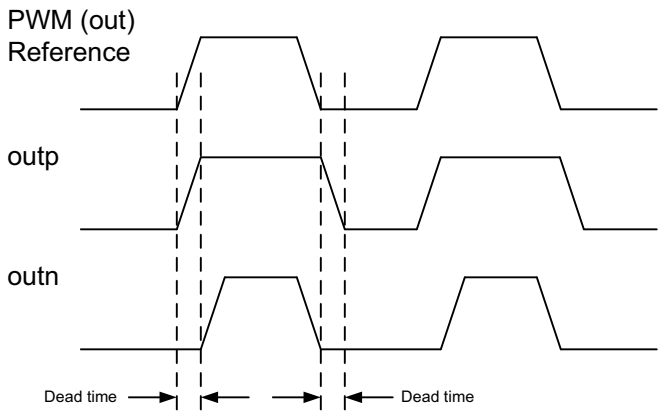


Figure 71. PWM Dead Band Control Timing Diagram

16.10 DCMP/PWM Power Down Control

The power down source for the DCMP/PWM logic cells is selected by reg <653> (shared with the ADC and PWM). The power down control DCMP/PWM logic cells comes from a register bit, otherwise it will come from connection matrix output 78 (in order for DCMP to turn on, this signal should be LOW). The DCMP/PWM logic cells can then be turned on or off individually with the appropriate register. The power down control of each logic cell is managed by the following register settings:

- When reg<612> = “0” DCMP0/PWM0 is powered down, when “1” logic cell is ON
- When reg<601> = “0” DCMP1/PWM1 is powered down, when “1” logic cell is ON
- When reg<590> = “0” DCMP2/PWM2 is powered down, when “1” logic cell is ON

16.11 DCMP/PWM Clock Invert Control

The three DCMP/PWM logic cells can invert the *CKOSC* input signal during the compare or PWM function. Reg<613>, reg<602>, and reg<591> are used to control the three logic cells clock inversion for PWM0, PWM1, and PWM2 respectively.

16.12 DCMP/PWM Register Settings

Table 74. DCMP/PWM Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
PWMDCMP2_pd	PWM2/DCMP2 power down control	<590>	0: power down 1: power on
PWMDCMP2_clk_in	PWM/DCMP2 clock invert	<591>	0: Disable 1: Enable
PWM2_mode_sel	PWM2 mode select	<592>	0: count down to 0% 1: count up to 100%
PWM2_db_sel	PWM2 Deadband Select	<594:593>	00: 10 ns 01: 20 ns 01: 40 ns 11: 80 ns
PWMDCMP2_pos_in	PWM2/DCMP2 positive input source select	<596:595>	00: from ADC 01: from SPI 10: from FSM0 11: reg3
PWMDCMP2_neg_in	PWM2/DCMP2 negative input source select	<598:597>	00: FSM0[7:0] 01: reg2 10: 8LSBs SPI 11: CNT1_Q[7:0]
PWMDCMP1_pd	PWM1/DCMP1 power down control	<601>	0: power down 1: power on
PWMDCMP1_clk_in	PWM/DCMP1 clock invert	<602>	0: Disable 1: Enable
PWM1_mode_sel	PWM1 mode select	<603>	0: count down to 0% 1: count up to 100%
PWM1_db_sel	PWM1 Deadband Select	<605:604>	00: 10 ns 01: 20 ns 01: 40 ns 11: 80 ns
PWMDCMP1_pos_in	PWM1/DCMP1 positive input source select	<607:606>	00: from ADC 01: from 8LSBs SPI 10: from FSM1[7:0] 11: reg1
PWMDCMP1_neg_in	PWM1/DCMP1 negative input source select	<609:608>	00: FSM1[7:0] 01: regs from MUX controlled by matrix_out[77:76] 10: 8MSBs SPI 11: FSM0[7:0]
PWMDCMP0_pd	PWM0/DCMP0 power down control	<612>	0: power down 1: power on
PWMDCMP0_clk_in	PWM/DCMP0 clock invert	<613>	0: Disable 1: Enable
PWM0_mode_sel	PWM0 mode select	<614>	0: count down to 0% 1: count up to 100%
PWM0_db_sel	PWM0 Deadband Select	<616:615>	00: 10 ns 01: 20 ns 01: 40 ns 11: 80 ns

Table 74. DCMP/PWM Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
PWMDCMP0_pos_in	PWM0/DCMP0 positive input source select	<618:617>	00: ADC [7:0] 01: 8MSBs SPI 10: FSM0[7:0] 11: regs from MUX controlled by matrix_out[77:76]
PWMDCMP0_neg_in	PWM0/DCMP0 negative input source select	<620:619>	00: FSM0[7:0] 01: reg0 10: 8LSBs SPI 11: FSM1[7:0]
ADC_PWM_OSC_pd_src_sel	ADC/PWM/OSC power down source select	<653>	0: power down is not synchronized with clock, when PWM/DCMP is power down 1: power down is synchronized with clock when PD=0, the clock is enabled after 2 clock cycles when PD=1, the clock is gated immediately
PWMDCMP2_pos_in	PWM2/DCMP2 positive input source select	<768:767>	00: from ADC 01: from 8MSBs SPI 10: from FSM0 [7:0] 11: reg3

17.0 Slave SPI - Serial to Parallel / Parallel to Serial Converter (SPI)

The Slave SPI data can be communicated between the SLG46140 and the larger system design through either the serial to parallel or parallel to serial interface. The SPI has two 8-bit registers (2 bytes) that are used for data transfer. The external clock signal and the nCSB (Enable Control Signal) comes from the Connection Matrix Out.

For serial to parallel operation (S2P), the serial data in (MOSI) comes from PIN 12 of the SLG46140. The S2P will produce a 16-bit parallel data output (S2P<15:0>) where the MSB <15:8> can be used by the PWM/DCMP0_IN+, PWM/DCMP1_IN-, PWM/DCMP2_IN+ and FSM0 logic cells, while the LSB <7:0> can be used by the PWM/DCMP0_IN-, PWM/DCMP1_IN+, PWM/DCMP2_IN- and FSM1 logic cells.

In parallel to serial mode (P2S) there is an additional configuration of the length of converted code – 8-bit and 16-bit. With 8-bit configuration the parallel data from FSM0 or ADC can be converted to serial data. PIN 12 is used to output this 8-bit serial data out (MISO) signal. With 16 bit configuration the parallel data from FSM0 and FSM1 can be converted into a serial code. 8 LSB bits of FSM1 data will be sent to PAR_IN<7:0> and 8 bits of FSM0 will be sent to PAR_IN<15:8>. Same as in 8-bit mode 16 bit serial data will be output to PIN12.

17.1 SPI Functional Diagram

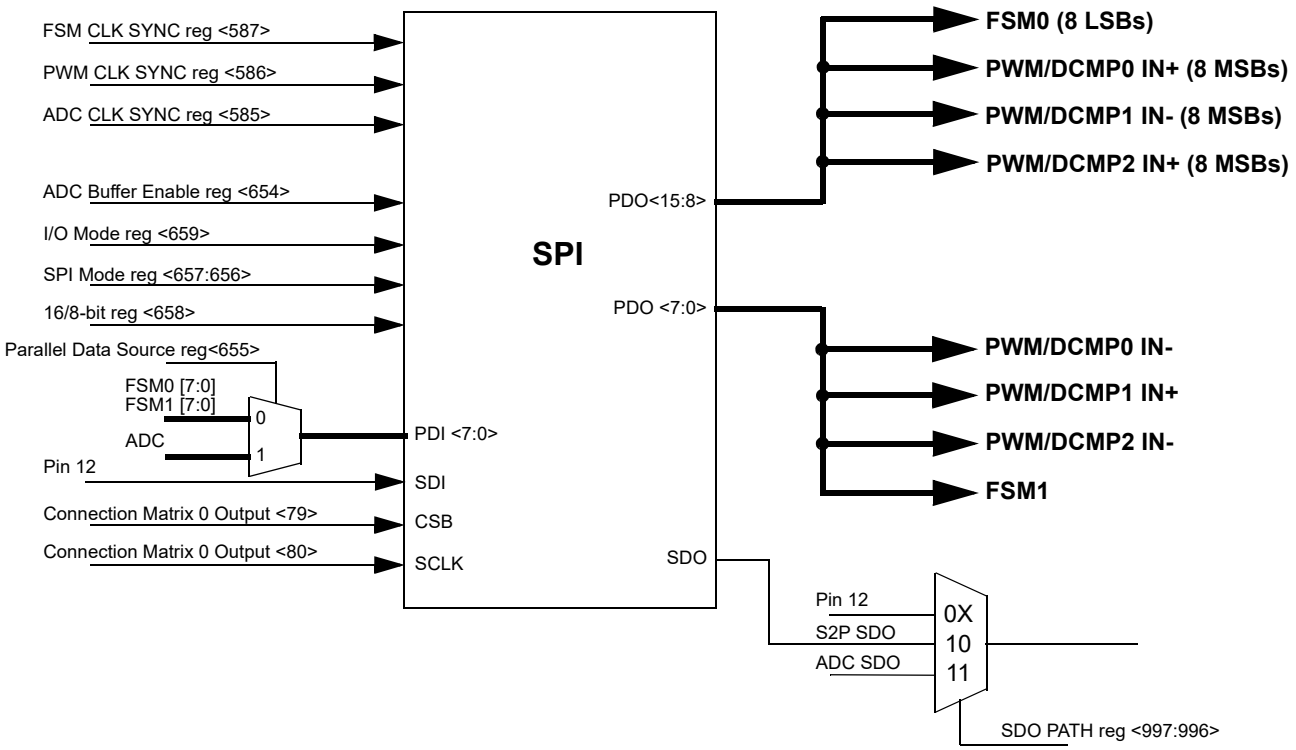


Figure 72. SPI Functional Diagram

17.2 Clock polarity and phase

In addition to setting the clock frequency, it is possible to configure the clock polarity and phase with respect to the data. This is configured by the CPOL and CPHA bits respectively.

Figure 73 shows the SPI timing diagram when CPHA = 0; in this mode data can only be transmitted from serial to parallel, not from parallel to serial. *Figure 74* shows the SPI timing diagram when CPHA= 1; in this mode data can be transmitted both from serial to parallel and from parallel to serial.

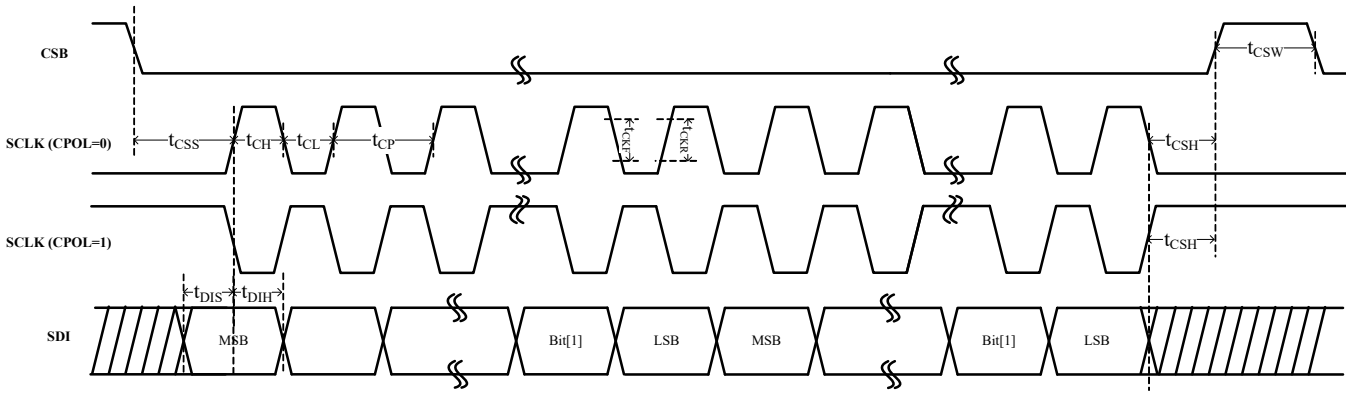


Figure 73. Timing Diagram showing Clock Polarity and Phase, CPHA = 0

Table 75. CPHA = 0 Timing Characteristics

Parameter	Symbol	Min	Max	Units
SCLK period	t_{CP}	500	--	ns
SCLK pulse width high	t_{CH}	250	--	ns
SCLK pulse width low	t_{CL}	250	--	ns
CSB fall to SCLK first edge setup	t_{CSS}	250	--	ns
SCLK last edge to CSB rise hold	t_{CSH}	250	--	ns
CSB pulse width high	t_{CSW}	500	--	ns
SCLK to SDI hold	t_{DIH}	100	--	ns
SCLK to SDI setup	t_{DIS}	50	--	ns
SCLK rise/fall time	t_{CKR}	--	20	ns

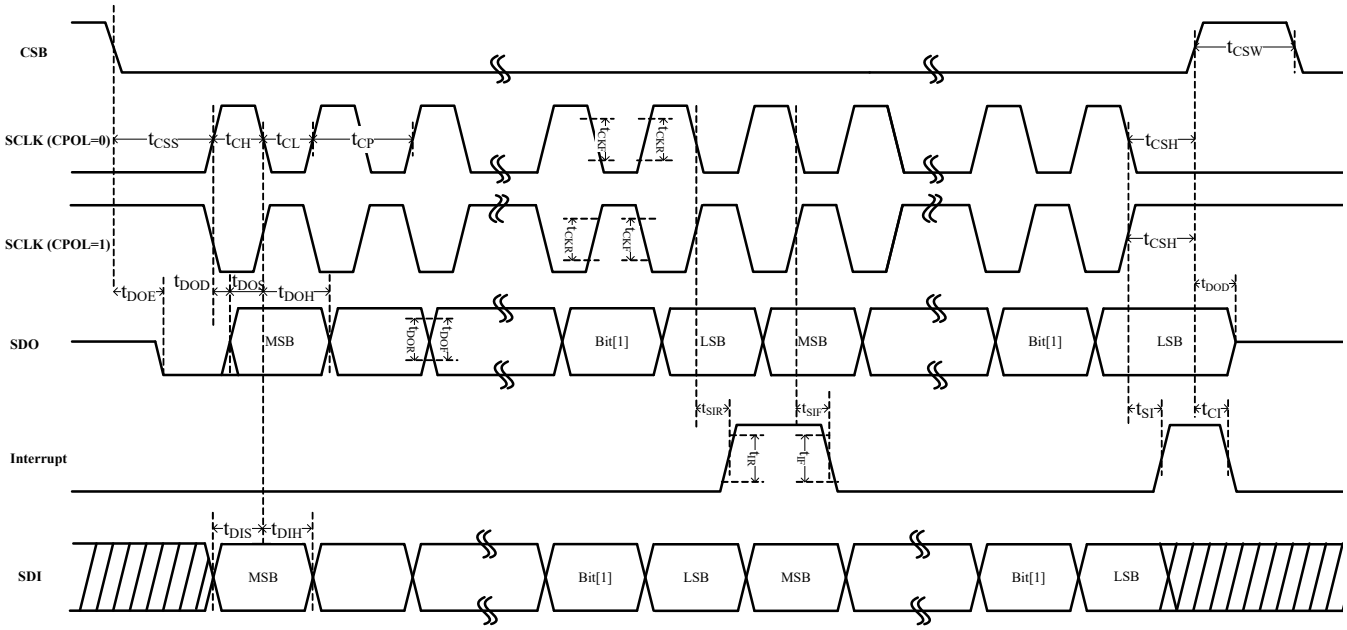


Figure 74. Timing Diagram showing Clock Polarity and Phase, CPHA = 1

Table 76. CPHA = 1 Timing Characteristics

Parameter	Symbol	Min	Max	Units
SCLK period	t_{CP}	500	--	ns
SCLK pulse width high	t_{CH}	250	--	ns
SCLK pulse width low	t_{CL}	250	--	ns
CSB fall to SCLK first edge setup	t_{CSS}	250	--	ns
SCLK last edge to CSB rise hold	t_{CSH}	250	--	ns
SCLK to SDO hold	t_{DOH}	100	--	ns
SCLK to SDO setup	t_{DOS}	100	--	ns
SCLK to SDO delay	t_{DOD}	--	150*	ns
CSB rise to SDO disable	t_{DOD}	5	150*	ns
CSB fall to SDO enable	t_{DOE}	5	150*	ns
CSB pulse width high	t_{CSW}	500	--	ns
LSB' SCLK fall to Interrupt high	t_{SIR}	5	150*	ns
MSB' SCLK fall to Interrupt low	t_{CIF}	5	150*	ns
SCLK to Interrupt high	t_{SI}	5	150*	ns
CSB rise to Interrupt low	t_{CI}	5	150*	ns
SCLK to SDI hold	t_{DIH}	100	--	ns
SCLK to SDI setup	t_{DIS}	50	--	ns
SCLK rise/fall time	t_{CKR}/t_{CKF}	--	20	ns
SDO rise/fall time	t_{DOR}/t_{DOF}	--	20*	ns
Interrupt rise/fall time	t_{IR}/t_{IF}	--	20*	ns
*Note: *The data is based on 50 pF loading on the output PIN, and the output drive strength is 2x option.*				

- At CPOL=0 the base value of the clock is zero
  - For CPHA=0, data are captured on the clock's rising edge (LOW→HIGH transition) and data is propagated on a falling edge. (HIGH→LOW clock transition).
  - For CPHA=1, data are captured on the clock's falling edge and data is propagated on a rising edge.
- At CPOL=1 the base value of the clock is one (inversion of CPOL=0)
  - For CPHA=0, data are captured on clock's falling edge and data is propagated on a rising edge.
  - For CPHA=1, data are captured on clock's rising edge and data is propagated on a falling edge.

That is, CPHA=0 means sample on the leading (first) clock edge, while CPHA=1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. Note that with CPHA=0, the data must be stable for a half cycle before the first clock cycle.

The MOSI and MISO signals are usually stable (at their reception points) for the half cycle until the next clock transition. SPI master and slave devices may well sample data at different points in that half cycle.

This adds more flexibility to the communication channel between the master and slave.

17.3 SPI Clock synchronization

When the parallel data is going to be loaded into the buffer in SPI, the SPI will generate the "sync" signal, it will be gating the ADC/PWM CLOCK or FSM CLOCK/256 to stop the running ADC, PWM, FSM or CNTs to avoid mis-catch data due to the asynchronization of SCLK and the internal clocks, see *Figure 75*.

Note: The internal clock and SPI clock must satisfy the: $2T_{CLK\_IN}T < 1/2T_{SCK}$

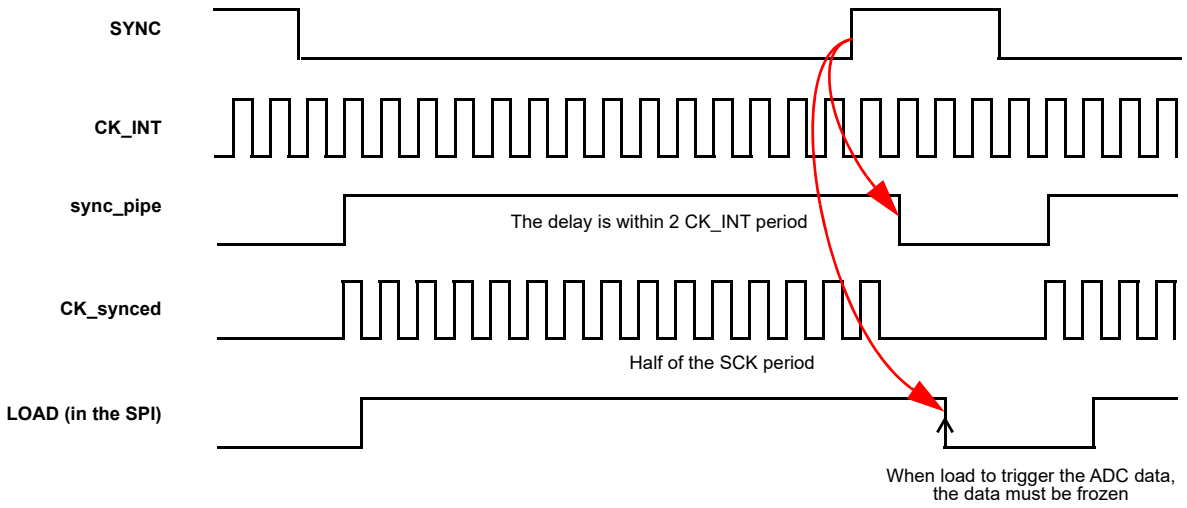


Figure 75. Timing Diagram showing SPI Clock synchronization

17.4 SPI data buffer function

SPI data buffer can be used to have DCMP compare two different ADC timing data. The ADC buffer is shared with the DFFs that are in the SPI macrocell. When the SPI is set to ADC buffer mode (reg[654]=1), the DFF ‘s data inputs of SPI’s parallel outputs are from ADC (reg[655]=1), and the DFF’s clock source comes from matrix_output80 which can be programmed by user. The DFF’s output (SPI[7:0]) is the ADC data’s buffered output which can be sent to DCMP/PWMs or FSM (CNT)s.

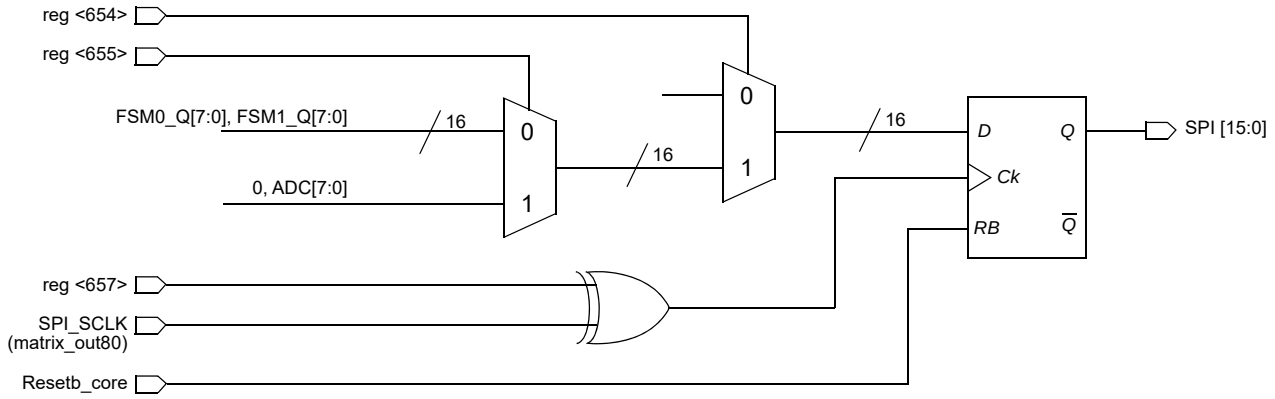


Figure 76. The SPI used as ADC/FSM data buffer diagram

17.5 SPI Register Settings

Table 77. SPI Register Settings

Signal Function	Register Bit Address	Register Definition
SPI used as ADC/FSM buffer enable (1 clock delayed)	<654>	0: Disable 1: Enable
SPI parallel input data source selection	<655>	0: FSM0[7:0],FSM1[7:0] 1: ADC
SPI clock phase (CHPA)	<656>	refer to SPI spec
SPI clock polarity (CHOL)	<657>	refer to SPI spec
byte selection	<658>	0: 16bits 1: 8bits (less significant 8 bits)
SPI input/output mode selection	<659>	0: serial in parallel out 1: parallel in serial out.
SPI SDIO output control	<997:996>	0x: pin12 dout from matrix 0 (out57) 10: from s2p (SDO) 11: from ADC serial output

18.0 Pipe Delay (PD)

The SLG46140 has one 16-stages DFF Pipe Delay Macrocell.

The Pipe Delay has three input signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide two delay options which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by register bits. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46140 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or any Oscillator within the SLG46140). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

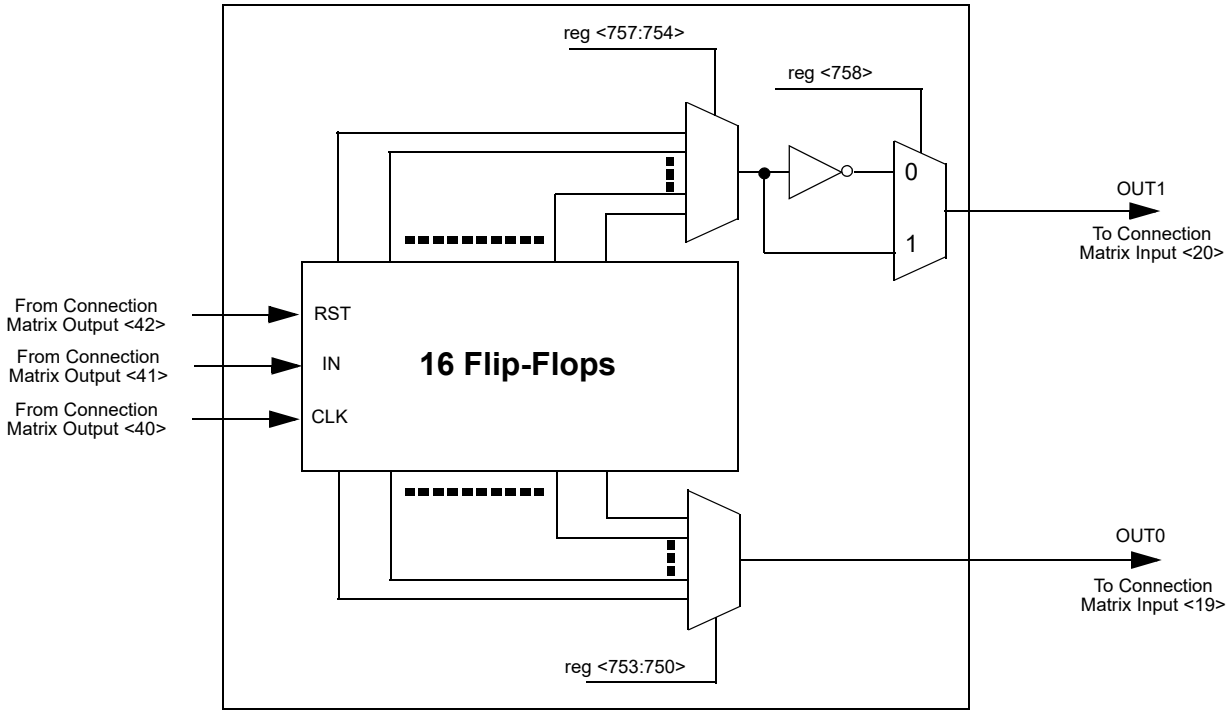


Figure 77. Pipe Delay

19.0 Programmable Delay / Edge Detector

The SLG46140 has one programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

Note: *The input signal must be longer than the delay, otherwise it will be filtered out.*

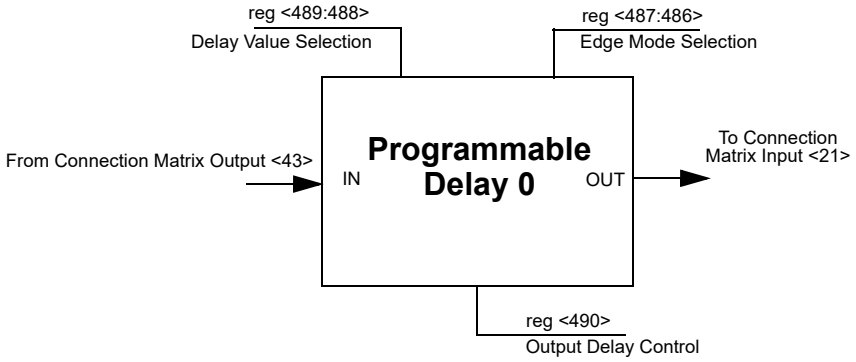


Figure 78. Programmable Delay

19.1 Programmable Delay Timing Diagram - Edge Detector Output

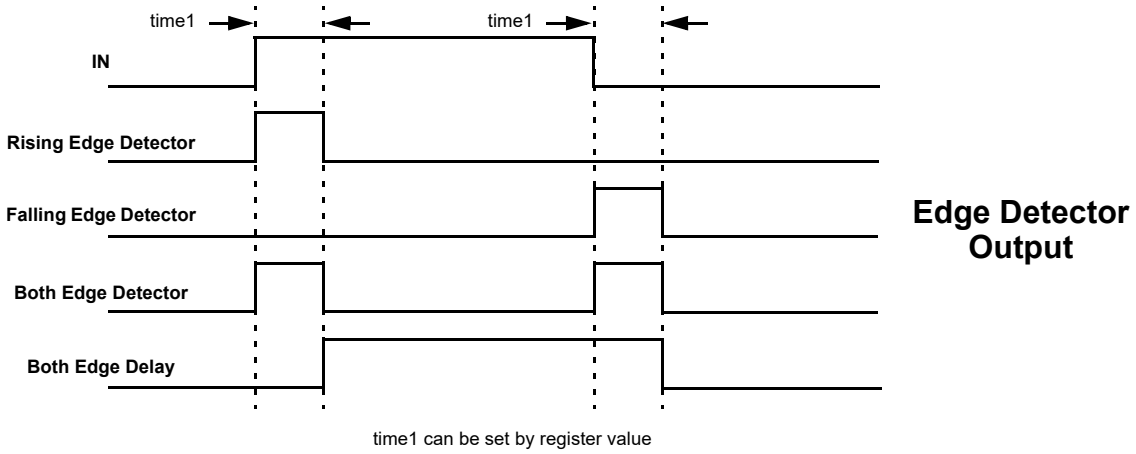


Figure 79. Edge Detector Output

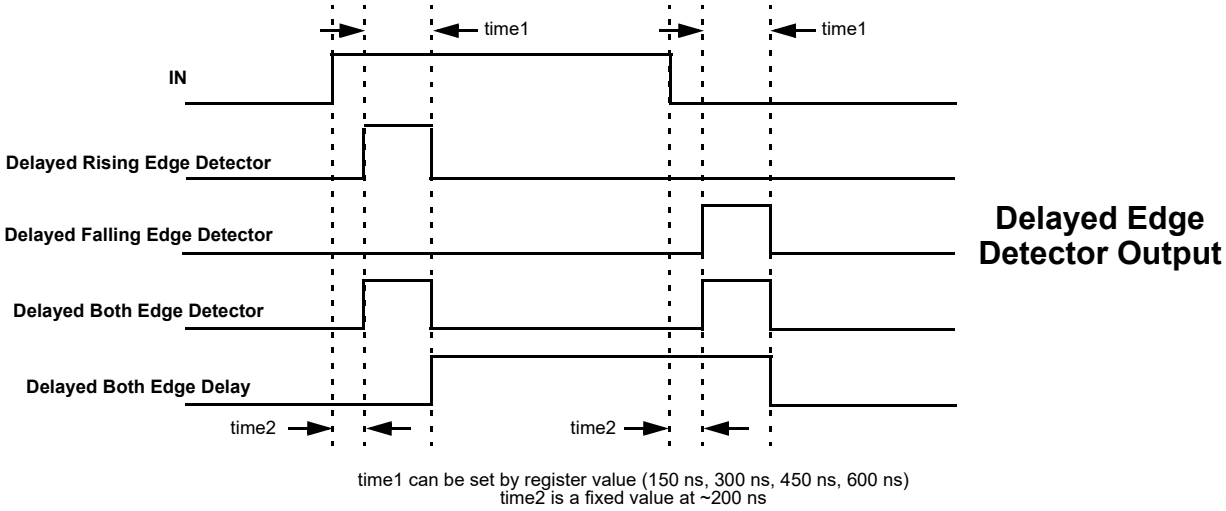


Figure 80. Delayed Edge Detector Output

19.2 Programmable Delay Timing Diagram - Glitch Filtering For Edge Detector Output

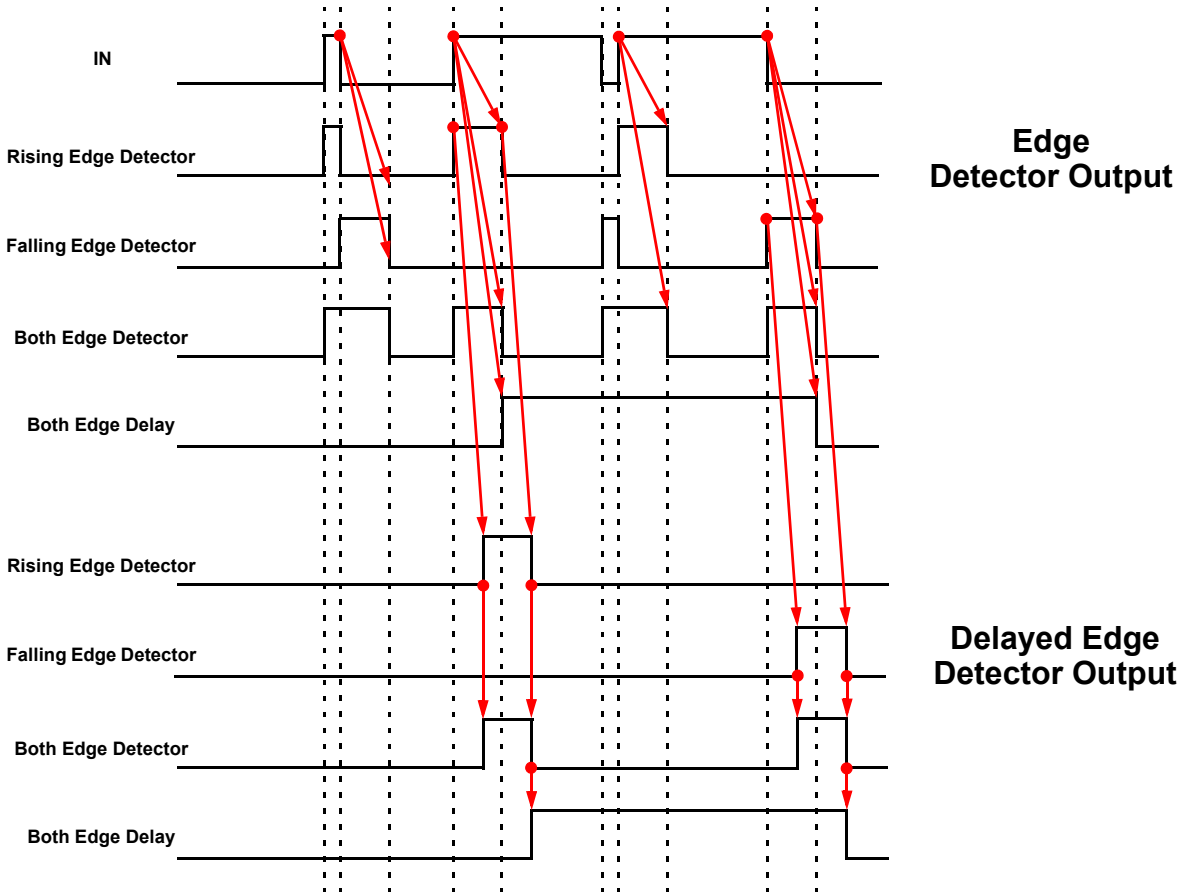


Figure 81. Glitch Filtering for Edge Detector Output

19.3 Programmable Delay 0 Register Settings

Table 78. Programmable Delay 0Register Settings

Signal Function	Register Bit Address	Register Definition
Select the edge mode of programmable delay & edge detector	reg<487:486>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	reg<489:488>	00: 150 ns 01: 300 ns 10: 450 ns 11: 600 ns
Select edge detector output mode	reg<490>	0: Non-Delayed Output 1: Delayed Output

20.0 Voltage Reference (VREF)

20.1 Voltage Reference Overview

The SLG46140 has a Voltage Reference Macrocell to provide references to the two analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from pins 4 and 5. The macrocell also has the option to output reference voltages on pin 3. See table below for the available selections for each analog comparator. Also see *Figure 82* below, which shows the reference output structure.

Table 79. VREF Selection Table

reg_acmpx-ref_sel <4:0>	ACMP0_VREF	ACMP1_VREF
11111	DAC0_out	DAC0_out
11110	DAC1_out	DAC1_out
11101	vref_ext_ac-mp0 / 2	vref_ext_ac-mp0 / 2
11100	vref_ext_ac-mp1 / 2	vref_ext_ac-mp1 / 2
11011	vref_ext_acmp0	vref_ext_acmp0
11010	vref_ext_acmp1	vref_ext_acmp1
11001	vdd/4	vdd/4
11000	vdd/3	vdd/3
10111	1.20	1.20
10110	1.15	1.15
10101	1.10	1.10
10100	1.05	1.05
10011	1.00	1.00
10010	0.95	0.95
10001	0.90	0.90
10000	0.85	0.85
01111	0.80	0.80
01110	0.75	0.75
01101	0.70	0.70
01100	0.65	0.65
01011	0.60	0.60
01010	0.55	0.55
01001	0.50	0.50
01000	0.45	0.45
00111	0.40	0.40
00110	0.35	0.35
00101	0.30	0.30
00100	0.25	0.25
00011	0.20	0.20
00010	0.15	0.15
00001	0.10	0.10
00000	0.05	0.05

Table 80. VREF Range

VDD	Practical VREF Range	Note
2.0 V - 5.5 V	50 mV ~1.2 V	Do not use external Vref when VDD > 5.0 V and T = 85°C
1.7 V - 2.0V	50 mV ~1.1 V	Do not operate above 1.1 V

20.2 VREF Block Diagram

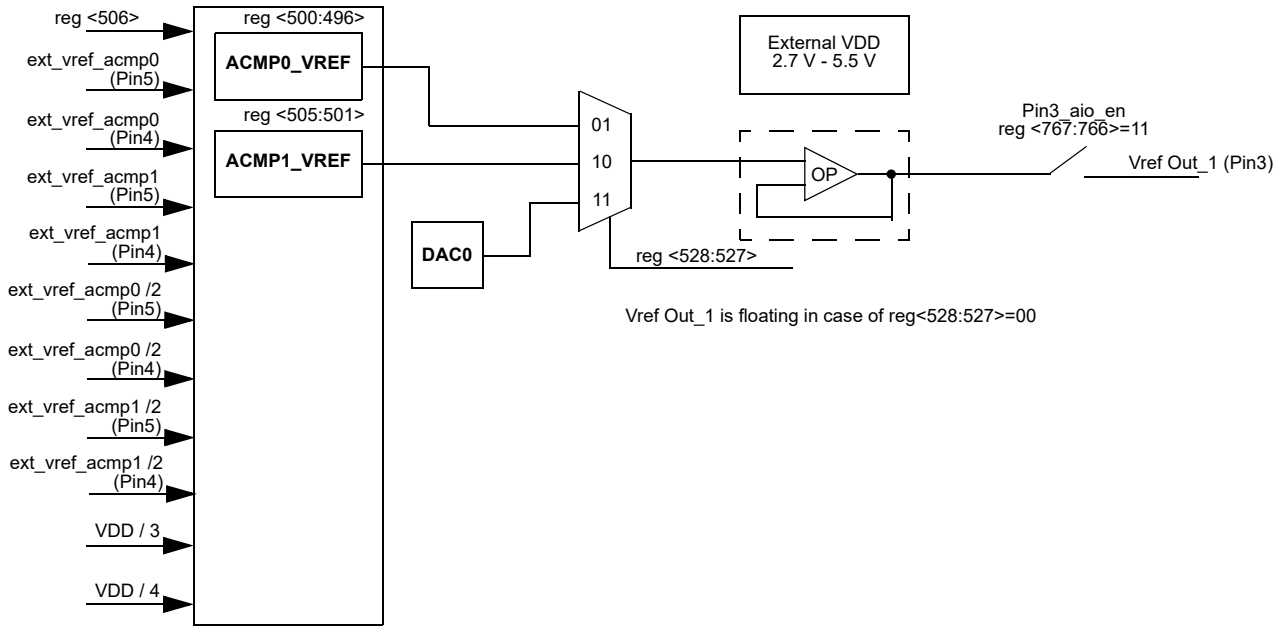


Figure 82. Voltage Reference Block Diagram

21.0 Oscillators

The SLG46140 has two internal RC oscillators (25 kHz or 2 MHz, user selectable), as well as one Low-Frequency oscillator (1.9 kHz) and one Ring oscillator (25 MHz).

There are two divider stages for the RC and Ring oscillators, and one divider stage for the Low-Frequency oscillator, that allow the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The predivider (first stage) for RC Oscillator allows the selection of /1, /2, /4 or /8, for LF Osc - /1, /2, /4 or /16 and for Ring Osc - /1, /4, /8 or /16 to divide down frequency from the fundamental. The second stage divider of RC oscillators has an input of frequency from the predivider, and outputs one of eight different frequencies on Connection Matrix Input line <35>. The output of LF Osc Predivider goes directly on Connection Matrix Input line <50>. Please see *Figure 83* below, for more details on the SLG46140 clock scheme.

The Matrix Power Down function allows to switch on/off the oscillators using an external pin (reg<567> for 25 kHz / 2 MHz OSC, reg<562> for LF OSC and reg<575> for Ring Osc):

- **Enable <1>**. If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input

of oscillator is HIGH the oscillator will be turned off.

- **Disable <0>**. Turns off the Matrix Power Down function.

The PWR CONTROL signal has the highest priority.

The user can select two OSC POWER MODEs (reg<564> for 25 kHz / 2 MHz RC OSC, reg<563> for LF OSC and reg<574> for Ring Osc):

- **If FORCE POWER ON <1>** is selected, the OSC will run when the SLG46140 is powered on.
- **If AUTO POWER ON <0>** is selected, the OSC will run only when any macrocell that uses OSC is powered on.

OSC can be turned on by:

- Register control (force power on);
- Delay mode, when delay requires OSC;
- ADC;
- PWM/DCMP.

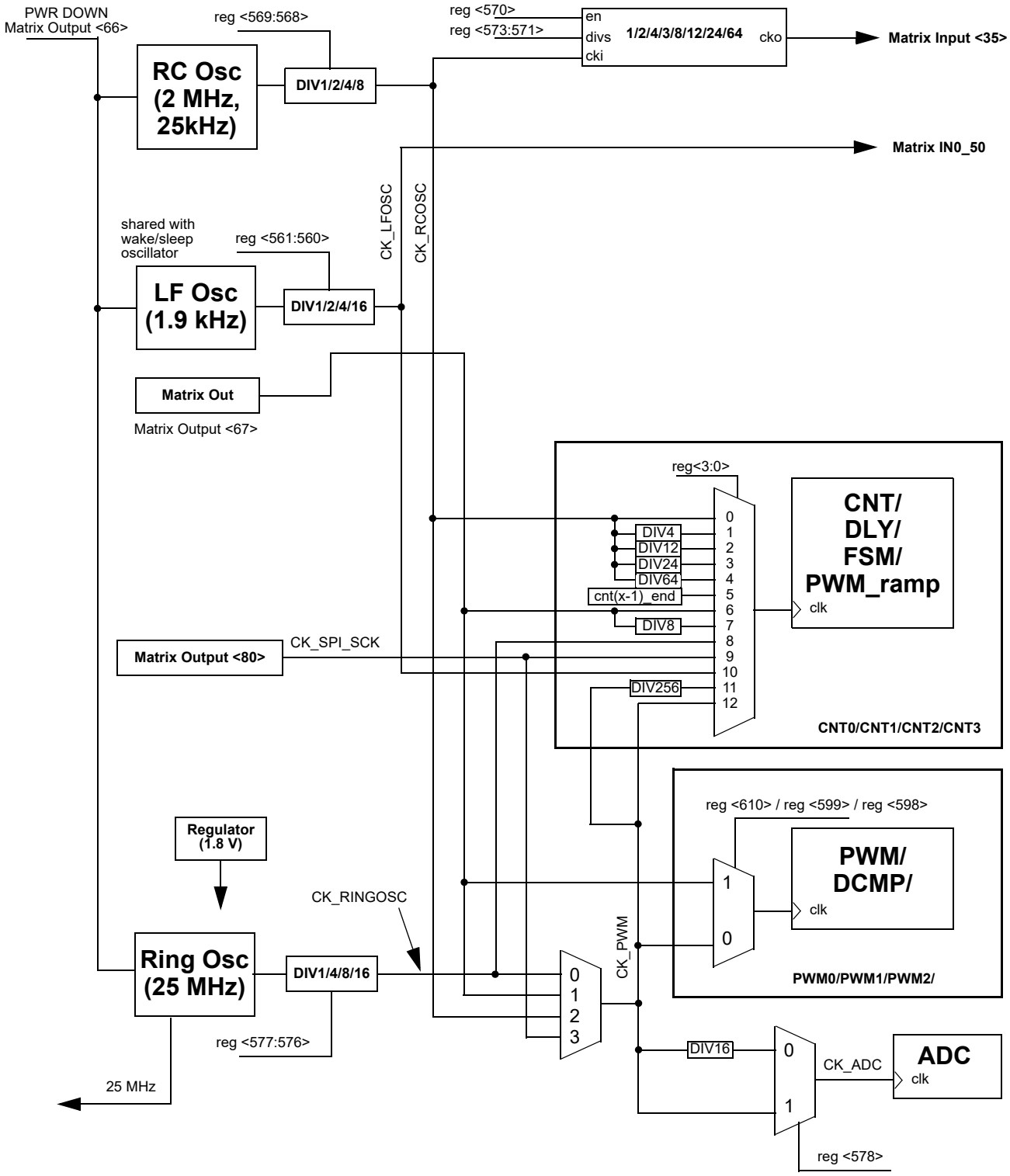


Figure 83. Oscillator Block Diagram

21.1 Oscillator Power On delay

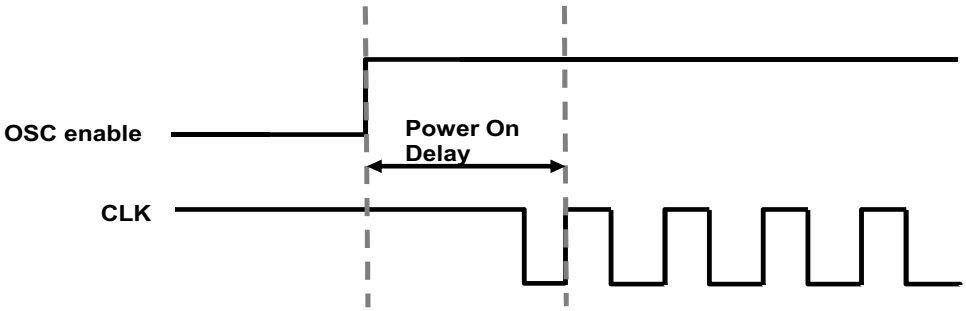


Figure 84. Oscillator Startup Diagram

Note 1: OSC power mode: "Auto Power On".

Note 2: 'OSC enable' signal appears when any block that uses OSC is powered on.

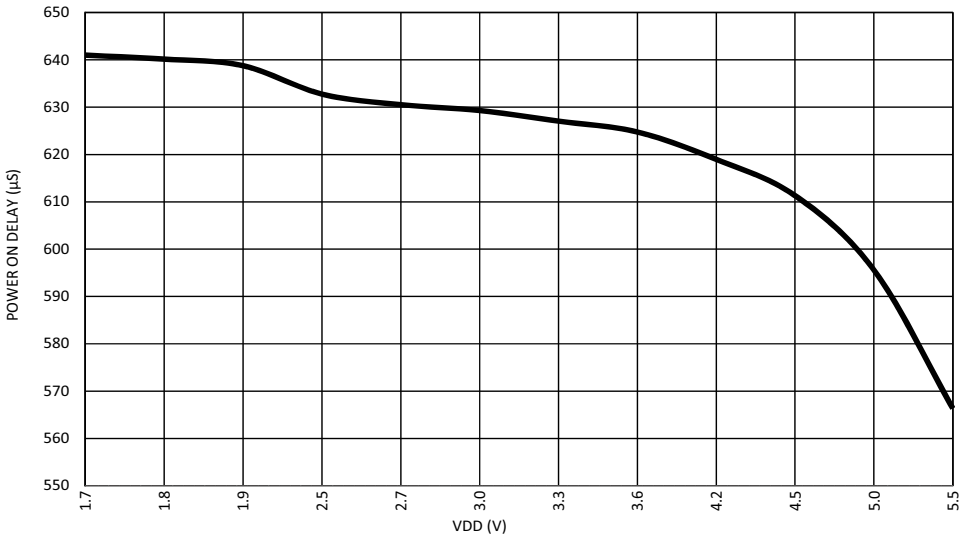


Figure 85. Low Frequency Oscillator Maximum Power On Delay vs. VDD at room temperature

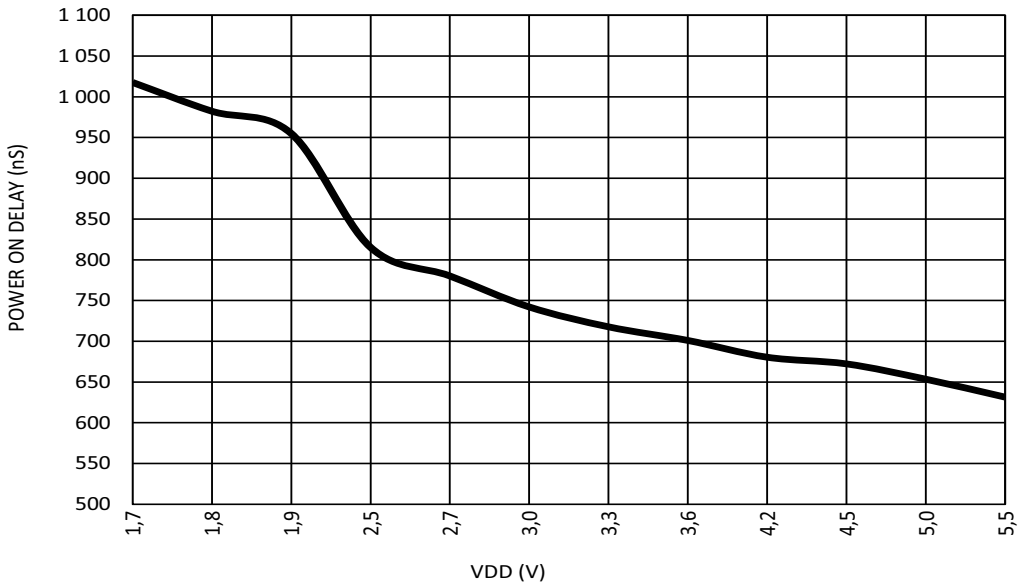


Figure 86. RC Oscillator Maximum Power On Delay vs. VDD at room temperature, RC OSC=2 MHz.

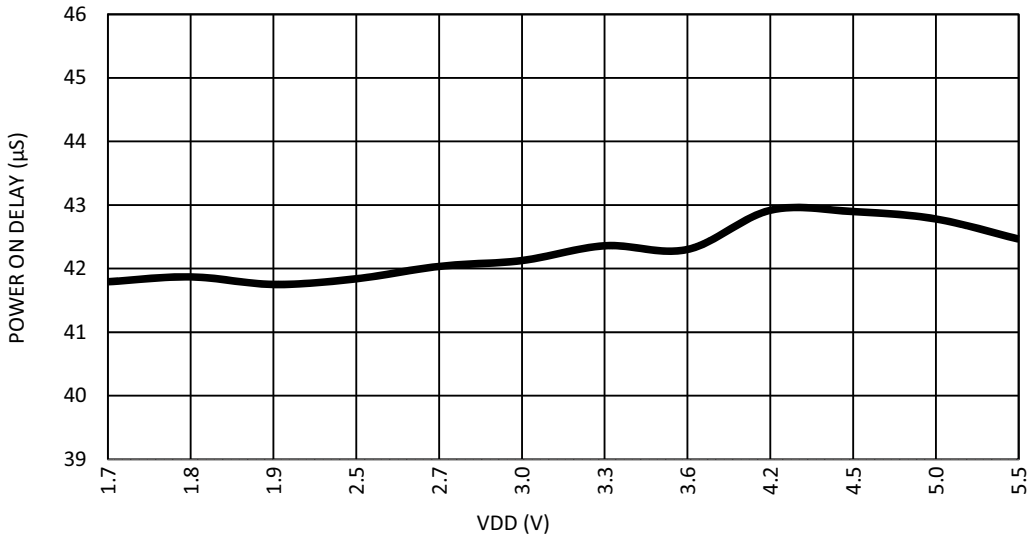


Figure 87. RC Oscillator Maximum Power On Delay vs. VDD at room temperature, RC OSC=25 kHz.

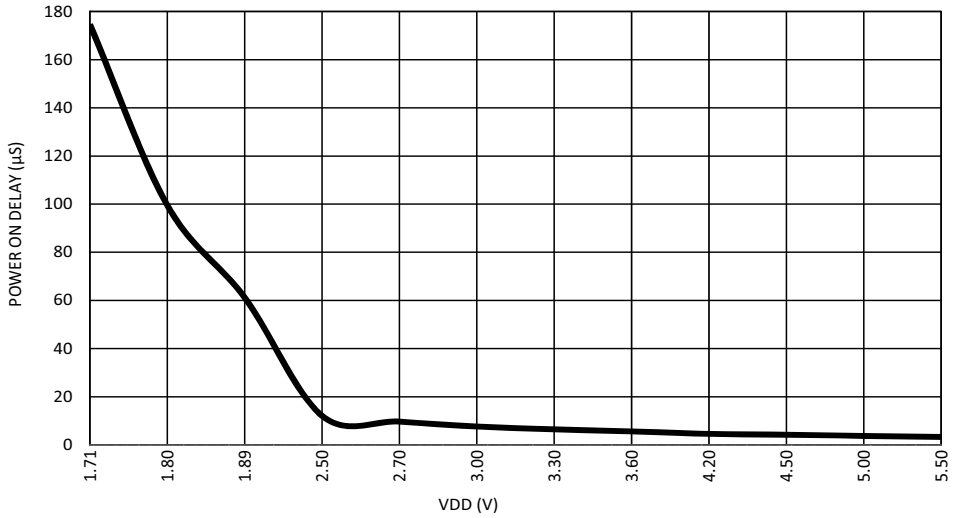


Figure 88. Ring Oscillator Maximum Power On Delay vs. VDD at room temperature.

21.2 Oscillator Accuracy

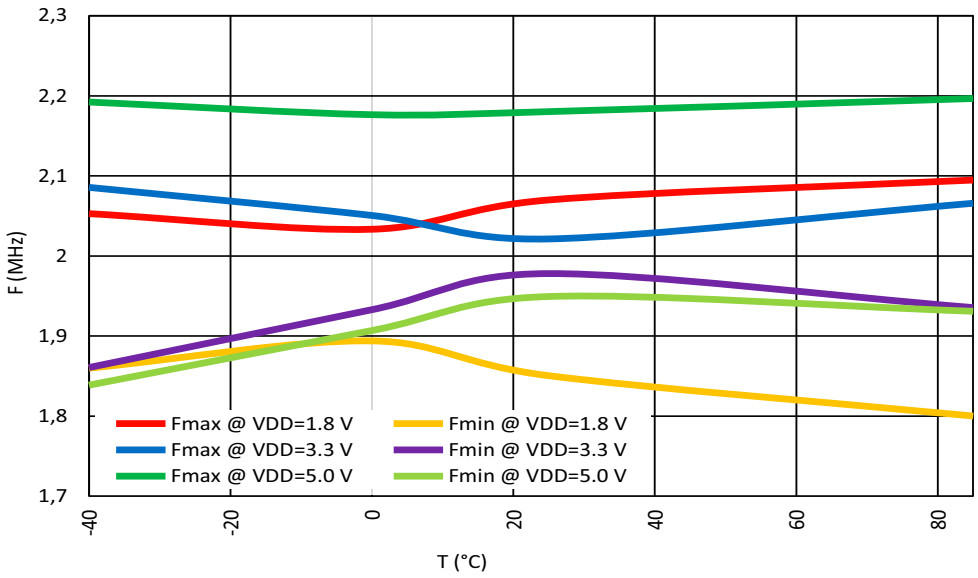


Figure 89. RC Oscillator Frequency vs. Temperature, RC OSC=2 MHz

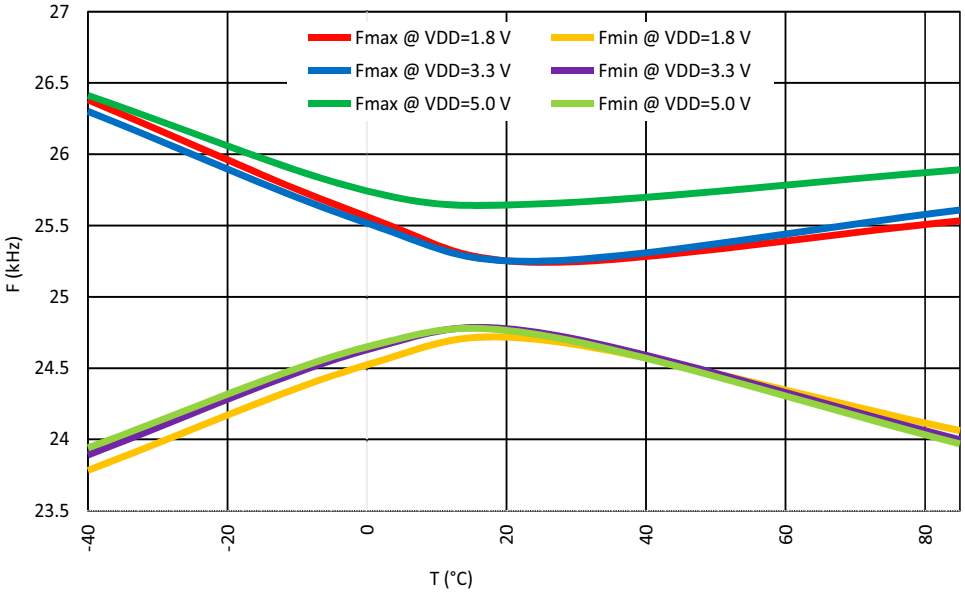


Figure 90. RC Oscillator Frequency vs. Temperature, RC OSC=25 kHz

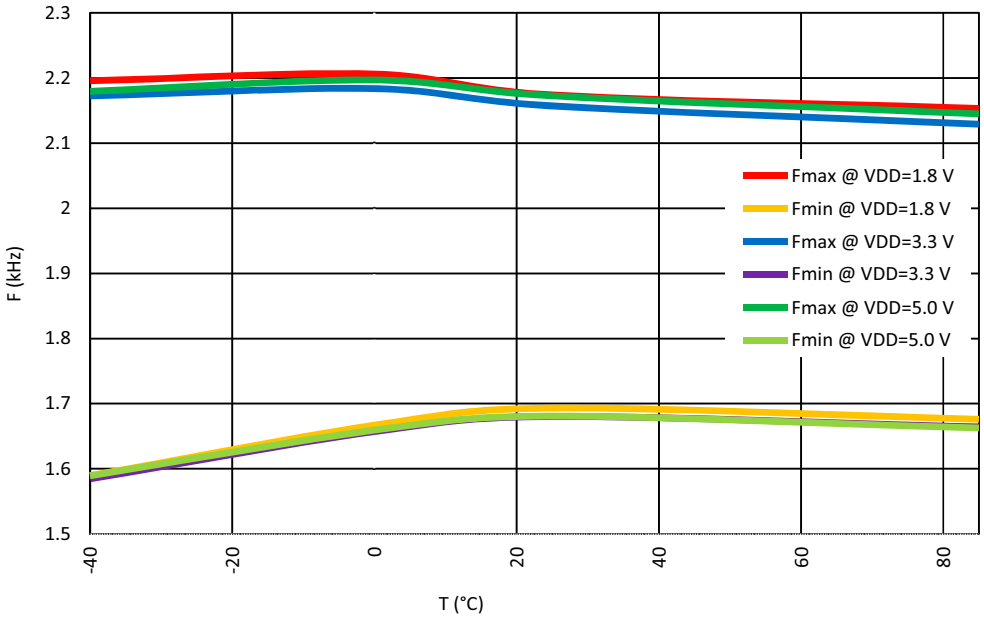


Figure 91. LF Oscillator Frequency vs. Temperature, LF OSC=1.9 kHz

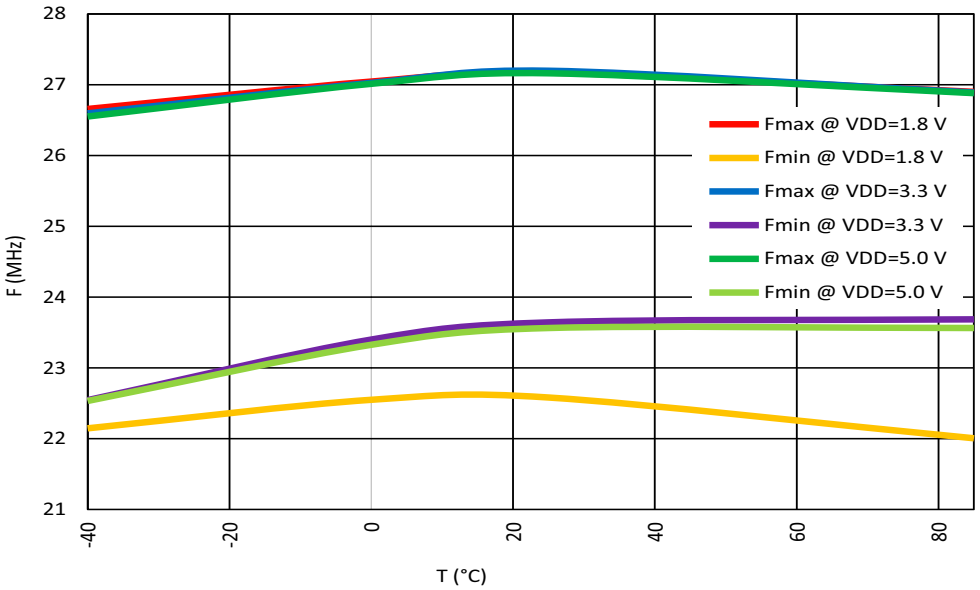


Figure 92. Ring Oscillator Frequency vs. Temperature, Ring OSC=25 MHz

Note: For more information see section 5.7 OSC Specifications.

22.0 Power On Reset (POR)

The SLG46140 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the VDD power is first ramping to the device, and also while the VDD is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the I/O pins.

22.1 General Operation

The SLG46140 is guaranteed to be powered down and nonoperational when the VDD voltage (voltage on PIN1) is less than Power Off Threshold (see in Electrical Characteristics table), but not less than -0.6V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 1) than the VDD voltage is applied to any other PIN. For example, if VDD voltage is 0.3V, applying a voltage higher than 0.3V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1. There is a 0.6V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46140, the voltage applied on the VDD should be higher than the Power_ON threshold (see Note 2). The full operational VDD range for the SLG46140 is 1.71V – 5.5V (1.8V ±5% - 5V±10%). This means that the VDD voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the VDD voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46140 will have a typical period of time to go through all the steps in the sequence (see *Figure 80* and *Figure 81*), and will be ready and completely operational after the POR sequence is complete.

Note 2. The Power_ON threshold is defined in Electrical Characteristics table.

Note 3. VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

To power down the chip the VDD voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the I/O structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can’t be bigger than the VDD, this rule also applies to the case when the chip is powered on.

22.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in *Figure 93*.

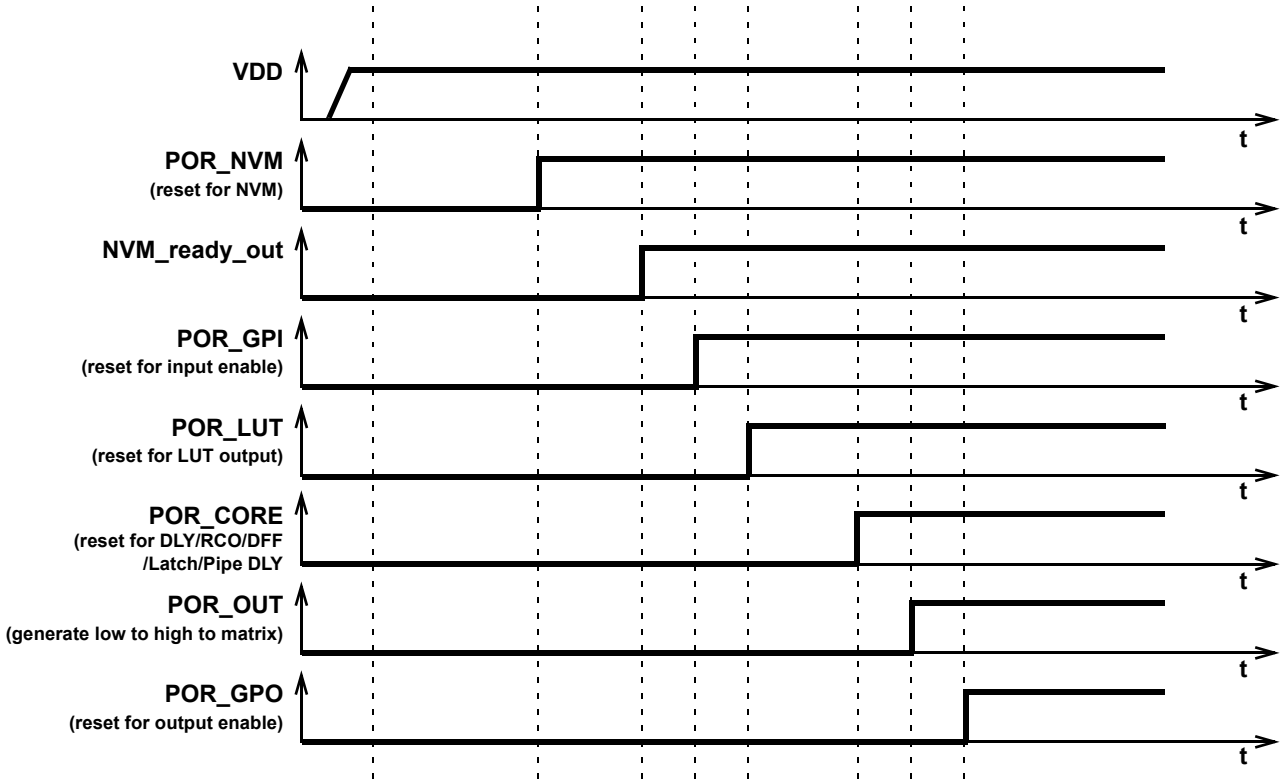


Figure 93. POR sequence

As can be seen from *Figure 93* after the VDD has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transit from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, VDD value, temperature and even will vary from chip to chip (process influence).

22.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46140 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (*Figure 94* describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

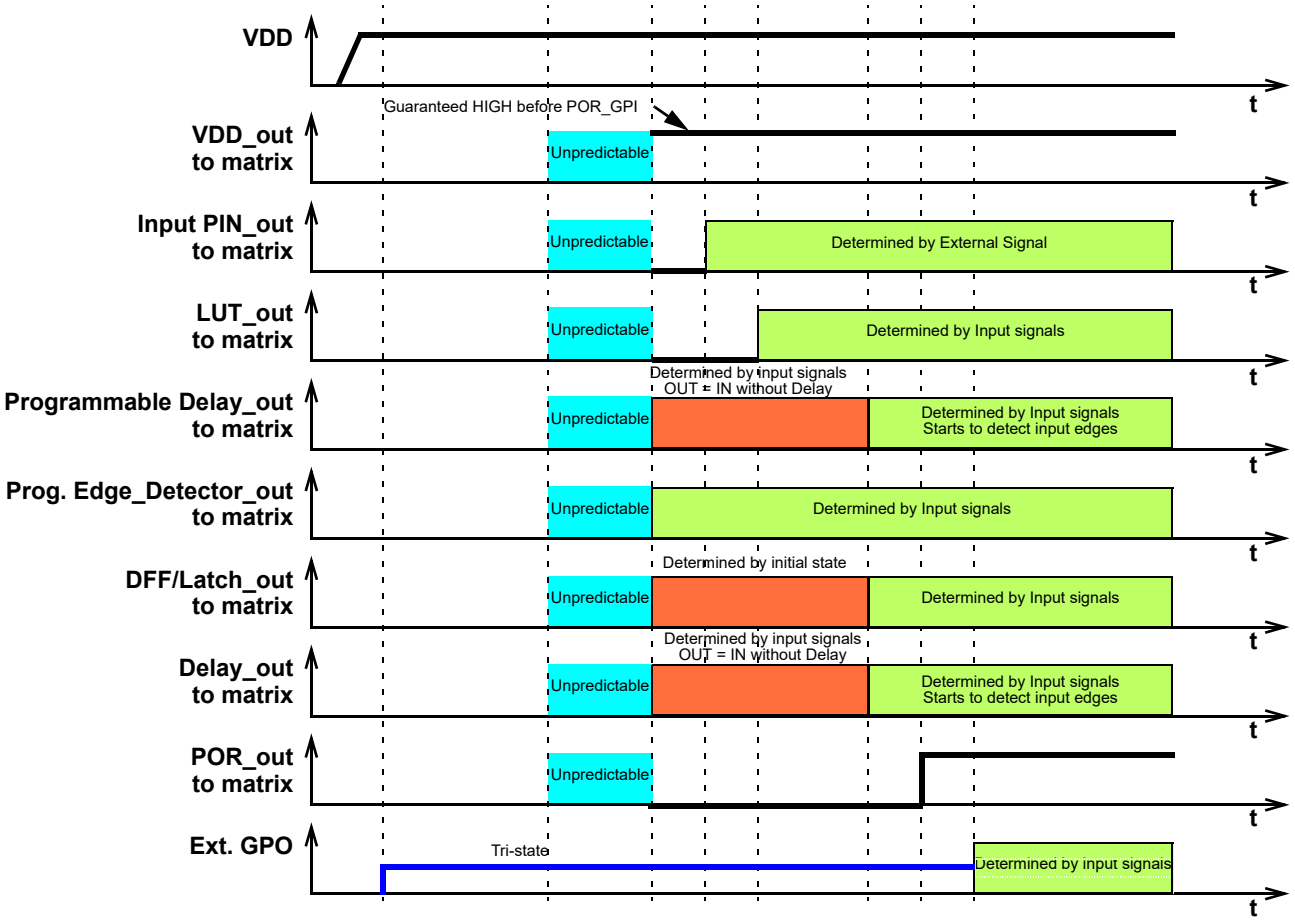


Figure 94. Internal Macrocell States during POR sequence

22.4 Initialization

All internal macrocells by default have initial low level. Starting from indicated powerup time of 1.15 V - 1.6 V, macrocells in GPAK4 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input PINs, ACMP, pull up/down;
2. LUTs;
3. DFFs, Delays/Counters, Pipe Delay;
4. POR output to matrix;
5. Output PIN corresponds to the internal logic

The VREF output pin driving signal can precede POR output signal going high by 3 μs - 5 μs. The POR signal going high indicates the mentioned powerup sequence is complete.

Note: The maximum voltage applied to any PIN should not be higher than the VDD level. There are ESD Diodes between PIN –> VDD and PIN –> GND on each PIN. So if the input signal applied to PIN is higher than VDD, then current will sink through the diode to VDD. Exceeding VDD results in leakage current on the input PIN, and VDD will be pulled up, following the voltage on the input PIN.There is no effect from input pin when input voltage is applied at the same time as VDD.

22.5 Power Down

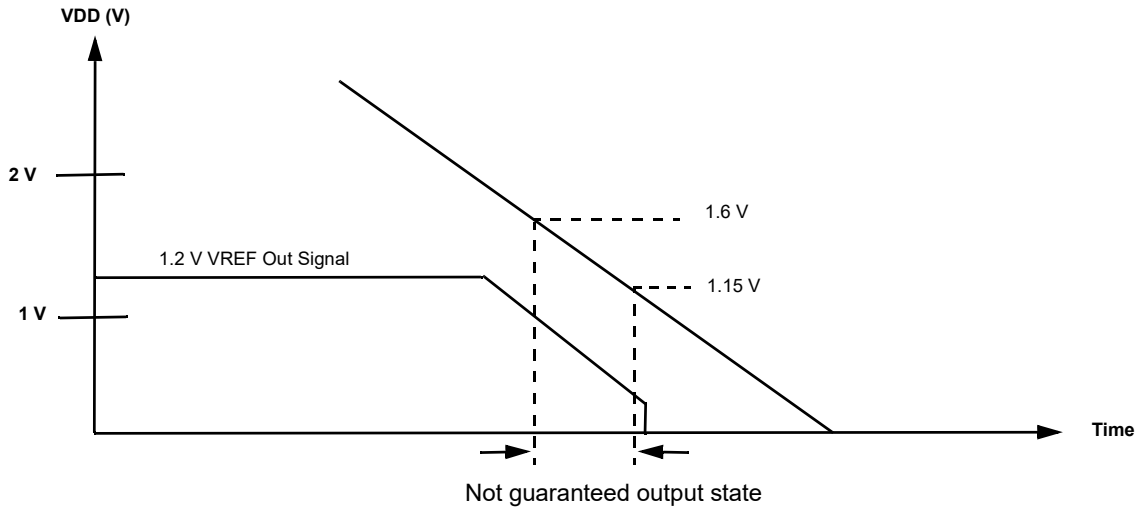


Figure 95. Power Down

During powerdown, macrocells in SLG46140 are powered off after VDD falling down below Power Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

22.6 POR Register Settings

Table 81. POR Register Settings

Signal Function	Register Bit Address	Register Definition
Bypass V_{DD} to 1.8 V device. Only when power is 1.8 V	<1003>	0: 1.8 V use regulator 1: Bypass VDD as 1.8 V device power
Input pad enable to core nRST delay 500 μs enable	<1004>	0: Delay 4 μs 1: Delay 500 μs
POR Auto Power Detect	<1005>	0: Enable 1: Disable

22.7 External reset

The SLG46140 has an optional External Reset function on Pin2. It allows to reset the chip while powered on.
Pin2 must be configured as Digital Input reg<762:761> and function Reset must be enabled also, reg<1002>: 0 - disabled, 1 - enabled. Unlike POR, External Reset affects only GPI, LUTs, DLY, RC OSC, DFFs, Latches, Pipe Delay, Matrix and GPO. While NVM remains its previous state, see *Figure 96* to *Figure 98*.

Note that during External Reset the output pin's status will depend on the OE control circuits and current consumption is determined by the design.

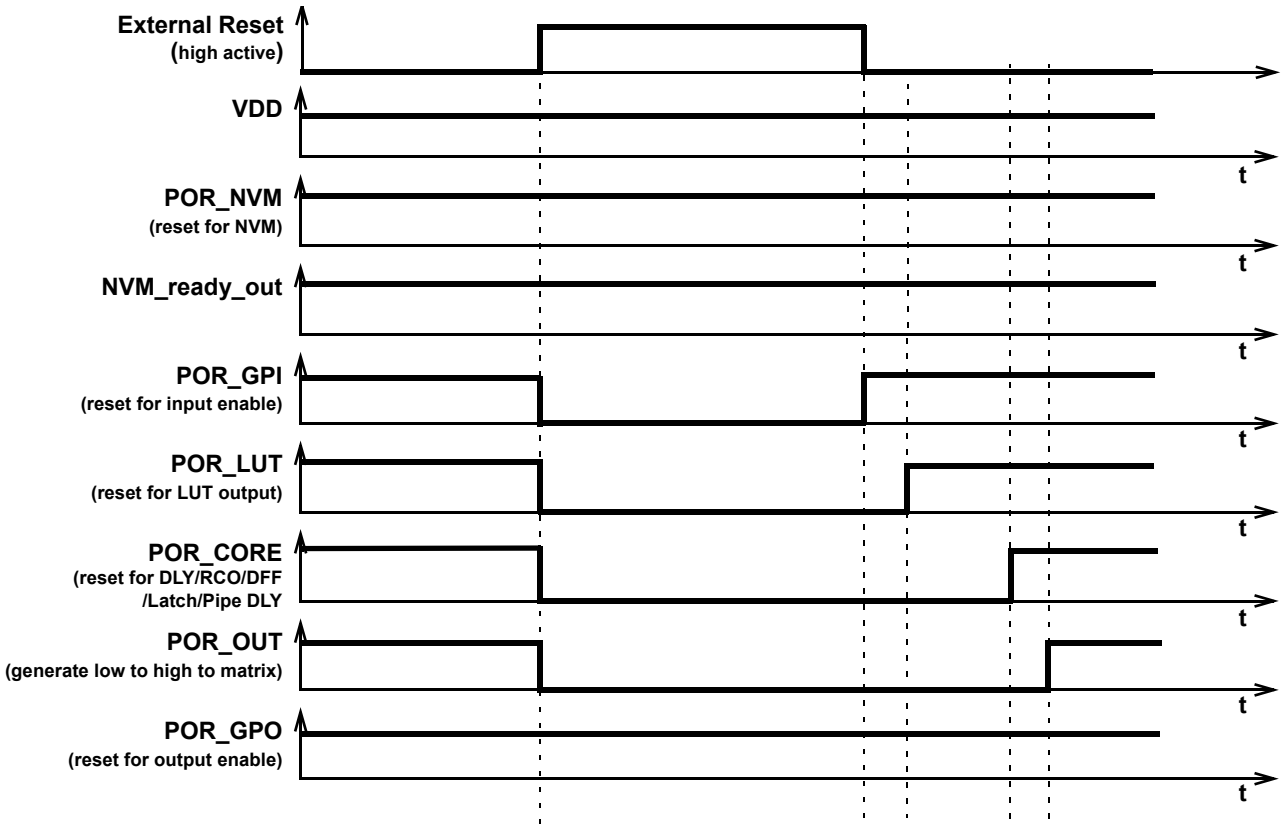


Figure 96. External reset sequence (High active).

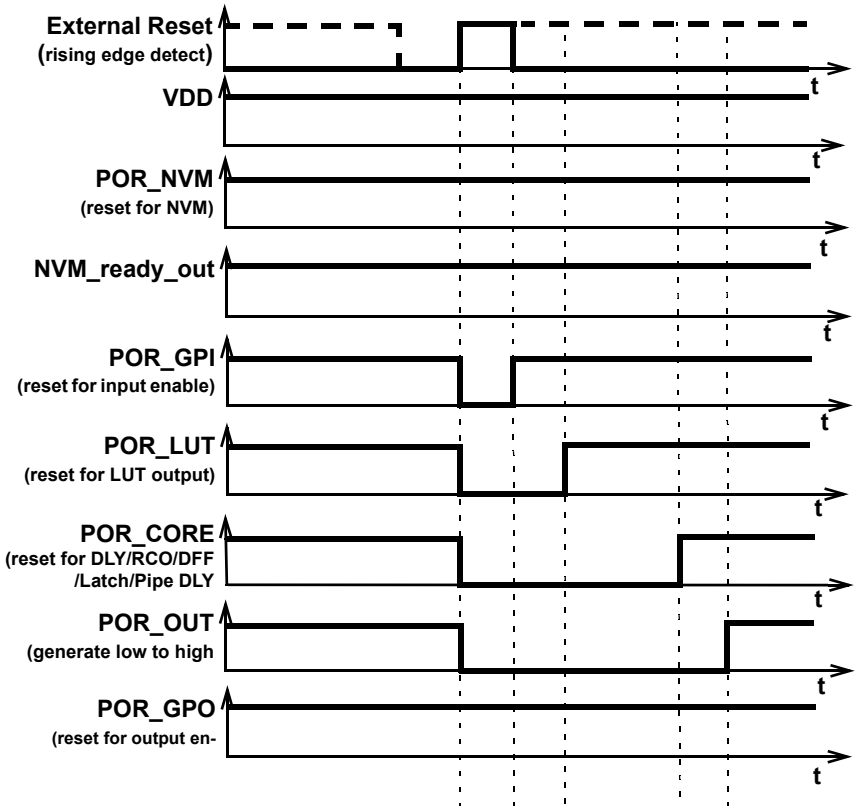


Figure 97. External reset sequence (Rising edge detect).

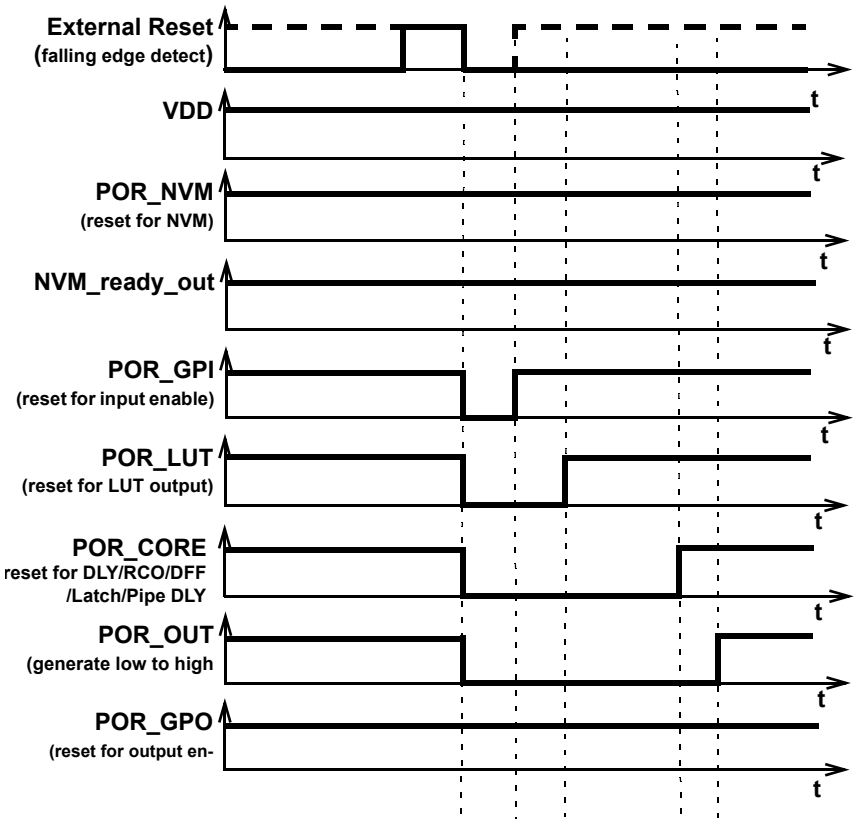


Figure 98. External reset sequence (Falling edge detect).

Table 82. External reset Register Settings

Signal Function	Register Bit Address	Register Definition
Pin2 edge reset enable	reg<1000>	0: edge reset enable (controlled by reg<1001>) 1: high level reset
Pin2 rising/falling edge reset	reg<1001>	0: rising 1: falling
Pin2 reset function	reg<1002>	0: disable 1: enable

23.0 Appendix A - SLG46140 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg<5:0>	in0 of LUT2_0 (out0)	
reg<11:6>	in1 of LUT2_0 (out1)	
reg<17:12>	in0 of LUT2_1 (out2)	
reg<23:18>	in1 of LUT2_1 (out3)	
reg<29:24>	in0 of LUT2_2 (out4)	
reg<35:30>	in1 of LUT2_2 (out5)	
reg<41:36>	in0 of LUT2_3 (out6)	
reg<47:42>	in1 of LUT2_3 (out7)	
reg<53:48>	in0 of LUT2_4 / data of DFF/Latch 0 (out8)	
reg<59:54>	in1 of LUT2_4 / clock of DFF/Latch 0 (out9)	
reg<65:60>	in0 of LUT2_5 / data of DFF/Latch 1 (out10)	
reg<71:66>	in1 of LUT2_5 / clock of DFF/Latch 1 (out11)	
reg<77:72>	in0 of LUT3_0 (out12)	
reg<83:78>	in1 of LUT3_0 (out13)	
reg<89:84>	in2 of LUT3_0 (out14)	
reg<95:90>	in0 of LUT3_1 (out15)	
reg<101:96>	in1 of LUT3_1 (out16)	
reg<107:102>	in2 of LUT3_1 (out17)	
reg<113:108>	in0 of LUT3_2 (out18)	
reg<119:114>	in1 of LUT3_2 (out19)	
reg<125:120>	in2 of LUT3_2 (out20)	
reg<131:126>	in0 of LUT3_3 (out21)	
reg<137:132>	in1 of LUT3_3 (out22)	
reg<143:138>	in2 of LUT3_3 (out23)	
reg<149:144>	in0 of LUT3_4 / resetb of DFF/Latch 2 (out24)	
reg<155:150>	in1 of LUT3_4 / data of DFF/Latch 2 (out25)	
reg<161:156>	in2 of LUT3_4 / clock of DFF/Latch 2 (out26)	
reg<167:162>	in0 of LUT3_5 / resetb of DFF/Latch 3 (out27)	
reg<173:168>	in1 of LUT3_5 / data of DFF/Latch 3 (out28)	
reg<179:174>	in2 of LUT3_5 / clock of DFF/Latch 3 (out29)	
reg<185:180>	in0 of LUT4_0 (out30)	
reg<191:186>	in1 of LUT4_0 (out31)	
reg<197:192>	in2 of LUT4_0 or PGEN (out32)	
reg<203:198>	in3 of LUT4_0 or PGEN (out33)	
reg<209:204>	nRST of DFF/Latch 4 (out34)	
reg<215:210>	data of DFF/Latch 4 (out35)	
reg<221:216>	clock of DFF/Latch 4 (out36)	
reg<227:222>	nRST of DFF/Latch 5 (out37)	
reg<233:228>	data of DFF/Latch 5 (out38)	
reg<239:234>	clock of DFF/Latch 5 (out39)	
reg<245:240>	clock of pipe delay / in0 of LUT3_6 (out40)	

Register Bit Address	Signal Function	Register Bit Definition
reg<251:246>	in of pipe delay / in1 of LUT3_6 (out41)	
reg<257:252>	porb of pipe delay / in2 of LUT3_6 (out42)	
reg<263:258>	input of edge detector and programmable delay (out43)	
reg<269:264>	digital output of PIN3 (out44)	
reg<275:270>	oe of PIN3 (out45)	
reg<281:276>	digital output of PIN4 (out46)	
reg<287:282>	oe of PIN4 (out47)	
reg<293:288>	digital output of PIN5 (out48)	
reg<299:294>	oe of PIN5 (out49)	
reg<305:300>	digital output of PIN6 (out50)	
reg<311:306>	digital output of PIN7 (out51)	
reg<317:312>	oe of PIN7 (out52)	
reg<323:318>	digital output of PIN9 (out53)	
reg<329:324>	oe of PIN9 (out54)	
reg<335:330>	digital output of PIN10 (out55)	
reg<341:336>	digital output of PIN11 (out56)	
reg<347:342>	digital output of PIN12 (out57)	
reg<353:348>	oe of PIN12 (out58)	
reg<359:354>	digital output of PIN13 (out59)	
reg<365:360>	oe of PIN13 (out60)	
reg<371:366>	digital output of PIN14 (out61)	
reg<377:372>	oe of PIN14 (out62)	
reg<383:378>	ADC power down (1: power down) (out63)	
reg<389:384>	pdb(power down) for acmp0 (0: power down) (out64)	
reg<395:390>	pdb(power down) for acmp1 (0: power down) (out65)	
reg<401:396>	oscillator power down (1: power down) (out66)	
reg<407:402>	counter external clock in3 of LUT4_1 (out67)	
reg<413:408>	input of dly/cnt0 (out68)	
reg<419:414>	input of dly/cnt1 (out69)	
reg<425:420>	input of dly/cnt2 in0 of LUT4_1(out70)	
reg<431:426>	keep of dly/cnt2 (fsm0) in1 of LUT4_1 (out71)	
reg<437:432>	up of dly/cnt2 (fsm0) in2 of LUT4_1 (out72)	
reg<443:438>	input of dly/cnt3 in0 of LUT3_7 (out73)	
reg<449:444>	keep of dly/cnt3 (fsm1) in1 of LUT3_7 (out74)	
reg<455:450>	up of dly/cnt3 (fsm1) in2 of LUT3_7 (out75)	
reg<461:456>	PWM/DCMP0 positive input and PWM/DCMP1 negative input register selection bit 0 (out76)	
reg<467:462>	PWM/DCMP0 positive input and PWM/DCMP1 negative input register selection bit 1 (out77)	
reg<473:468>	PWM power down (1: power down) (out78)	
reg<479:474>	csb of SPI (out79)	
reg<485:480>	sclk of SPI (out80)	

Register Bit Address	Signal Function	Register Bit Definition
Programmable Delay		
reg<487:486>	Mode selection	00: rising edge detect 01: falling edge detect 10: both edge detect 11: both edge delay
reg<489:488>	Delay time selection	00: 110 ns delay 01: 220 ns delay 10: 330 ns delay 11: 440 ns delay
reg<490>	Output delay control	0: output no delay 1: output delay
Bandgap/Reference		
reg<495:491>	Reserved	
reg<500:496>	ACMP0 vref value selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: vref_ext_acmp1 11011: vref_ext_acmp0 11100: vref_ext_acmp1 / 2 11101: vref_ext_acmp0 / 2 11100: DAC1_out 11111: DAC0_out
reg<505:501>	ACMP1 vref value selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: vref_ext_acmp1 11011: vref_ext_acmp0 11100: vref_ext_acmp1 / 2 11101: vref_ext_acmp0 / 2 11100: DAC1_out 11111: DAC0_out
reg<506>	Reserved	
reg<507>	Bandgap OK for ADC, ACMP output delay time select, the start time is porb_core go to high	0: 550 us 1:100 us

Register Bit Address	Signal Function	Register Bit Definition
reg<509:508>	ACMP1 hysteresis control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<511:510>	ACMP0 hysteresis control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<512>	Bandgap turn on by register	0: off 1: turn on (if chip is power down, the bandgap will power down even if it is set to 1)
reg<513>	Reserved	
reg<514>	Reserved	
reg<515>	Reserved	
ADC and ACMP		
reg<517:516>	ACMP 1 input selection	00: Pin9 input 01: ADC PGA out 10: Pin10 input 11: none
reg<518>	ACMP 1 low bandwidth enable	0: disable 1: enable
reg<520:519>	ACMP 1 gain control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
reg<521>	ACMP wake sleep enable	0: disable 1: enable
reg<523:522>	ACMP 0 gain control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
reg<524>	ACMP 0 low bandwidth enable	0: disable 1: enable
reg<526:525>	ACMP 0 input selection	00: Pin10 input 01: PGA out 10: VDD 11: none
reg<528:527>	Output buffer source selection	00: buffer power down 01: ACMP0's in 10: ACMP1's in 11: DAC0's output
reg<529>	ADC negative input from internal DAC0	0: disable 1: enable
reg<530>	Multichannel input Mux enable (controlled by pin11)	0: disable (pin11 can not control) 1: enable
reg<531>	ADC input mode control	0:single ended 1: differential input

Register Bit Address	Signal Function	Register Bit Definition
reg<534:532>	ADC PGA gain selection	000: 0.25x (For single-ended operation only) 001: 0.5x (For single-ended operation only) 010: 1x 011: 2x 100: 4x 101: 8x (For single-ended and differential operation) 110: 16x (For differential operation only) 111: Reserved
reg<535>	PGA power on signal	0: power down 1: power on Note: in ADC wake sleep/dynamic on/off mode, it should set to 0
reg<536>	ADC Pseudo-Differential mode enable	0: disable 1: enable
reg<537>	Reserved	
reg<538>	DAC1 power on signal	0: power down 1: power on When DAC0 used only, need set this bit
reg<539>	Reserved	
reg<540>	ACMP 0 input 100u current source enable	0: disable 1: enable
reg<541>	ACMP 1 input 100u current source enable	0: disable 1: enable
reg<543:542>	ADC speed selection	00: Reserved 01: Reserved 10: 100 kHz 11: Reserved
reg<544>	DAC0 power on signal	0: power down 1: power on When DAC0 used only, need set this bit
reg<546:545>	ADC vref source select	00: ADC V_{REF} 01: Reserved 10: 1/4 Vdd 11: None
reg<547>	DAC0 input selection	0: from register 1: from DCMP1's input
reg<555:548>	DAC0 8 bit register control	00: DAC0 output is 0 FF: DAC0's output is 1 v
reg<556>	DAC1 input selection	0: from DCMP1's input 1: all input are 0
reg<557>	ADC wake sleep enable	0: disable 1: enable
reg<558>	force ADC analog part on	0: disable 1: enable
reg<559>	PGA output enable	0: disable 1: enable
LF OSC		

Register Bit Address	Signal Function	Register Bit Definition
reg<561:560>	Clock divide ratio control for LF osc	00: /1 01: /2 10: /4 11: /16
reg<562>	Matrix power down (matrix_out66)enable for LF oscillator	0: disable 1: enable
reg<563>	Low Frequency osc turn on by register	0: off 1: turn on (if chip is power down, the LFosc will power down even if it is set to 1)
RC OSC		
reg<564>	RC osc turn on by register	0: off 1: turn on (if chip is power down, the RCosc will power down even if it is set to 1)
reg<565>	RC osc frequency select	0:25 KHz 1:2 MHz
reg<566>	Current source in RC osc always turn on enable, it shorten the RC oscillator start up time but with 200nA DC current on.	0: disable 1: enable
reg<567>	Matrix power down (matrix_out66)enable for RC oscillator	0: disable 1: enable
reg<569:568>	Clock divide ratio control for RC osc	00: /1 01:/2 10:/4 11: /8
reg<570>	RC osc clock to matrix input enable	0: disable 1: enable
reg<573:571>	Clock divide ratio control for RC osc to matrix	000: /1 001:/2 010:/4 011: /3 100: /8 101: /12 110: /24 111: /64
Ring OSC		
reg<574>	Ring osc turn on by register	0: off 1: turn on (if chip is power down, the Ring Osc will power down even if it is set to 1)
reg<575>	Matrix power down (matrix_out66)enable for ring oscillator	0: disable 1: enable
reg<577:576>	Clock divide ratio control for ring osc	00: /1 01:/4 10:/8 11: /16
reg<578>	ADC clock divide by 16 BYPASS	0: no bypass 1: bypass
reg<580:579>	PWM and ADC clock source select	00: CK_RINGOSC 01:CK_MATRIX(matrix_out67) 10:CK_RCOSC 11:CK_SPI_SCLK(matrix_out80)
reg<581>	Ring osc clock to matrix input enable	0: disable 1: enable

Register Bit Address	Signal Function	Register Bit Definition
reg<584:582>	clock divide ratio control for ring osc to matrix	000: /1 001:/2 010:/4 011: /3 100: /8 101: /12 110: /24 111: /64
reg<585>	ADC data synchronized with SPI clock enable	0: disable 1: enable
reg<586>	PWM data synchronized with SPI clock enable	0: disable 1: enable
reg<587>	FSM data synchronized with SPI clock enable	0: disable 1: enable
PWM/DCMP 2		
reg<588>	PWM/DCMP2 clock source selection	0:clock from mux controlled by reg[580:579] 1: matrix_out67
reg<589>	PWM/DCMP2 function selection	0: PWM 1: DCMP. when in PWM mode, OUTN2 is pwm2's negative output. when in DCMP mode, OUTN2 is dcmp2's match output
reg<590>	PWM/DCMP2 turn on by register	0: disable 1: enable
reg<591>	PWM/DCMP2 clock inversion	0: disable 1: enable
reg<592>	PWM/DCMP2 mode selection	0: PWM output duty cycle down to 0% and DCMP out=1 if A>B, 1: PWM output duty cycle up to 100% and DCMP out=1 if A>=B
reg<594:593>	PWM2 dead band zone control	00: 10 ns 01: 20 ns 10:40 ns 11:80 ns
reg<596:595>	PWM/DCMP2 positive input source selection	00: ADC 01: 8MSBs SPI 10: FSM0[7:0] 11: reg3
reg<598:597>	PWM/DCMP2 negative input	00: FSM0[7:0] 01:reg2 10: 8LSBs SPI 11:CNT1_Q[7:0]
PWM/DCMP 1		
reg<599>	PWM/DCMP1 clock source selection	0:clock from mux controlled by reg<580:579> 1: matrix_out67
reg<600>	PWM/DCMP1 function selection	0: PWM 1: DCMP. when in PWM mode, OUTN1 is pwm1's negative output. when in DCMP mode, OUTN1 is dcmp1's match output
reg<601>	PWM/DCMP1 turn on by register	0: disable 1: enable
reg<602>	PWM/DCMP1 clock inversion	0: disable 1: enable

Register Bit Address	Signal Function	Register Bit Definition
reg<603>	PWM/DCMP1 mode selection	0: PWM output duty cycle down to 0% and DCMP out=1 if A>B 1: PWM output duty cycle up to 100% and DCMP out=1 if A>=B
reg<605:604>	PWM1 dead band zone control	00: 10 ns 01: 20 ns 10: 40 ns 11: 80 ns
reg<607:606>	PWM/DCMP1 positive input source selection	00: ADC 01: 8LSBs SPI 10: FSM1[7:0] 11: reg1
reg<609:608>	PWM/DCMP1 negative input	00: FSM1[7:0] 01:regs from MUX controlled by matrix_out[77:76] 10: 8MSBs SPI 11:FSM0[7:0]
PWM/DCMP 0		
reg<611>	PWM/DCMP0 function selection	0: PWM 1: DCMP. when in PWM mode, OUTN0 is pwm0's negative output. when in DCMP mode, OUTN0 is dcmp0's match output
reg<612>	PWM/DCMP0 turn on by register	0: disable 1: enable
reg<613>	PWM/DCMP0 clock inversion	0: disable 1: enable
reg<614>	PWM/DCMP0 mode selection	0: PWM output duty cycle down to 0% and DCMP out=1 if A>B, 1: PWM output duty cycle up to 100% and DCMP out=1 if A>=B.
reg<616:615>	PWM0 dead band zone control	00: 10 ns 01: 20 ns 10: 40 ns 1 1: 80 ns
reg<618:617>	PWM/DCMP0 positive input source selection	00: ADC 01: 8MSBs SPI 10: FSM0[7:0] 11: regs from MUX controlled by matrix_out[77:76]
reg<620:619>	PWM/DCMP0 negative input	00: FSM0[7:0] 01:reg0 10: 8LSBs SPI 11:FSM1[7:0]
PWM/DCMP or DAC Data		
reg<628:621>	reg0, 8 bits NVM data to PWM/DCMP or DAC input	data
reg<636:629>	reg1, 8 bits NVM data to PWM/DCMP or DAC input	data
reg<644:637>	reg2, 8 bits NVM data to PWM/DCMP or DAC input	data
reg<652:645>	reg3, 8 bits NVM data to PWM/DCMP or DAC input	data
reg<653>	power down sync to clock and output state control in power down mode	0: power down is not synchronized with clock, and output reset to 0 when PWM/DCMP is power down, 1: power down is synchronized with clock, when PD=0, the clock is enabled after 2 clock cycles, while when PD=1, the clock is gated immediately. and the output is kept at current state when PD=1.
SPI		

Register Bit Address	Signal Function	Register Bit Definition
reg<654>	SPI used as ADC/FSM buffer enable (1 clock delayed)	1: enable
reg<655>	SPI parallel input data source selection	0: FSM0[7:0],FSM1[7:0] 1: ADC
reg<656>	SPI clock phase (CHPA)	refer to SPI spec
reg<657>	SPI clock polarity (CHOL)	refer to SPI spec
reg<658>	byte selection	0: 16 bits 1: 8 bits (less significant 8 bits)
reg<659>	SPI input/output mode selection	0: Serial In Parallel out 1: Parallel In Serial out
reg<660>	CNT test enable	0: disable 1: enable
LUT3_7 or CNT3/DLY/FSM		
reg<668:661>	LUT3_7 data (if reg<677:676>=11) or CNT3/DLY/FSM 8-bits data	data
reg<669>	CNT3 Value Control	0: Reset (CNT value = 0) 1: Set (CNT value = FSM data)
reg<673:670>	DLY3/CNT3/FSM1 clock source select	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END2 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM. 1101: Reserved 1110: Reserved 1111: Reserved
reg<675:674>	DLY3 edge mode select	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<677:676>	DLY/CNT3 macrocell function select	00: DLY0 01: CNT/FSM 10: edge detect 11: 3bit LUT3_7
reg<679:678>	FSM1 input data source select	00: 8 bits NVM data 01: 8 bits ADC data 10: 0 11: 8LSBs SPI parallel data
DLY2/CNT2/FSM0 or LUT4_1		
reg<693:680>	LUT4_1 data [bits 13:0] (if reg<702:701>=11) or DLY2/CNT2/FSM0 data	data

Register Bit Address	Signal Function	Register Bit Definition
reg<694>	LUT4_1 data [bit 14] (if reg<702:701>=11) or CNT2 Value Control	0: Reset (CNT value = 0) 1: Set (CNT value = FSM data)
reg<698:695>	reg<698>LUT4_1 data [bit 15] (if reg<702:701>=11) or DLY2/CNT2/FSM0 clock source select	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: DLY_OUT1 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
reg<700:699>	DLY2 edge mode select	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<702:701>	DLY/CNT2 macrocell function select	00: DLY 01: CNT/FSM 10: edge detect 11:4bit LUT4_1
reg<704:703>	FSM0 input data source select	00: 8 bits NVM data 01: 8bits ADC data 10: 0 11: 8MSBs SPI parallel data
DLY1/CNT1		
reg<712:705>	CNT1 8-bits data from register	data
reg<713>	CNT1's Q are set to 1s or reset 0s selection	0: reset to 0s 1: set to Data
reg<717:714>	DLY1/CNT1 clock source select	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: DLY_OUT0 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM

Register Bit Address	Signal Function	Register Bit Definition
reg<719:718>	DLY1 edge mode select	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<721:720>	DLY/CNT1 macrocell function select	00: DLY 01: CNT/FSM 10: edge detect 11: 3bit LUT
DLY0/CNT0		
reg<735:722>	CNT0 14bits data from register	data
reg<736>	CNT0's Q are set to 1s or reset 0s selection	0: reset to 0s 1: set to Data
reg<740:737>	DLY0/CNT0 clock source select	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: DLY_OUT3 0110: matrix_out67 0111: matrix_out67 divide by 8 1000: CK_RINGOSC 1001: matrix_out80(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM
reg<742:741>	DLY0 edge mode select	If DLY Mode or Edge Detect: 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT/FSM: 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<744:743>	DLY/CNT0 macrocell function select	00: DLY 01: CNT/FSM 10: edge detect 11: 3bit LUT
reg<745>	Wake sleep output state when ws oscillator is powered down	0: in power down mode 1: in normal operation state
reg<746>	RC osc and LF osc bypass enable	0:disable 1: enable Clock is from matrix_out67
reg<749:747>	Reserved (need to set to 0)	data = 000
LUT3_6 or Pipe Delay		
reg<757:750>	LUT3_6 Data (if reg.<759>=0) or Pipe Delay	

Register Bit Address	Signal Function	Register Bit Definition
reg<753:750>	Pipe Delay out0 selection bits	register bits from 0 to 15, data delay from 1 to 16 pipes
reg<757:754>	Pipe Delay out1 selection bits	register bits from 0 to 15, data delay from 1 to 16 pipes
reg<758>	out1 output polarity control.	0: non-inverted 1: inverted
reg<759>	function selection	0: PIPE Delay 1: 3-bit LUT
All PINs		
reg<760>	IO precharge enable bit	0: disable 1: enable
PIN 2		
reg<762:761>	PIN2 mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in
reg<764:763>	PIN2 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<765>	PIN2 pull up resistor enable	0: pull down 1: pull up
PIN 3		
reg<767:766>	PIN3 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO
reg<769:768>	PIN3 output mode control	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<771:770>	PIN3 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<772>	PIN3 pull up resistor enable	0: pull down 1: pull up
PIN 4		
reg<774:773>	PIN4 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO
reg<776:775>	PIN4 output mode control.	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<778:777>	PIN4 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<779>	PIN4 pull up resistor enable	0: pull down 1: pull up
PIN 5		

Register Bit Address	Signal Function	Register Bit Definition
reg<781:780>	PIN5 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO
reg<783:782>	PIN5 output mode control.	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<785:784>	PIN5 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<786>	PIN5 pull up resistor enable	0: pull down 1: pull up
PIN 6		
reg<787>	Reserved	
reg<790:788>	PIN6 input mode control	000: digital in without schmitt trigger 001: digital in with schmitt trigger 010: Low Voltage Digital in 011: analog IO 100: push-pull mode 101: NMOS open-drain 110: PMOS open-drain 111: analog IO and NMOS open-drain mode
reg<792:791>	PIN6 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<793>	PIN6 pull up resistor enable	0: pull down 1: pull up
reg<794>	PIN6 output driver current x2 enable	0: disable 1: enable
PIN 7		
reg<796:795>	PIN7 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO
reg<798:797>	PIN7 output mode control	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<800:799>	PIN7 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<801>	PIN7 pull up resistor enable	0: pull down 1: pull up
PIN 9		
reg<803:802>	PIN9 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO

Register Bit Address	Signal Function	Register Bit Definition
reg<805:804>	PIN9 output mode control.	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<807:806>	PIN9 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<808>	PIN9 pull up resistor enable	0: pull down 1: pull up
reg<809>	PIN9 4x Drive enable	0: disable 1: enable
PIN 10		
reg<810>	Reserved	
reg<813:811>	PIN10 input mode control	000: digital in without schmitt trigger 001: digital in with schmitt trigger 010: Low Voltage Digital in 011: analog IO 100: push-pull mode 101: NMOS open-drain 110: PMOS open-drain 111: analog IO and NMOS open-drain mode
reg<815:814>	PIN10 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<816>	PIN10 pull up resistor enable	0: pull down 1: pull up
reg<817>	PIN10 output driver current x2 enable	0: disable 1: enable
reg<818>	PIN10 4x Drive enable	0: disable 1: enable
PIN 11		
reg<819>	Reserved	
reg<822:820>	PIN11 input mode control	000: digital in without schmitt trigger 001: digital in with schmitt trigger 010: Low Voltage Digital in 011: analog IO 100: push-pull mode 101: NMOS open-drain 110: PMOS open-drain 111: analog IO and NMOS open-drain mode
reg<824:823>	PIN11 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<825>	PIN11 pull up resistor enable	0: pull down 1: pull up
reg<826>	PIN11 output driver current x2 enable	0: disable 1: enable
PIN 12		

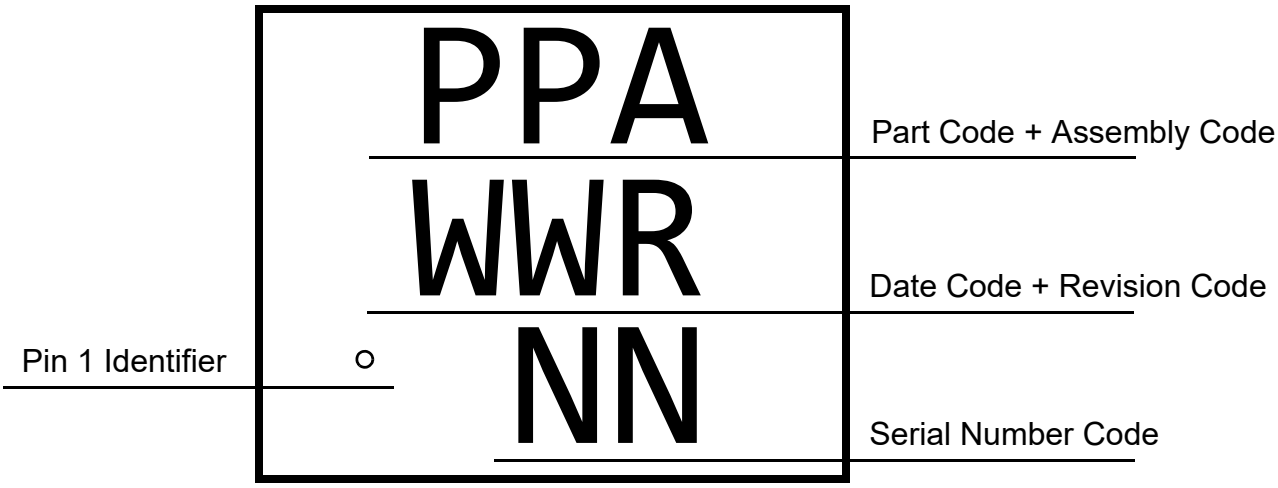
Register Bit Address	Signal Function	Register Bit Definition
reg<828:827>	PIN12 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO
reg<830:829>	PIN12 output mode control.	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<832:831>	PIN12 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<833>	PIN12 pull up resistor enable	0: pull down 1: pull up
PIN 13		
reg<835:834>	PIN13 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO
reg<837:836>	PIN13 output mode control.	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<839:838>	PIN13 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<840>	PIN13 pull up resistor enable	0: pull down 1: pull up
PIN 14		
reg<842:841>	PIN14 input mode control	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: Low Voltage Digital in 11: analog IO
reg<844:843>	PIN14 output mode control.	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
reg<846:845>	PIN14 pull up/down resistor selection	00: floating 01: 10 K 10: 100 K 11: 1 M
reg<847>	PIN14 pull up resistor enable	0: pull down 1: pull up
LUT2_0		
reg<851:848>	LUT2_0 data	Data
LUT2_1		
reg<855:852>	LUT2_1 data	Data
LUT2_2		
reg<859:856>	LUT2_2 data	Data
LUT2_3		

Register Bit Address	Signal Function	Register Bit Definition
reg<863:860>	LUT2_3 data	Data
LUT2_4 or DFF/Latch0		
reg<867:864>	LUT2_4 Data (if reg<868>=0) or DFF/Latch0	
reg<864>	DFF/Latch Mode Select	0: DFF function 1: Latch function
reg<865>	DFF/Latch output polarity control	0: Q output 1: QB output
reg<866>	DFF/Latch initial state during POR	0: initial state is 0 1: initial state is 1
reg<867>	Unused if DFF/Latch Function Selected	Unused if DFF/Latch Function Selected
reg<868>	Function Selection	0: LUT2 function 1: DFF/Latch function.
LUT2_5 or DFF/Latch1		
reg<872:869>	LUT2_5 Data (if reg.<873>=0) or DFF/Latch1	
reg<869>	DFF/Latch Mode Select	0: DFF function 1: Latch function
reg<870>	DFF/Latch output polarity control	0: Q output 1: QB output
reg<871>	DFF/Latch initial state during POR	0: initial state is 0 1: initial state is 1
reg<872>	Unused if DFF/Latch Function Selected	Unused if DFF/Latch Function Selected
reg<873>	Function Selection.	0: LUT2 function 1: DFF/Latch function.
LUT3_0		
reg<881:874>	LUT3 data	Data
LUT3_1		
reg<889:882>	LUT3 data	Data
LUT3_2		
reg<897:890>	LUT3 data	Data
LUT3_3		
reg<905:898>	LUT3 data	Data
LUT3_4 or DFF/Latch2		
reg<913:906>	LUT3_4 Data (if reg.<914>=0) or DFF/Latch2	
reg<906>	DFF/Latch Mode Select	0: DFF function 1: Latch function
reg<907>	DFF/Latch output polarity control	0: Q output 1: QB output
reg<908>	DFF/Latch set or reset selection	0: reset controlled by matrix 1: set controlled by matrix
reg<909>	DFF/Latch initial state during POR	0: initial state is 0 1: initial state is 1
reg<913:910>	Unused if DFF/Latch Function Selected	Unused if DFF/Latch Function Selected
reg<914>	Function Selection.	0: LUT3 function 1: DFF/Latch function.
LUT3_5 or DFF/Latch3		
reg<923:915>	LUT3_5 Data (if reg.<923>=0) or DFF/Latch3	

Register Bit Address	Signal Function	Register Bit Definition
reg<915>	DFF/Latch Mode Select	0: DFF function 1: Latch function
reg<916>	DFF/Latch output polarity control	0: Q output 1: QB output
reg<917>	DFF/Latch set or reset selection	0: reset controlled by matrix 1: set controlled by matrix
reg<918>	DFF/Latch initial state during POR	0: initial state is 0 1: initial state is 1
reg<922:919>	Unused if DFF/Latch Function Selected	Unused if DFF/Latch Function Selected
reg<923>	Function Selection	0: LUT3 function 1: DFF/Latch function
DFF/Latch4		
reg<924>	DFF/Latch mode select	0: DFF function 1: Latch function
reg<925>	DFF/Latch set or reset selection	0: reset controlled by matrix 1: set controlled by matrix
reg<926>	DFF/Latch initial state during POR	0: initial state is 0 1: initial state is 1
DFF/Latch5		
reg<927>	DFF/Latch mode select	0: DFF function 1: Latch function
reg<928>	DFF/Latch set or reset selection	0: reset controlled by matrix 1: set controlled by matrix
reg<929>	DFF/Latch initial state during POR	0: initial state is 0 1: initial state is 1
LUT4_0 or PGEN		
reg<945:930>	LUT4_0 data or PGEN data	Data
reg<949:946>	4-Bit Counter for PGEN	Data
reg <950>	Function Selection	0: LUT4 function 1: PGEN function.
Miscellaneous		
reg<957:951>	Reserved	
reg<963:958>	Reserved	
reg<971:964>	Reserved	
reg<977:972>	Reserved	
reg<983:978>	Reserved	
reg<991:984>	Reserved	
reg<992>	Reserved	Reserved
reg<993>	Reserved	
reg<995:994>	NVM load repeat time control	00: 1 time load & check 01: 2 times load & check 10: 3 times load & check 11: 4 times load & check.
reg<997:996>	SPI SDIO output control	0x: pin12 dout from matrix 0 (out57) 10: from SPI (SDO) 11: from ADC serial output

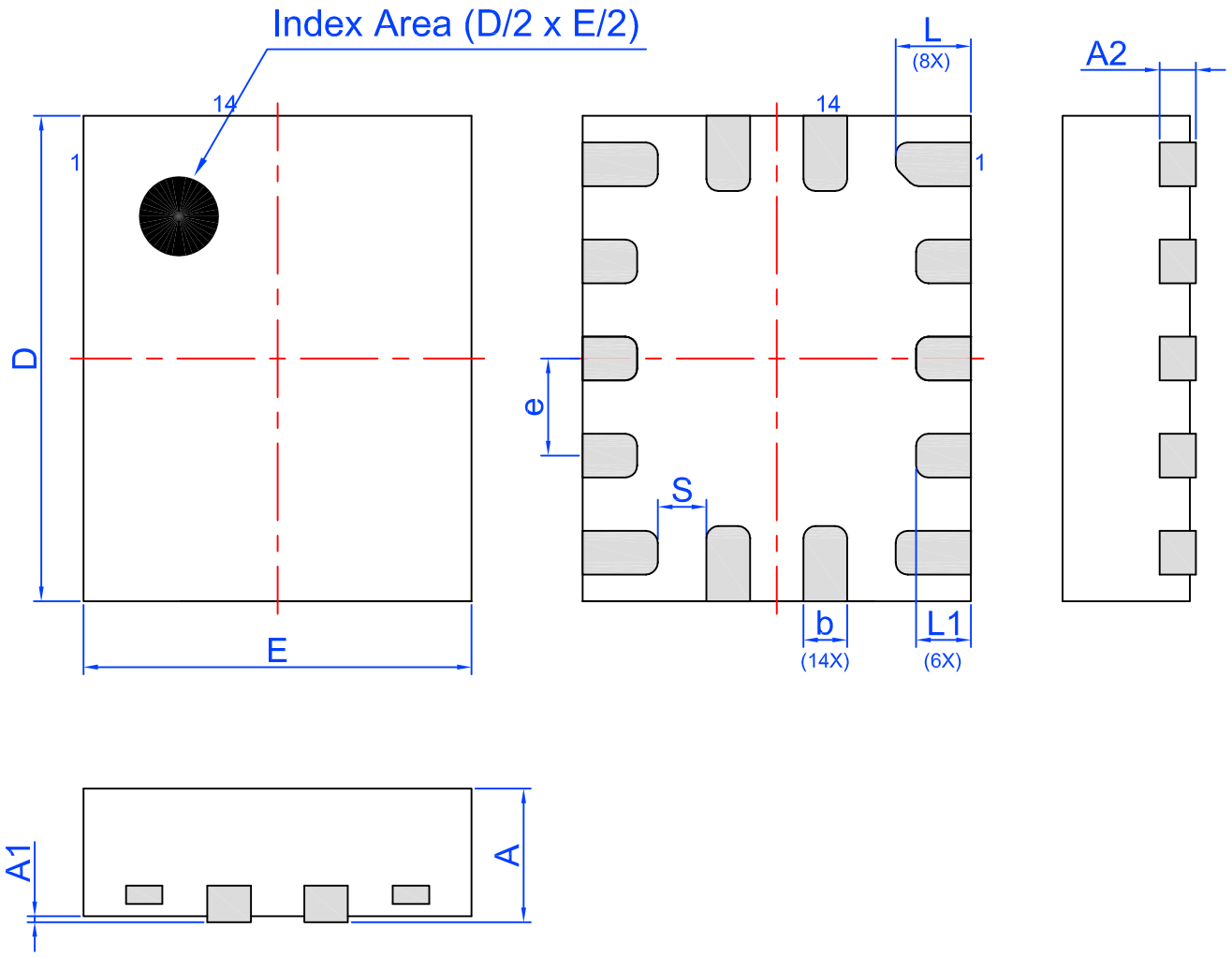
Register Bit Address	Signal Function	Register Bit Definition
reg<999:998>	reset output control from pin13	0x: digital output from pin13 10: reset output from pin13 11: digital output from pin13
PIN2 Reset Control		
reg<1000>		0: pin2 edge active 1: pin2 high active
reg<1001>		0: rising edge 1: falling edge
reg<1002>		0: disable 1: enable
POR and Regulator		
reg<1003>	Bypass V_{DD} to 1.8 V device. Only when power is 1.8 V	0: 1.8v use regulator 1: bypass vdd as 1.8v device power
reg<1004>	Input pad enable to core resetb delay 500us enable	0: delay 4us 1: delay 500us
reg<1005>	Disable power auto detector function for charge pump	0: enable 1: disable
reg<1006>	Reserved	
reg<1014:1007>	Pattern ID	Pattern ID
reg<1015>	Reserved	
reg<1023:1016>	Reserved	

24.0 Package Top Marking System Definition



25.0 Package Drawing and Dimensions

14 Lead STQFN FC Green Package 1.6 x 2.0 x 0.55 mm



Unit: mm

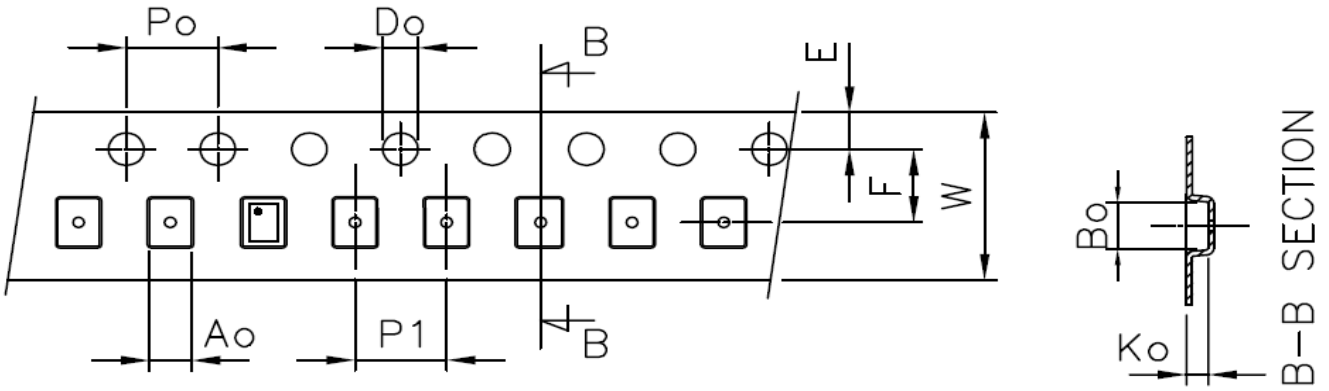
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

26.0 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2 mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178/60	100	400	100	400	8	4

26.1 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.8	4	4	1.5	1.75	3.5	8

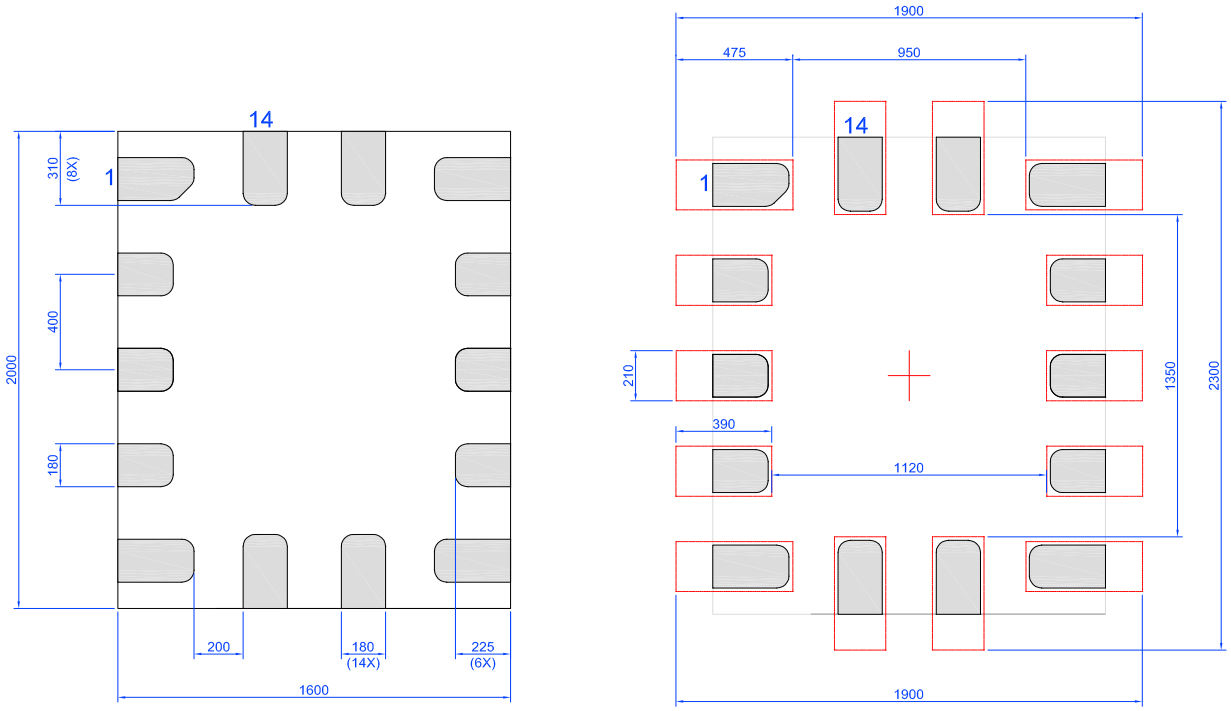


27.0 Recommended Land Pattern

Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)

Units: µm



28.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.76 mm^3 (nominal). More information can be found at www.jedec.org.

29.0 Revision History

Date	Version	Change
11/22/2017	1.09	Fixed typos
11/7/2017	1.08	Updated OSC Electrical Spec Fixed typos
10/11/2017	1.07	Updated Electrical Spec Fixed typos
10/2/2017	1.06	Fixed typos Updated ADC Typical Current Consumption
7/3/2017	1.05	Fixed typos
5/31/2017	1.04	Fixed typos Updated PGA Specification Conditions Updated POR section Updated Absolute Maximum Conditions and Electrical Characteristics
2/17/2017	1.03	Fixed typos
1/18/2017	1.02	Updated Silego Website & Support Updated Section Programmable Delay / Edge Detector Fixed typos
10/25/2016	1.01	Fixed typos
10/20/2016	1.00	Production Release

Silego Website & Support

Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit our website.

Our Green product lines feature:

GreenPAK: Programmable Mixed Signal Matrix products
GreenFET1 / GreenFET3 / HFET1: MOSFET Drivers and ultra-small, low RDSon Load Switches
GreenCLK1 / GreenCLK2 / GreenCLK3: Crystal replacement technology

Products are also available for purchase directly from Silego at the Silego Online Store at http://www.silego.com/buy/.

Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send e-mail requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

Contact Silego Directly

Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL:

http://support.silego.com/

Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of world wide Silego Technology offices and representatives are all available at http://www.silego.com/