Z-Communications, Inc.
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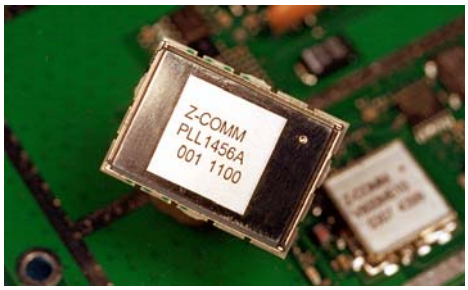
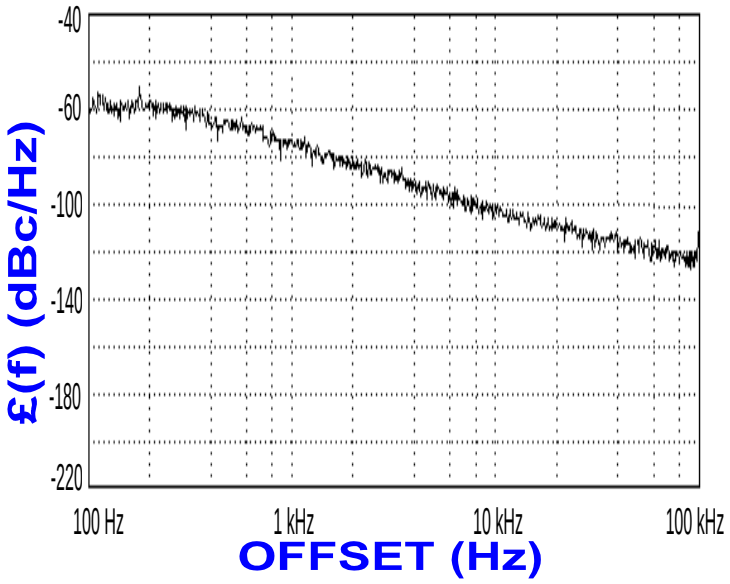
PSN1810A

PHASE LOCKED LOOP

Rev A1



PHASE NOISE (1 Hz BW, typical)



FEATURES

- Frequency Range: 1780 - 1840 MHz
- Step Size: 50 KHz
- PLL - Style Package

APPLICATIONS

- Telecommunications
- Satellite
- Telemetry

PERFORMANCE SPECIFICATIONS	VALUE	UNITS
Frequency Range	1780 - 1840	MHz
Phase Noise @ 10 kHz offset (1 Hz BW, typ.)	-101	dBc/Hz
Harmonic Suppression (2nd, typ.)	-15	dBc
Sideband Spurs (typ.)	-70	dBc
Power Output	4±2	dBm
Load Impedance	50	Ω
Step Size	50	KHz
Charge Pump Output Current	1000	µA
Switching Speed (typ., adjacent channel)	5	mSec
Startup Lock Time (typ.)	10	mSec
Operating Temperature Range	-40 to 85	°C
Package Style	PLL	
POWER SUPPLY REQUIREMENTS		
Supply Voltage (Vcc, nom.)	5	Vdc
Supply Current (Icc, typ.)	34	mA

All specifications are typical unless otherwise noted and subject to change without notice.

APPLICATION NOTES

- AN-107 : How to Solder Z-COMM VCOs / PLLs
- AN-200 : Mounting and Grounding of Z-COMM PLLs
- AN-201 : PLL Fundamentals AN-202 : PLL Functional Description

NOTES:

Reference Oscillator Signal: 5 MHz<f_{osc}<40 MHz
Frequency Synthesizer: National Semiconductor - LMX2326

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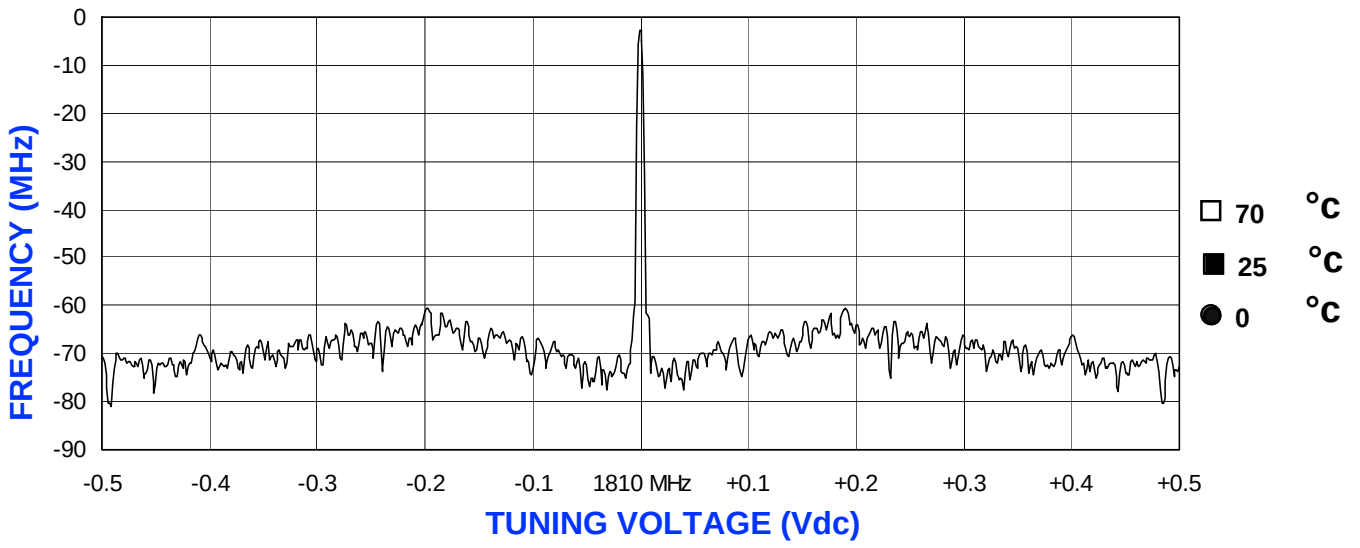
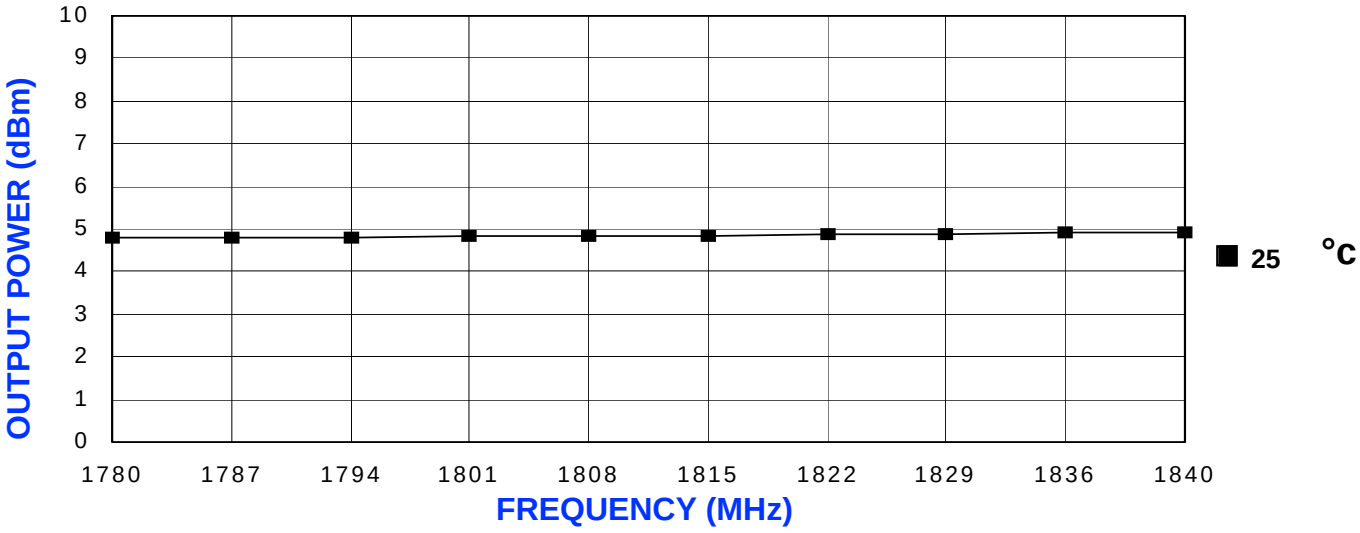
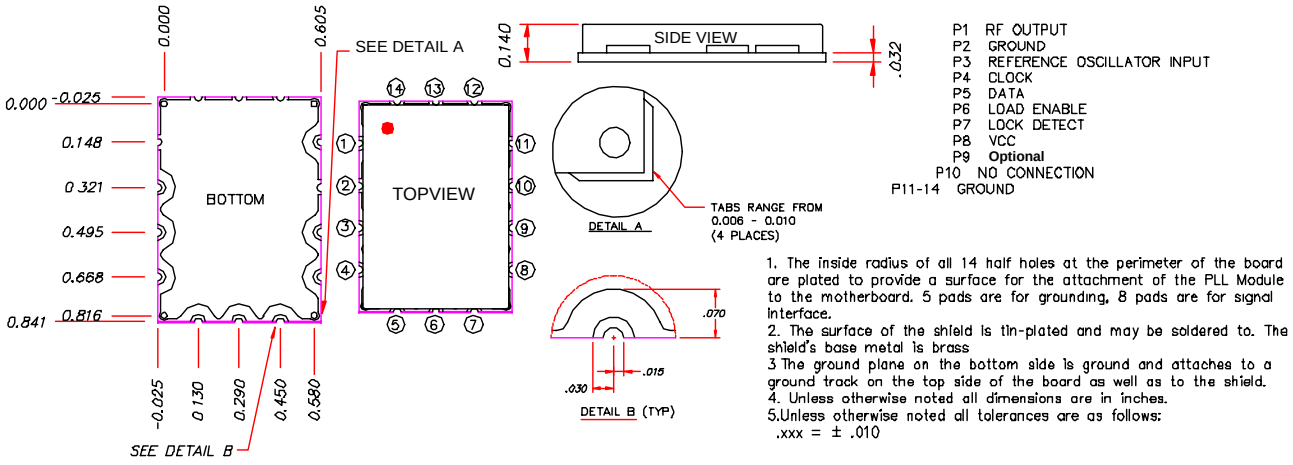
VCO TUNING CURVE, typ.



VCO POWER CURVE, typ.



PHYSICAL DIMENSIONS



1. The inside radius of all 14 half holes at the perimeter of the board are plated to provide a surface for the attachment of the PLL Module to the motherboard. 5 pads are for grounding, 8 pads are for signal interface.
2. The surface of the shield is tin-plated and may be soldered to. The shield's base metal is brass
3 The ground plane on the bottom side is ground and attaches to a ground track on the top side of the board as well as to the shield.
4. Unless otherwise noted all dimensions are in inches.
5.Unless otherwise noted all tolerances are as follows:
.xxx = ± .010

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