10W Stereo Class-D Speaker Driver Amplifier

General Description

The RT9116 is a 10W per channel, high efficiency Class D stereo audio amplifier for driving bridge tied load (BTL) speakers. The RT9116 can drive stereo speakers with load as low as 4Ω. Its high efficiency eliminates the need for an extra heat sink when playing music. The gain of the amplifier can be controlled by gain select pins. The outputs are fully protected against shorts to GND, PVCC, and output to output with an auto recovery feature and monitored output.

The RT9116 is available in the WQFN-28L 4x5 package.

Ordering Information

RT9116□□

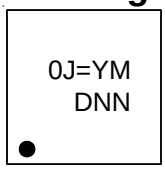
- Package Type
  QW : WQFN-28L 4x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



0J= : Product Code

YMDNN : Date Code

Features

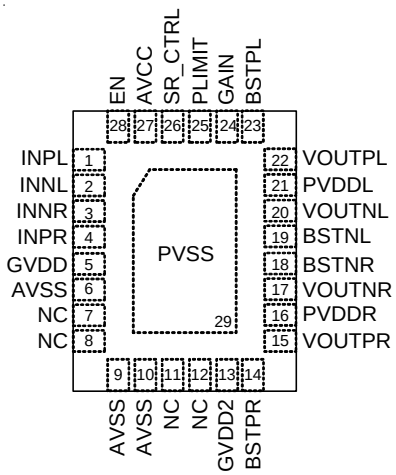
- **8V to 17V Input Supply Range**
  - **10W / CH for an 8Ω Load, 13V Supply at 10% THD +N**
  - **15W / CH for an 8Ω Load, 16V Supply at 10% THD +N**
  - **90% Efficiency Eliminates Need for Heat Sink**
- **DC Detect Protection**
- **Filter-Less Operation**
- **Over-Temperature Protection (OTP) with Auto Recovery Option**
- **Surface Mount 28-Lead WQFN Package**

Applications

- LCD-TV
- Monitors
- Home Audio
- Amusement Equipment
- Electronic Music Equipment

Pin Configuration

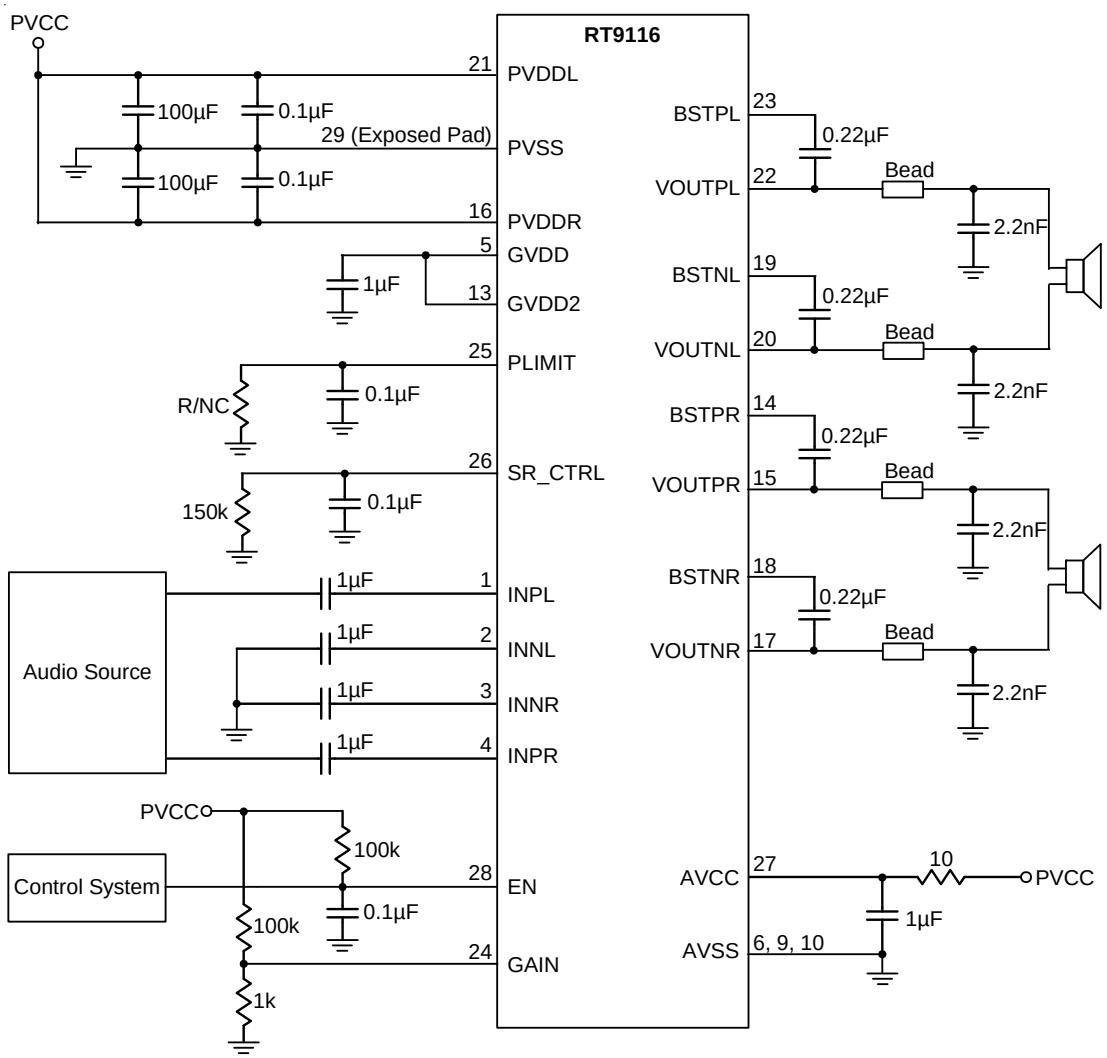
(TOP VIEW)



WQFN-28L 4x5

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Typical Application Circuit



Note :
When pin GAIN connect (a) 100kΩ to PVCC, SPK gain = 31dB; (b) 1kΩ to GND, SPK gain = 26dB

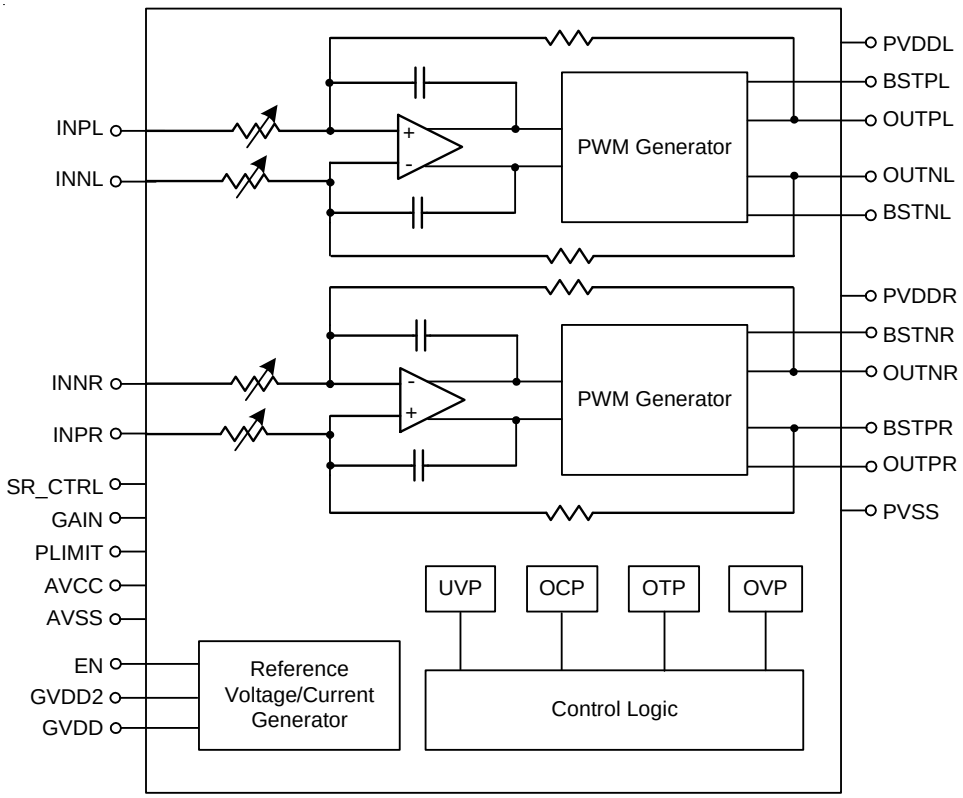
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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	INPL	Positive audio input for left channel.
2	INNL	Negative audio input for left channel.
3	INNR	Negative audio input for right channel.
4	INPR	Positive audio input for right channel.
5	GVDD	High-side FET gate drive supply.
6, 9, 10	AVSS	Analog ground.
7, 8, 11, 12	NC	No internal connection.
13	GVDD2	Reference voltage from GVDD.
14	BSTPR	Bootstrap I/O for right channel, positive high-side MOSFET.
15	VOUTPR	Class-D H-Bridge positive output for right channel.
16	PVDDR	Power supply input for right channel H-Bridge. Right channel and left channel power supply inputs are connected internally.
17	VOUTNR	Class-D H-Bridge negative output for right channel.
18	BSTNR	Bootstrap I/O for right channel, negative high-side MOSFET.
19	BSTNL	Bootstrap I/O for left channel, negative high-side MOSFET.
20	VOUTNL	Class-D H-Bridge negative output for left channel.
21	PVDDL	Power supply input for left channel H-Bridge. Right channel and left channel power supply inputs are connected internally.
22	VOUTPL	Class-D H-Bridge positive output for left channel.
23	BSTPL	Bootstrap I/O for left channel, positive high-side MOSFET.
24	GAIN	Gain select least significant bit.
25	PLIMIT	Power limit level adjustment.
26	SR_CTRL	Control output stage driver slew rate
27	AVCC	Analog supply input.
28	EN	Chip enable (active high).
29 (Exposed Pad)	PVSS	Power ground for power stage

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Functional Block Diagram



Operation

The RT9116 is a dual-channel 2 x 10W efficient, Class D audio power amplifier for driving bridge-tied stereo speakers. The RT9116 uses the three-level modulation (BD model) scheme that allows operation without external LC reconstruction when the amplifier is driving an inductive load.

Moreover, the built-in spread spectrum modulation can efficiently reduce EMI and save the cost of the external inductor, replaced by ferrite beads.

A closed-loop modulator, which enables negative error feedback, can improve THD+N and PSRR of output signals.

The RT9116 offers two selectable power limit thresholds, 5W/10W under 8Ω for protecting load speakers.

These two limit thresholds can be set easily by connecting two different resistors, 25kΩ/150kΩ, from the PLIMIT pin to ground.

Though there is no requirement for power limit, the resistance connected from the PLIMIT pin to ground must be greater than 500kΩ.

The RT9116 features over-current protection against output stage short-circuit conditions.

When a short-circuit condition occurs, amplifier outputs will be switched to a Hi-Z state, and the short-circuit protection latch will be triggered. Once the short-circuit condition is removed, the RT9116 will be automatically recovered.

The RT9116 can drive stereo speakers as low as 4Ω. The high efficiency of the RT9116, 90%, eliminates the need for an external heat sink when playing music.

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Absolute Maximum Ratings (Note 1)

- Supply Voltage, PVDDL, PVDDR, AVCC ---------- –0.3V to 21V
- Input Voltage, EN, GAIN ---------- –0.3V to (PVDDx + 0.3V)
- Output Voltage, OUTPL,OUTPR,OUTNL,OUTNR ---------- –0.3V to (PVDDx + 0.3V)
- Bootstrap Voltage, BSTPL,BSTPR,BSTNL,BSTNR ---------- –0.3V to (PVDDx + 6V)
- Other Pins ---------- –0.3V to (GVDD + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-28L 4x5 ---------- 3.64W
- Package Thermal Resistance (Note 2)
  WQFN-28L 4x5, θ_{JA} ---------- 27.4°C/W
  WQFN-28L 4x5, θ_{JC} ---------- 2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, PVDDL, PVDDR, AVCC ---------- 8V to 17V
- Min. SPK load in BTL mode, Rspk (BTL) ---------- 4Ω
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(PVDDx = 12V, R_L = 8Ω, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Condition		Min	Typ	Max	Unit
Gate Drive Supply Voltage		V_{GVDD}	I_{GVDD} = 2mA		--	5	5.5	V
EN, Gain Input Voltage	V_{IH} : High-Level	V_{IH}			3	--	--	V
	V_{IL} : Low-Level	V_{IL}			--	--	0.8	V
EN, Gain Input Current	V_{IH} : High-Level	I_{IH}	EN, Gain, VI = 5V		--	--	50	μA
	V_{IL} : Low-Level	I_{IL}	EN, Gain, VI = 0.8V		--	--	10	μA
Output Offset Voltage		Vos	PVDDx = 12V, Gain = 31dB		--	--	20	mV
Quiescent Current		I_Q	PVDDx = 12V, GVDD2 = 5V, no filter and load		--	10	15	mA
Shutdown Current		I_{SD}	PVDDx = 12V, GVDD2 = 5V, EN = Low		--	1	1.5	mA
Drain-Source On State Resistance		$R_{DS(ON)}$	PVDDx = 12V, I_O = 500mA	High-side	--	250	--	mΩ
				Low-side	--	200	--	
Gain		Gain	Gain = 0		25	26	27	dB
			Gain = 1		30	31	32	

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Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Integrated Noise	Vn	PVDDx = 12V, Gain = 26dB, A-weighted		--	100	--	μV
		PVDDx = 12V, Gain = 31dB, A-weighted		--	200	--	
Signal-to-Noise Ratio	SNR	PVCC = 12V, Gain = 26dB, A-weighted, THD+N = 1%		--	98	--	dB
Output Power	Po	THD+N = 7%, PVCC = 11.3V, R_L = 8Ω		--	8	--	W
		THD+N = 10%, PVCC = 16V, R_L = 8Ω		--	15	--	W
Total Harmonic Distortion Plus Noise	THD+N	PVDDx = 12V, fin = 1kHz	Po = 5W	--	0.2	--	%
			Po = 1W	--	0.1	--	
Crosstalk		Vo = 1Vrms, Gain = 26dB, fin = 1kHz		--	–70	--	dB
Power Supply Ripple Rejection	PSRR	200mVPP ripple at 1kHz, Gain = 26dB, Inputs ac-coupled to AGND		--	–70	--	dB
Turn On Time	t_{ON}			--	25	--	ms
Turn Off Time	t_{OFF}			--	2	--	μs
Oscillator Frequency	f_{OSC}			--	330	--	kHz
Output Power Limit		V_{IN} 1Vrms, Plimit , 25kΩ to GND		5	--	6.5	W
		V_{IN} = 1Vrms, Plimit , 150kΩ to GND		10	--	13	
Protection Circuitry							
Under-Voltage Protection	V_{UVP}			--	6.5	--	V
Under-Voltage Protection Hysteresis	ΔV_{UVP}			--	1	--	V
Over-Voltage Protection	V_{OVP}			--	19	--	V
Over-Voltage Protection Hysteresis	ΔV_{OVP}			--	2	--	V
Over-Temperature Protection	T_{SD}			--	170	--	°C
Over-Temperature Protection Hysteresis	ΔT_{SD}			--	15	--	°C
SPK Over-Current Protection	I_{OCP}			--	3.5	--	A

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

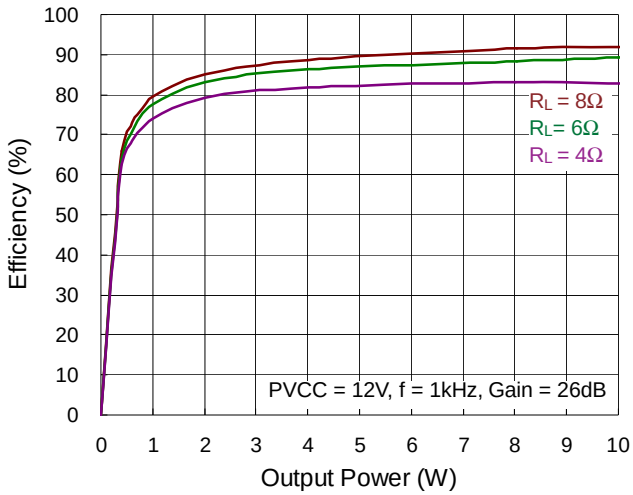
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

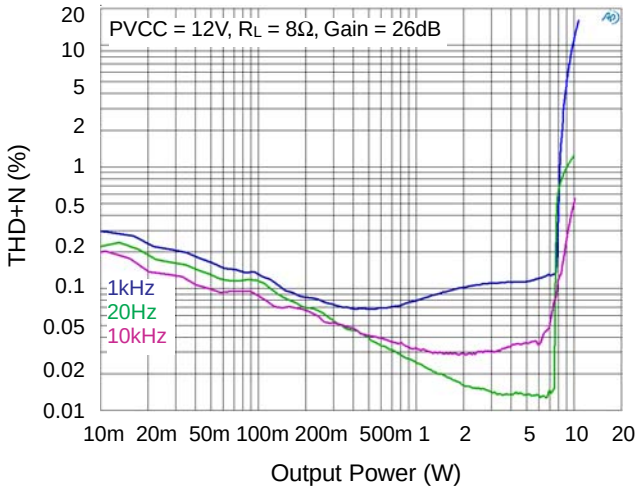
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Typical Operating Characteristics

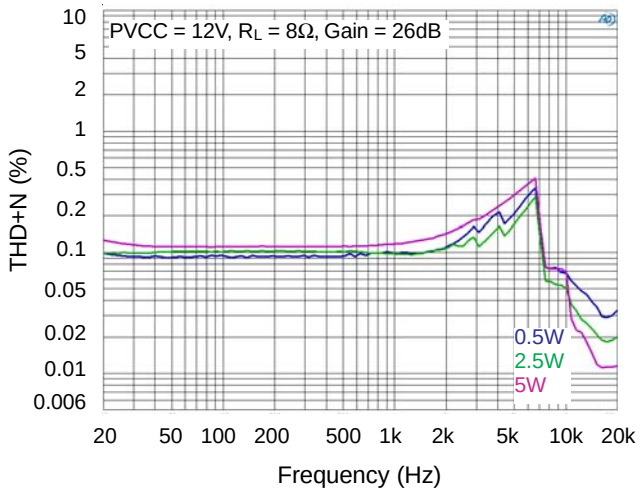
Efficiency vs. Output Power



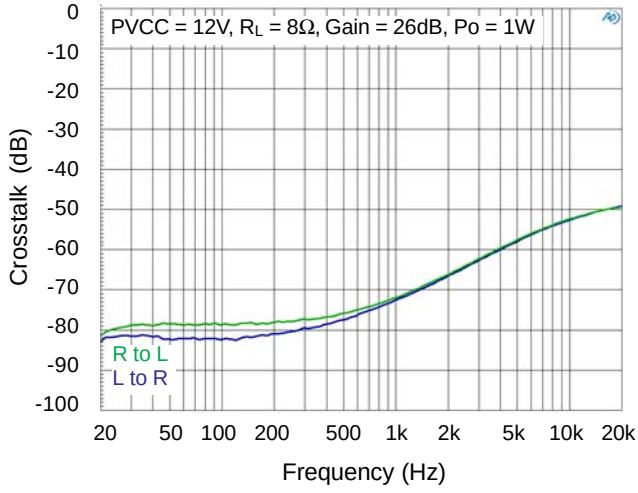
THD+N vs. Output Power



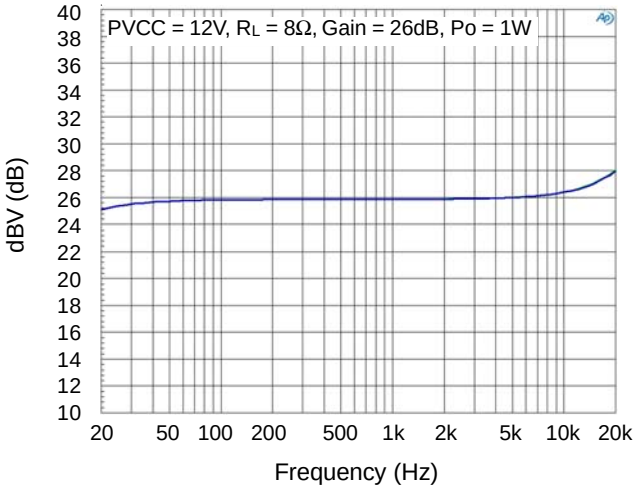
THD+N vs. Frequency



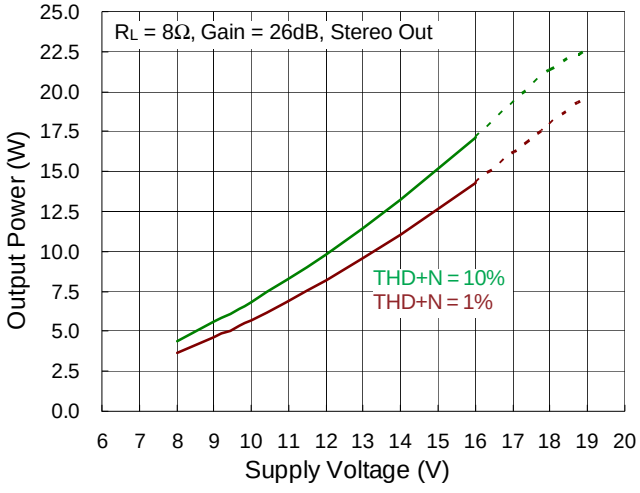
Crosstalk vs. Frequency



Frequency Results



Output Power vs. Supply Voltage



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Application Information

GVDD Supply

The GVDD is used to supply the Gate Drivers for the output full bridge transistors. Connect a 1μF capacitor from this pin to ground for good bypass. The typical GVDD output voltage is 5V.

Amplifier Gain Setting

The gain of the RT9116 amplifier can be set by one input terminals, GAIN shown as Table 1.

The gain setting is realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (ZI) to be dependent on the gain setting. The actual gain settings are controlled by the ratios of the resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

Table 1. Gain Setting

GAIN	Amplifier GAIN (dB)	Input Impedance (kΩ)
	Typ	Typ
0	26	20
1	31	10

EN Operation

The RT9116 employs a shutdown mode operation designed to reduce supply current (ICC) to the absolute minimum level for power saving. The EN input terminal should be held high (see specification table for trip point) in normal operation. Pulling EN low causes the outputs to mute and the amplifier to enter a low current state. Leaving EN floating will cause the amplifier operation to be unpredictable. Never leave EN pin unconnected. For the best power-off pop performance, turn off the amplifier in the shutdown mode prior to removing the power supply voltage.

Over-Current Protection (OCP)

The RT9116 provides OCP function to prevent the device from damages during overload or short-circuit conditions. The current are detected by an internal sensing circuit. Once overload happens, the OCP function is designed to operate in auto-recovery mode.

DC Detect Protection

RT9116 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. To clear the DC Detect it is necessary to cycle the PVCC supply.

ADC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 18% (for example, +59%, –41%) for more than 290 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 4Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Under-Voltage Protection (UVP)

The RT9116 monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL and PVDDR pin falls below the under voltage threshold, 7V (typ.), the UVP circuit turns off the output immediately and operates in cycle by cycle auto-recovery mode.

Over-Voltage Protection (OVP)

The RT9116 monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL and PVDDR pin rise behind the over voltage threshold, 15V (typ.), the OVP circuit turns off the output immediately and operates in cycle by cycle auto-recovery mode.

Over-Temperature Protection (OTP)

The OTP prevents damage to the device when the internal die temperature exceeds 170°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the OTP threshold, the device enters

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into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Power-On/Off Sequence

Use the following sequence to power on the device

- PVCC power supply ready.

  Past EN = 1 (EN pin goes high)

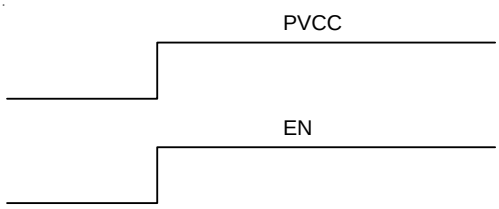


Figure 1. Power On Sequence

Use the following sequence to power off the device

- EN = 0 (EN pin goes Low) Past PVCC power supply shutdown

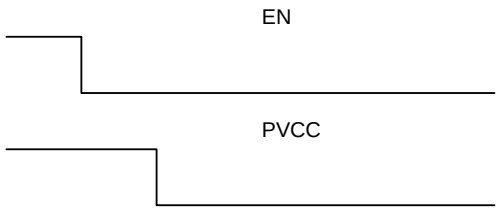


Figure 2. Power Off Sequence

Power Limit

The voltage at the PLIMIT pin can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor (Table 2) to ground set the voltage at the PLIMIT pin. Also add a 1μF capacitor from the PLIMIT pin to ground. The PLIMIT circuit sets a limit on the output Power.

Table 2. Plimit Setting

Resistor (kΩ)	Output Power (W)
25	5.75
150	11.5
Open	MAX

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-28L 4x5 package, the thermal resistance, θ_{JA}, is 27.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.4°C/W) = 3.64W for a WQFN-28L 4x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

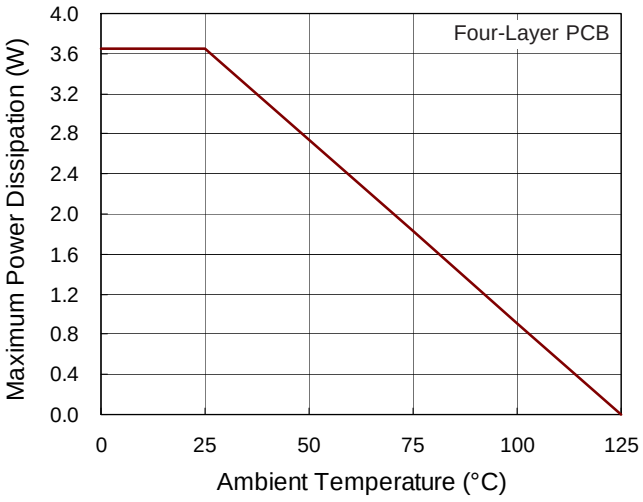


Figure 3. Derating Curve of Maximum Power Dissipation

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Layout Considerations

For the best performance of the RT9116, the below PCB layout guidelines must be strictly followed.

Place the decoupling capacitors as close as possible to the AVCC, PVDDL, PVDDR and GND pins. For achieving a good quality, consider adding a small, good performance low ESR ceramic capacitor between 220pF and 1000pF and a larger mid-frequency capacitor between 0.1µF and 1µF to the PVDD pins of the chip. The traces of (LINP & LINN, RINP & RINN) and (OUTPL & OUTNL, OUTPR & OUTNR) should be kept equal width and length respectively. The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be larger for application. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB.

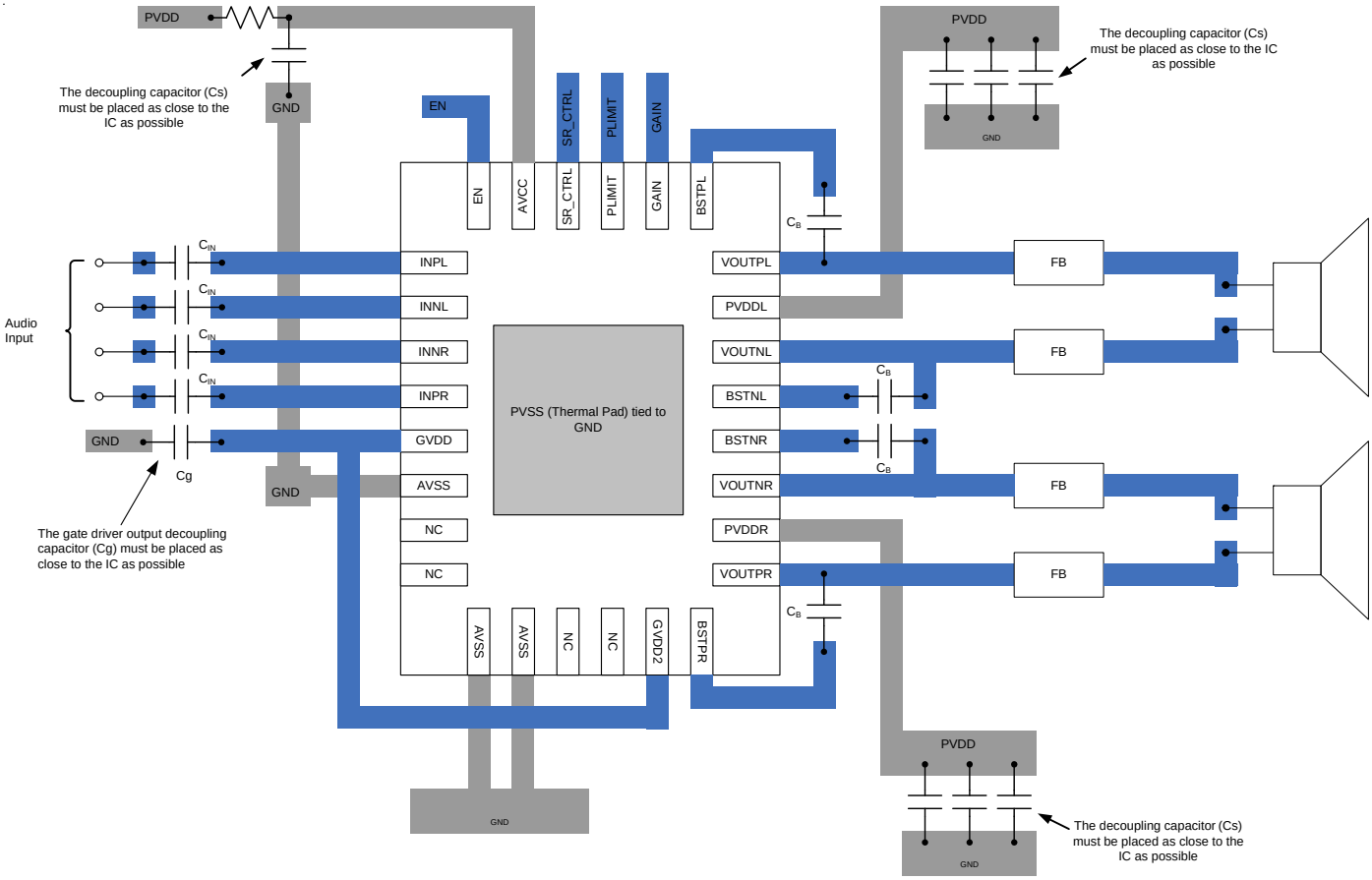
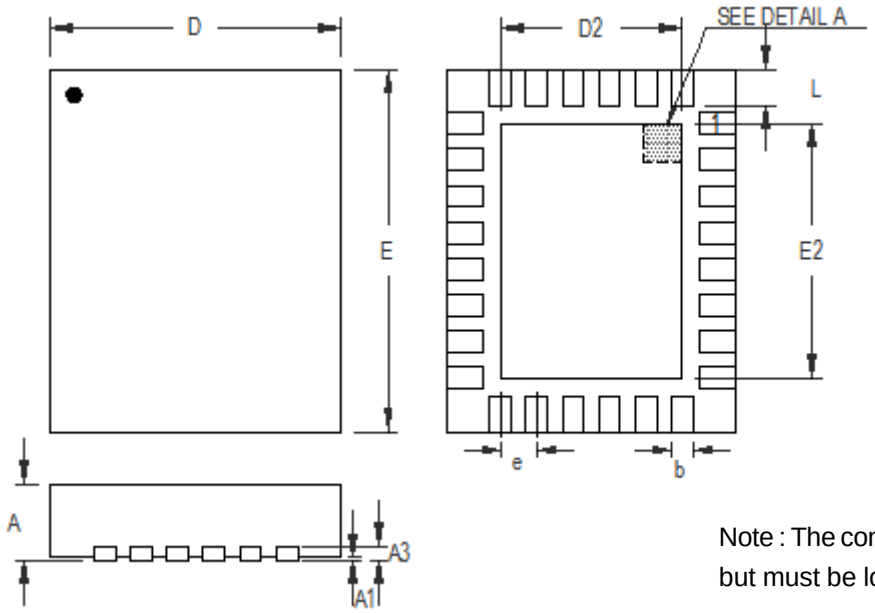
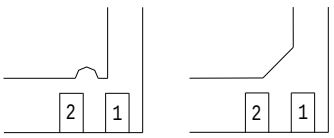


Figure 4. PCB Layout Guide

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.900	4.100	0.154	0.161
D2	2.600	2.700	0.102	0.106
E	4.900	5.100	0.193	0.201
E2	3.600	3.700	0.142	0.146
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 28L QFN 4x5 Package

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