NEC

MOS INTEGRATED CIRCUIT

μPD43256B

256K-BIT CMOS STATIC RAM
32K-WORD BY 8-BIT

Description

The μPD43256B is a high speed, low power, and 262,144 bits (32,768 words by 8 bits) CMOS static RAM.

Battery backup is available. And A and B versions are wide voltage operations.

The μPD43256B is packed in 28-pin PLASTIC DIP, 28-pin PLASTIC SOP and 28-pin PLASTIC TSOP (I) (8 x 13.4 mm).

Features

- 32,768 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation (A version: V_{CC} = 3.0 to 5.5 V, B version: V_{CC} = 2.7 to 5.5 V)
- Low V_{CC} data retention: 2.0 V (MIN.)
- /OE input for easy application

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.) Note1
μPD43256B-xxL	70, 85	4.5 to 5.5	0 to 70	45	50	3
μPD43256B-xxLL					15	2
μPD43256B-Axx	85, 100 Note2, 120 Note2	3.0 to 5.5				
μPD43256B-Bxx Note2	100, 120, 150	2.7 to 5.5				

Notes 1. $T_A \leq 40$ °C, V_{CC} = 3.0 V

2. Access time: 85 ns (MAX.) (V_{CC} = 4.5 to 5.5 V)

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Ordering Information

(1/2)

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Remark
μPD43256BCZ-70L	28-pin PLASTIC DIP	70	4.5 to 5.5	0 to 70	L version
μPD43256BCZ-85L	(15.24 mm (600))	85			
μPD43256BCZ-70LL		70			LL version
μPD43256BCZ-85LL		85			
μPD43256BGU-70L	28-pin PLASTIC SOP	70			L version
μPD43256BGU-85L	(11.43 mm (450))	85			
μPD43256BGU-70LL		70			LL version
μPD43256BGU-85LL		85			
μPD43256BGU-A85		85	3.0 to 5.5		A version
μPD43256BGU-A10		100			
μPD43256BGU-A12		120			
μPD43256BGU-B10		100	2.7 to 5.5		B version
μPD43256BGU-B12		120			
μPD43256BGW-70LL-9JL	28-pin PLASTIC TSOP (I)	70	4.5 to 5.5		LL version
μPD43256BGW-85LL-9JL	(8x13.4) (Normal bent)	85			
μPD43256BGW-A85-9JL		85	3.0 to 5.5		A version
μPD43256BGW-A10-9JL		100			
μPD43256BGW-A12-9JL		120			
μPD43256BGW-B10-9JL		100	2.7 to 5.5		B version
μPD43256BGW-B12-9JL		120			
μPD43256BGW-B15-9JL		150			
μPD43256BGW-70LL-9KL	28-pin PLASTIC TSOP (I)	70	4.5 to 5.5		LL version
μPD43256BGW-85LL-9KL	(8x13.4) (Reverse bent)	85			
μPD43256BGW-A85-9KL		85	3.0 to 5.5		A version
μPD43256BGW-A10-9KL		100			
μPD43256BGW-A12-9KL		120			
μPD43256BGW-B10-9KL		100	2.7 to 5.5		B version
μPD43256BGW-B12-9KL		120			
μPD43256BGW-B15-9KL		150			

(2/2)

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Remark
μPD43256BGU-70L-A	28-pin PLASTIC SOP	70	4.5 to 5.5	0 to 70	L version
μPD43256BGU-85L-A	(11.43 mm (450))	85			
μPD43256BGU-70LL-A		70			LL version
μPD43256BGU-85LL-A		85			
μPD43256BGU-A85-A		85	3.0 to 5.5		A version
μPD43256BGU-A10-A		100			
μPD43256BGU-A12-A		120			
μPD43256BGU-B10-A		100	2.7 to 5.5		B version
μPD43256BGU-B12-A		120			
μPD43256BGW-70LL-9JL-A	28-pin PLASTIC TSOP (I)	70	4.5 to 5.5		LL version
μPD43256BGW-85LL-9JL-A	(8x13.4) (Normal bent)	85			
μPD43256BGW-A85-9JL-A		85	3.0 to 5.5		A version
μPD43256BGW-A10-9JL-A		100			
μPD43256BGW-A12-9JL-A		120			
μPD43256BGW-B10-9JL-A		100	2.7 to 5.5		B version
μPD43256BGW-B12-9JL-A		120			
μPD43256BGW-B15-9JL-A		150			
μPD43256BGW-70LL-9KL-A	28-pin PLASTIC TSOP (I)	70	4.5 to 5.5		LL version
μPD43256BGW-85LL-9KL-A	(8x13.4) (Reverse bent)	85			
μPD43256BGW-A85-9KL-A		85	3.0 to 5.5		A version
μPD43256BGW-A10-9KL-A		100			
μPD43256BGW-A12-9KL-A		120			
μPD43256BGW-B10-9KL-A		100	2.7 to 5.5		B version
μPD43256BGW-B12-9KL-A		120			
μPD43256BGW-B15-9KL-A		150			

Remark Products with -A at the end of the part number are lead-free products.

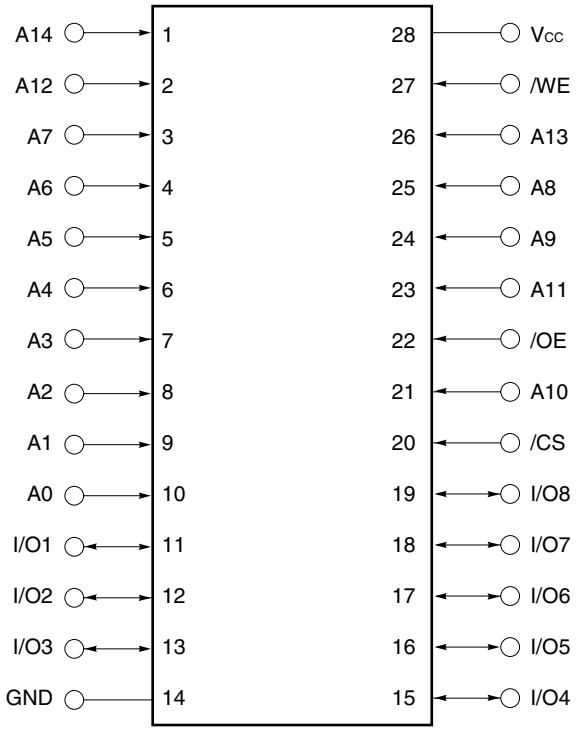
Pin Configurations (Marking Side)

/xxx indicates active low signal.

28-pin PLASTIC DIP (15.24 mm (600))

[μPD43256BCZ-xxL]

[μPD43256BCZ-xxLL]



A0 - A14	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CS	:	Chip Select
/WE	:	Write Enable
/OE	:	Output Enable
VCC	:	Power supply
GND	:	Ground

Remark Refer to **Package Drawings** for the 1-pin index mark.

28-pin PLASTIC SOP (11.43 mm (450))

[μPD43256BGU-xxL]

[μPD43256BGU-xxLL]

[μPD43256BGU-Axx]

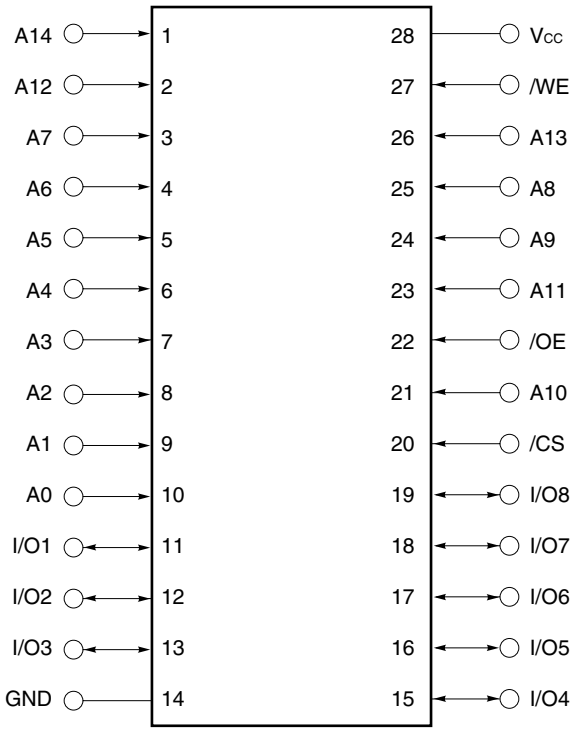
[μPD43256BGU-Bxx]

[μPD43256BGU-xxL-A]

[μPD43256BGU-xxLL-A]

[μPD43256BGU-Axx-A]

[μPD43256BGU-Bxx-A]



A0 - A14	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CS	:	Chip Select
/WE	:	Write Enable
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground

Remark Refer to **Package Drawings** for the 1-pin index mark.

28-pin PLASTIC TSOP (I) (8x13.4) (Normal bent)

[μPD43256BGW-xxLL-9JL]

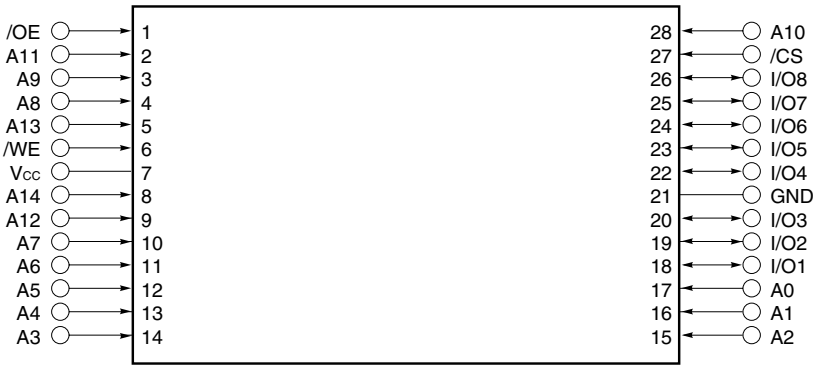
[μPD43256BGW-Axx-9JL]

[μPD43256BGW-Bxx-9JL]

[μPD43256BGW-xxLL-9JL-A]

[μPD43256BGW-Axx-9JL-A]

[μPD43256BGW-Bxx-9JL-A]



28-pin PLASTIC TSOP (I) (8x13.4) (Reverse bent)

[μPD43256BGW-xxLL-9KL]

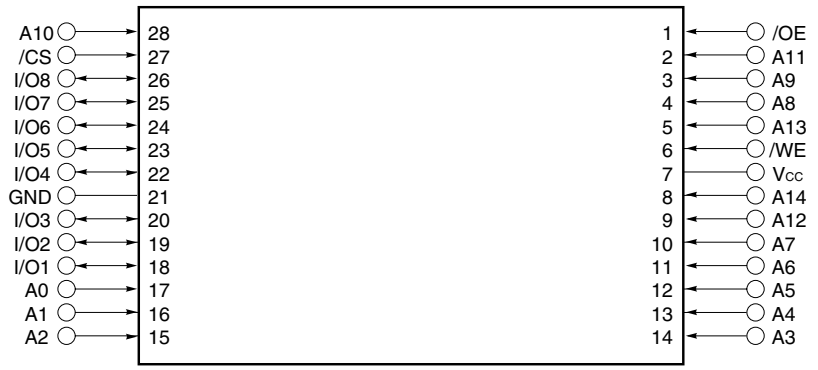
[μPD43256BGW-Axx-9KL]

[μPD43256BGW-Bxx-9KL]

[μPD43256BGW-xxLL-9KL-A]

[μPD43256BGW-Axx-9KL-A]

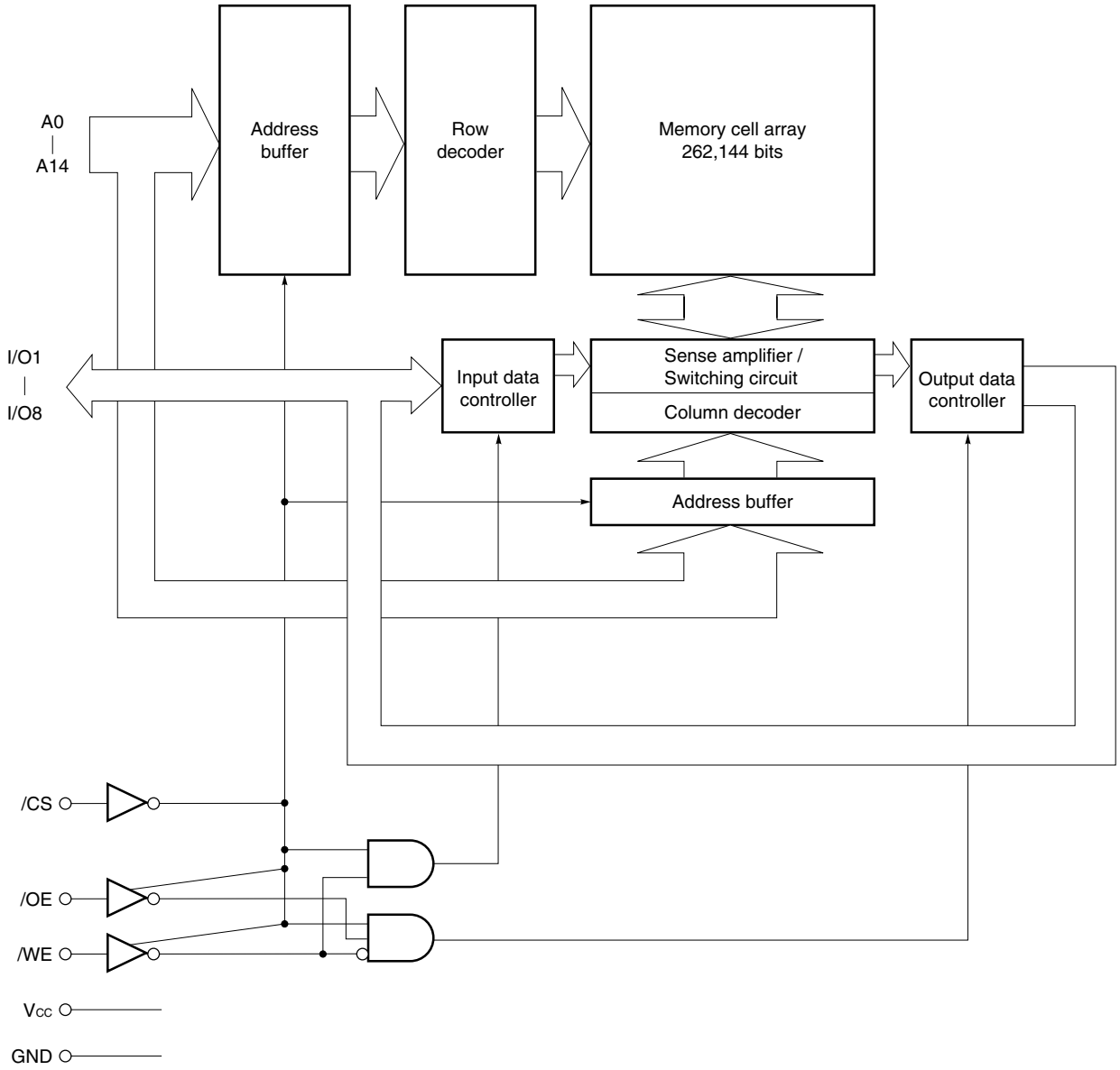
[μPD43256BGW-Bxx-9KL-A]



A0 - A14	:	Address inputs	/OE	:	Output Enable
I/O1 - I/O8	:	Data inputs / outputs	Vcc	:	Power supply
/CS	:	Chip Select	GND	:	Ground
/WE	:	Write Enable			

Remark Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

/CS	/OE	/WE	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I_{SB}
L	H	H	Output disable		I_{CCA}
L	×	L	Write	D_{IN}	
L	L	H	Read	D_{OUT}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +7.0	V
Input / Output voltage	V_T		–0.5 Note to V_{CC} + 0.5	V
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 50 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD43256B-xxL μPD43256B-xxLL		μPD43256B-Axx		μPD43256B-Bxx		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	V_{IH}		2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	V
Low level input voltage	V_{IL}		–0.3 Note	+0.8	–0.3 Note	+0.5	–0.3 Note	+0.5	V
Operating ambient temperature	T_A		0	70	0	70	0	70	°C

Note –3.0 V (MIN.) (Pulse width: 50 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			5	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Parameter	Symbol	Test condition	μPD43256B-xxL			μPD43256B-xxLL			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /OE = V_{IH} or /CS = V_{IH} or /WE = V_{IL}	–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CS = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA			45			45	mA
	I_{CCA2}	/CS = V_{IL}, $I_{I/O}$ = 0 mA			10			10	
	I_{CCA3}	/CS ≤ 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V			10			10	
Standby supply current	I_{SB}	/CS = V_{IH}			3			3	mA
	I_{SB1}	/CS ≥ V_{CC} – 0.2 V		1.0	50		0.5	15	μA
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA	2.4			2.4			V
	V_{OH2}	I_{OH} = –0.1 mA	V_{CC}–0.5			V_{CC}–0.5			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4			0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of package types.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition		μPD43256B-Axx			μPD43256B-Bxx			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /OE = V_{IH} or /CS = V_{IH} or /WE = V_{IL}		–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CS = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA	μPD43256B-Axx			45			–	mA
			μPD43256B-Bxx			–			45	
			V_{CC} ≤ 3.3 V			–			20	
	I_{CCA2}	/CS = V_{IL}, $I_{I/O}$ = 0 mA				10			10	
			V_{CC} ≤ 3.3 V			–			5	
	I_{CCA3}	/CS ≤ 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA,				10			10	
		V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V	V_{CC} ≤ 3.3 V			–			5	
Standby supply current	I_{SB}	/CS = V_{IH}				3			3	mA
			V_{CC} ≤ 3.3 V			–			2	
	I_{SB1}	/CS ≥ V_{CC} – 0.2 V			0.5	15		0.5	15	μA
			V_{CC} ≤ 3.3 V			–		0.5	10	
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA, V_{CC} ≥ 4.5 V		2.4			2.4			V
		I_{OH} = –0.5 mA, V_{CC} < 4.5 V		2.4			2.4			
	V_{OH2}	I_{OH} = –0.02 mA		V_{CC}–0.1			V_{CC}–0.1			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} ≥ 4.5 V				0.4			0.4	V
		I_{OL} = 1.0 mA, V_{CC} < 4.5 V				0.4			0.4	
	V_{OL1}	I_{OL} = 0.02 mA				0.1			0.1	

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

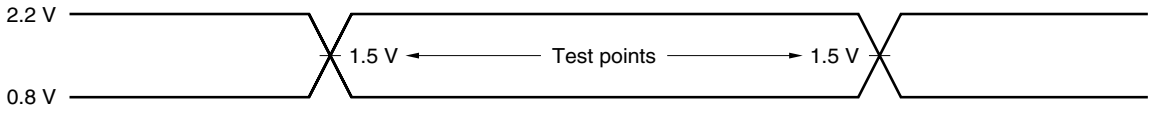
2. These DC characteristics are in common regardless of package types.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

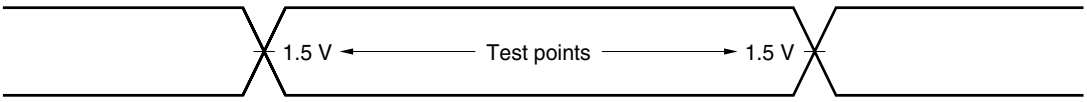
AC Test Conditions

[μPD43256B-70L, μPD43256B-85L, μPD43256B-70LL, μPD43256B-85LL]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics should be measured with the following output load conditions.

Figure 1

(t_{AA}, t_{ACS}, t_{OE}, t_{OH})

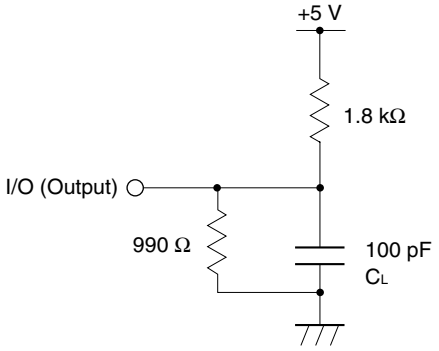
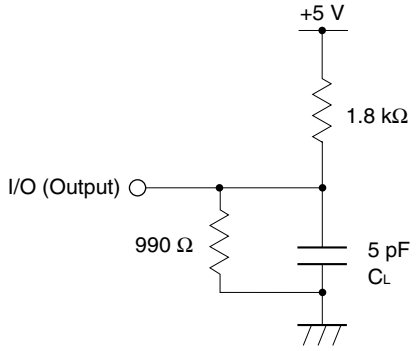


Figure 2

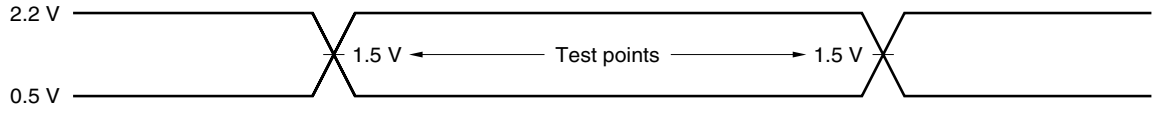
(t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})



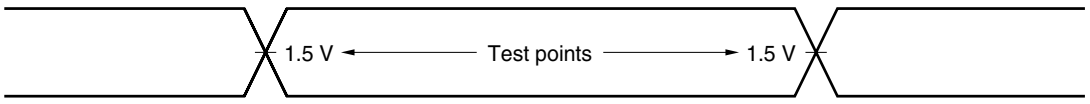
Remark C_L includes capacitance of the probe and jig, and stray capacitance.

[μPD43256B-A85, μPD43256B-A10, μPD43256B-A12, μPD43256B-B10, μPD43256B-B12, μPD43256B-B15]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics should be measured with the following output load conditions.

t_{AA}, t_{ACS}, t_{OE}, t_{OH}	t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW}
1TTL + 100 pF	1TTL + 5 pF

Read Cycle (1/2)

Parameter	Symbol	$V_{CC} \geq 4.5$ V				Unit	Condition
		μPD43256B-70		μPD43256B-85 μPD43256B-A85/A10/A12 μPD43256B-B10/B12/B15			
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		ns	
Address access time	t_{AA}		70		85	ns	**Note**
/CS access time	t_{ACS}		70		85	ns	
/OE access time	t_{OE}		35		40	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CS to output in low impedance	t_{CLZ}	10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/CS to output in high impedance	t_{CHZ}		30		30	ns	
/OE to output in high impedance	t_{OHZ}		30		30	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

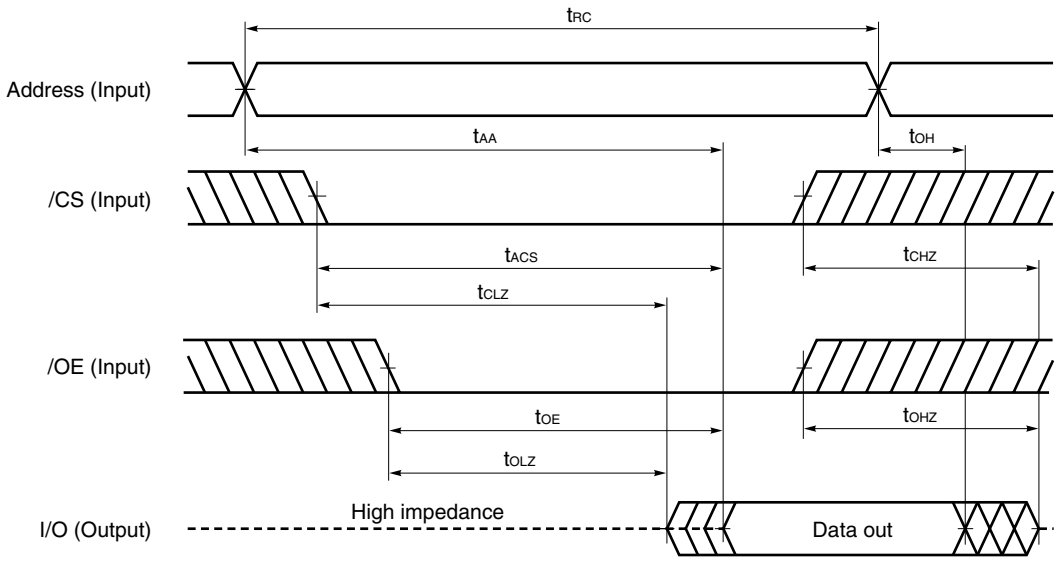
Read Cycle (2/2)

Parameter	Symbol	$V_{CC} \geq 3.0$ V						$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD43256B-A85		μPD43256B-A10		μPD43256B-A12		μPD43256B-B10		μPD43256B-B12		μPD43256B-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	85		100		120		100		120		150		ns	
Address access time	t_{AA}		85		100		120		100		120		150	ns	**Note**
/CS access time	t_{ACS}		85		100		120		100		120		150	ns	
/OE access time	t_{OE}		50		60		60		60		60		70	ns	
Output hold from address change	t_{OH}	10		10		10		10		10		10		ns	
/CS to output in low impedance	t_{CLZ}	10		10		10		10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		5		5		ns	
/CS to output in high impedance	t_{CHZ}		35		35		40		35		40		50	ns	
/OE to output in high impedance	t_{OHZ}		35		35		40		35		40		50	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/2)

Parameter	Symbol	$V_{CC} \geq 4.5$ V				Unit	Condition
		μPD43256B-70		μPD43256B-85 μPD43256B-A85/A10/A12 μPD43256B-B10/B12/B15			
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		ns	
/CS to end of write	t_{CW}	50		70		ns	
Address valid to end of write	t_{AW}	50		70		ns	
Write pulse width	t_{WP}	55		60		ns	
Data valid to end of write	t_{DW}	30		35		ns	
Data hold time	t_{DH}	0		0		ns	
Address setup time	t_{AS}	0		0		ns	
Write recovery time	t_{WR}	0		0		ns	
/WE to output in high impedance	t_{WHZ}		30		30	ns	**Note**
Output active from end of write	t_{OW}	10		10		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

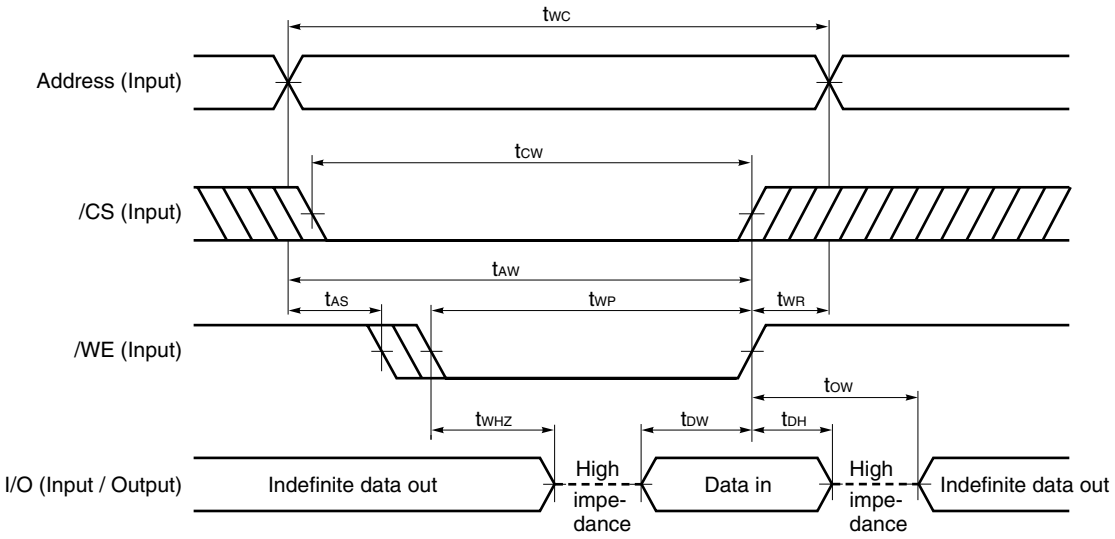
Write Cycle (2/2)

Parameter	Symbol	$V_{CC} \geq 3.0$ V						$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD43256B-A85		μPD43256B-A10		μPD43256B-A12		μPD43256B-B10		μPD43256B-B12		μPD43256B-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	85		100		120		100		120		150		ns	
/CS to end of write	t_{CW}	70		70		90		70		90		100		ns	
Address valid to end of write	t_{AW}	70		70		90		70		90		100		ns	
Write pulse width	t_{WP}	60		60		80		60		80		90		ns	
Data valid to end of write	t_{DW}	60		60		70		60		70		80		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Address setup	t_{AS}	0		0		0		0		0		0		ns	
Write recovery	t_{WR}	0		0		0		0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		30		35		40		35		40		50	ns	**Note**
Output active from end of write	t_{OW}	10		10		10		10		10		10		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. /CS or /WE should be fixed to high level during address transition.

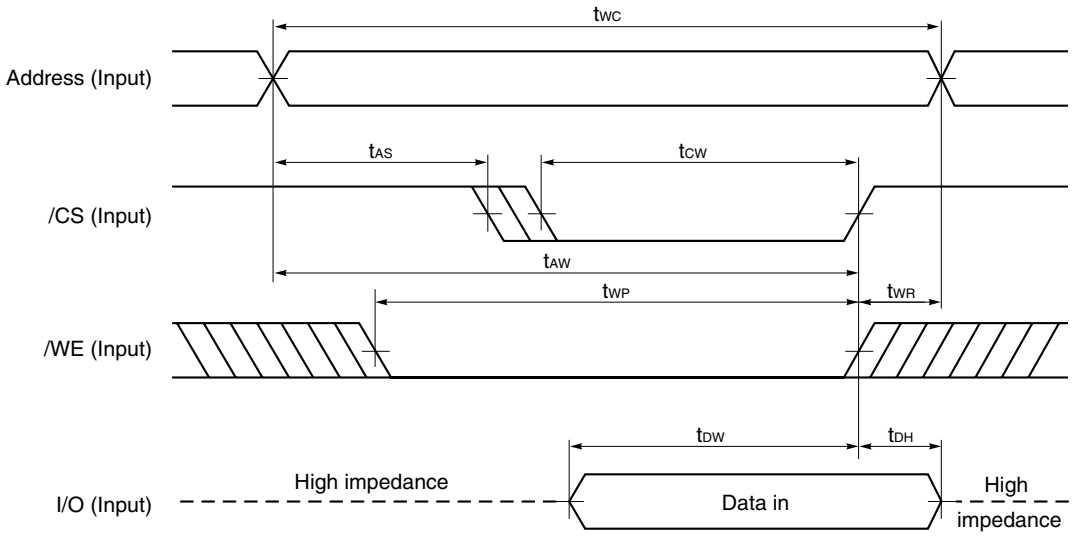
2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.

Remarks 1. Write operation is done during the overlap time of a low level /CS and a low level /WE.

2. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

3. If /CS changes to low level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

Write Cycle Timing Chart 2 (/CS Controlled)



Cautions 1. /CS or /WE should be fixed to high level during address transition.

2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.

Remark Write operation is done during the overlap time of a low level /CS and a low level /WE.

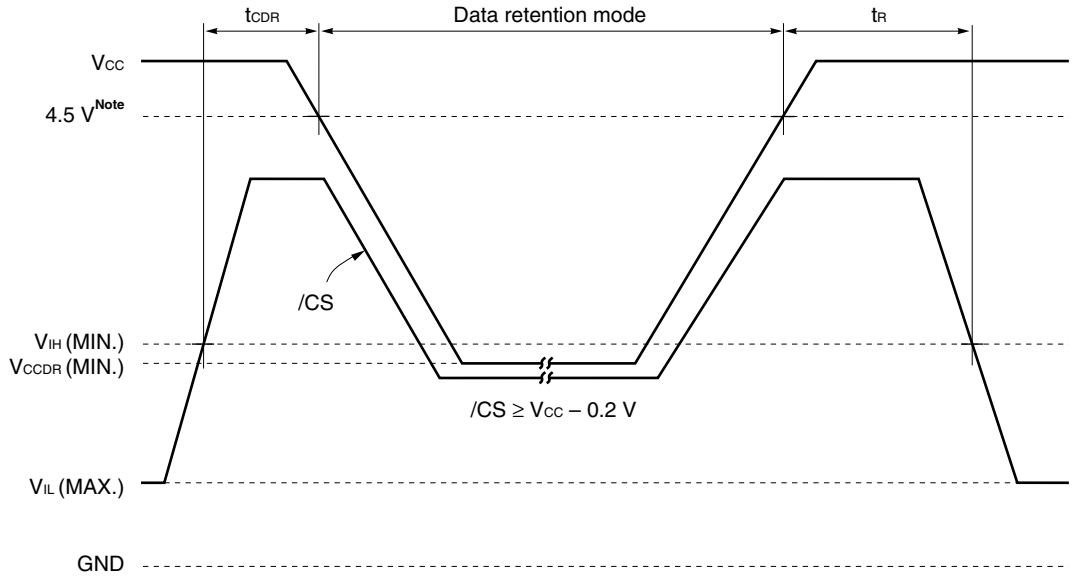
Low V_{CC} Data Retention Characteristics (T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	μPD43256B-xxL			μPD43256B-xxLL μPD43256B-Axx μPD43256B-Bxx			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR}	/CS ≥ V_{CC} – 0.2 V	2.0		5.5	2.0		5.5	V
Data retention supply current	I_{CCDR}	V_{CC} = 3.0 V, /CS ≥ V_{CC} – 0.2 V		0.5	20 Note1		0.5	7 Note2	μA
Chip deselection to data retention mode	t_{CDR}		0			0			ns
Operation recovery time	t_R		5			5			ms

Notes 1. 3 μA (T_A ≤ 40 °C)

2. 2 μA (T_A ≤ 40 °C), 1 μA (T_A ≤ 25 °C)

Data Retention Timing Chart

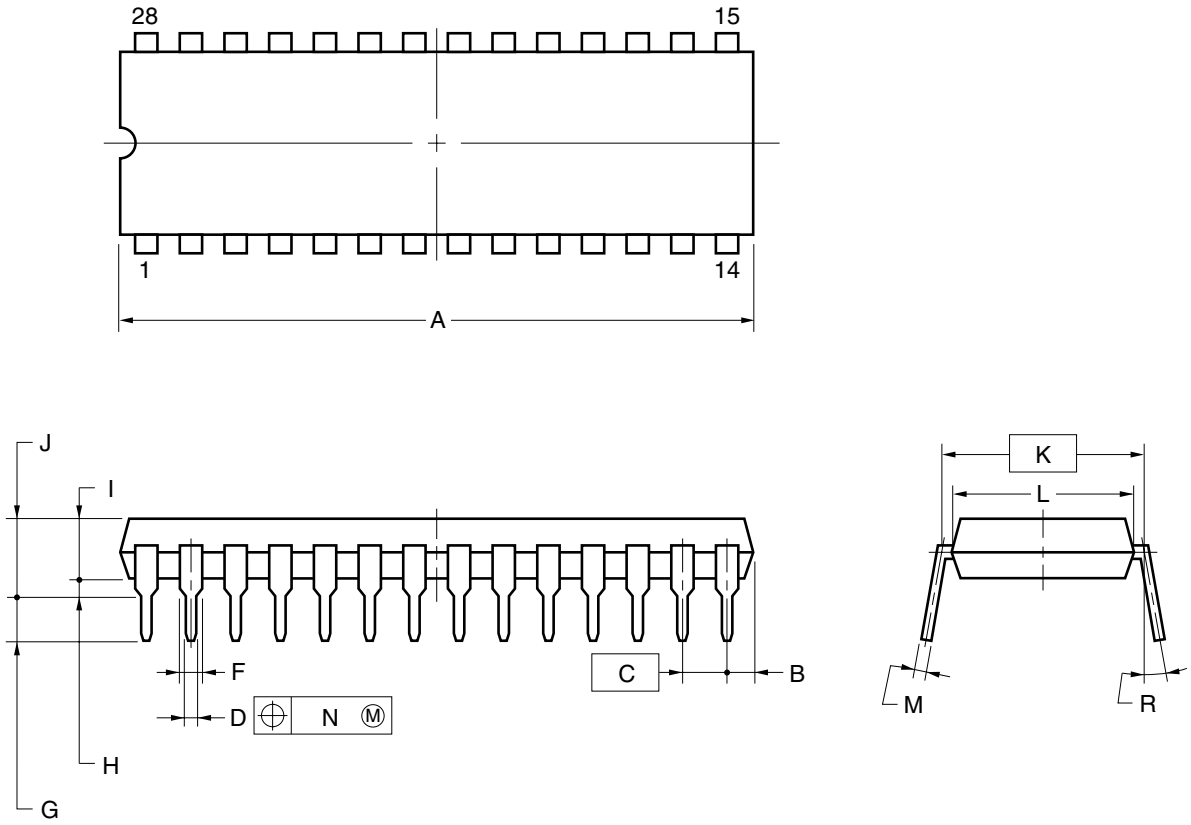


Note A version : 3.0 V, B version : 2.7 V

Remark The other pins (Address, /OE, /WE, I/O) can be in high impedance state.

Package Drawings

28-PIN PLASTIC DIP (15.24 mm (600))



NOTES

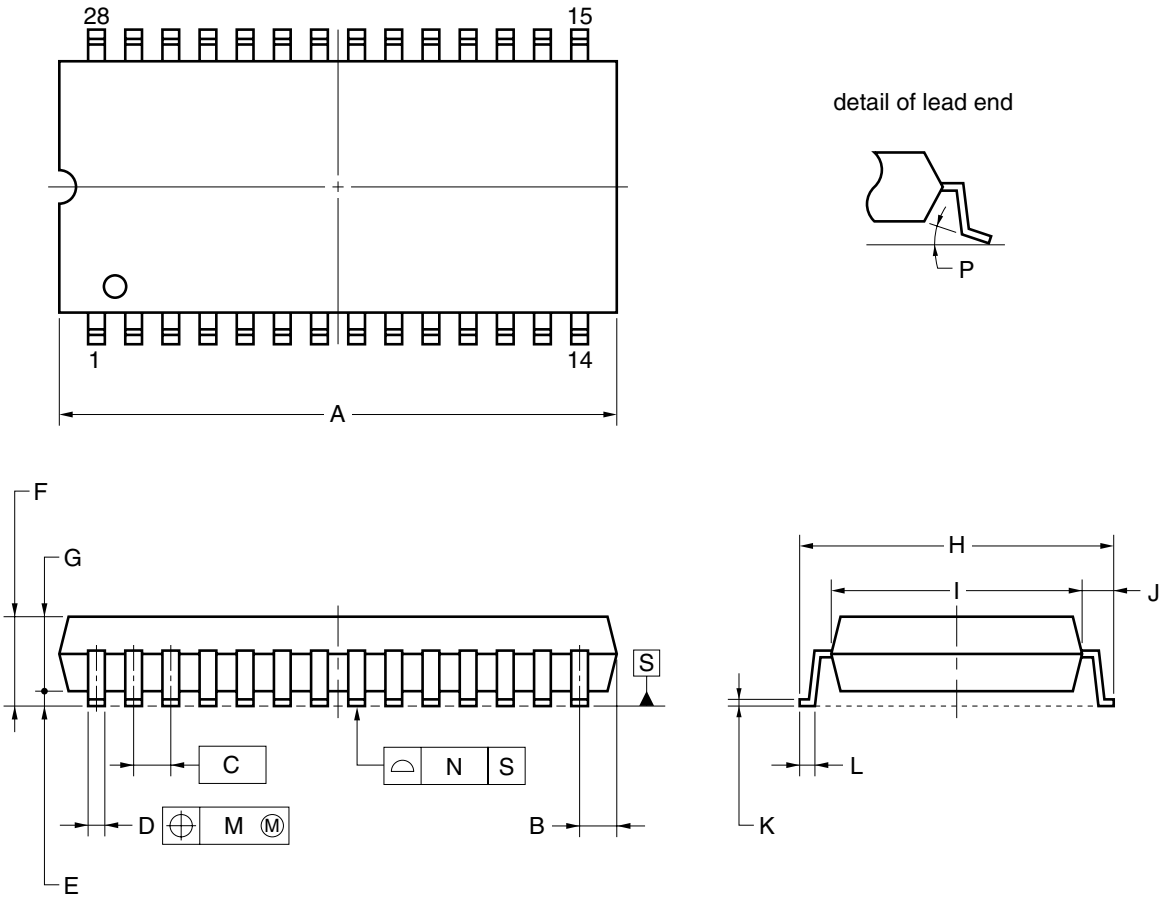
1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.

2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.2 MIN.
G	3.6±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.25
R	0 - 15°

P28C-100-600A1-2

28-PIN PLASTIC SOP (11.43 mm (450))



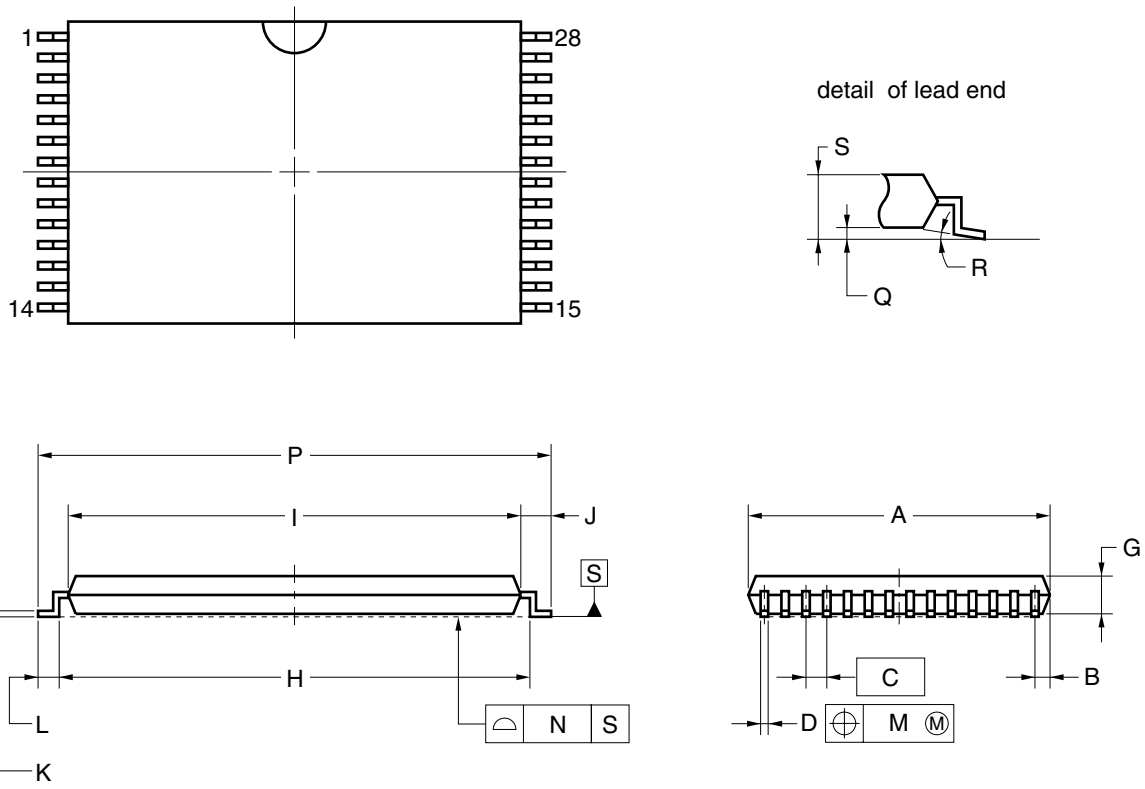
NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$18.0^{+0.6}_{-0.05}$
B	1.27 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.2±0.1
F	2.95 MAX.
G	2.55±0.1
H	11.8±0.3
I	8.4±0.1
J	1.7±0.2
K	0.22±0.05
L	0.7±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P28GU-50-450A-4

28-PIN PLASTIC TSOP(I) (8x13.4)



NOTES

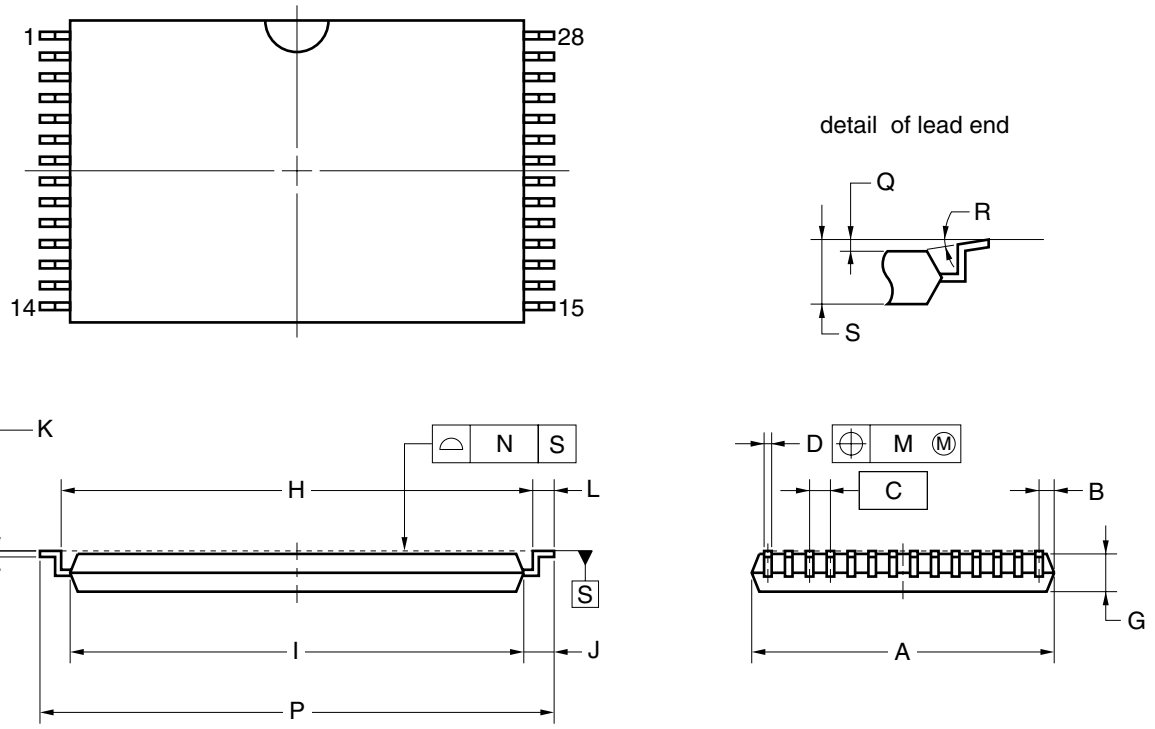
1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

2. "A" excludes mold flash. (Includes mold flash : 8.4mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.6 MAX.
C	0.55 (T.P.)
D	$0.22^{+0.08}_{-0.07}$
G	1.0
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5±0.1
M	0.08
N	0.10
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.

P28GW-55-9JL-2

28-PIN PLASTIC TSOP(I) (8x13.4)



NOTE

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.4mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.6 MAX.
C	0.55 (T.P.)
D	$0.22^{+0.08}_{-0.07}$
G	1.0
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5±0.1
M	0.08
N	0.10
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.

P28GW-55-9KL-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD43256B.

Types of Surface Mount Device

μPD43256BGU-xxL : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGU-xxLL : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGU-Axx : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGU-Bxx : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGW-xxLL-9JL : 28-pin PLASTIC TSOP (I) (8x13.4) (Normal bent)
μPD43256BGW-xxLL-9KL : 28-pin PLASTIC TSOP (I) (8x13.4) (Reverse bent)
μPD43256BGW-Axx-9JL : 28-pin PLASTIC TSOP (I) (8x13.4) (Normal bent)
μPD43256BGW-Axx-9KL : 28-pin PLASTIC TSOP (I) (8x13.4) (Reverse bent)
μPD43256BGW-Bxx-9JL : 28-pin PLASTIC TSOP (I) (8x13.4) (Normal bent)
μPD43256BGW-Bxx-9KL : 28-pin PLASTIC TSOP (I) (8x13.4) (Reverse bent)
μPD43256BGU-xxL-A : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGU-xxLL-A : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGU-Axx-A : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGU-Bxx-A : 28-pin PLASTIC SOP (11.43 mm (450))
μPD43256BGW-xxLL-9JL-A : 28-pin PLASTIC TSOP (I) (8x13.4) (Normal bent)
μPD43256BGW-xxLL-9KL-A : 28-pin PLASTIC TSOP (I) (8x13.4) (Reverse bent)
μPD43256BGW-Axx-9JL-A : 28-pin PLASTIC TSOP (I) (8x13.4) (Normal bent)
μPD43256BGW-Axx-9KL-A : 28-pin PLASTIC TSOP (I) (8x13.4) (Reverse bent)
μPD43256BGW-Bxx-9JL-A : 28-pin PLASTIC TSOP (I) (8x13.4) (Normal bent)
μPD43256BGW-Bxx-9KL-A : 28-pin PLASTIC TSOP (I) (8x13.4) (Reverse bent)

Types of Through Hole Mount Device

μPD43256BCZ-xxL : 28-pin PLASTIC DIP (15.24 mm (600))
μPD43256BCZ-xxLL : 28-pin PLASTIC DIP (15.24 mm (600))

Soldering process	Soldering conditions
Wave soldering (only to leads)	Solder temperature : 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
14th edition/ Jun. 2006	p.1	p.1	Deletion	–	Description of Version X and P has been deleted.

[MEMO]

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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