SONY

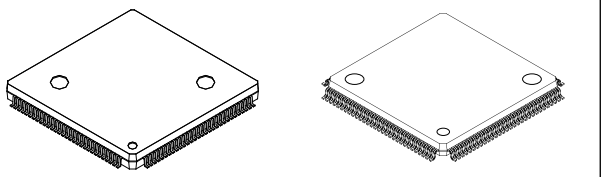
CXD1856Q/R

MPEG1 Decoder

Description

The CXD1856Q/R is a single-chip MPEG1 decoder with a built-in CD-ROM decoder which allows decoding of MPEG1 system, video and audio layers. A built-in CD-ROM decoder enables direct connection with a CD-DSP. Combining this chip with a control microcomputer and 4-Mbit DRAM, etc. allows configuration of a MPEG1 decoding system for video CD players, etc.

120 pin QFP (Plastic) 120 pin LQFP (Plastic)



Structure

Silicon gate CMOS IC

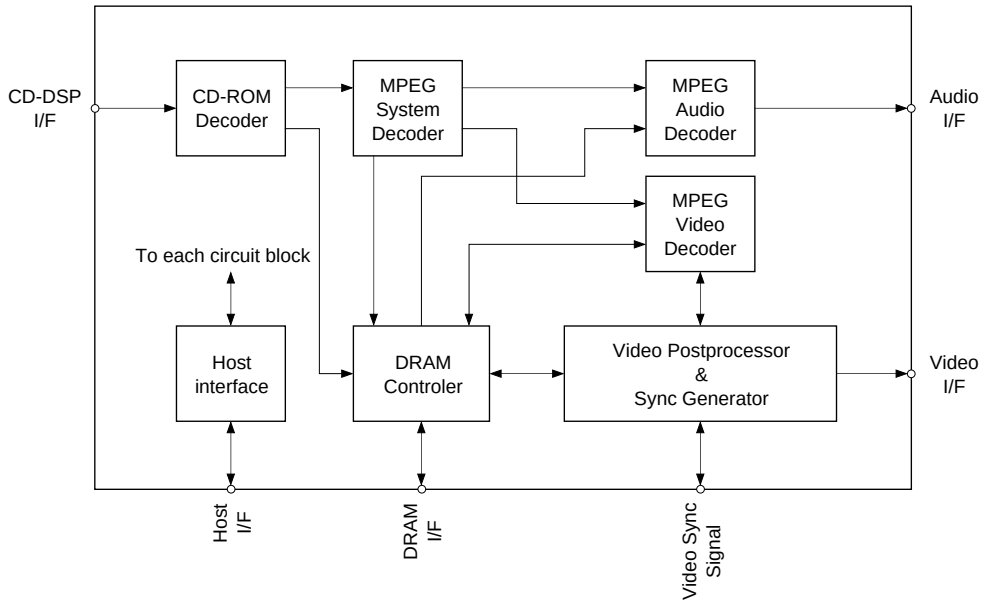
Applications

Video CD players, MPEG1 decoder boards, etc.

Features

- Supply voltage: 3.3 ± 0.3V
- Input and output voltages: LVTTL compatible
- 5V can be applied as the input voltage (excluding some pins)
- Allows decoding of MPEG1 system, video and audio layers
- Built-in CD-ROM decoder allows direct connection with a CD-DSP
- CD-ROM decoded output can be transferred to and stored in an external DRAM
- RGB and YCbCr video data output allowed
- Built-in video sync generator
- Audio data output can support various DAC
- Supports various special playback modes
- Video CD PAL high resolution still picture can be decoded with a single 4-Mbit DRAM
- 8-bit parallel and 4-line serial host interfaces
- CD-DA through operation allowed

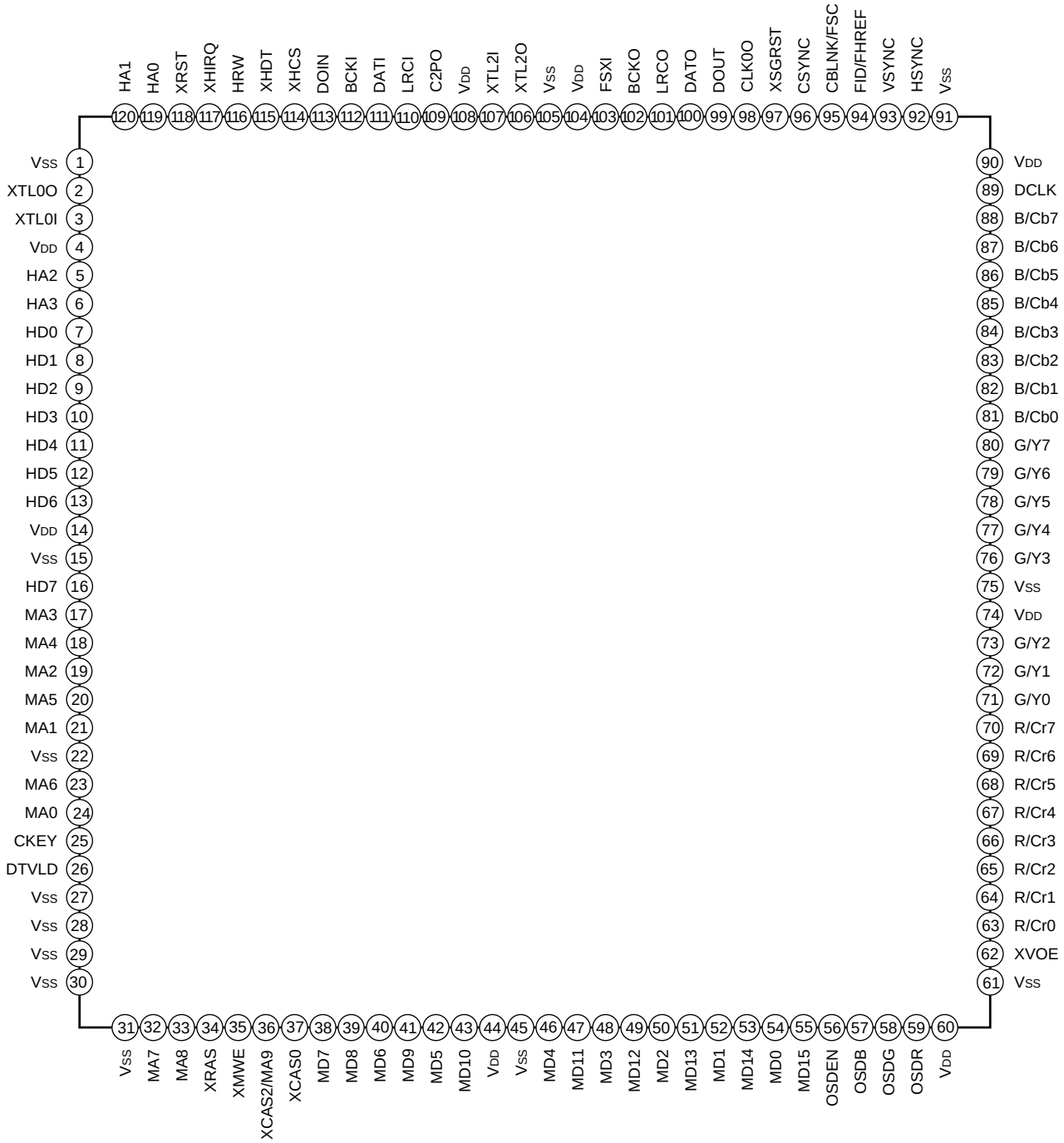
Block Diagram



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E97815-PS

1. Pin Configuration



2. Pin Description

Pin No.	Symbol	I/O	Description
	V_{DD}		+3.3V power supply
	V_{SS}		Connect to ground.
2	XTL0O	O	Video decoder master clock. Input the clock to XTL0I or connect an oscillator between XTL0I and XTL0O. The recommended frequencies are 27MHz, 28.6363MHz (NTSC 8fsc) and 35.4686MHz (PAL 8fsc).
3	XTL0I	I	
5, 6, 119, 120	HA0 to HA3	I	When the host interface operates in parallel mode, these pins are the register address inputs. In serial mode, HA0 is the serial data input, and HA1 to HA3 should be fixed to low level.
7 to 13, 16	HD0 to HD7	I/O	When the host interface operates in parallel mode, these pins are the register data I/Os. In serial mode, HD0 is the serial data output, and HD1 to HD7 should be fixed to low level.
17 to 21, 23, 24, 32, 33	MA0 to MA8	O	DRAM address signal outputs. Connect to the DRAM address pins so that the numbers match.
34	XRAS	O	Row address strobe signal output. Connect to the DRAM $\overline{RAS}$ signal pin.
35	XMWE	O	DRAM write enable signal output. Connect to the DRAM $\overline{WE}$ signal pin.
36	XCAS2/ MA9	O	Used when connecting 8 Mbits of DRAM. Connect to the upper word (256K to 512K-1) DRAM $\overline{CAS}$ signal pin (for both the upper and lower bytes) when the DRAM configuration is 256 Kwords $\times$ 16 bits $\times$ 2, and to the MA9 pin (for two DRAMs) when the DRAM configuration is 512 Kwords $\times$ 8 bits $\times$ 2.
37	XCAS0	O	DRAM column address strobe signal output. Connect to the lower word (0 to 256K-1) DRAM $\overline{CAS}$ signal pin (for both the upper and lower bytes) when the DRAM configuration is 256Kwords $\times$ 16 bits $\times$ 2, and to all DRAM $\overline{CAS}$ signal pins in all other cases.
38 to 43, 46 to 55	MD0 to MD15	I/O	DRAM data signal I/Os. Connect to the DRAM data pins so that the numbers match.
56	OSDEN	I	OSD enable signal. The enabled polarity is changed by the register settings.
57 to 59	OSDB, OSDG, OSDR	I	OSD data inputs. When the signal input to the OSDEN pin is enabled, the color registered in the color table which is specified by these three inputs (3 bits) is output as the image data.
62	XVOE	I	Video output enable signal. Image data output and DCLK output are enabled when this pin is low, and disabled when this pin is high (high impedance). Note that the output control register must be set to output enable for output to be enabled.
63 to 70	R/Cr0 to R/Cr7	O	Image data outputs. The output data format (RGB, YCbCr, etc.) and the correspondence between the pins and output data can be changed by setting the registers.
71 to 73, 76 to 88	G/Y0 to G/Y7		
81 to 88	B/Cb0 to B/Cb7		
89	DCLK	I/O	Dot clock (DCLK) signal. The DCLK frequency is normally 13.5MHz. DCLK can be input from this pin, or frequency divided from the clock input and output from this pin.

Pin No.	Symbol	I/O	Description
92	HSYNC	I/O	Horizontal sync signal. When using the built-in sync generator, the dot clock (DCLK) is frequency divided and output. When not using the sync generator, this pin is an input.
93	VSYNC	I/O	Vertical sync signal. When using the built-in sync generator, the dot clock (DCLK) is frequency divided and output. When not using the built-in sync generator, this pin is an input.
94	FID/FHREF	I/O	Field identification signal (FID) and horizontal sync phase reference signal (FHREF). The signal to be used is set in the register. When set to FID, this pin is an output if using the built-in sync generator, and an input if not using the built-in sync generator. High corresponds to odd fields. When set to FHREF, this pin outputs the signal obtained by frequency dividing XTL0. When XTL0 is 8fsc, this signal is equivalent to the HSYNC cycle, and can be used for phase comparison with the HSYNC signal.
95	CBLNK/ FSC	I/O	Composite blanking signal (CBLNK) and fsc signal. The signal to be used is set in the register. When set to CBLNK, this pin is an output if using the built-in sync generator, and an input if not using the built-in sync generator. When set to fsc, this pin outputs the signal obtained by frequency dividing XTL0. The frequency division ratio can be selected from 1/8 or 1/16.
96	CSYNC	O	Composite sync signal obtained by frequency dividing DCLK. This pin cannot be input.
97	XSGRST	I	Sync generator reset signal input. The built-in sync generator is initialized by setting this pin low.
98	CLK0O	O	Output for clock obtained by frequency dividing XTL0. The frequency division ratio can be selected from 1, 1/2, 1/4 or 1/8.
99	DOUT	O	Audio digital output.
100	DATO	O	Audio serial data output to DAC.
101	LRCO	O	L/R clock output to DAC.
102	BCKO	O	Bit clock output to DAC.
103	FSXI	I	Audio interface clock input. Input 256fs (11.2896MHz), 384fs (16.9344MHz), 512fs (22.5792MHz), or 768fs (33.8688MHz), etc.
106	XTL2O	O	Master clock for CD-ROM and audio decoders. Input the clock to XTL2I or connect an oscillator between XTL2I and XTL2O. The recommended frequency is 45MHz. Note that this clock is for the internal circuits, and the input and output are not synchronized.
107	XTL2I	I	
109	C2PO	I	C2 pointer input from CD-DSP. Indicates that the DATI input contains an error.
110	LRCI	I	LR clock input from CD-DSP. Indicates the L or R channel of DATI.
111	DATI	I	Serial data input from CD-DSP.
112	BCKI	I	Bit clock input from CD-DSP. This clock strobes the DATI input.
113	DOIN	I	Digital data input from CD-DSP.
114	XHCS	I	Chip select signal input during register access.
115	XHDT	I/O	Wait signal output during register access. Host interface operates in parallel mode and the wait signal is output by the register switching during DRAM access. This pin functions as an open drain, and should therefore be pulled up. It should be pulled up when the host interface operates in serial mode as well.

Pin No.	Symbol	I/O	Description
116	HRW	I	R/$\overline{W}$ signal input when the host interface operates in parallel mode. Serial clock input in serial mode.
117	XHIRQ	O	Interrupt request signal output. This pin functions as an open drain, and should therefore be pulled up.
118	XRST	I	Hardware reset signal input. All operation is initialized by setting this pin low.
25	CKEY	O	Chroma key signal. While the color specified as the key is output, this pin becomes low. When not used, leave this pin open.
26	DTVLD	O	Video data judgement signal. While the image data within the frame memory is output, this pin becomes high; during the border color output or blanking, low. When not used, leave this pin open.

3. Electrical Characteristics

3-1. Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.5 to +4.6	V	
Input pin voltage	V_I	–0.5 to V_{DD} + 0.5	V	*1
Input pin voltage	V_I	–0.5 to +5.5	V	*2
Output pin voltage	V_O	–0.5 to V_{DD} + 0.5	V	*3
Output pin voltage	V_O	–0.5 to +5.5	V	*4
I/O pin voltage	$V_{I/O}$	–0.5 to +5.5	V	
Allowable power dissipation	P_D	1.0	W	
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	

*1 XTL0I and XTL2I pins

*2 Input pins other than those in *1 above.

*3 XTL0O and XTL2O pins

*4 Output pins other than those in *3 above.

3-2. Recommended Operating Conditions (Ta = –20 to +75°C, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
High level input voltage	V_{IH}	2.2	—	V_{DD}	V	*1
High level input voltage	V_{IH}	2.2	—	5.0	V	*2
Low level input voltage	V_{IL}	0	—	0.8	V	
Input rise time	Tr	0	—	50	ns	
Input fall time	Tf	0	—	50	ns	
Operating temperature	Topr	–20	—	75	°C	

*1 XTL0I and XTL2I pins

*2 I/O pins and input pins other than those in *1 above.

3-3. DC Characteristics

(Ta = –20 to +75°C, V_{SS} = 0V, V_{DD} = 3.3 ± 0.3V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Remarks
Average operating supply current	I_{DD}		—	—	100	mA	
Input leak current	I_I	V_I = 0 to 5.0V	–40	—	40	µA	*1
High level output voltage	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8	—	—	V	*2
High level output voltage	V_{OH}	I_{OH} = –100µA	—	V_{DD} – 0.4	—	V	*2
Low level output voltage	V_{OL}	I_{OL} = 4mA	—	—	0.4	V	*2
Low level output voltage	V_{OL}	I_{OL} = 100µA	—	0.04	—	V	*2
Output leak current	I_{OZ}	V_O = 0 to 5.0V, output disabled status	–40	—	40	µA	*2
Feedback resistance	R_{FB}	V_I = 0V or V_I = V_{DD}	250k	1M	2.5M	Ω	*3
Logic threshold value	LVth		—	V_{DD}/2	—	V	*4
High level output voltage	V_{OH}	I_{OH} = –12mA	V_{DD}/2	—	—	V	*5
Low level output voltage	V_{OL}	I_{OL} = 12mA	—	—	V_{DD}/2	V	*5

*1 Input pins other than XTL0I and XTL2I

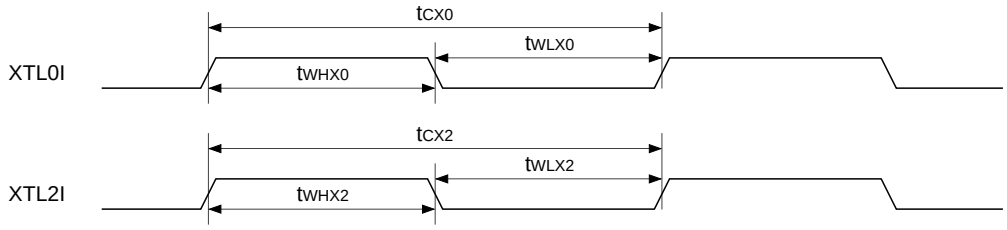
*2 I/O pins and output pins other than XTL0O and XTL2O

*3 Oscillators (between XTL0I and XTL0O, and between XTL2I and XTL2O)

*4 XTL0I and XTL2I pins

*5 XTL0O and XTL2O pins

3-4. Clock Signal AC Characteristics



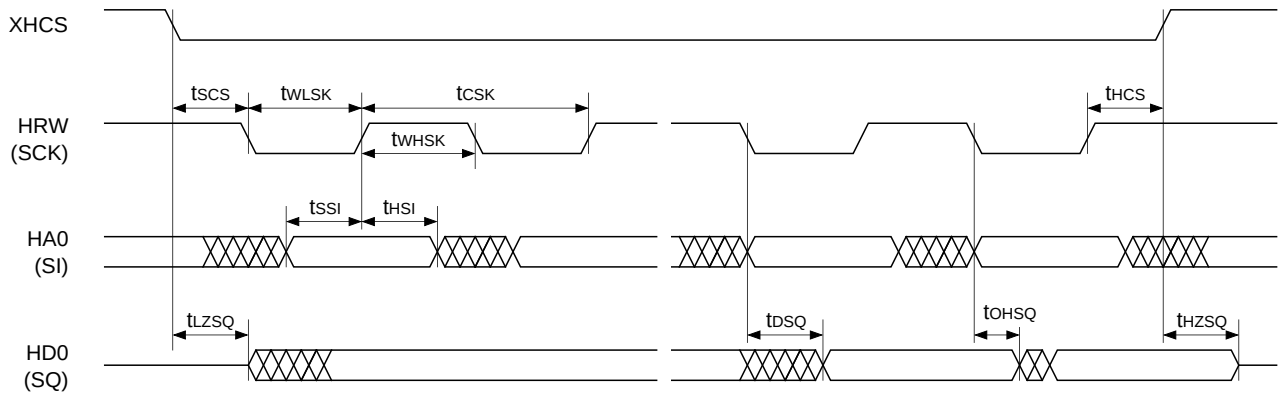
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XTL0I frequency	f_{X0}	—	—	60	MHz	*1
XTL0I cycle	t_{CX0}	33.3	—	—	ns	*1
XTL0I high level interval	t_{WHX0}	10	—	—	ns	
XTL0I low level interval	t_{WLX0}	10	—	—	ns	
XTL2I frequency	f_{X2}	44.7	45.1584	45.4	MHz	*2
XTL2I cycle	t_{CX2}	—	22.2	—	ns	*2
XTL2I high level interval	t_{WHX2}	8	—	—	ns	
XTL2I low level interval	t_{WLX2}	8	—	—	ns	

*1 When using in combination with the XTL0O pin as an oscillator, the maximum oscillation frequency is 50MHz.

*2 When using in combination with the XTL2O pin as an oscillator, the maximum oscillation frequency is 50MHz.

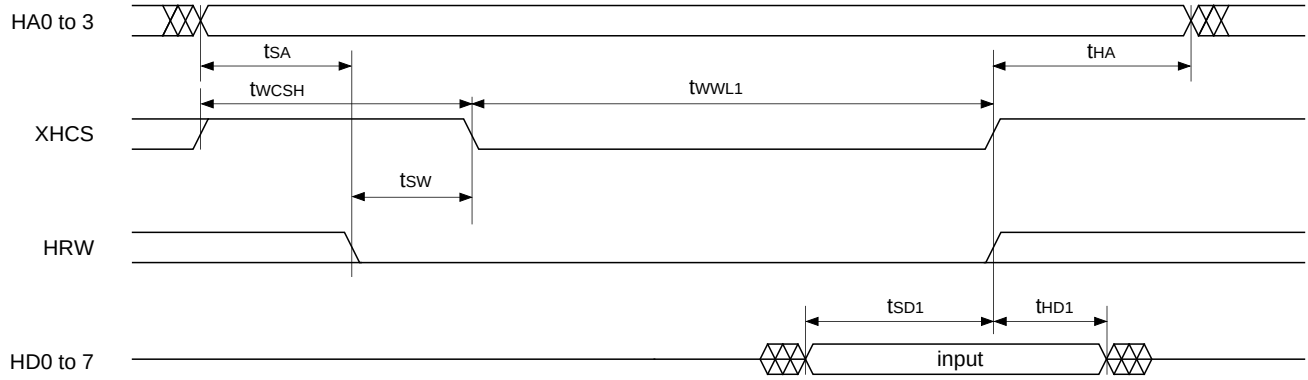
3-5. Host Interface AC Characteristics

3-5-1. Serial Mode (write, read)



Item	Symbol	Min.	Max.	Unit	Remarks
Serial clock frequency	f_{SK}	—	2	MHz	
Serial clock cycle	t_{CSK}	500	—	ns	
Serial clock high level interval	t_{WHSK}	100	—	ns	
Serial clock low level interval	t_{WLSK}	100	—	ns	
Chip select setup time	t_{SCS}	0	—	ns	
Chip select hold time	t_{HCS}	500	—	ns	
Serial input setup time	t_{SSI}	30	—	ns	
Serial input hold time	t_{HSI}	30	—	ns	
Serial output enable time	t_{LZSQ}	0	15	ns	
Serial output determination time	t_{DSQ}	—	40	ns	
Serial output hold time	t_{OHSQ}	5	—	ns	
Serial output disable time	t_{HZSQ}	0	15	ns	

3-5-2. Parallel Mode, Register Write



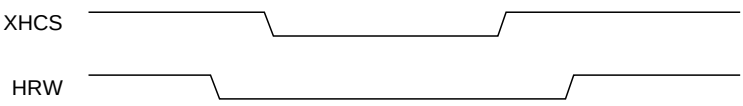
Item	Symbol	Min.	Max.	Unit	Remarks
Address setup time	t_{SA}	20	—	ns	
Address hold time	t_{HA}	20	—	ns	
Chip disable time	t_{WCSH}	20	—	ns	
Write pulse width	t_{WWL1}	70	—	ns	*2
Write command setup time	t_{SW}	0	—	ns	
HD input setup time	t_{SD1}	25	—	ns	*1
HD input hold time	t_{HD1}	25	—	ns	*1

*1 Specified for the edge of XHCS or HRW, whichever is earlier.
The data bus does not enter the read mode even when HRW rises ealier than XHCS.

*2 Interval during which both XHCS and HRW are low.

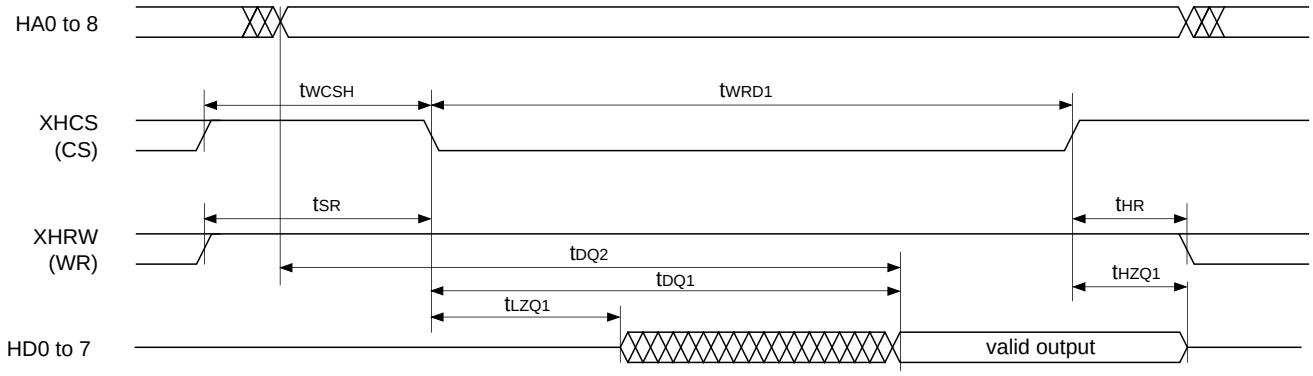
<Notes on Operating Timing>

Pay attention to the timing shown below for the CXD1856Q/R parallel mode write.



1. XHCS is enable after determining HRW.
2. It is recommended that XHCS rises firstly and then HRW rises, through the rising order is not so much considered.

3-5-3. Parallel Mode, Register Read



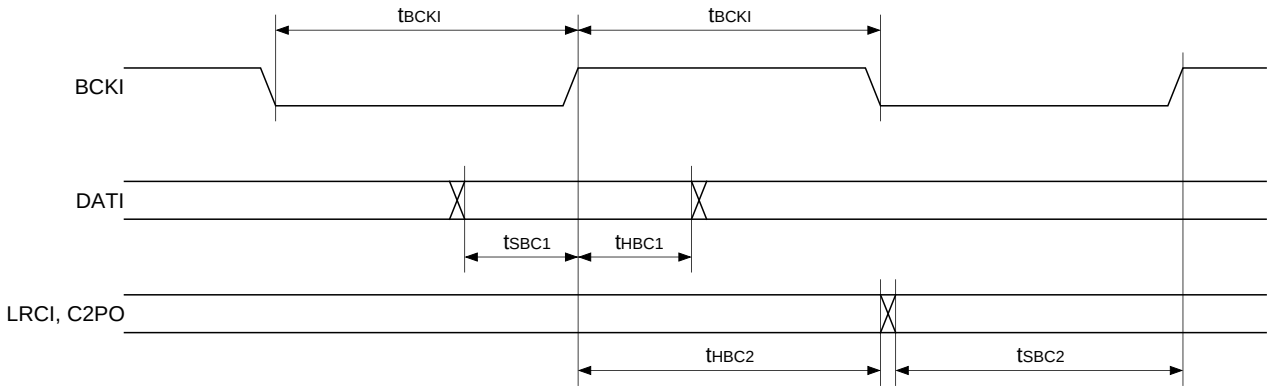
Item	Symbol	Min.	Max.	Unit	Remarks
Chip disable time	t_{WCSH}	20	—	ns	
Read pulse width	t_{WRD1}	70	—	ns	
Read setup time	t_{SR}	10	—	ns	
Read hold time	t_{HR}	10	—	ns	
HD output enable time (for CE)	t_{LZQ1}	0	—	ns	*1
HD output determination time (for CE)	t_{DQ1}	—	60	ns	*2
HD output determination time (for HA)	t_{DQ2}	0	60	ns	*2
HD output disable time (for CE)	t_{HZQ1}	—	15	ns	

*1 HD output is enabled when both conditions are met.

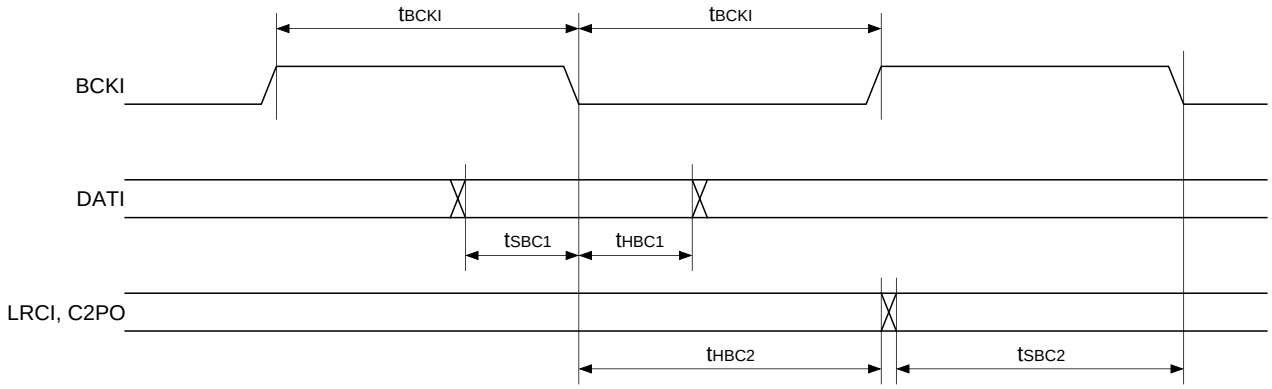
*2 HD output is determined when all conditions are met.

3-6. Interface for CD Signal Processing LSI

BCKFEDG = 0

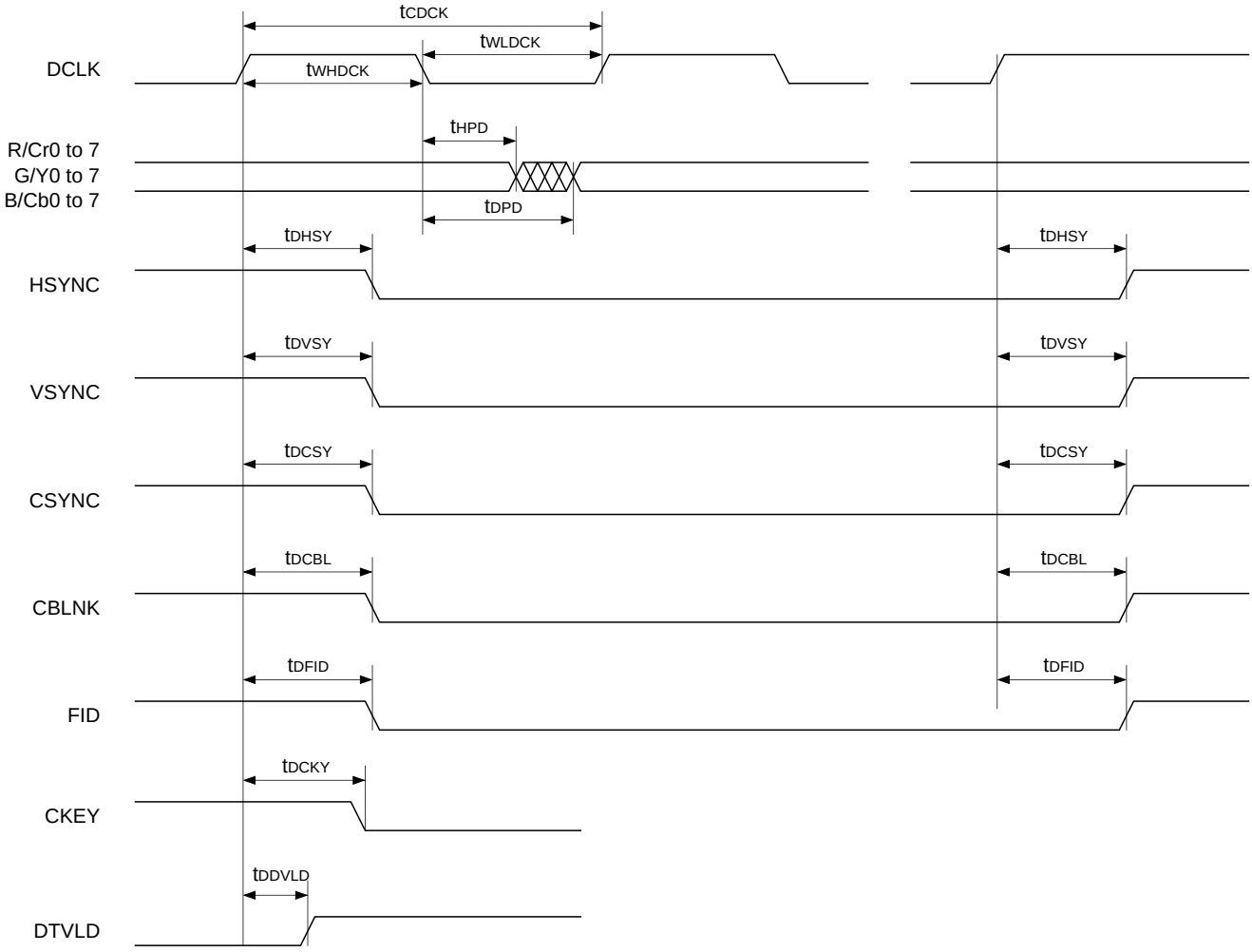


BCKFEDG = 1



Item	Symbol	Min.	Max.	Unit	Remarks
BCKI frequency	f_{BCKI}		5.7	MHz	
BCKI pulse width	t_{BCKI}	87	—	ns	
DATI setting time (for BCKI)	t_{SBC1}	20	—	ns	
DATI hold time (for BCKI)	t_{HBC1}	20	—	ns	
LRCI, C2PO setting time (for BCKI)	t_{SBC2}	20	—	ns	
LRCI, C2PO hold time (for BCKI)	t_{HBC2}	20	—	ns	

3-7. Image Data Output, Video Sync Signal Output AC Characteristics

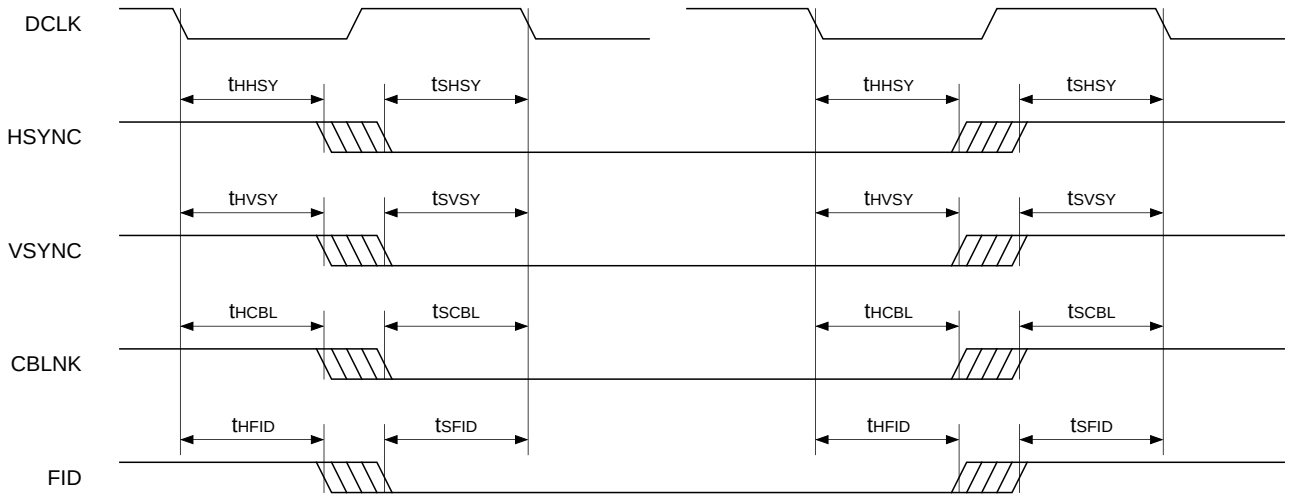


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCLK frequency	f_{DCK}	—	13.5	—	MHz	*1
DCLK cycle	t_{CDCK}	—	74.1	—	ns	*1
DCLK high level interval	t_{WHDCK}	—	37	—	ns	*1
DCLK low level interval	t_{WLDCK}	—	37	—	ns	*1
Image data output determination time	t_{DPD}	—	—	15	ns	*1, *2
Image data output hold time	t_{HPD}	0	—	—	ns	*1, *2
HSYNC output delay time	t_{DHSY}	—	—	30	ns	*1
VSYNC output delay time	t_{DVSY}	—	—	30	ns	*1
CSYNC output delay time	t_{DCSY}	—	—	30	ns	*1
CBLNK output delay time	t_{DCBL}	—	—	30	ns	*1
FID output delay time	t_{DFID}	—	—	30	ns	*1
CKEY output delay time	t_{DCKY}	—	—	47	ns	
DTVLD output delay time	t_{DDVLD}	—	—	48	ns	

*1 When both inputting and outputting DCLK. For output, a load of 75pF is connected to DCLK.

*2 The chart shows the case where the pixel data output is synchronized to the fall of DCLK, but is also the same when synchronized to the rise of DCLK.

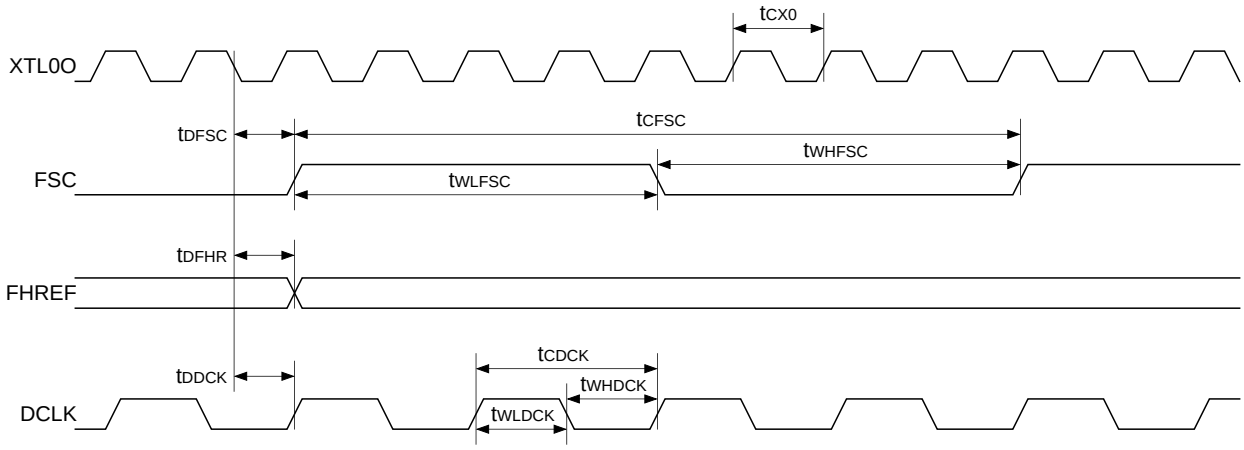
3-8. Video Sync Signal Input AC Characteristics



Item	Symbol	Min.	Max.	Unit	Remarks
HSYNC hold time	t_{HHSY}	5	—	ns	*1
HSYNC setup time	t_{SHSY}	5	—	ns	*1
VSYNC hold time	t_{HVSY}	5	—	ns	*1
VSYNC setup time	t_{SVSY}	5	—	ns	*1
CBLNK hold time	t_{HCBL}	5	—	ns	*1
CBLNK setup time	t_{SCBL}	5	—	ns	*1
FID hold time	t_{HFID}	5	—	ns	*1
FID setup time	t_{SFID}	5	—	ns	*1

*1 When both inputting and outputting DCLK. For output, a load of 75pF is connected to DCLK.

3-9. fsc System Signal Output, DCLK Output AC Characteristics

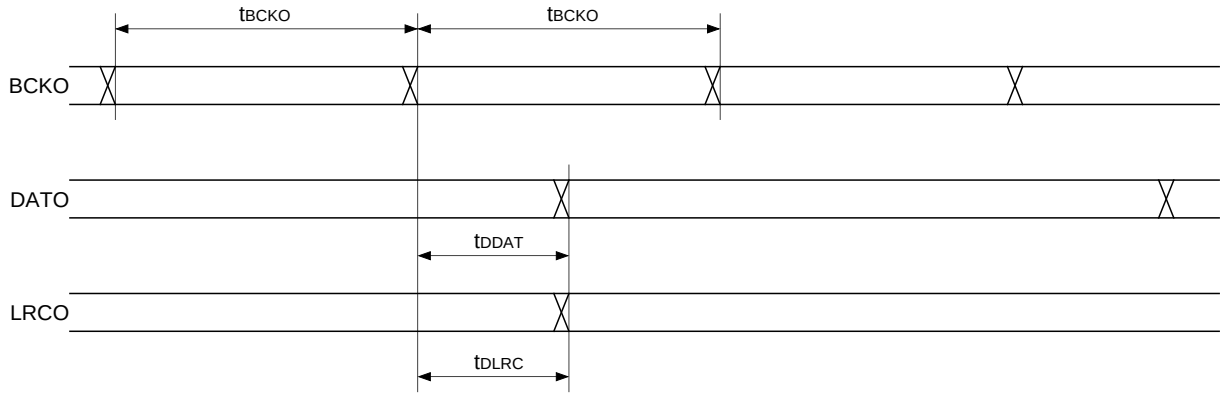


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
FSC frequency	f_{FSC}	—	$1/(i \times t_{CX0})$	—		*1
FSC cycle	t_{CFSC}	—	$i \times t_{CX0}$	—		*1
FSC high level interval	t_{WHFSC}	—	$i \times t_{CX0}/2$	—		*1
FSC low level interval	t_{WLFSC}	—	$i \times t_{CX0}/2$	—		*1
FSC output delay time	t_{DFSC}	—	—	15	ns	
FHREF output delay time	t_{DFHR}	—	—	15	ns	
DCLK frequency	f_{DCK}	—	$1/(j \times t_{CX0})$	—		*2
DCLK cycle	t_{CDCK}	—	$j \times t_{CX0}$	—		*2
DCLK high level interval	t_{WHDCK}	—	$j \times t_{CX0}/2$	—		*2
DCLK low level interval	t_{WLDCK}	—	$j \times t_{CX0}/2$	—		*2
DCLK output delay time	t_{DDCK}	—	—	15	ns	

*1 The frequency division ratio i can be selected from 8 or 16.

*2 The frequency division ratio j can be selected from 2 or 4.

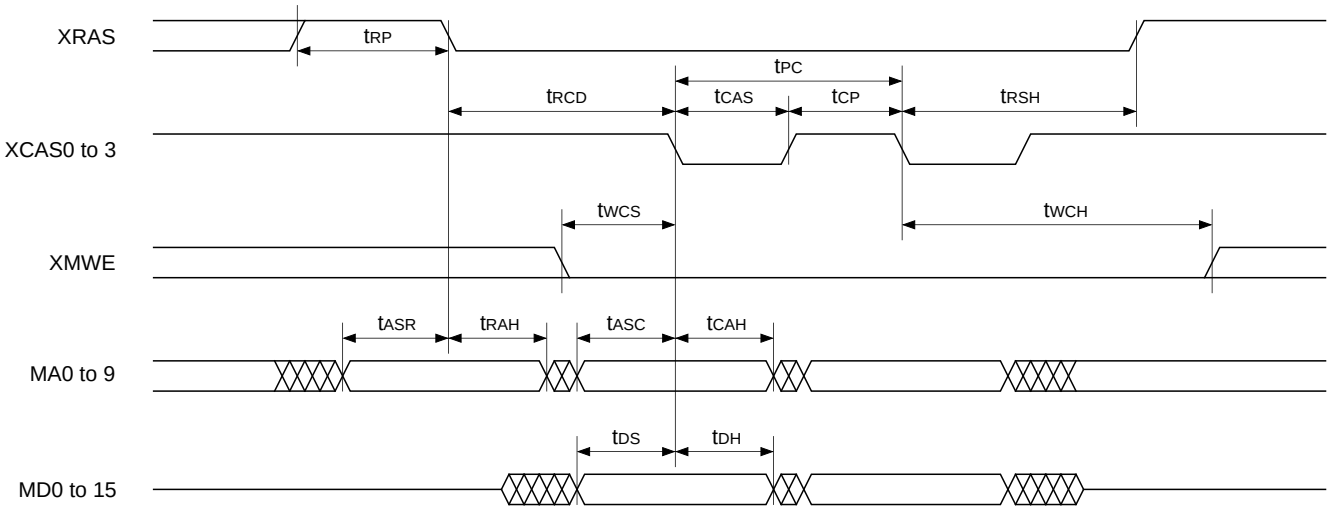
3-10. Audio Interface



Item	Symbol	Min.	Max.	Unit	Remarks
BCKO frequency	f_{BCKO}		3.1	MHz	
BCKO pulse width	t_{BCKO}	160	—	ns	
DATO delay time (for BCKO)	t_{DDAT}	—	40	ns	
LRCO delay time (for BCKO)	t_{DLRC}	—	40	ns	

3-11. DRAM Interface AC Characteristics

3-11-1. Write Cycle

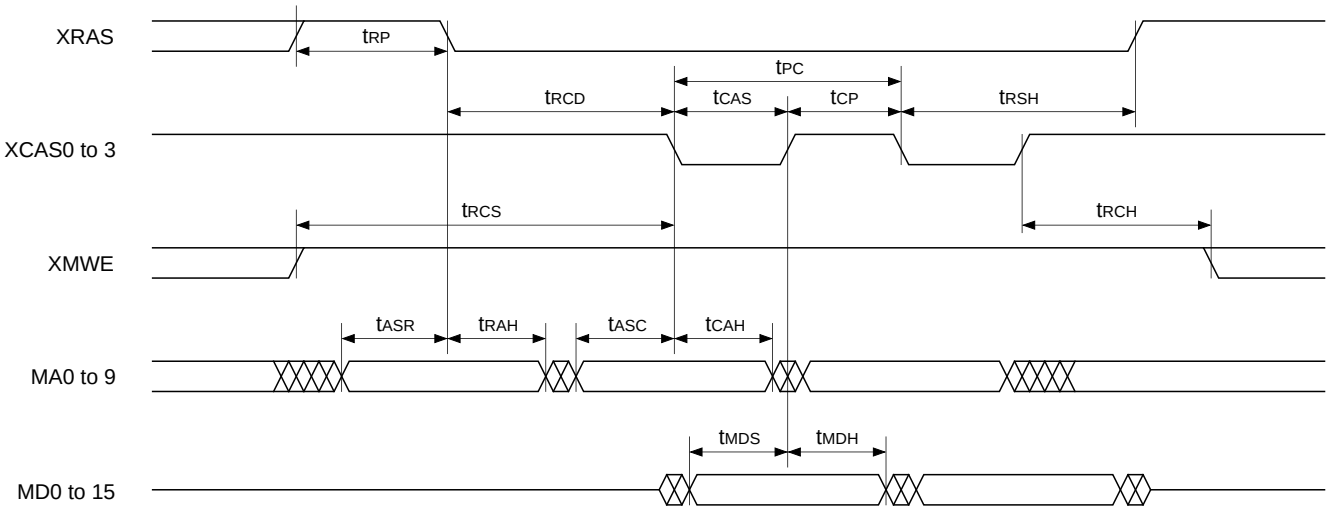


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
RAS precharge time	t_{RP}		$2 \times tv$	—	ns	*2
RAS to CAS delay time	t_{RCD}		$2 \times tv$	—	ns	*2
RAS hold time	t_{RSH}		tv	—	ns	*2
Fast page mode cycle time	t_{PC}		$2 \times tv$	—	ns	*2
CAS pulse width	t_{CAS}		tv	—	ns	*2
CAS precharge time	t_{CP}		tv	—	ns	*2
Write command setup time	t_{WCS}		tv	—	ns	
Write command hold time	t_{WCH}		$2 \times tv$	—	ns	
Row address setup time	t_{ASR}		tv	—	ns	*2
Row address hold time	t_{RAH}		tv	—	ns	*2
Column address setup time	t_{ASC}		tv	—	ns	*2
Column address hold time	t_{CAH}		tv	—	ns	*2
Write data setup time	t_{DS}		tv	—	ns	
Write data hold time	t_{DH}		tv	—	ns	

*1 tv is the basic clock cycle for the DRAM interface circuit.

*2 Same as the DRAM interface read cycle.

3-11-2. Read Cycle



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read command setup time	t_{RCS}		$4 \times tv$	—	ns	
Read command hold time	t_{RCH}		tv	—	ns	
Read data setup time	t_{MDS}		2	—	ns	
Read data hold time	t_{MDH}		8	—	ns	

*1 tv is the basic clock cycle for the DRAM interface circuit.

*2 See the DRAM interface write cycle for items which appear in the timing chart but not in the table.

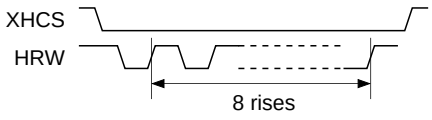
4. Description of Functions

4-1. Host Interface Function

- The CXD1856Q/R operation is controlled by writing and reading registers. Write and read can also be performed to an external DRAM via the registers. See the separately issued Register Manual for the relationship between the registers and operation.
- The host interface operates while XHCS is low and does not operate while XHCS is high.
- The host interface operating mode can be set to 4-line serial or 8-bit parallel. The operating mode is selected automatically at the end of the initial access after the hardware has been reset. (See the figure below.) Registers are not accessed correctly until this selection has been determined, or in other words until the end of the initial access after the hardware has been reset. Also, the HA3 to HA0 inputs should all be fixed low during the operating mode selection access.

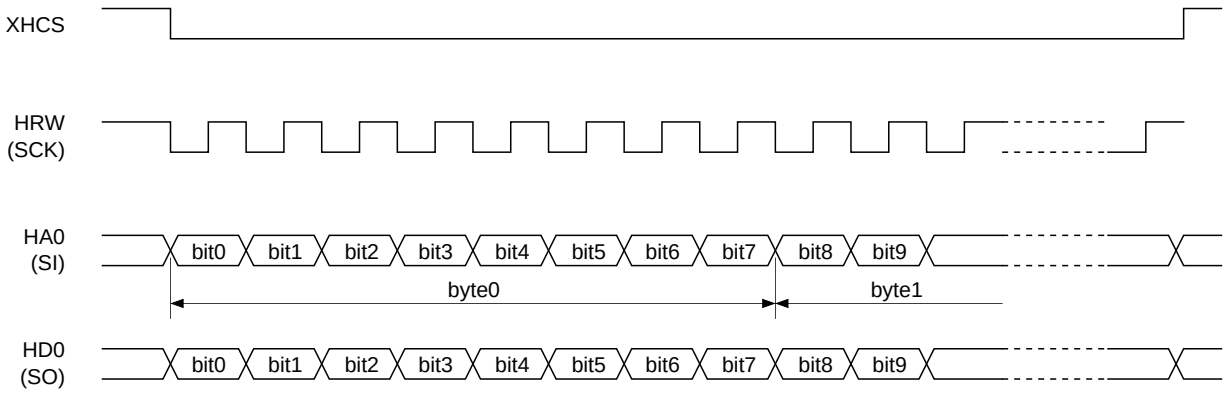


Access judged as parallel mode



Access judged as serial mode

- The serial mode signal format is as follows.



1) In serial mode, input data is fetched in sync with the rise of HRW (SCK). Output data is synchronized with the fall of HRW.
2) The initial byte (byte0) of the input after XHCS changes to low is a command. This command determines the subsequent byte processing. See the following page for a description of commands and processing.
3) Input data is processed in one byte units. Therefore, when the final data consists of a number of bits which is less than one byte, this deficient data is not processed. Be sure to input data with a number of bits which is an integer multiple of 8. Also, the 0x20, 0x60, 0xA0 and 0xE0 commands process data in two byte units, so data which is an even multiple of 8 should be input when using these commands.

Command bit7 ⋯ bit0	write read	2nd input byte	3rd input byte	4th input byte	Successive odd-numbered input bytes	Successive even-numbered input bytes	first bit	Auto inc.
00000000	write	Register No. +U/L byte select	Register data	Register No. +U/L byte select	Register data	Register No. +U/L byte select	LSB first	No
00010000	read	Register No. +U/L byte select	don't care	Register No. +U/L byte select	don't care	Register No. +U/L byte select	LSB first	No
00100000	write	Register No.	Register data (Lower byte)	Register data (Upper byte)	Register data (Lower byte)	Register data (Upper byte)	LSB first	No
00110000	read	Register No.	don't care	don't care	don't care	don't care	LSB first	No
01100000	write	Register No.	Register data (Lower byte)	Register data (Upper byte)	Register data (Lower byte)	Register data (Upper byte)	LSB first	Yes
01110000	read	Register No.	don't care	don't care	don't care	don't care	LSB first	Yes
10000000	write	Register No. +U/L byte select	Register data	Register No. +U/L byte select	Register data	Register No. +U/L byte select	MSB first	No
10010000	read	Register No. +U/L byte select	don't care	Register No. +U/L byte select	don't care	Register No. +U/L byte select	MSB first	No
10100000	write	Register No.	Register data (Upper byte)	Register data (Lower byte)	Register data (Upper byte)	Register data (Lower byte)	MSB first	No
10110000	read	Register No.	don't care	don't care	don't care	don't care	MSB first	No
11100000	write	Register No.	Register data (Upper byte)	Register data (Lower byte)	Register data (Upper byte)	Register data (Lower byte)	MSB first	Yes
11110000	read	Register No.	don't care	don't care	don't care	don't care	MSB first	Yes

Description of Commands

1) The "write read" column indicates whether that command writes data to or reads data from the registers.
2) Bytes marked with "Register No. + U/L byte select" specify the register to be accessed as well as whether to access the upper or lower bytes of the register. The upper 7 bits specify the register No., and the lowermost bit specifies the upper or lower bytes. When the lowermost bit is "0", the lower bytes are selected, when "1", the upper bytes are selected.
3) Bytes marked with "Register No." specify the register to be accessed. The upper 7 bits specify the register No., and the lowermost bit can be either "0" or "1".
4) The "Auto inc." column indicates the presence of the register No. auto increment function. For commands without this function, the most recently input register No. is valid. For example, in case of the command 0x00, the register data input by the odd bytes is written to the register specified by the previous byte's input. For the command 0x20, all subsequent data is written sequentially to the register specified by the 2nd input byte.
5) For commands with the register No. auto increment function, the register specified by the 2nd input byte is accessed first, and then access shifts to the register No. incremented by one each time the data for one register (2 bytes) is read or written. For example, when using the command 0x60, if 0x08 is specified by the 2nd input byte, the 3rd and 4th input bytes are written to register 0x08, and the 5th and 6th input bytes are written to register 0x09.
6) Bytes marked with "register data" are the data to be written to the registers during write commands.

7) When executing read commands, register data output starts from the 3rd output byte (bit 16). All earlier output data is invalid data. Access shifts to a new register each time the output for one register (2 bytes) is finished. For example, in case of the command 0x10, the byte data specified by the 2nd input byte is output to the 3rd output byte, the other byte data in the same register is output to the 4th byte, and the byte data specified by the 4th input byte is output to the 5th output byte.
8) The "first bit" column indicates whether LSB first or MSB first processing is performed for input or output of the 2nd and subsequent bytes. This specification does not apply to the 1st byte (command). Commands are normally LSB first. If LSB first is specified, processing is performed in the order where the initial bit in each byte is LSB and the final bit is MSB. This order is reversed for MSB first. Note that for registers, bit 15 noted in the Register Manual is MSB and bit 0 is LSB.

4-2. DRAM Interface Function

- The applicable DRAMs are speed version 70 devices (RAS access time (Trac) of 70ns or less) with the fast page mode function.
- When the total capacity of the external DRAM is 4 Mbits, use a 2CAS type DRAM with a configuration of 256 Kwords × 16 bits. When the total capacity is 8 Mbits, use two 2CAS type DRAMs with a configuration of 256 Kwords × 16 bits or 512 Kwords × 8 bits.
- Refresh is performed automatically using RAS-only-refresh. External control is not necessary.
- The DRAM is divided into the image frame memory, audio bit stream buffer, video bit stream buffer, user data and on-memory register areas.
- The user data area can be used freely by the user, and CD-ROM decoded output can also be transferred to this area. This area can be used to store video CD PSD, etc.
- The desired DRAM areas can be accessed from the control microcomputer via the registers.

4-3. CD-ROM Decoder Function

- CD signal processor LSI interface
  The CD-ROM decoder has a CD signal processor LSI (CD-DSP) interface which directly interfaces the serial data output from the CD-DSP. This interface supports a wide variety of input formats to enable connection with general CD-DSP.
- CD-ROM data decoding (supports CD-ROM XA format mode2, form1 and form2)
  CD-ROM data input from the CD-DSP supports CD-ROM XA format (mode2, form1 and form2).
- Input CD-ROM data is decoded by the CD-ROM decoder block. Also, the CD-DA signal input from the CD-DSP can be output directly from the audio interface.
- The CD-ROM decoder has the following decoding and data transfer operating modes. The real-time correction and write-only modes facilitate the loading of video CD PSD to the external DRAM, etc.

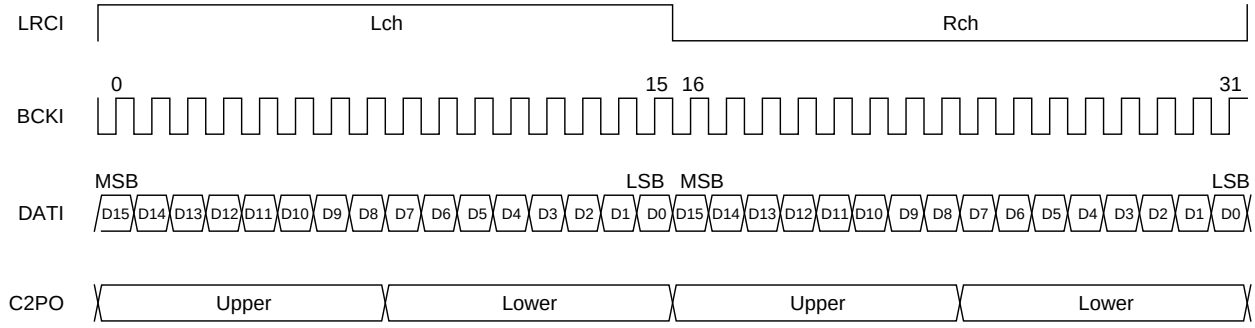
1) Auto transfer mode
   The MPEG pack data within one sector of the video CD is automatically transferred to the system decoder, where the audio stream sector or video stream sector can be decoded. This mode transfers 2324 bytes counted from the initial byte of user data within one sector to the system decoder.

2) Real-time correction mode
   This mode executes error detection and correction processing for mode2, form1 sectors. The 2048 bytes of user data within the error processed sector are transferred to the user area of the external DRAM. The 4 bytes of header information within the sector can also be loaded in the on-memory register within the DRAM.

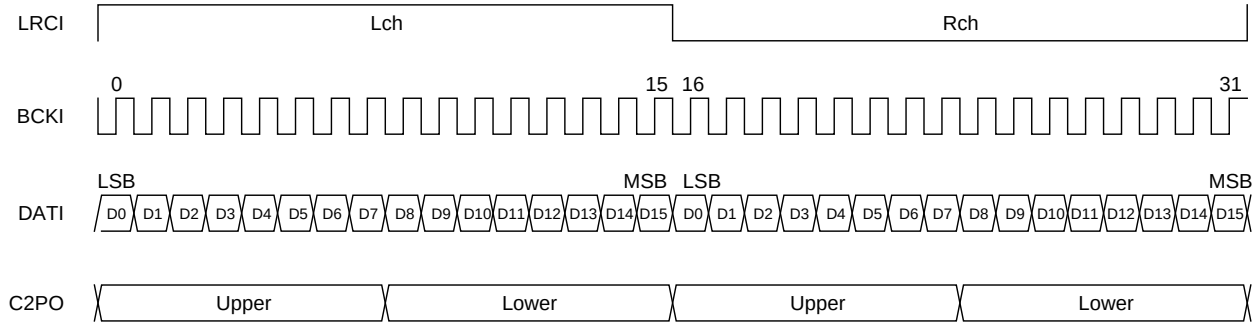
3) Write-only mode
   This mode transfers the 2340 bytes of header, subheader and user data within one sector to the user area of the external DRAM. When a form1 sector is input, error detection and correction processing is performed and then the data is transferred to the buffer memory. When a form2 sector is input, the data is transferred as is.

CD-DSP Input Signal Formats

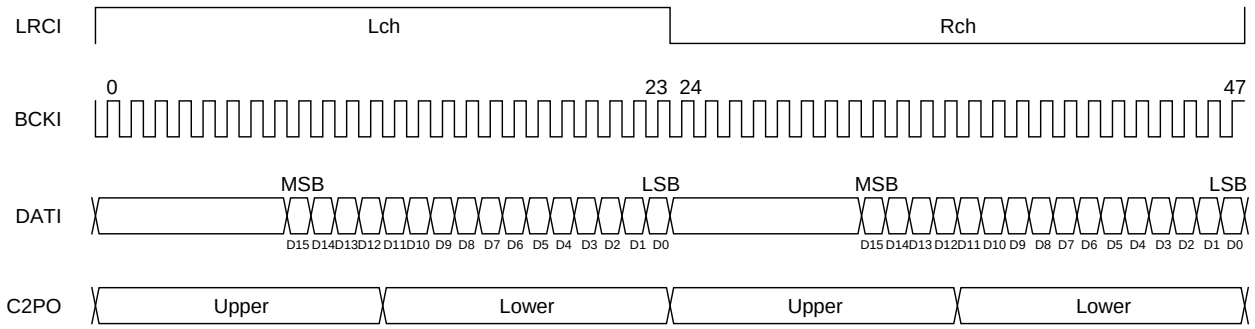
1) 32-bit slot, MSB first, BCKMOD1, 0 = 00, LSBFST = 0



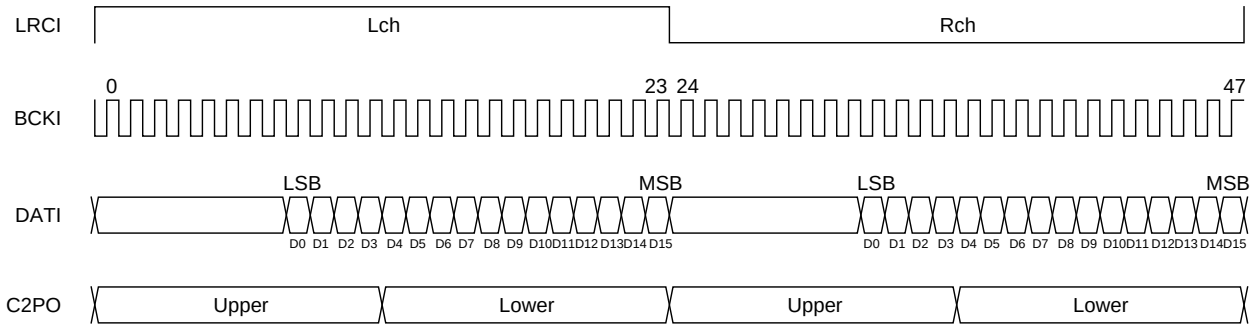
2) 32-bit slot, LSB first, BCKMOD1, 0 = 00, LSBFST = 1



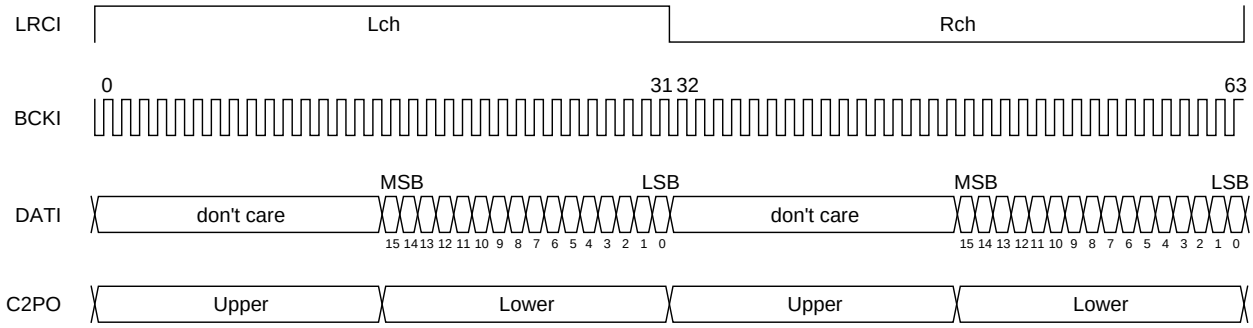
3) 48-bit slot, MSB first, BCKMOD1, 0 = 01, LSBFST = 0



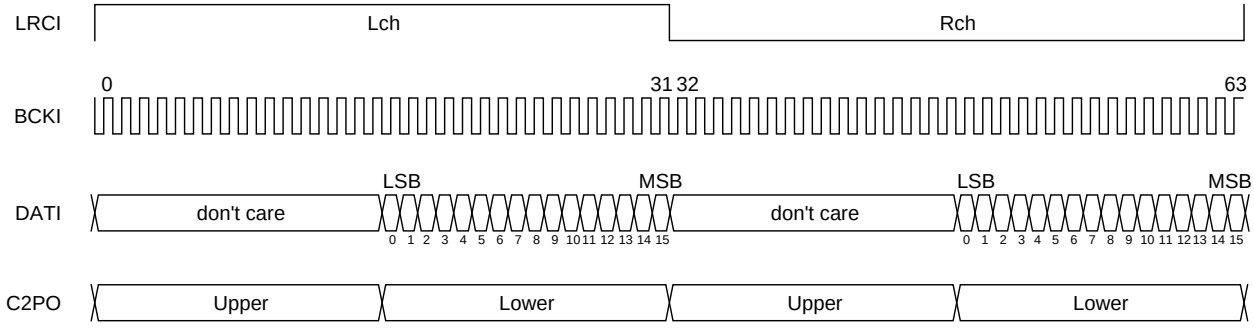
4) 48-bit slot, LSB first, BCKMOD1, 0 = 01, LSBFST = 1



5) 64-bit slot, MSB first, BCKMOD1, 0 = 10, LSBFST = 0



6) 64-bit slot, LSB first, BCKMOD1, 0 = 10, LSBFST = 1



4-4. System Decoder Function

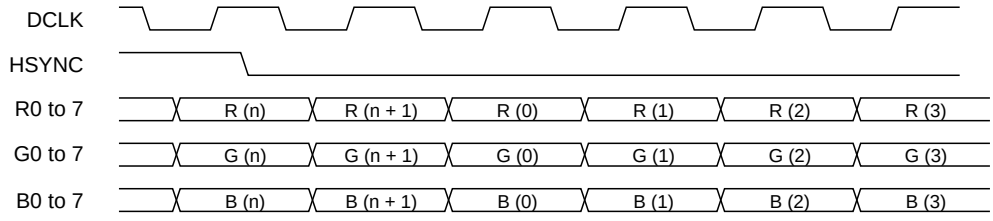
- The MPEG1 system layer (ISO/IEC 11172-1) is decoded, the audio and video bit streams are separated, and each bit stream is transferred to the respective bit stream buffer.
- The MPEG1 bit stream input can be selected from either the built-in CD-ROM decoder or the host interface.
- The system decoder has a 128-word (256-byte) FIFO for the bit stream input.
- Audio and video sync playback are controlled according to the time stamp within the bit stream.

4-5. Video Decoder Function

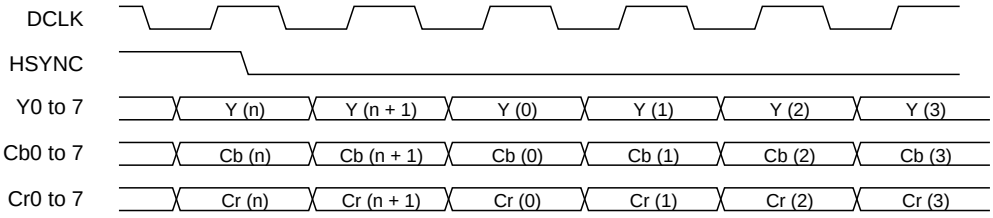
- The MPEG1 video layer (ISO/IEC 11172-2) is decoded. This function supports the range where constrained_parameter_flag = "1" and video CD high resolution still picture.
- Video CD high resolution still picture (NTSC, PAL) can be decoded with a single external 4-Mbit DRAM.
- Special decoding functions are as follows. Slow playback, fast forward and other modes can be realized by combining these functions.
  I-Play: Only I-Pictures are decoded.
  Still (Pause): Decoding is paused.
  1 Frame Play: Only one frame (picture) is decoded.
  IP-Play: Only I and P-Pictures are decoded.
  IPB-Play: Alternate frames of continuous B-Pictures and all I and P-Pictures are decoded.
- This function supports digest play.
- The various information in the bit stream is loaded to the on-memory register area within the external DRAM.

4-6. Video Post Processor and Sync Generator Functions

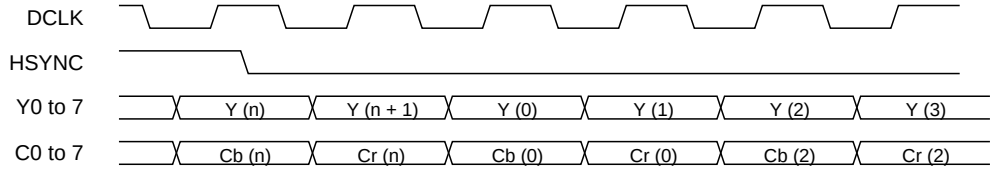
- The image data output format can be selected from 24-bit RGB, 24-bit YCbCr and 16-bit YCbCr. See the following page.
- Fade in and fade out are allowed.
- Image enlargement and reduction are allowed.
- The CXD1856Q/R contains an OSD color table and selector, and OSD display is achieved by inputting the OSD character signal.
- The video sync signal can be generated using the built-in sync generator. Image data can also be output in sync with an externally input video sync signal.



24-bit RGB output format



24-bit YCbCr output format



16-bit YCbCr output format

Note)

- The subscript (i) indicates the data for pixel i.
- The above timing charts show the timing when the pixel data output is synchronized with the fall of DCLK. The pixel data output can also be synchronized with the rise of DCLK.

4-7. Audio Decoder Function

- MPEG audio stream decoding is performed for MPEG1 standard (ISO/IEC 11172-3) layer 1 and layer 2.
- Monaural, dual, stereo and joint stereo decoding modes are supported.
- All MPEG1 standard sampling frequencies (32kHz, 44.1kHz, 48kHz) are supported.
- All MPEG1 standard bit rates are supported.
  Layer 1: 32Kbps (monaural/stereo) to 448Kbps (monaural/stereo)
  Layer 2: 32Kbps (monaural) to 384Kbps (stereo)
- The audio decoder's audio interface output port is equipped with a PCM audio output which outputs decoded audio data in bit serial format and a digital audio interface output (digital out). The audio interface is set by setting the internal registers.

1) LRCK and BCK generation
   The LR clock and bit clock can be generated by frequency dividing the clock input from external pins XTLI or FSXI. The generated clocks are output from the BCKO and LRCO pins, respectively. LRCO and BCKO can be output in the desired polarity. Also, the number of slots per sample supports the three types of 32, 48 and 64 bit clocks/LRCK.

2) PCM audio output format
   The PCM audio output format can be set to any of the following combinations to allow connection with a wide range of 1-bit D/A converters.
   16-bit word length, MSB first or LSB first, frontward truncation or rearward truncation
   18-bit word length, MSB first or LSB first, frontward truncation or rearward truncation
   20-bit word length, MSB first or LSB first, frontward truncation or rearward truncation
   24-bit word length, MSB first or LSB first, frontward truncation or rearward truncation

3) Digital out format
   The digital out output format supports the type2, form1 format for consumer use. The output word length can be selected from 16, 18, 20 or 24 bits.

4) Decoded channel assignment
   Channels 1 and 0 of the audio sample obtained by decoding the MPEG audio stream can be assigned to the L and R channel outputs in any combination.

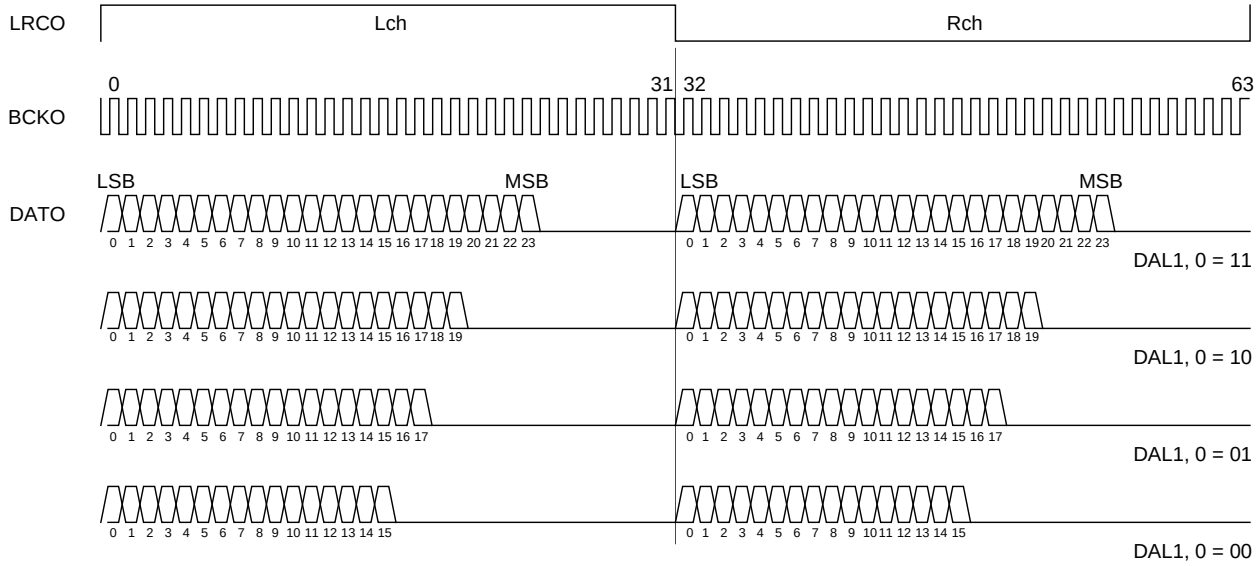
5) Audio mute
   The audio output contains a zero-cross mute circuit. Zero-cross detection is performed for 44 sample sections (approximately 0.1ms when fs = 44.1kHz), and if zero-cross is not detected, the output is forcibly muted.

6) Attenuator
   The audio output contains an attenuator circuit. Attenuation of –12dB can be obtained by setting the internal register.

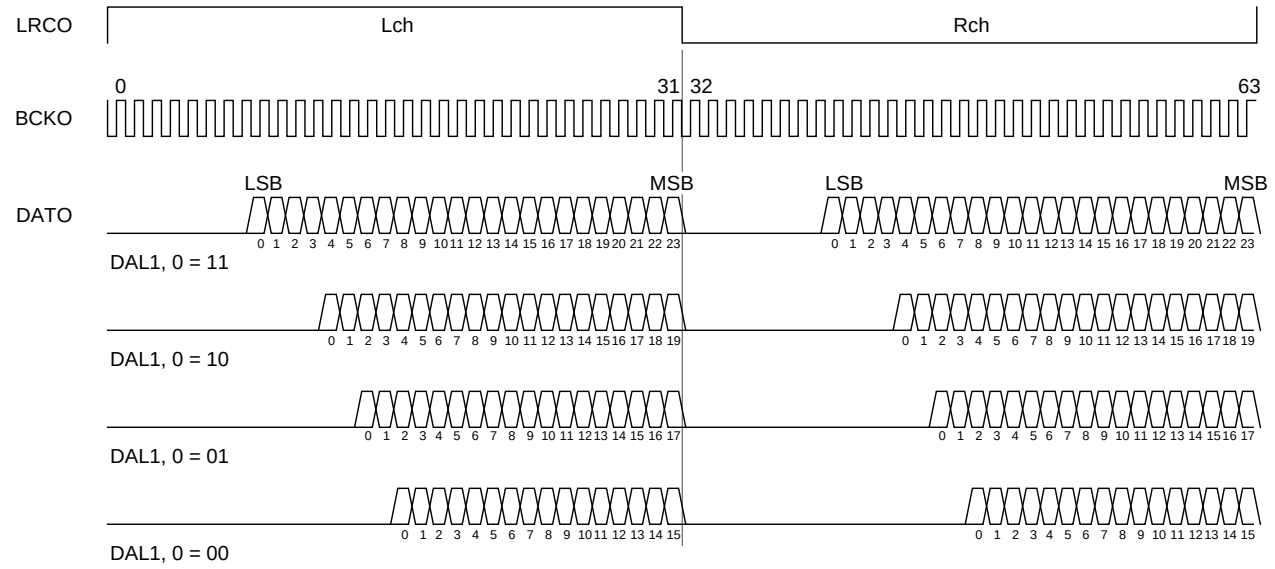
7) CD-DA output mode
   When playing back a CD-DA disc, the data input from the CD-DSP can be output directly from the PCM audio output (DATO) and the digital audio interface output port (DOUT). Output ports LRCO and BCKO can also select and output the clock inputs LRCI and BCKI from the CD-DSP.

PCM Audio Output Formats

1) 64-bit slot, frontward truncation, LSB first, OSLT1, 0 = 10, OTRUNK = 1, OLSBFST = 1



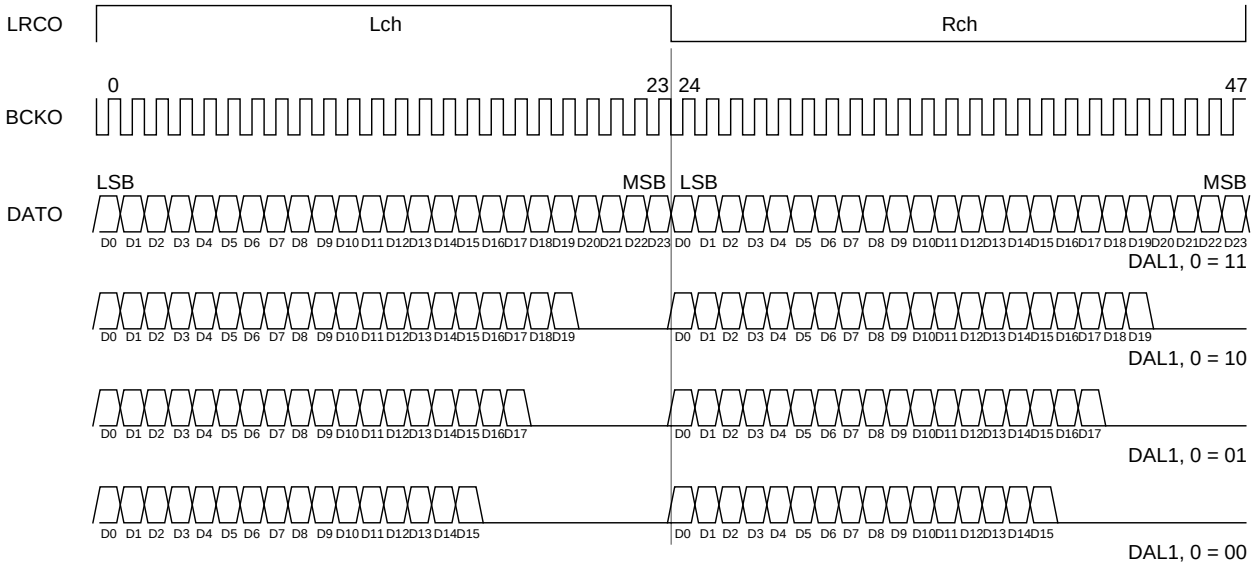
2) 64-bit slot, rearward truncation, LSB first, OSLT1, 0 = 10, OTRUNK = 0, OLSBFST = 1



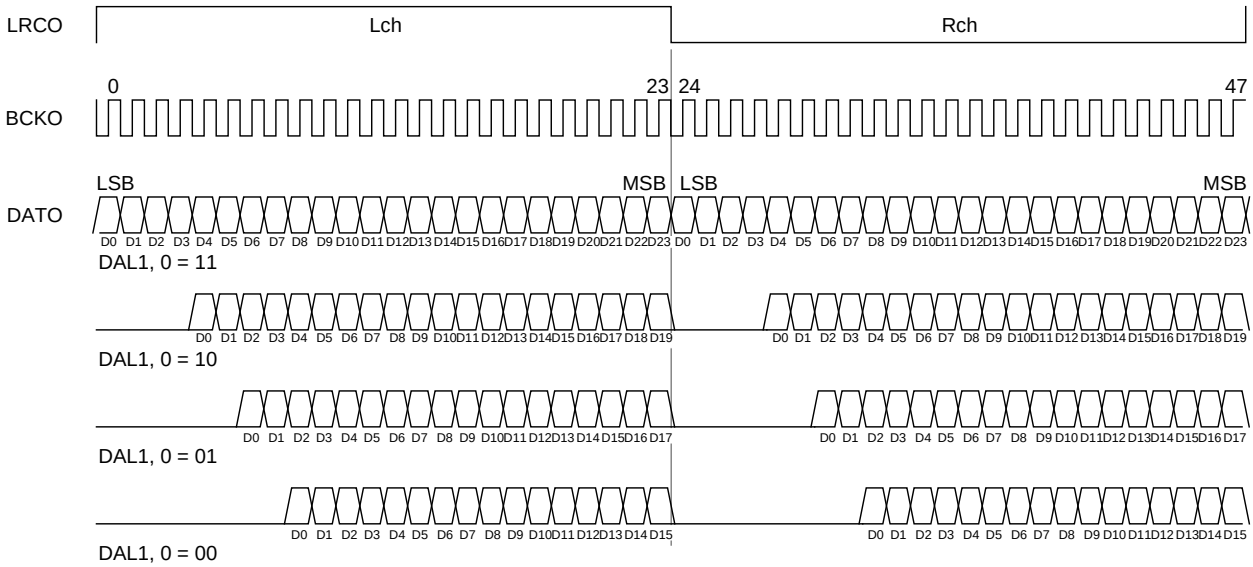
LSB/MSB first setting
OLSBF = 1: set to LSB first
OLSBF = 0: set to MSB first

Data word length setting
DAL1, 0 = 11: 24 bits
DAL1, 0 = 10: 20 bits
DAL1, 0 = 01: 18 bits
DAL1, 0 = 00: 16 bits

3) 48-bit slot, frontward truncation, LSB first, OSLT1, 0 = 01, OTRUNK = 1, OLSBFST = 1



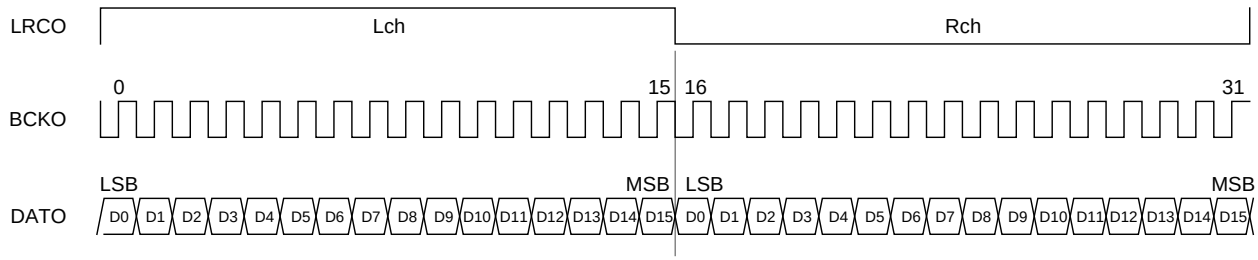
4) 48-bit slot, rearward truncation, LSB first, OSLT1, 0 = 01, OTRUNK = 0, OLSBFST = 1



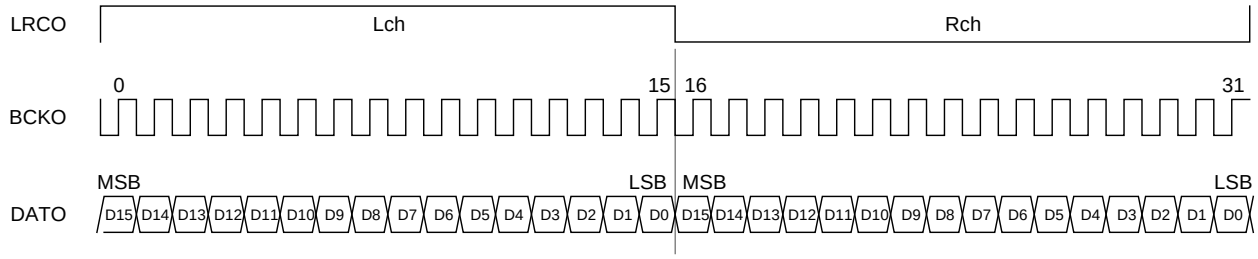
LSB/MSB first setting
OLSBF = 1: set to LSB first
OLSBF = 0: set to MSB first

Data word length setting
DAL1, 0 = 11: 24 bits
DAL1, 0 = 10: 20 bits
DAL1, 0 = 01: 18 bits
DAL1, 0 = 00: 16 bits

5) 32-bit slot, LSB first, OSLT1, 0 = 00, OLSBFST = 1



6) 32-bit slot, MSB first, OSLT1, 0 = 00, OLSBFST = 0

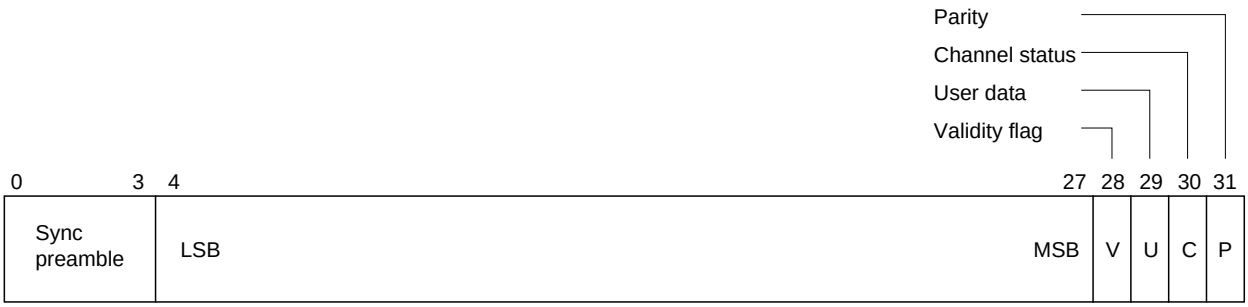


LSB/MSB first setting
OLSBF = 1: set to LSB first
OLSBF = 0: set to MSB first

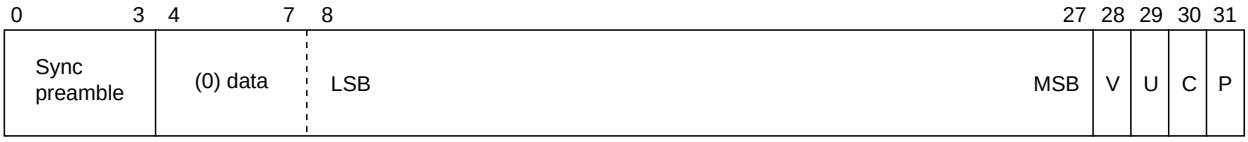
Data word length: 16 bits

Digital Audio Interface Output Formats

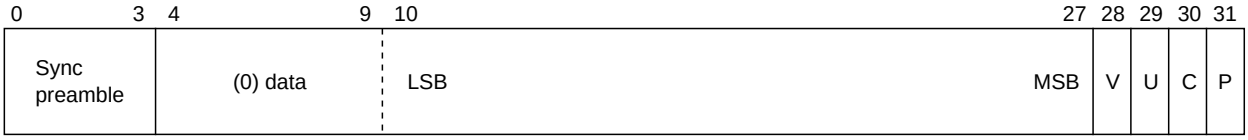
1) 24 bits/word



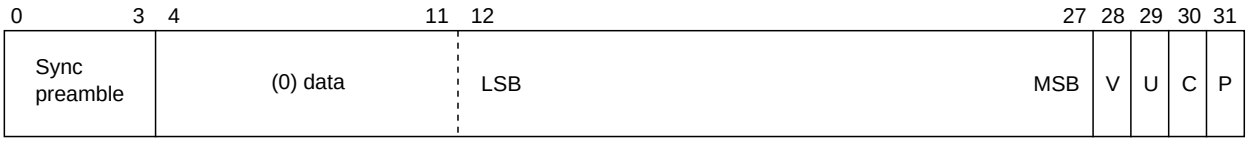
2) 20 bits/word



3) 18 bits/word



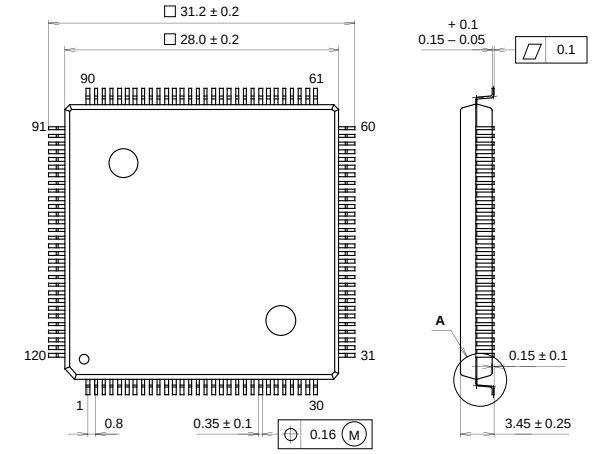
4) 16 bits/word

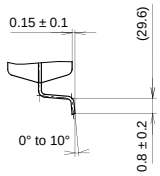


Data word length setting
DOL1, 0 = 11: 24 bits
DOL1, 0 = 10: 20 bits
DOL1, 0 = 01: 18 bits
DOL1, 0 = 00: 16 bits

Package Outline Unit: mm

120PIN QFP (PLASTIC)





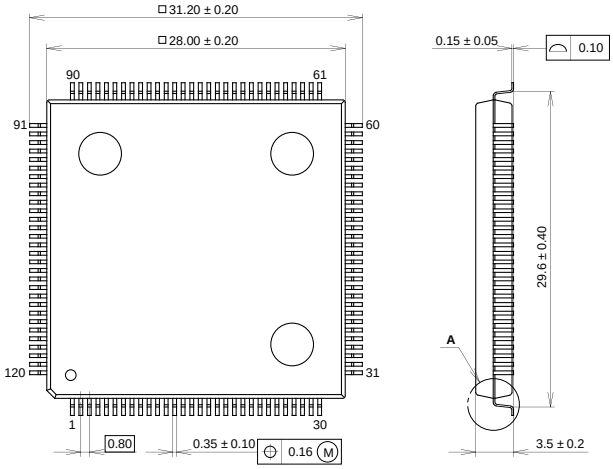
DETAIL **A**

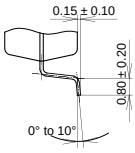
SONY CODE	QFP-120P-L01
EIAJ CODE	*QFP120-P-2828-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	4.9g

120PIN QFP (PLASTIC)





DETAIL **A**

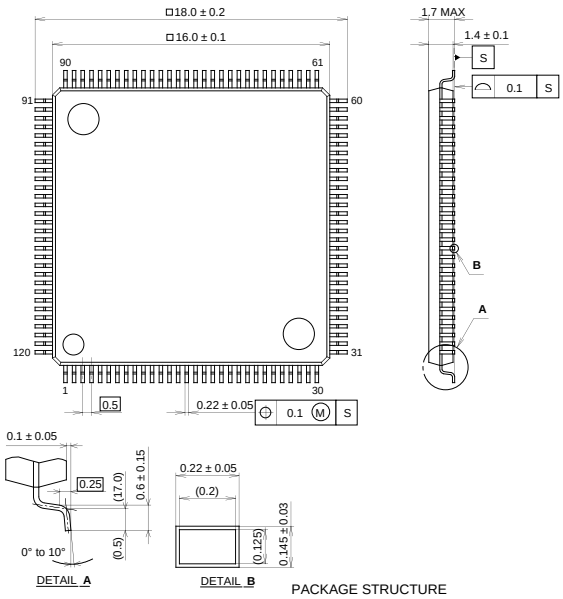
SONY CODE	QFP-120P-L022
EIAJ CODE	QFP120-P-2828
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	4.9 g

Package Outline Unit: mm

120PIN LQFP (PLASTIC)



SONY CODE	LQFP-120P-L01
EIAJ CODE	LQFP120-P-1616
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.8g