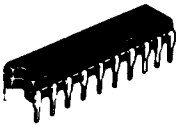
16384-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 35/45/55ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.)/5μW (typ.) (L-version),
  Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

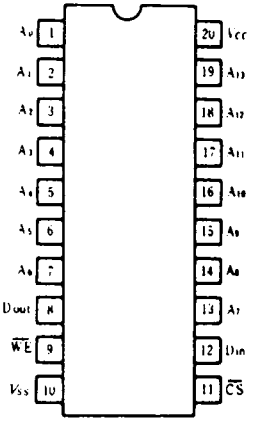


(DP-20N)

■ ORDERING INFORMATION

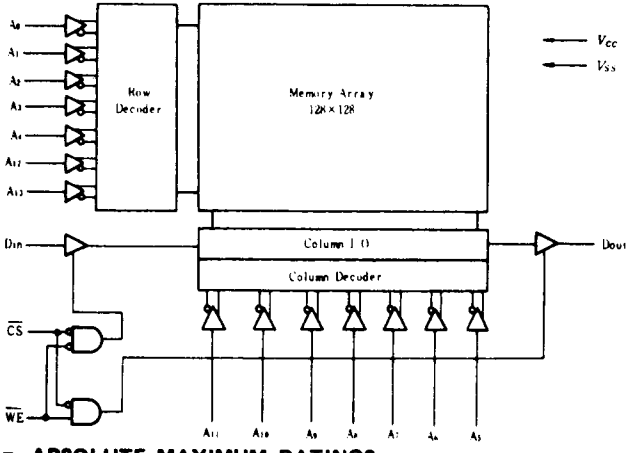
Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plactic DIP
HM6267P-45	45ns	
HM6267P-55	55ns	
HM6267LP-35	35ns	
HM6267LP-45	45ns	
HM6267LP-55	55ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*1	V_T	-0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

Notes) *1. With respect ot V_{SS}.
*2. -3.5V for pulse width ≦ 20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6267-35			HM6267-45/55			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT}=0mA, min. cycle	–	40	100	–	40	80	mA
Stand by Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, min cycle	–	10	20	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} − 0.2V, 0V ≦ V_{IN} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{IN}	–	0.02	2	–	0.02	2	mA
			–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = −4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limts are at V_{CC} = 5V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	—	7	pF	V_{OUT}=0V

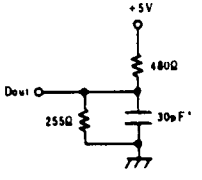
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

● AC TEST CONDITIONS

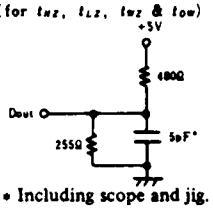
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{WZ}, t_{LZ}, t_{WZ} & t_{OW})

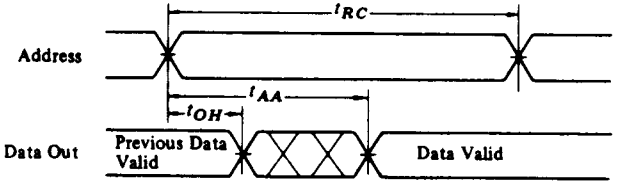


* Including scope and jig.

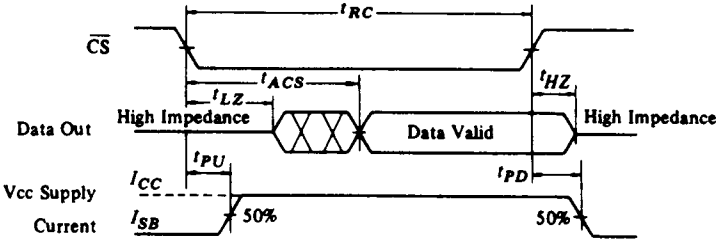
• Read Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	-	45	–	55	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	-	55	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2,3,7
Chip Deselectio to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2,3,7
Chip Selectio to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	–	30	ns	

• TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



• TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

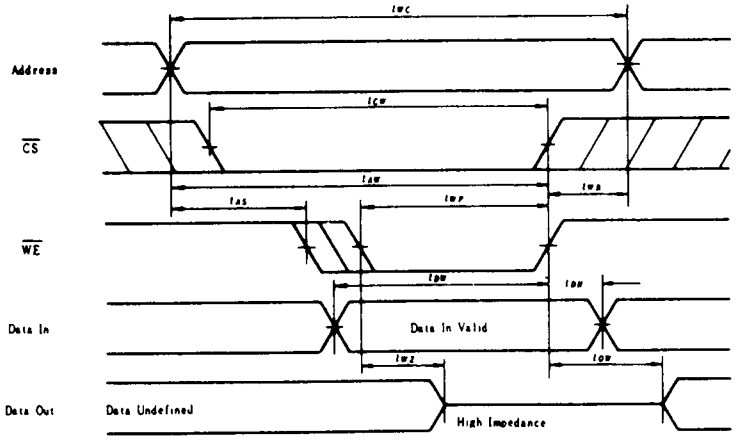


Notes) 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

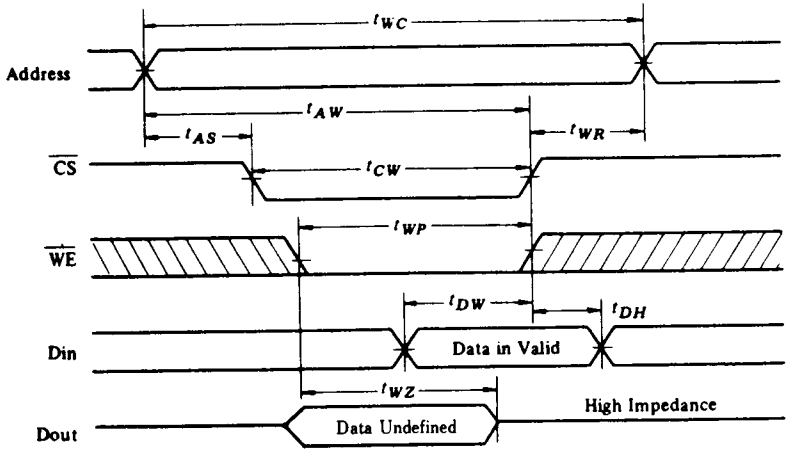
• Write Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	55	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	25	ns	3,4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3,4

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

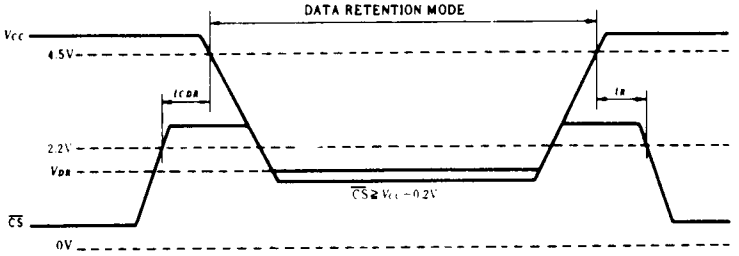
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics is guaranteed only for L-version.

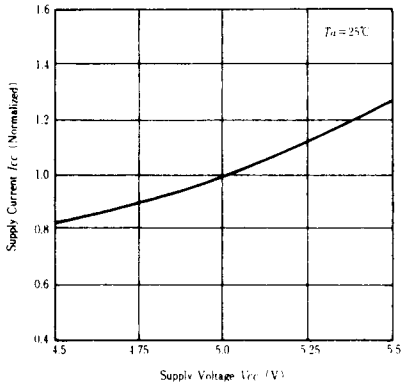
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	—	—	30*2 20*3	μA
Chip Deselect to Data Retention Time	t_{CDR}	see retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. $V_{CC} = 3.0V$ *3. $V_{CC} = 2.0V$

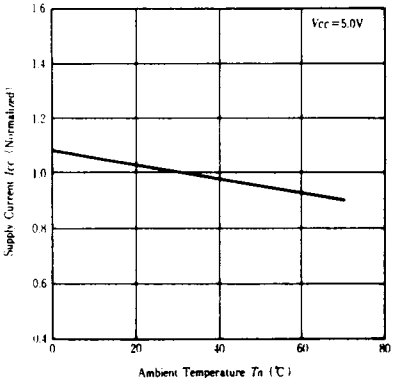
●LOW V_{CC} DATA RETENTION WAVEFORM



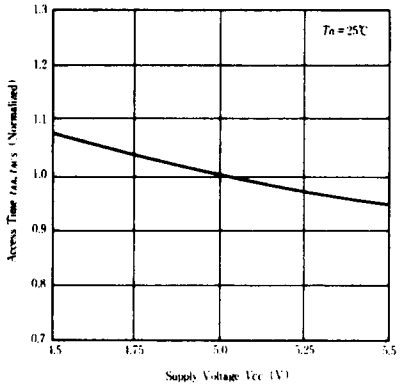
SUPPLY CURRENT VS. SUPPLY VOLTAGE



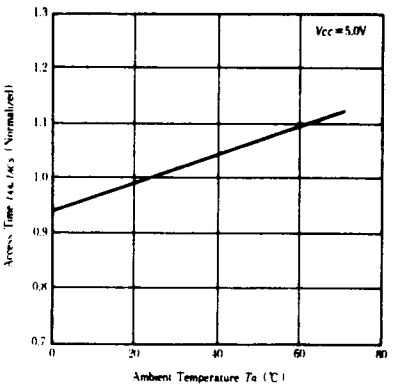
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



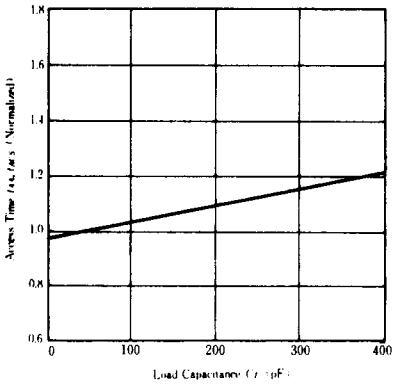
ACCESS TIME VS. SUPPLY VOLTAGE



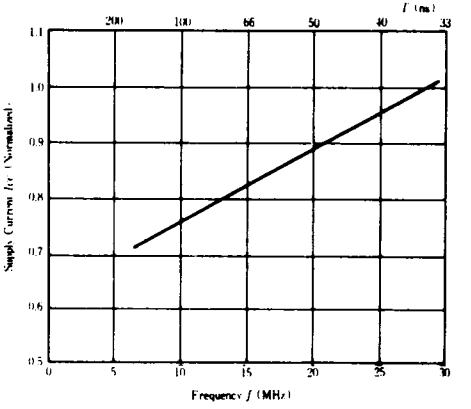
ACCESS TIME VS. AMBIENT TEMPERATURE



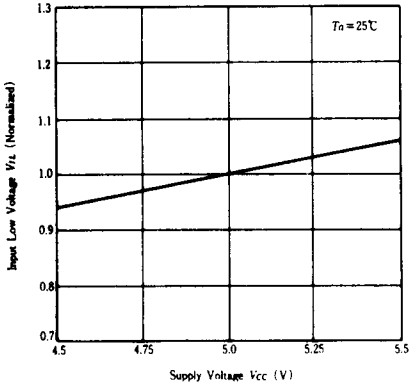
ACCESS TIME VS. LOAD CAPACITANCE



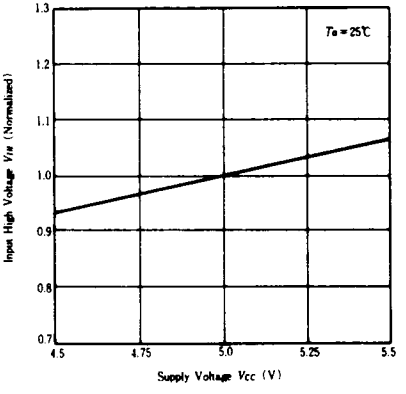
SUPPLY CURRENT VS. FREQUENCY



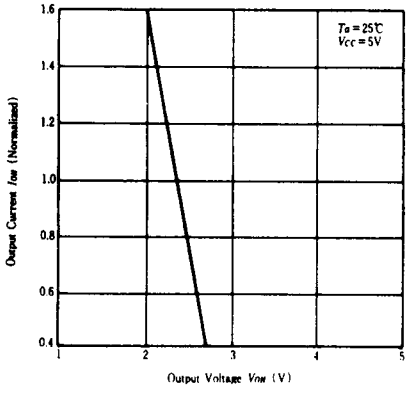
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



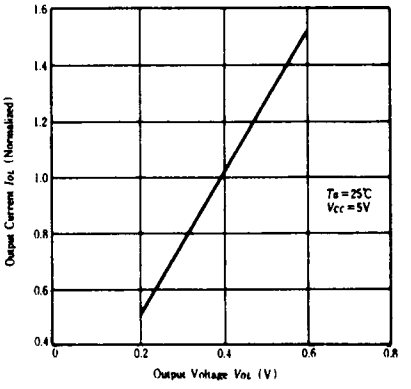
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



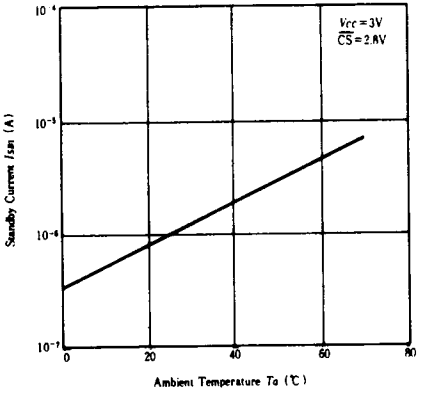
OUTPUT CURRENT VS. OUTPUT VOLTAGE



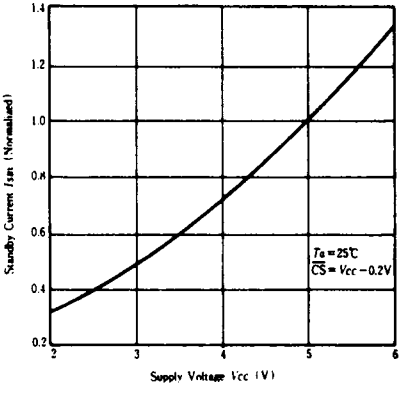
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



2