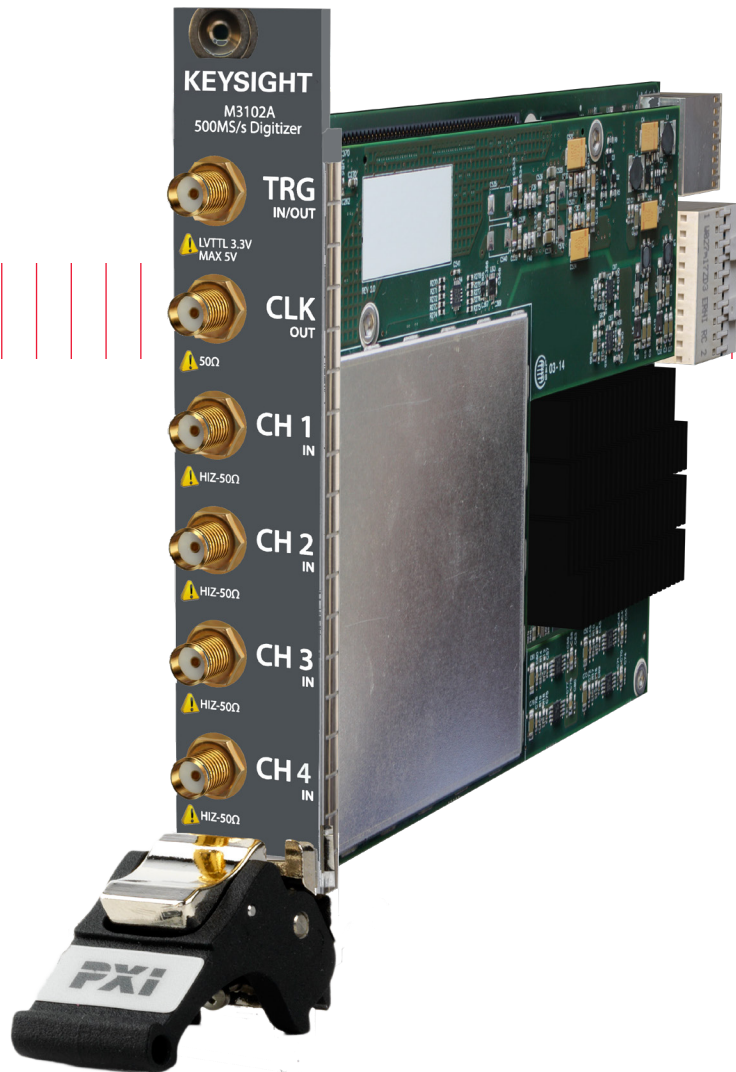


Keysight M3102A

PXIe Digitizers with Optional Real-Time Sequencing and FPGA Programming

500 MSa/s, 14 Bits, 2/4 Channels

Data Sheet



Improve Your Measurement Fidelity, Signal Integrity and Measurement Throughput

The M3102A are high-performance, high-bandwidth digitizers with an advanced data acquisition system (DAQ). Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI), and graphical FPGA programming technology.

Features

500 MSa/s simultaneous sampling, 14 bits, 2/4 channels, 200 MHz BW

Advanced data acquisition system (DAQ)

- Flexible triggering (HW trigger, HVI trigger, SW trigger)
- Programmable cycles and data bursts to avoid PC saturation

Optional HW programming for high-performance applications

- Real-time sequencing (HVI technology)
- FPGA programming
 - Xilinx Kintex-7, 325T or 410T FPGA

Up to 2 GB of onboard RAM (~ 1 Gsamples)

Mechanical/interface

- 1 slot 3U (PXIe)
- Up to 200 MB/s transfer BW with P2P capabilities
- Independent DMA channels for fast and efficient data transfer

Applications

General purpose digitizer

BB electronics designs and manufacturing in wireless devices

R&D/scientific research equipment

Aerospace & defense (A/D), angle of arrival (AoA)

Programming Technology and Software Tools

Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python, and more

Hardware programming (optional)

- Real-time sequencing ((Hard Virtual Instrumentation or HVI technology))
 - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
 - Ultra-fast, fully-parallelized hard real-time execution
 - Ultra-fast, time-deterministic decision-making
 - Off-the-shelf inter-module synchronization & data exchange
- FPGA programming
 - Graphical M3602A FPGA design environment (-FP1 option required on HW)
 - No FPGA know-how required
 - Include high-level to low-level design elements: off-the-shelf DSP blocks, MATLAB/Simulink designs, Xilinx CORE Generator IP cores, Xilinx VIVADO/ISE projects, VHDL or Verilog code
 - Ultra-fast, one-click compiling and on-the-fly programming

No programming

- Ready-to-use SD1 SPF (software front panels)

PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Outputs (AWGs)				Inputs (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	2/4	400				
M3201A	AWG	500	16	2/4	200				
M3102A	Digitizer					500	14	2/4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	200	100	14	4/8	DC-100

Functional Block Diagram

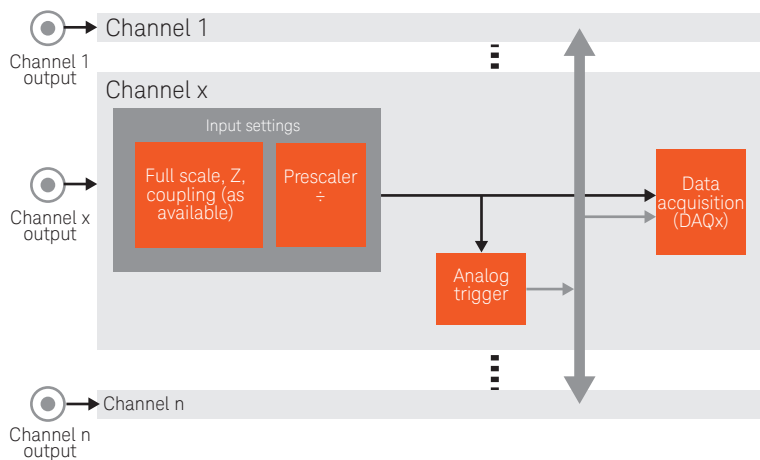


Figure 1. M3102A input functional block diagram, all channels have identical input structure

Ordering Information ¹

Product	Description
M3102A	PXIe digitizer: 500 MSa/s, 14 Bits
Options	Description
M3102A-CH2 / -CH4	Two channels ² / four channels
M3102A-CLV / -CLF	Variable sampling clock / Fixed sampling clock, low jitter ²
M3102A-M01 / -M12 / -M20	Memory 16 MB, 8 MSamples ² / 128 MB, 60 MSamples / 2 GB, 1 GSamples
HW programming options	Description
M3102A-HVI	Enabled HVI programming, requires an HVI design environment license (M3601A)
M3102A-FP1	Enabled FPGA programming, requires -K32 or -K41 option and an FPGA design environment license (M3602A)
M3102A-K32 / -K41	FPGA, Xilinx 7K325T / 7K410T, required for -FP1 option only (needs memory option -M20)
Related software	Description
M3601A	HVI design environment
M3602A	FPGA design environment

1. All options must be selected at time of purchase and are not upgradable
 2. These options represent the standard configuration

Technical Specifications and Characteristics

General characteristics

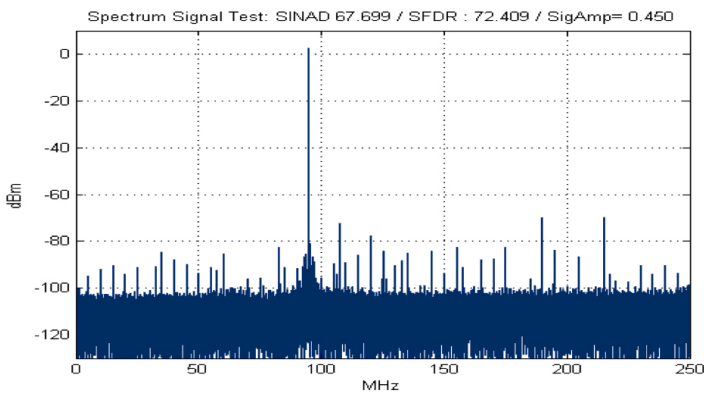
Parameter	M3102A-CH2			M3102A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
Inputs and outputs								
Channels	2			4			Out	
Reference clock ¹	1			1			Out	
Reference clock ²	1			1			In	
Triggers/markers ^{1,3}	1			1			In/out	Reconfigurable
Triggers/markers ^{2,3}	8			8			In/out	Reconfigurable
Input channels overview								
Sampling rate ⁴	500			500			MSa/s	
Voltage resolution	14			14			Bits	
Input frequency	0	200		0	200		MHz	
Real-time BW	200			200			MHz	
Time skew	< 50			< 50			ps	Between channels
Built-in functionalities								
Input conditioning blocks	2			4				1 per channel
Analog trigger processors	2			4				1 per channel
Data acquisition blocks	2			4				1 per channel
Onboard memory								
RAM memory	16	2048		16	2048		MBytes	

1. At front panel
2. At backplane
3. Markers available from firmware version v3.0 or later
4. 100 to 500 MSa/s (-CLV) option with variable sampling clock

I/O specifications

Analog input characteristics	
Number of channels	CH2 or CH4
Sampling rate	500 MSa/s option CLF (Table 4) variable rate option CLV (Table 4)
Configurable inputs: impedance	50Ω or 1MΩ (HiZ)
Configurable inputs: Coupling	AC or DC
Input voltage range (50Ω)	125 mVpp to 8Vpp (7 scales: 0.125, 0.25, 0.5, 1, 2, 4, 8 Vpp)
Input voltage range (HiZ)	200 mVpp to 16Vpp (7 scales: 0.2, 0.4, 0.8, 2, 4, 8, 16 Vpp)
Bandwidth limit filters	200 MHz
Effective number of bits (ENOB) ¹	10.6 bits @ 95 MHz (typical)
Noise floor ¹	-146 dBm/Hz
SINAD ¹	66 dB @ 95 MHz (typical)
Spurious free dynamic range (SFDR) + Total Harmonic Distorsion ¹	71 dBc @ 95 MHz (typical)

1. Measured at -1 DBFS input signal with 1 Vpp 50Ω



Parameter	M3102A			Units	Comments
	Min	Typ	Max		
Reference clock output					
Frequency		10 to 12.5 ²		MHz	Generated from the internal clock. User selectable
Voltage		800		mVpp	On a 50 Ω load
Power		2		dBm	On a 50 Ω load
Source impedance		50		Ω	AC coupled
External I/O trigger/marker					
V _{IH}	2		5	V	
V _{IL}	0		0.8	V	
V _{OH}	2.4		3.3	V	On a high Z load
V _{OL}	0		0.25	V	On a high Z load
Input impedance		10		K Ω	
Source impedance		TTL		-	
Speed		100		MHz	

2. CLF option is set to 10 MHz while with CLV option varies from 12.5 MHz to 10 MHz

Data acquisition blocks (DAQs) specifications

Parameter	M3102A-CH2			M3102A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
General specifications								
DAQs	2			4				1 per channel
Aggregated speed	1000			2000			MSa/s	For all onboard DAQs combined
Acquisition burst multiple	5			5			Samples	Burst length must be a multiple of this value
Acquisition RAM capacity	15		957M	15		957M	Samples	Maximum depends on onboard RAM
Acquisition RAM capacity effic.	93.5			93.5			%	Effic. = waveform size / waveform size in RAM
Trigger	Selec.			Selec.				Hardware trigger (analog channels, input trigger, backplane triggers), software trigger
DAQ specifications								
Speed	500			500			MSa/s	Per DAQ
Resolution	14			14			Bits	

Clock system specifications

Parameter	M3102A		Units	Comments
	Min	Max		
General specifications				
Clock frequency (-CLF)	500	500	MHz	Fixed clock
Clock frequency (-CLV)	100	500	MHz	Variable clock

System Specifications

Environmental specifications (PXI Express)

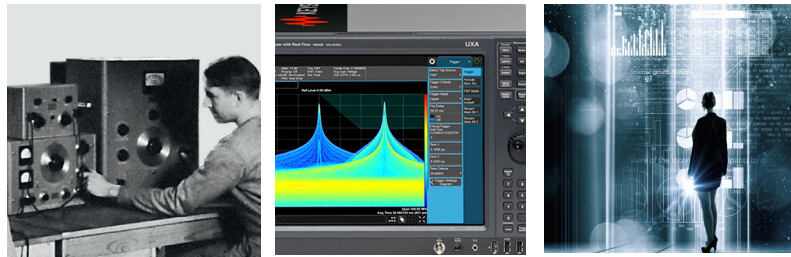
Parameter	M3102A-CH2			M3102A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
System bus								
Slots	1			1			Slot	PXI Express (CompactPCI Express compatible)
PCI Express type	Gen 1		Gen 2	Gen 1		Gen 2	–	Automatic gen negotiation, chassis dependent
PCI Express link	1		4	1		4	Lanes	Automatic lane negotiation, chassis dependent
Power dissipation								
3.3V PXIe power supply	1.5			1.5			A	~ 5 W
12V PXIe power supply	2			2			A	~ 24 W

Environmental ¹		
Temperature range	Operating Non-operating	0 to +55°C (10,000 feet) -40 to +70°C (up to 15,000 feet)
Max operative altitude		4000 m (10,000 feet)
Operating Humidity range (%RH)		10 to 95% at 40°C
Non-operating Humidity range (%RH): 5 to 95		5 to 95%
Calibration interval		1 year
EMC		Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada. This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

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 Published in USA, February 20, 2018
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