

August 1997

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See HI3050
or contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

Triple 10-Bit, 50 MSPS, RGB, 3-Channel D/A Converter

Features

- ResolutionTriple 10-Bit
- Maximum Conversion Speed 50MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error ± 0.5 LSB
- Low Power Consumption300mW (Max)
- Single Power Supply+5V
- Low Glitch
- Direct Replacement for Sony CXD2307

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

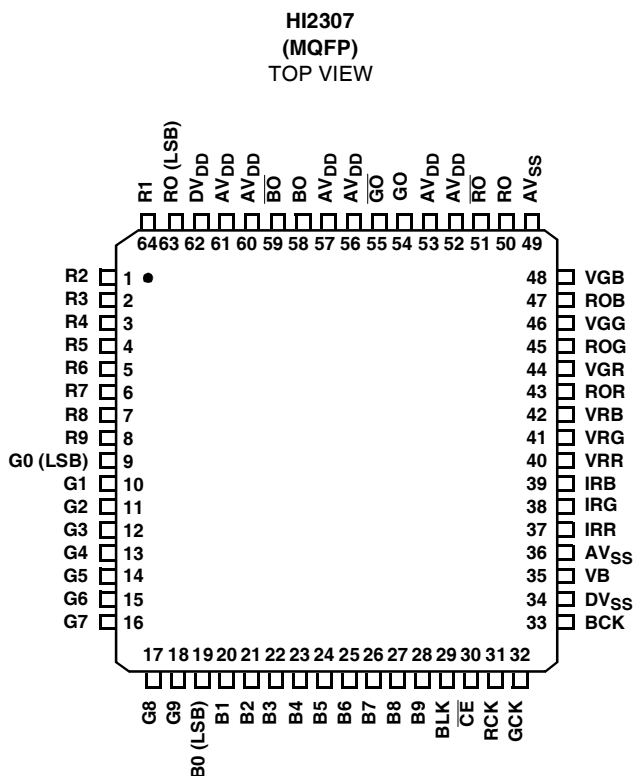
Description

The HI2307 is a triple 10-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 10-bit, pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. Each channel clock input can be controlled individually, or connected together as one. The HI2307 also has BLANK video control signal.

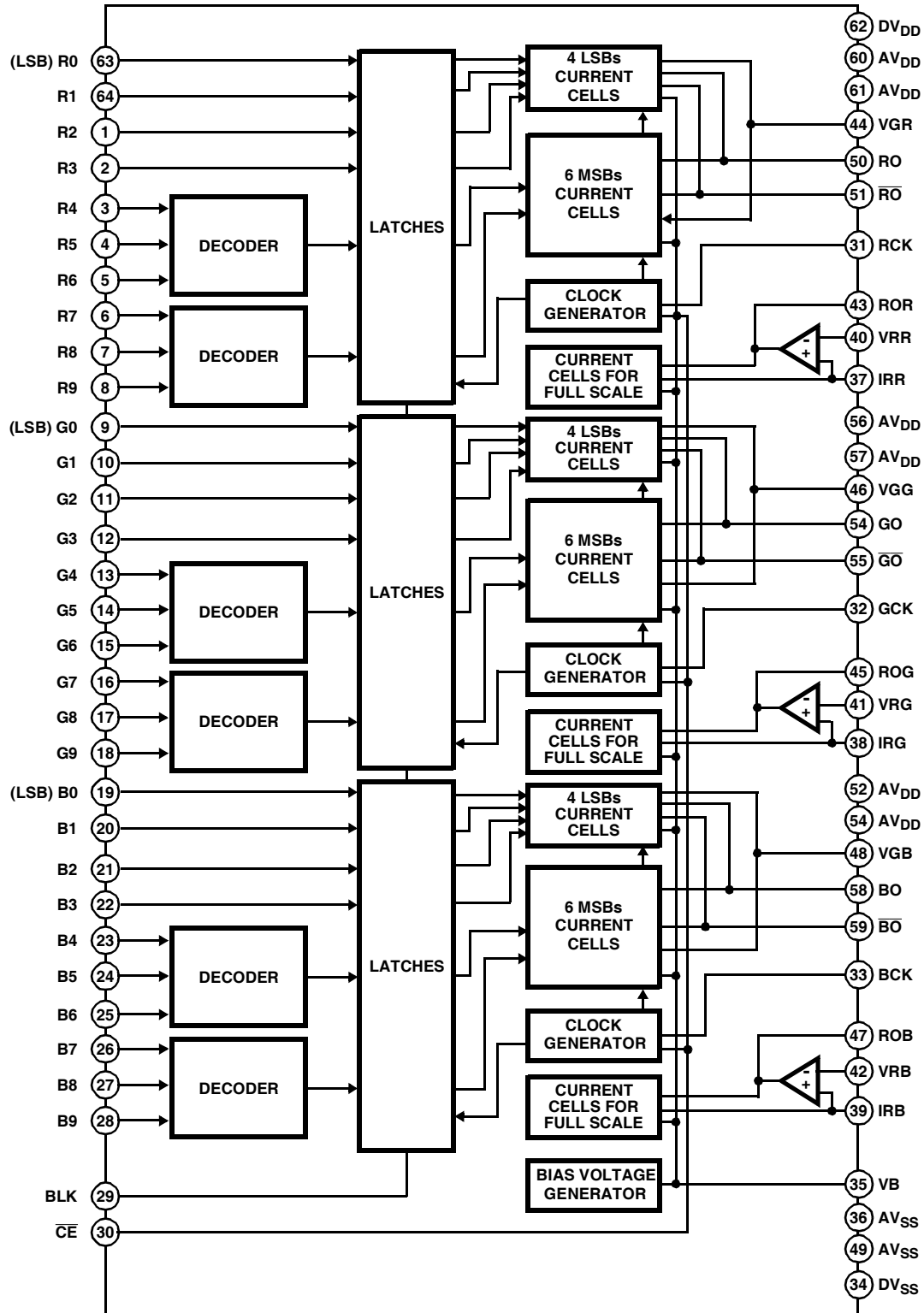
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2307JCQ	-20 to 75	64 Ld MQFP	Q64.10x10-S

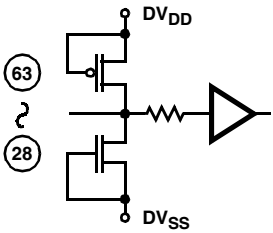
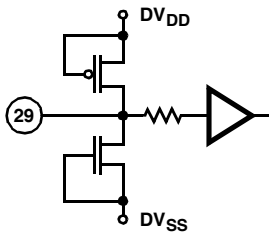
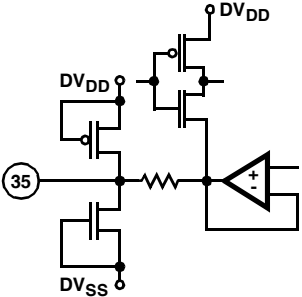
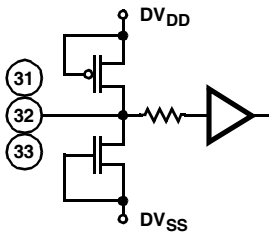
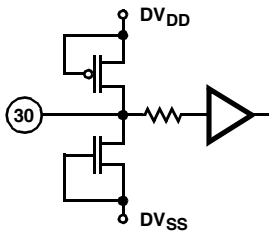
Pinout



Functional Block Diagram



Pin Descriptions

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
63 to 8	R0 to R9		Digital Input.
9 to 18	G0 to G9		
19 to 28	B0 to B9		
29	BLK		Blanking pin. No signal for High (0V output). Output generated for Low.
35	VB		Connect to DVSS with a capacitor of approximately 0.1μF.
31	RCK		Clock pins. All input pins are TTL compatible.
32	GCK		
33	BCK		
34	DVSS		Digital GND.
36, 49	AVSS		Analog GND.
30	$\overline{CE}$		Chip Enable pin. No signal for High (0V output) to minimize power consumption.
52, 53, 56, 57, 60, 61	AVDD		Analog VDD.

Pin Descriptions (Continued)

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
43 45 47	ROR ROG ROB		Connect to VGR, VGG, and VGB with the control method of output amplitude. See Application Circuit.
44 46 48	VGR VGG VGB		Connect a capacitor of approximately 0.1μF.
37 38 39	IRR IRG IRB		Connect to AVSS with a resistance of 3.3kΩ.
40 41 42	VRR VRG VRB		Set output fullscale value (2.0V).
50 54 58 51 55 59	RO GO BO $\overline{RO}$ $\overline{GO}$ $\overline{BO}$		Current output pins. Output can be retrieved by connecting a resistance of 200Ω to AVSS.
			Reverse current output pins. Normally connect to AVSS.
62	DVDD		Digital VDD.

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Supply Voltage, V_{DD} 7.0V
 Input Voltage, V_{IN} V_{DD} to V_{SS}
 Output Current (for Each Channel), I_{OUT} 0 to 15mA

Operating Conditions

Supply Voltage
 AV_{DD}, AV_{SS} 4.75V to 5.25V
 DV_{DD}, DV_{SS} 4.75V to 5.25V
 Reference Input Voltage, V_{REF} 0.5V to 2.0V
 Clock Pulse Width
 t_{PW1} 10ns (Min)
 t_{PW0} 10ns (Min)
 Temperature Range, T_{OPR} -20°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 7) θ_{JA} ($^\circ\text{C}/\text{W}$)
 MQFP Package 93
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

Electrical Specifications $T_A = 25^\circ\text{C}$, $f_{CLK} = 50\text{MHz}$, $V_{DD} = 5\text{V}$, $R_{OUT} = 200\Omega$, $V_{REF} = 2.0\text{V}$

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	10	-	Bit
Maximum Conversion Speed		f_{MAX}		50	-	-	MHz
Linearity Error		E_L		-2.0	-	2.0	LSB
Differential Linearity Error		E_D		-0.5	-	0.5	LSB
Output Full Scale Voltage		V_{FS}		1.8	1.9	2.0	V
Output Full Scale Ratio (Note 8)		F_{SR}	For the Equal Gain	0	1.5	3	%
Output Full Scale Current		I_{FS}		-	9.5	10	mA
Output Offset Voltage		V_{OS}		-	-	1	mV
Supply Current		I_{DD}		-	55	60	mA
Digital Input Current	High Level	I_{IH}		-	-	5	μA
	Low Level	I_{IL}		-5	-	-	μA
Precision Guaranteed Output Voltage Range		V_{OC}		1.8	1.9	2.0	V
Setup Time		t_S		-	5	7	ns
Hold Time		t_H		-	1	3	ns
Propagation Delay Time		t_{PD}		-	10	-	ns
Glitch Energy		GE		-	100	-	pV-s
Cross Talk		CT	For 10MHz Sinewave Output	-	54	-	dB

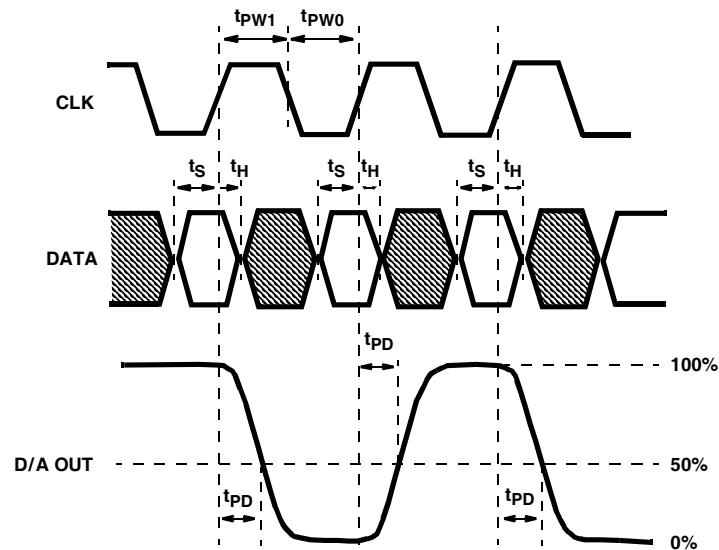
NOTE:

2. Output Full Scale Ratio = $\left| \frac{\text{Full scale voltage of channel}}{\text{Average of the full scale voltage of the channels}} (-1) \right| \times 100(\%)$.

I/O Correspondence Table (Output Full Scale Voltage: 2.0V)

INPUT CODE										OUTPUT VOLTAGE
MSB									LSB	
1	1	1	1	1	1	1	1	1	1	2.0V
⋮										
1	0	0	0	0	0	0	0	0	0	1.0V
⋮										
0	0	0	0	0	0	0	0	0	0	0V

Timing Diagram



Test Circuits

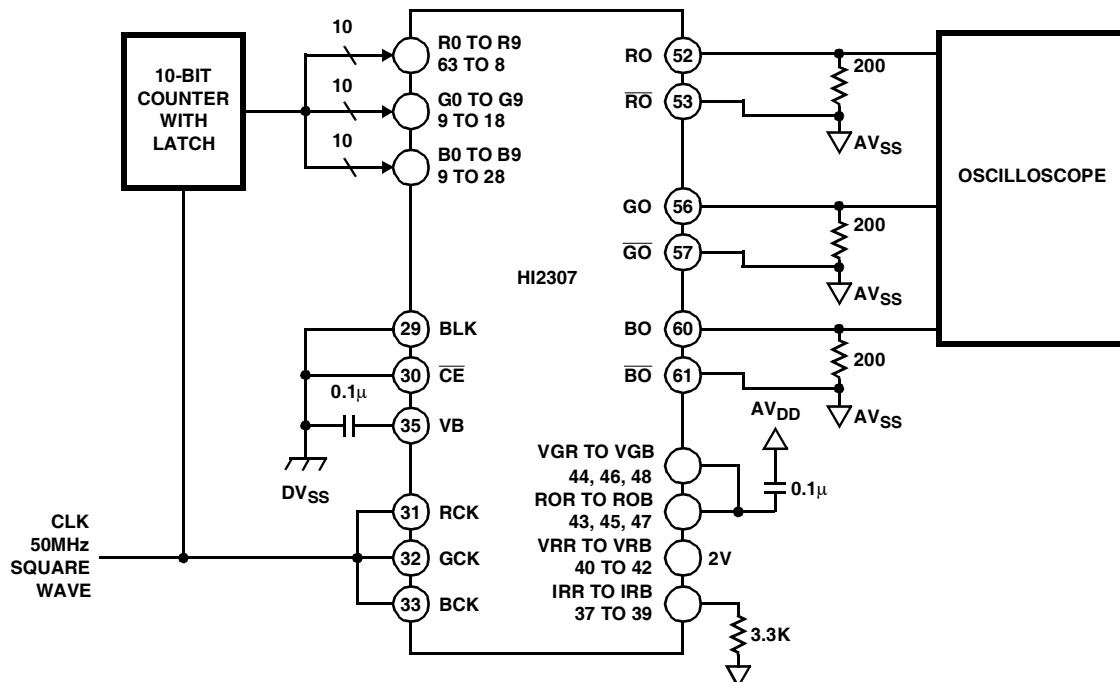


FIGURE 1. MAXIMUM CONVERSION RATE

Test Circuits (Continued)



Test Circuits (Continued)

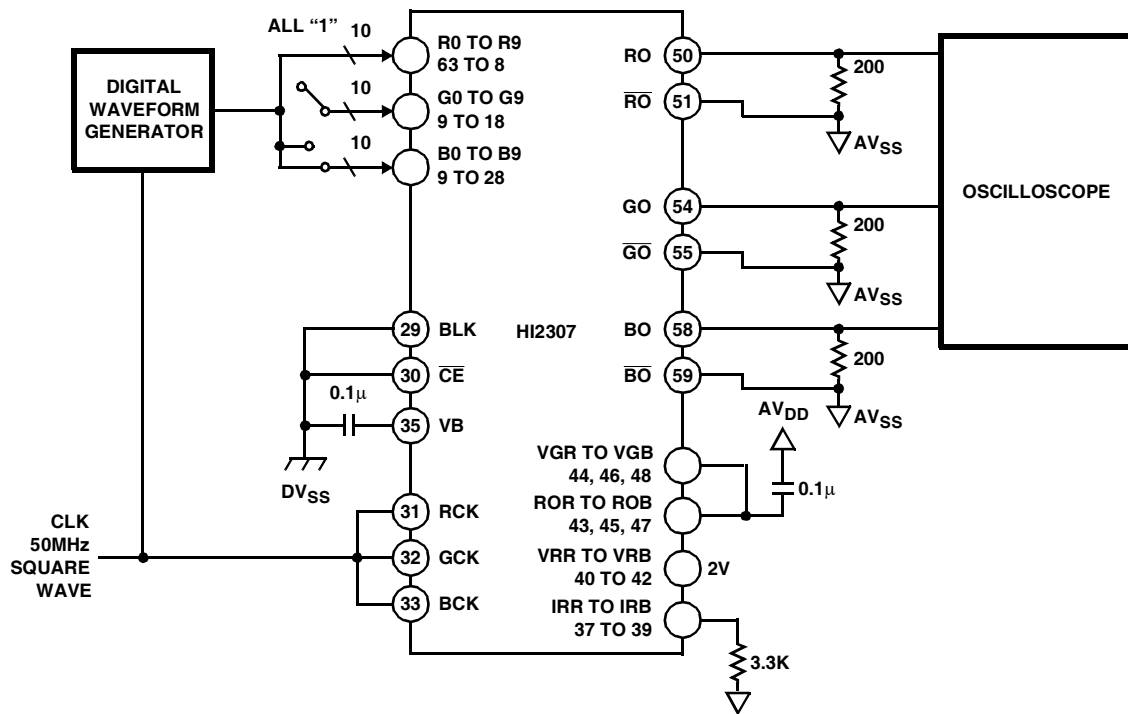


FIGURE 3. CROSS TALK TEST CIRCUIT

Typical Performance Curves

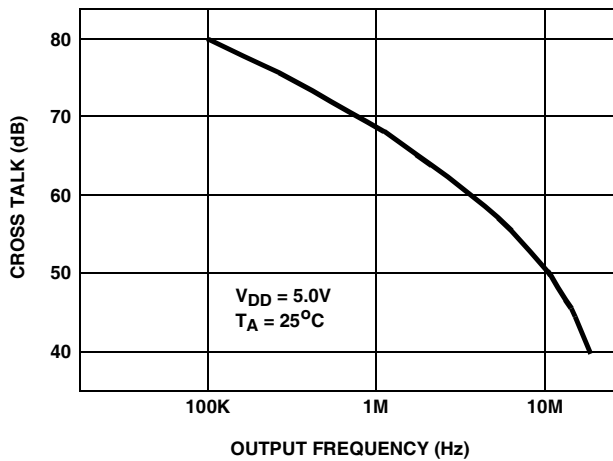


FIGURE 4. OUTPUT FREQUENCY vs CROSS TALK

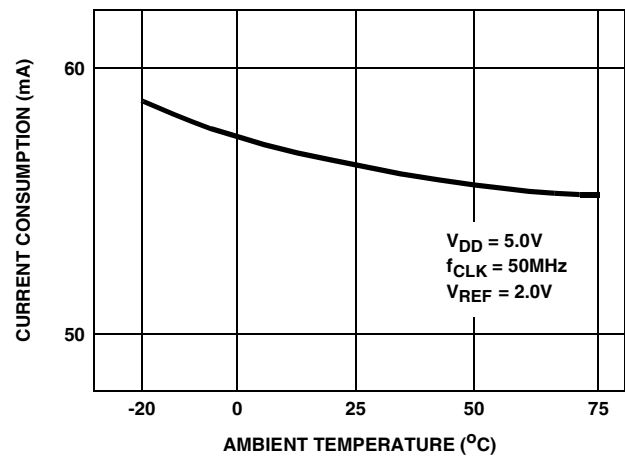


FIGURE 5. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

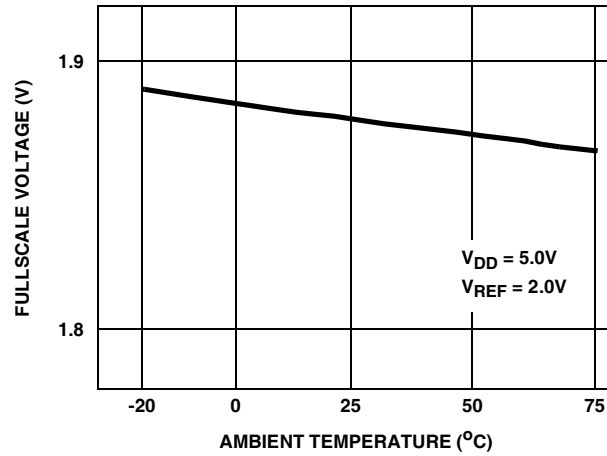


FIGURE 6. FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

Application Circuits

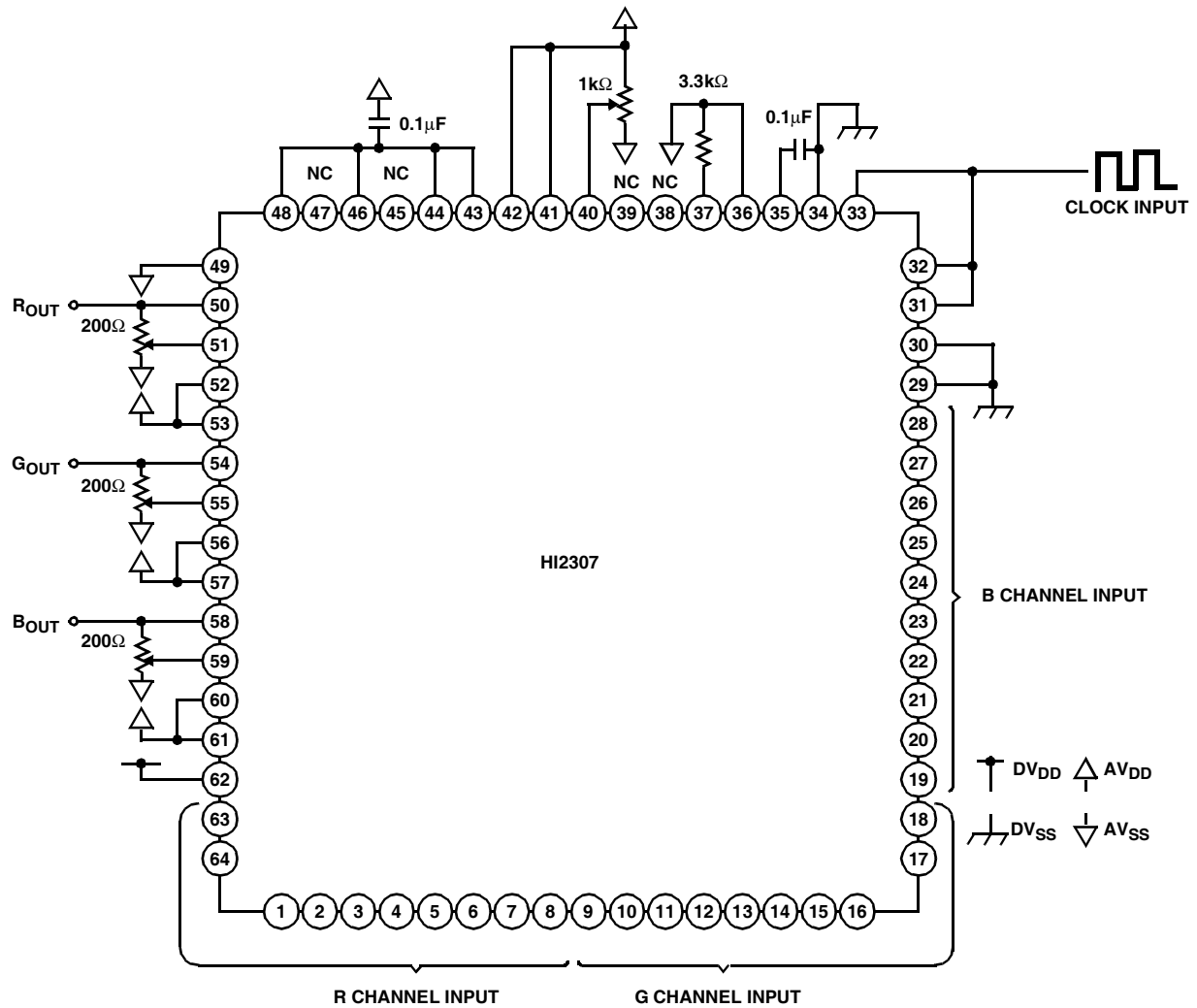


FIGURE 7. GAIN EQUAL

Application Circuits (Continued)

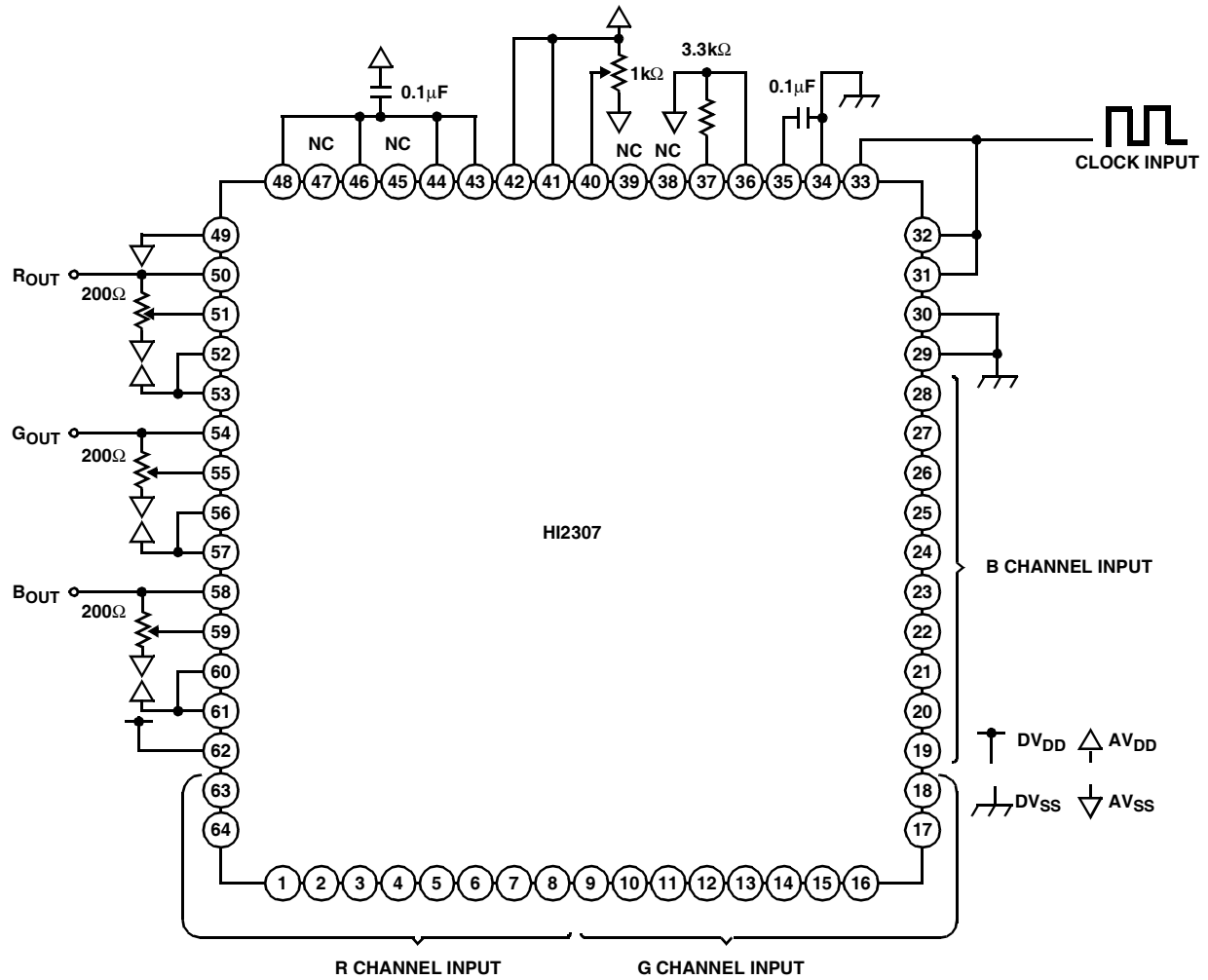


FIGURE 8. GAIN INDEPENDENTLY