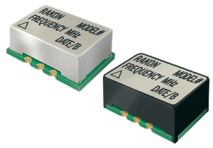
RV1490P VCXO

`Tiger' SMD Voltage Control Crystal Oscillator Series



High Performance PLL Voltage Control Crystal Oscillator.

Product description

This PLL VCXO offers ultra low RMS phase jitter, high linearity pull range and high frequency stability in an industry standard 14 mm x 9 mm SMD package.

Applications

- Basestation
- Communications
- DSL/ADSL
- Ethernet
- Other
- SONET/SDH
- WiMAX/WLAN

Features

- Low Jitter
- LVPECL output

Specifications

1.0 SPECIFICATION REFERENCES

Line	Parameter	Description
1.1	Model Series	RV1490P VCXO
1.2	RoHS Compliant	Yes
1.3	Custom P#	
1.4	Package Type	P6, P4, M6 or M4 - select only one

2.0 FREQUENCY CHARACTERISTIC

Line	Parameter	Test Condition	Value	Unit
2.1	Frequency Range		10 to 800	MHz
2.2	Operating Temperature Range	(Note 1)	-40 to 85	°C
2.3	Frequency Stability	Including temperature range, Supply variation, Load variation and 15 years Aging	±15 to 50	ppm

3.0 POWER SUPPLY

Line	Parameter	Test Condition	Value	Unit
3.1	Supply Voltage	With a tolerance of ±10%	2.97 to 3.63	V
3.2	Supply Current	(Note 2)	10 to 120	mA

4.0 CONTROL VOLTAGE (VCO)

Line	Parameter	Test Condition	Value	Unit
4.1	Absolute Pulling Range		±	ppm
4.2	Pulling Range	Frequency shift from minimum to maximum control voltage (Note 3)	±40 to 250	ppm
4.3	Control Voltage	Vcc ÷ 2	0 to 3.3	V
4.4	Linearity		10 max	%
4.5	Slope	Positive only	±10 to 100	ppm/V
4.6	Modulation BW		0.3 to 100	kHz

4.7	Input Impedance	10 to 2000	kΩ

5.0 OUTPUT CHARACTERISTICS - LVPECL ONLY

Line	Parameter	Test Condition	Value	Unit
5.1	Output	LVPECL		
5.2	Duty Cycle	@ VCC -1.3V	40 to 60	%
5.3	Output Load	With VCC -2V @ 50Ω		
5.4	Rise time/fall time	80%/20% (Note 4)	0.5 to 3	ns
5.5	Logic `1' on Pad 2	Tristate GND (Note 5)		
5.6	Logic `0' on Pad 2	Enable (VCC or open) (Note 5)		
5.7	RMS Phase Jitter	Integrated 12 kHz to 20 MHz. Typical @ 155.52 MHz (Note 6)	0.5 max	ps
5.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 6)	5 max	ps
5.9	Sub-harmonics		-30 max	dBc

6.0 OUTPUT CHARACTERISTICS - LVCMOS ONLY

Line	Parameter	Test Condition	Value	Unit
6.1	Output	LVCMOS		
6.2	Duty Cycle	@ 50% VCC	40 to 60	%
6.3	Output Load		15 to 50	pF
6.4	Rise time / fall time	90%/10% (Note 4)	0.5 to 3	ns
6.5	Logic `0' on Pad 2	Tristate GND (Note 5)		
6.6	Logic `1' on Pad 2	Enable (VCC or open) (Note 5)		
6.7	RMS Phase Jitter	Integrated 12 kHz to 20 MHz. Typical @ 155.52 MHz (Note 6)	0.5 max	ps
6.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 6)	5 max	ps
6.9	Sub-harmonics		-30 max	dBc

7.0 OUTPUT CHARACTERISTICS - LVDS ONLY

Line	Parameter	Test Condition	Value	Unit
7.1	Output	LVDS		
7.2	Duty Cycle	Measured at 1.25 V	40 to 60	%
7.3	Output Load	RL - 100 Ω / CL = 10 pF		
7.4	Rise time / fall time	RL - 100 Ω / CL = 10 pF (Note 4)	0.5 to 3	ns
7.5	Logic `0' on Pad 2	Tristate GND (Note 5)		
7.6	Logic `1' on Pad 2	Enable (VCC or open) (Note 5)		
7.7	RMS Phase Jitter	Integrated 12 kHz to 20 MHz. Typical @ 155.52 MHz (Note 6)	0.5 max	ps
7.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 6)	5 max	ps
7.9	Sub-harmonics		-30 max	dBc

8.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
8.1	SSB Phase Noise power density @ 10 Hz offset	Value for a 77.76 MHz VCXO @ 25°C	-56	dBc/Hz
8.2	SSB Phase Noise power density @ 100 Hz offset	Value for a 77.76 MHz VCXO @ 25°C	-86	dBc/Hz
8.3	SSB Phase Noise power density @ 1 kHz offset	Value for a 77.76 MHz VCXO @ 25°C	-114	dBc/Hz
8.4	SSB Phase Noise power density @ 10 kHz offset	Value for a 77.76 MHz VCXO @ 25°C	-126	dBc/Hz
8.5	SSB Phase Noise power density @ 100 kHz offset	Value for a 77.76 MHz VCXO @ 25°C	-122	dBc/Hz

9.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
9.1	SSB Phase Noise power density @ 10 Hz offset	Value for a 155.52 MHz VCXO @ 25°C	-52	dBc/Hz
9.2	SSB Phase Noise power density @ 100 Hz offset	Value for a 155.52 MHz VCXO @ 25°C	-82	dBc/Hz
9.3	SSB Phase Noise power density @ 1 kHz offset	Value for a 155.52 MHz VCXO @ 25°C	-110	dBc/Hz
9.4	SSB Phase Noise power density @ 10 kHz offset	Value for a 155.52 MHz VCXO @ 25°C	-122	dBc/Hz
9.5	SSB Phase Noise power density @ 100 kHz offset	Value for a 155.52 MHz VCXO @ 25°C	-118	dBc/Hz

10.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
10.1	SSB Phase Noise power density @ 10 Hz offset	Value for a 622.08 MHz VCXO @ 25°C	-38	dBc/Hz
10.2	SSB Phase Noise power density @ 100 Hz offset	Value for a 622.08 MHz VCXO @ 25°C	-70	dBc/Hz
10.3	SSB Phase Noise power density @ 1 kHz offset	Value for a 622.08 MHz VCXO @ 25°C	-98	dBc/Hz
10.4	SSB Phase Noise power density @ 10 kHz offset	Value for a 622.08 MHz VCXO @ 25°C	-108	dBc/Hz
10.5	SSB Phase Noise power density @ 100 kHz offset	Value for a 622.08 MHz VCXO @ 25°C	-104	dBc/Hz

11.0 ENVIRONMENTAL SPECIFICATION

Line	Parameter	Description
11.1	SMD	Product suitable for Pb-free convection reflow soldering, compliant with JEDEC standard. J-STD-020, Level 1.
11.2	Storage Temperature Range	-55 to 125 °C
11.3	Sealing	Non-hermetic package
11.4	Shock	981ms-² (100gn) acceleration for 6ms duration, 3 shocks in each direction along 3 mutually perpendicular axis. IEC 60068-2-27 Test Ea
11.5	Vibration	10-60Hz 0.75mm displacements, 60-500Hz 98.1ms-² (10gn) acceleration. 30 minutes in each of three mutually perpendicular planes at 1 octave per minute. IEC 60068-2-6 Test Fc Procedure B4
11.6	Marking	Resistant to all common solvents
11.7	RoHS	Parts are fully compliant with the European Union Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment. Note: The RoHS compliant parts are suitable for assembly using both Lead-free solders and Tin/Lead solders.

12.0 MANUFACTURING INFORMATION

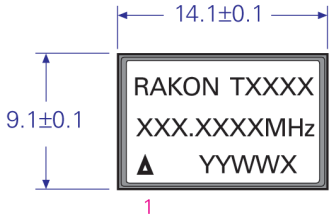
Line	Parameter	Description
12.1	Packaging Description	Tape and Reel as shown
12.2	Reflow	Solder reflow process as per attached profile

13.0 SPECIFICATION NOTES

Line	Parameter	Description
13.1	Note 1	The operating temperature range needs to be specified.
13.2	Note 2	Output current depends on the frequency selected and the output characteristic chosen
13.3	Note 3	Select the exact tuning range required. The values listed are maximum normally available and may require some trade-off in frequency stability. Standard options are ±50ppm, ± 75ppm, ±100ppm and ±150ppm.
13.4	Note 4	The exact value will be frequency dependant
13.5	Note 5	Enable high or low is available as an option
13.6	Note 6	The jitter values will vary depending on the frequency selected

Drawing Name: RS/RV1490 Plastic Model Drawing

MODEL OUTLINE (P6 & P4)

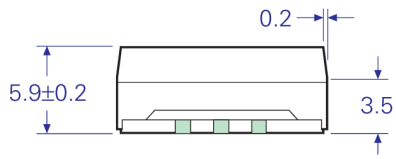


TOP VIEW

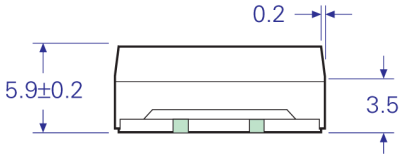
PIN CONNECTIONS

P6		
PIN	VCXO & XO (LVPECL/LVDS)	VCXO (LV/HCMOS/Sinewave)
1	VCO (VCXO only) E/D or NC (XO only)	VCO
2	E/D or NC	E/D or NC
3	GND	GND
4	OUTPUT	OUTPUT
5	$\overline{\text{OUTPUT}}$	NC
6	VCC	VCC

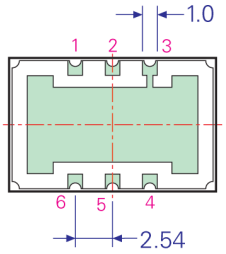
P4	
PIN	VCXO & XO (LV/HCMOS/Sinewave)
1	VCO (VCXO only) E/D or NC (XO only)
2	GND
3	OUTPUT
4	VCC



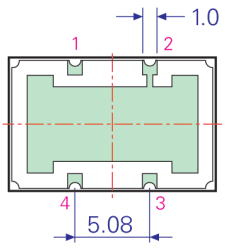
SIDE VIEW (6 PAD)



SIDE VIEW (4 PAD)

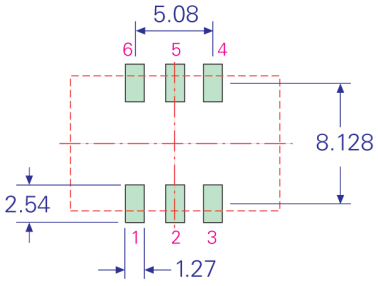


BOTTOM VIEW (6 PAD)

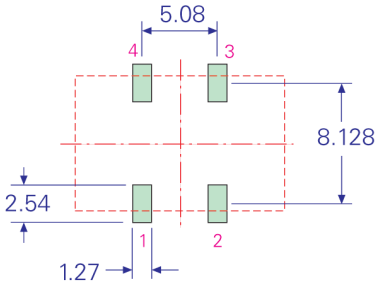


BOTTOM VIEW (4 PAD)

RECOMMENDED PAD LAYOUT - P6



RECOMMENDED PAD LAYOUT - P4



TITLE: RV/RS1490 PLASTIC MODEL DRAWING

RELATED DRAWINGS:

FILENAME: CAT519

REVISION: B

DATE: 12-Sep-11

SCALE: 2 : 1

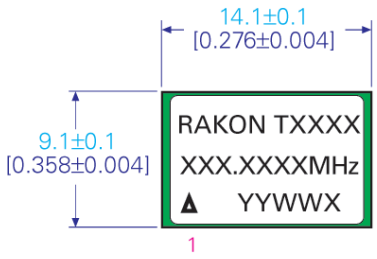
Millimetres

Tolerance:
XX =
X.X = ±0.2
X.XX = ±0.10
X.XXX = ±0.05
X° =
Hole =

©2009 Rakon Limited

Drawing Name: RS/RV1490 Metal Model Drawing

MODEL OUTLINE (M6 & M4)

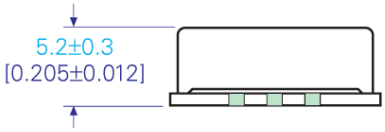


TOP VIEW

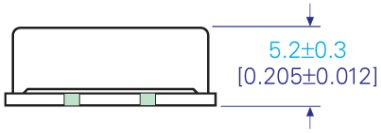
PIN CONNECTIONS

M6		
PIN	VCXO & XO (LVPECL/LVDS)	VCXO (LV/HCMOS)
1	VCO (VCXO only) E/D or NC (XO only)	VCO
2	E/D or NC	E/D or NC
3	GND	GND
4	OUTPUT	OUTPUT
5	$\overline{\text{OUTPUT}}$	NC
6	VCC	VCC

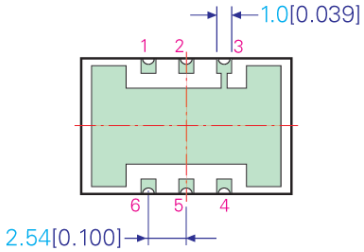
M4	
PIN	VCXO & XO (LV/HCMOS)
1	VCO (VCXO only) E/D or NC (XO only)
2	GND
3	OUTPUT
4	VCC



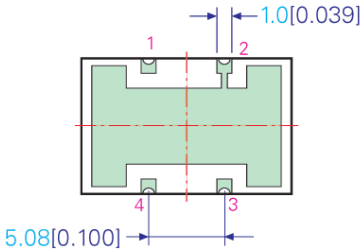
SIDE VIEW (6 PAD)



SIDE VIEW (4 PAD)

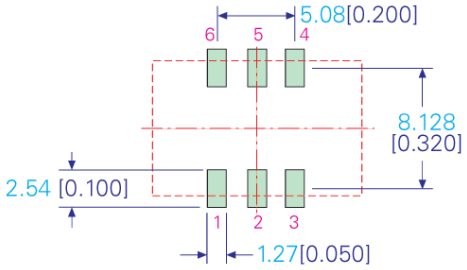


BOTTOM VIEW (6 PAD)

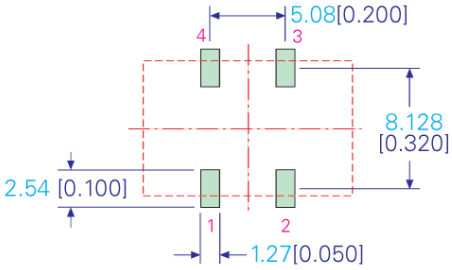


BOTTOM VIEW (4 PAD)

RECOMMENDED PAD LAYOUT - M6



RECOMMENDED PAD LAYOUT -M4

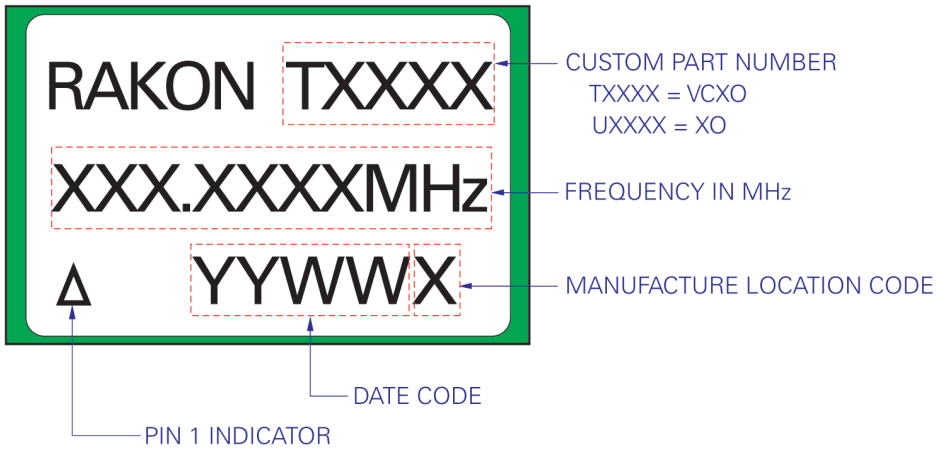


TITLE: RV/RS1490 METAL MODEL DRAWING	FILENAME: CAT525	Tolerance:	
RELATED DRAWINGS:	REVISION: A	XX	=±0.5
	DATE: 16-Sep-09	X.X	=±0.2
	SCALE: 2 : 1	X.XX	=±0.10
	Millimetres [inch]	X.XXX	=±0.05
		X°	=±1.0°
		Hole	=±0.10

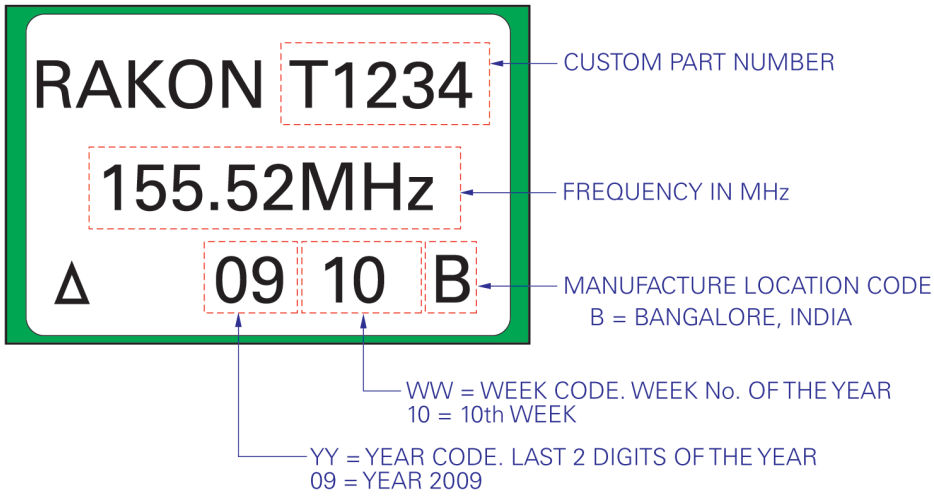
©2009 Rakon Limited

Drawing Name: RS/RV 1490 Series Marking

GENERAL MARKING



MARKING EXAMPLE

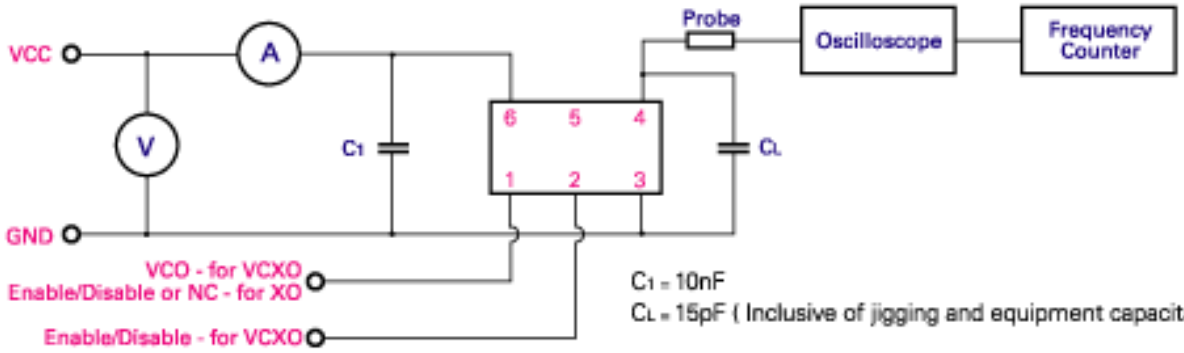


TITLE: RS/RV 1490 SERIES MARKING	FILENAME: CAT524
RELATED DRAWINGS:	REVISION: A
	DATE: 16-Sep-09
	SCALE: NTS
	Millimetres

©2009 Rakon Limited

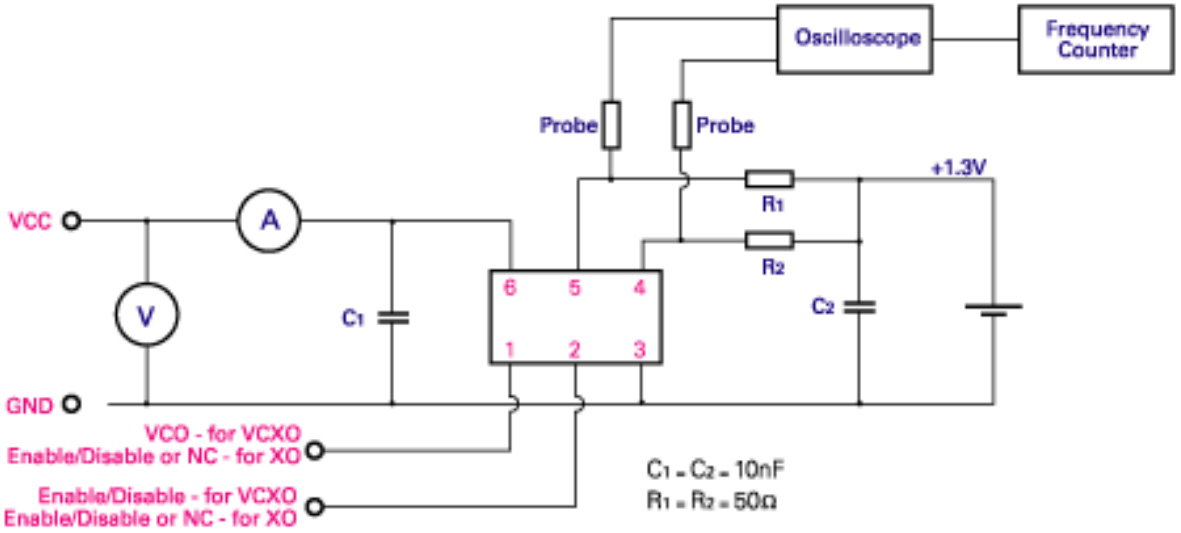
Drawing Name: RS/RV1490 Series Test Circuit

HCMOS TEST CIRCUIT :



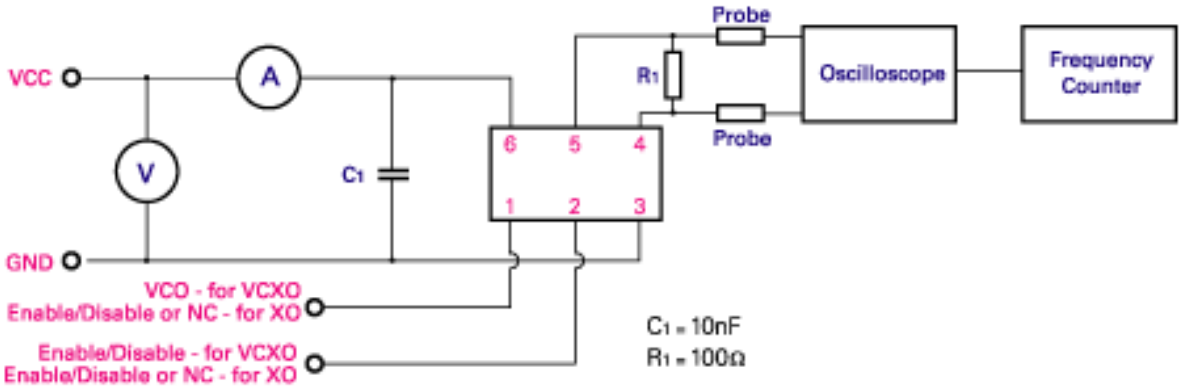
C_1 = 10nF
C_L = 15pF (Inclusive of jigging and equipment capacitance)

LVPECL TEST CIRCUIT :



$C_1 = C_2$ = 10nF
$R_1 = R_2$ = 50Ω

LVDS TEST CIRCUIT :



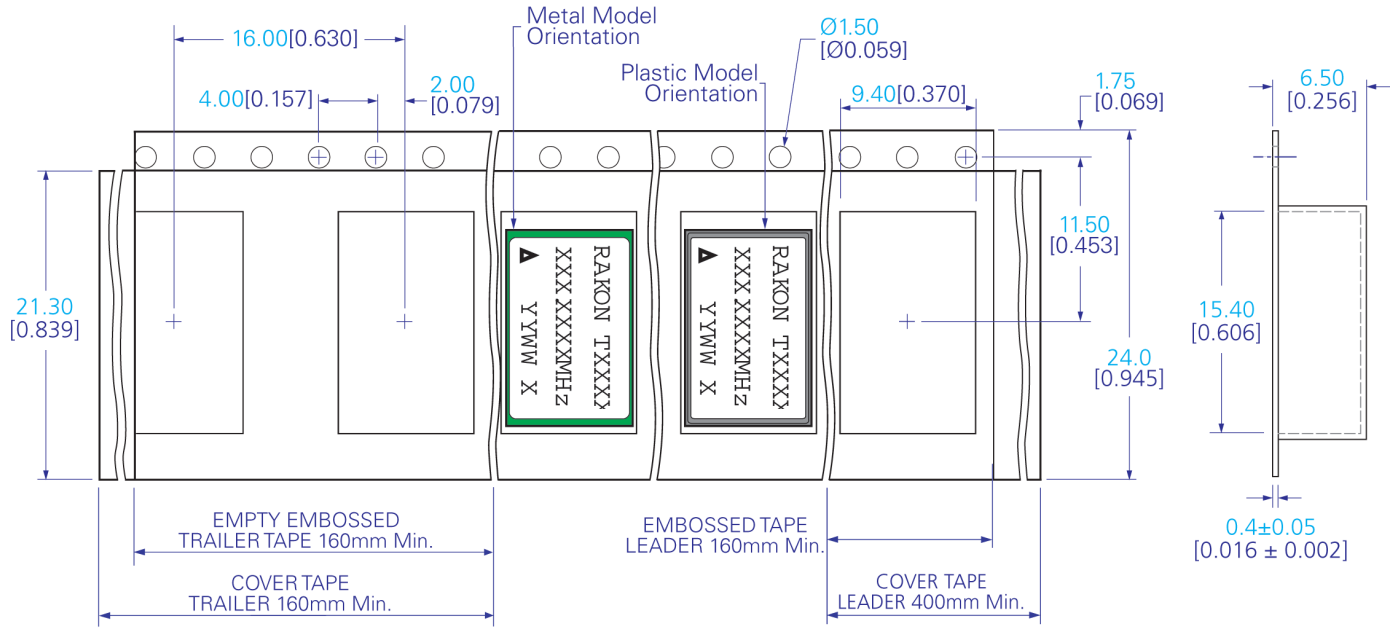
C_1 = 10nF
R_1 = 100Ω

TITLE: RV/RS1490 SERIES TEST CIRCUIT	FILENAME: CAT521
RELATED DRAWINGS:	REVISION: A
	DATE: 16-Sep-09
	SCALE: NTS
	Millimetres [inch]

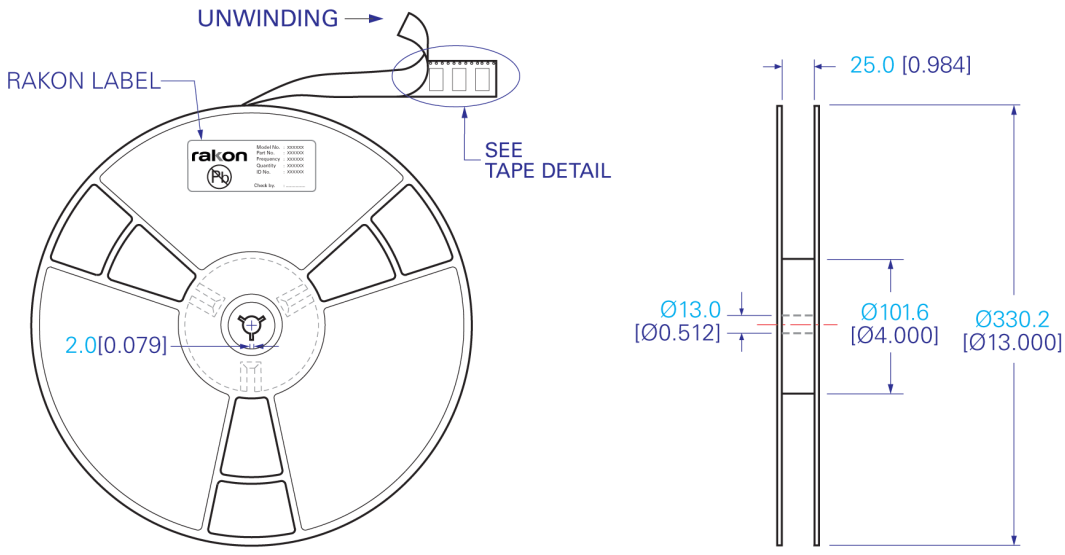
©2009 Rakon Limited

Drawing Name: RS/RV1490 Series Tape & Reel

TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 5)

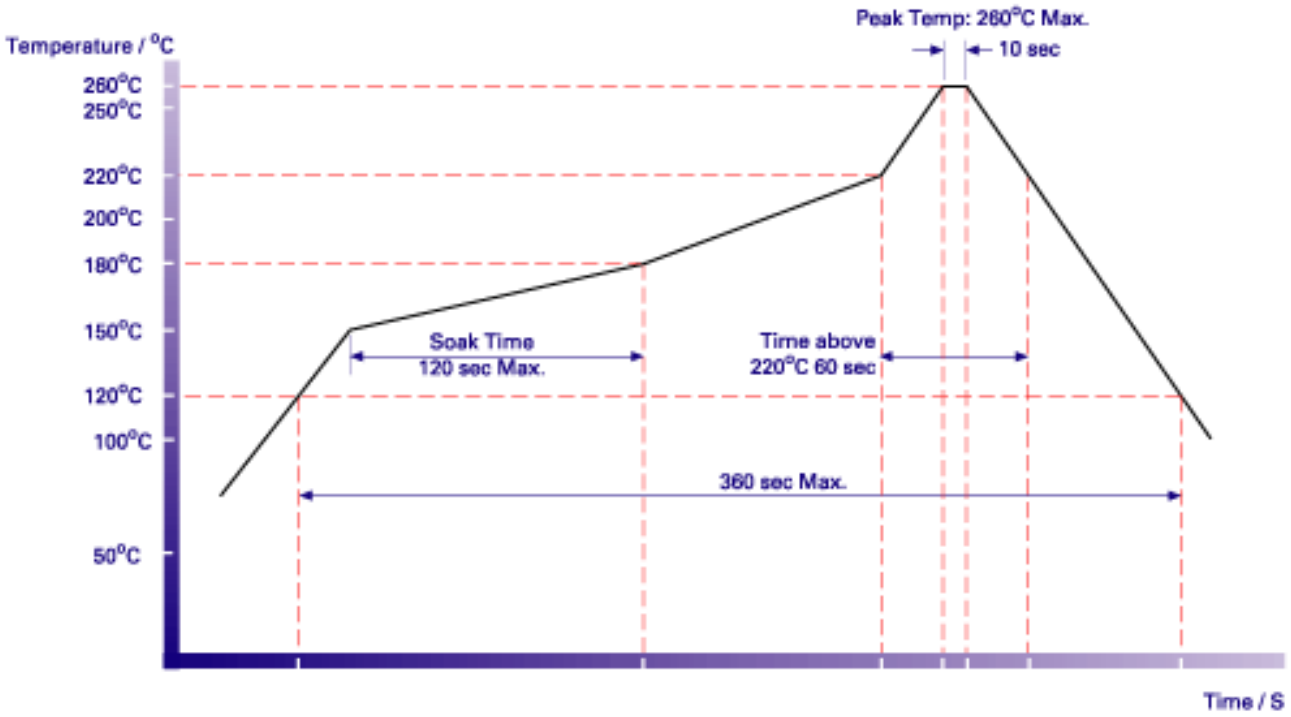


NOTE: Ø330mm REEL'S STANDARD PACKING QUANTITY IS 500 OSCILLATORS PER REEL.

TITLE: RV/RS1490 SERIES TAPE & REEL	FILENAME: CAT522	Tolerance:
RELATED DRAWINGS:	REVISION: A	XX =±0.5
	DATE: 16-Sep-09	X.X =±0.2
	SCALE: See above	X.XX =±0.10
	Millimetres [inch]	X.XXX =±0.05
		X° =±1.0°
		Hole =±0.10

©2009 Rakon Limited

Drawing Name: RF-CAT523



NOTE:
The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder Rakon VCXO/XO is determined by the solder paste manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.

TITLE: RV/RS1490 SERIES Pb-FREE REFLOW	FILENAME: CAT523
RELATED DRAWINGS:	REVISION: A
	DATE: 16-Sep-09
	SCALE: NTS
	Millimetres [inch]

©2009 Rakon Limited

Specification History

Current Version : 1.01

Version	User	Change	Note	Date