



Package: MCM, 7mm x 7mm

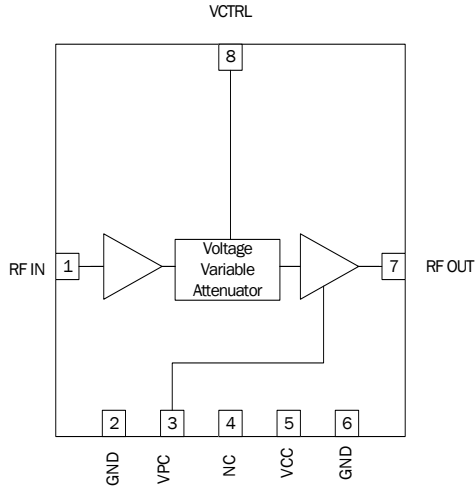


Features

- 731MHz to 881MHz Operation
- Gain = 24dB Typical
- Gain Adjustment Range >19dB
- ACPR = <-60dBc at +10dBm P_{OUT} (Dual Carrier WCDMA)
- Small 7mm x 7mm, Multi-Chip Module

Applications

- Cellular, 3G and 4G Infrastructure
- WiBro, WiMax, LTE
- Microwave Radio
- High Linearity Power Control



Functional Block Diagram

Product Description

RFMD's RFVA1027 is a fully integrated analog controlled variable gain amplifier featuring exceptional linearity over a greater than 19dB gain control range. This variable gain amplifier is controlled by a single 0V to 3.3V positive supply voltage. The RFVA1027 is packaged in a small 7mm x 7mm leadless laminate MCM which contains solid thermal vias for ultra low thermal resistance. This module is internally matched to 50Ω and is easy to use with no external matching components required.

Ordering Information

RFVA1027SQ	Sample bag with 25 pieces
RFVA1027SR	7" Sample reel with 100 pieces
RFVA1027TR7	7" Reel with 1500 pieces
RFVA1027TR13	13" Reel with 2500 pieces
RFVA1027PCK-410	731MHz to 881MHz PCBA with 5-piece sample bag

Optimum Technology Matching® Applied

- | | | | |
|---|--------------------------------------|--|------------------------------------|
| <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input type="checkbox"/> Si CMOS | <input type="checkbox"/> BiFET HBT |
| <input checked="" type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | <input type="checkbox"/> LDMOS |

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Absolute Maximum Ratings

Parameter	Rating	Unit
Max Device Current	770	mA
Max Device Voltage	5.5	V
Max Control Line Voltage	6	V
Max RF Input Power*	25	dBm
Max Junction Temp (T _J)	+150	°C
Max Storage Temp	+150	°C
Thermal Resistance (junction to backside)	14.8	°C/W
ESD	Class 1C (1000V min)	
Moisture Sensitivity Level	MSL3	

*Load condition: Z_L = 50Ω



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2011/65/EU (at time of this document revision).

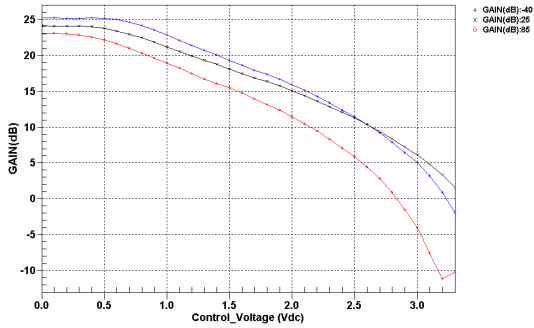
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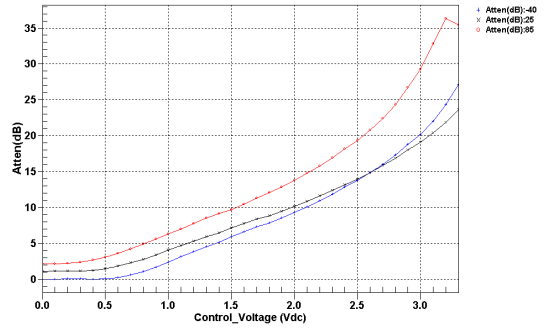
RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and < 2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency	731		881	MHz	
Temperature Range	-40	25	85	°C	Operating Range
Gain	21	24	26	dB	Min attenuator setting
Nominal Operating Output Power		10		dBm	Operating power for ACPR rating
Output IP3	37	42		dBm	In high gain setting
P1dB	24	28		dBm	High gain setting
ACPR	-60	-65		dBc	Dual carrier WCDMA, 7.5dB CF at nominal operating power
Gain Flatness		0.2	0.9	dB	Over 50MHz BW
Gain Adjustment Range	19	22		dB	
Control Voltage Range	0		3.3	V	
Noise Figure		5.25		dB	Min attenuator setting
Impedance		50		Ω	
Input Return Loss	11	15		dB	Over attenuation range
Output Return Loss	8	18		dB	Over attenuation range
Supply Voltage	4.75	5.0	5.25	V	
Supply Current	300	460	600	mA	Max current is at -40 °C
Supply Current (VPC = 0V)	120	135	150	mA	Output amplifier shutdown; total current

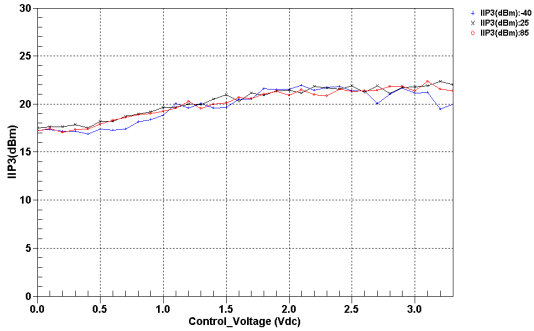
GAIN Vs. CONTROL VOLTAGE @ 806 MHz



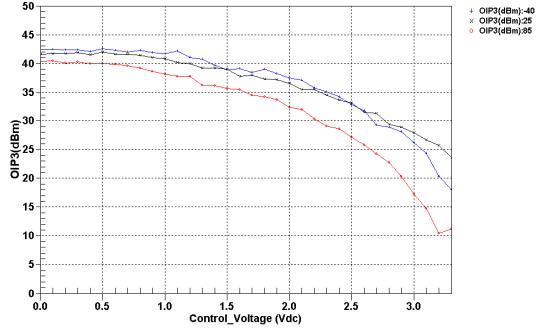
ATTEN Vs. CONTROL VOLTAGE @ 806 MHz



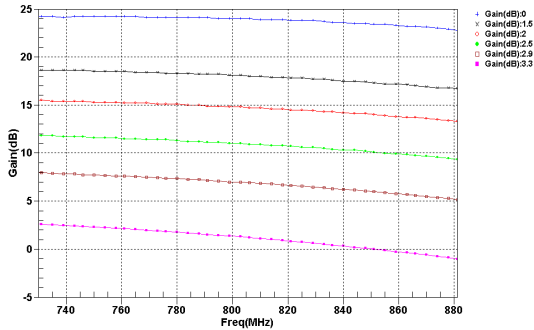
INPUT IIP3 Vs. CONTROL VOLTAGE @ 806 MHz



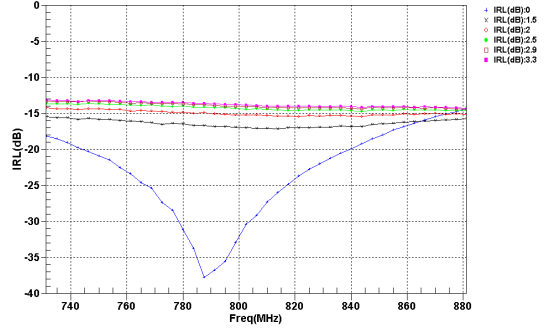
OUTPUT IIP3 Vs. CONTROL VOLTAGE @ 806 MHz



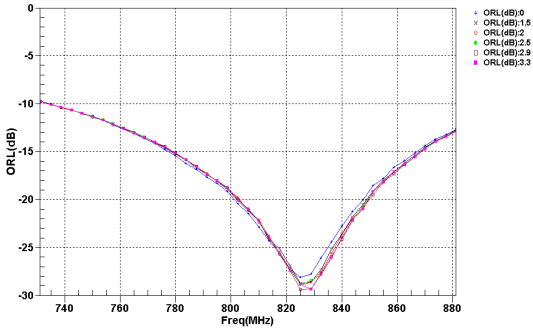
GAIN Vs. FREQUENCY Vs. CONTROL VOLTAGE



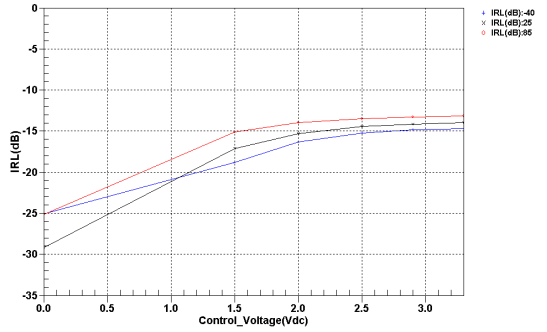
IRL Vs. FREQUENCY Vs. CONTROL VOLTAGE



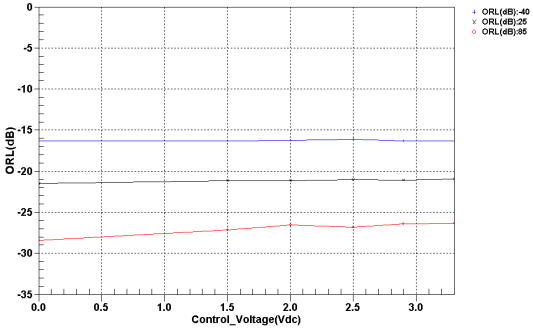
ORL Vs. FREQUENCY Vs. CONTROL VOLTAGE



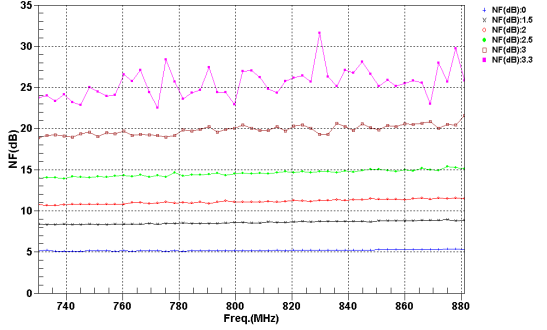
INPUT RETURN LOSS Vs. CONTROL VOLTAGE Vs. TEMPERATURE @ 806 MHz



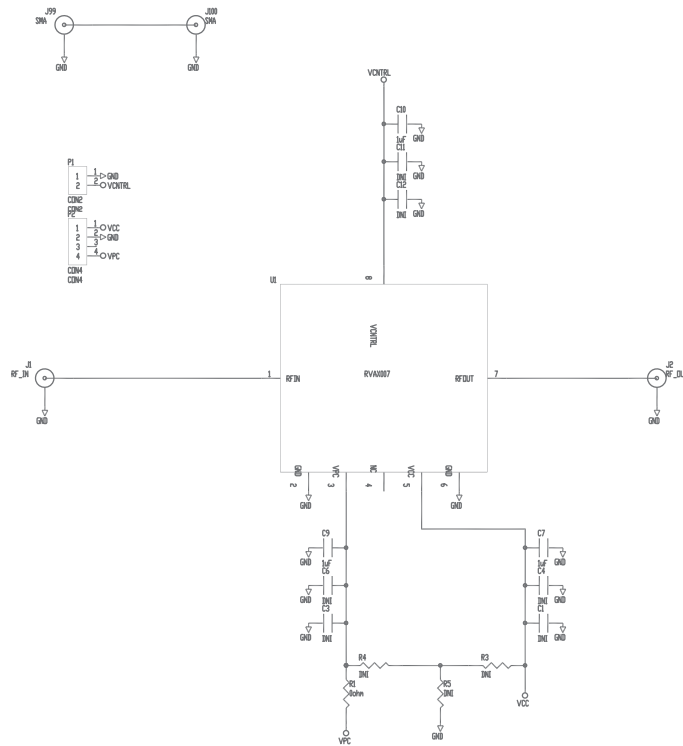
OUTPUT RETURN LOSS Vs. CONTROL VOLTAGE Vs. TEMPERATURE @ 806 MHz



NOISE FIGURE Vs. FREQUENCY Vs. CONTROL VOLTAGE



Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)

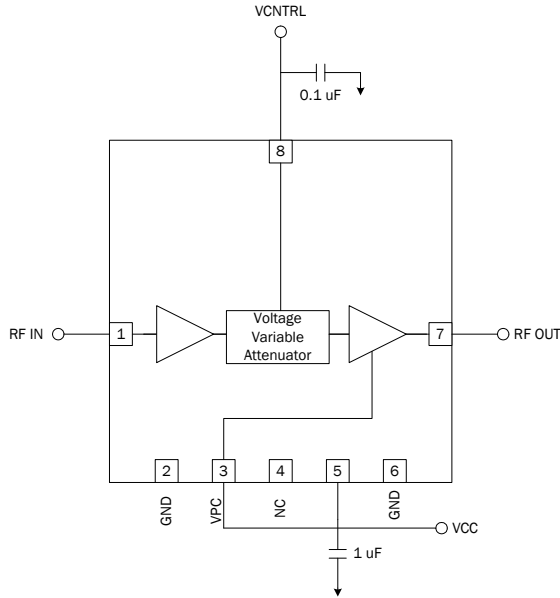
Description	Reference Designator	Manufacturer	Manufacturer's P/N
EVALUATION BOARD		DDI	RFVax007L410(A)
CAP, 1 μ F, 10%, 10V, X5R, 0402	C7, C9-C10	MURATA ELECTRONICS	GRM155R61A105KE15D
RES, 0 Ω , 0402	R1	KAMAYA, INC	RMCI/16SJPTH
CONN, SMA, END LAUNCH, UNIV, HYB MNT, FLT	J1-J2	HEILIND ELECTRONICS	PER MAT-21-1038
CONN, HDR, ST, PLRZD, 4-PIN, 0.100"	P2	ITW PANCON	MPSS100-4-C
CONN, HDR, ST, PLRZD, 2-PIN, 0.100"	P1	ITW PANCON	MPSS100-2-C
DNP	C1, C3-C4, C6, C11-C12, R3-R5		
RFVA1027 MODULE	U1	RFMD	RFVA1027

Pin Table and Description

Pin	Function	Description
1	RFIN	RF input pin. Internal DC block.
2	GND	Ground pin.
3	VPC	Power up/down control for 2nd stage amplifier. Apply V_{CC} to power on 2nd stage amplifier. Apply 0V to disable 2nd stage amplifier. Do not exceed $V_{CC} + 0.5V$. Connect to V_{CC} if not needed. Decoupling capacitor may be desired on application board for control line noise.
4	NC	No connection.
5	VCC	Power supply for the module. Recommending 1 μ F decoupling cap on the application board.
6	GND	Ground pin.
7	RFOUT	RF output pin. Internal DC block.
8	VCTRL	Gain control voltage; 0V to 3.3V range. Maximum gain at 0V. Recommending 0.1 μ F decoupling on the application board.
Center Pad	GND	Center ground pads need to have a good thermal path on the application board. Use solder stencil pattern shown in the document to define solder paste during assembly.

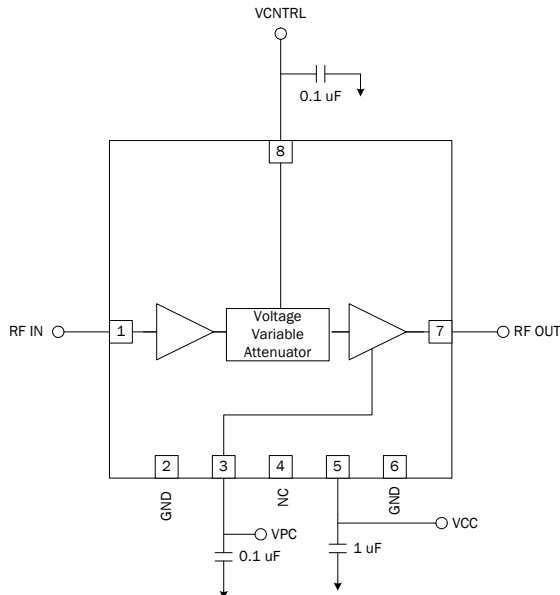
Application Schematic

(Without using final stage amplifier power down control)



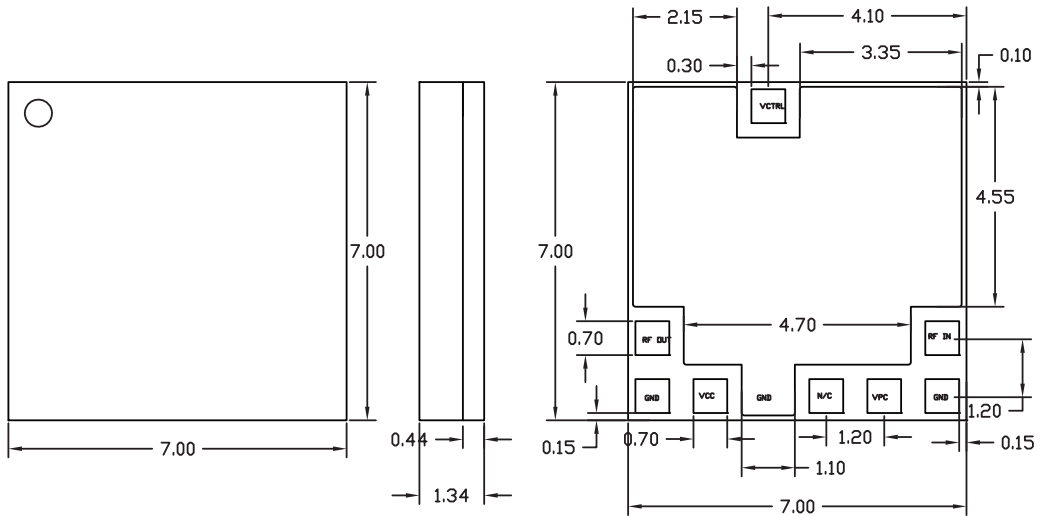
Application Schematic

(Using final stage amplifier power down control)

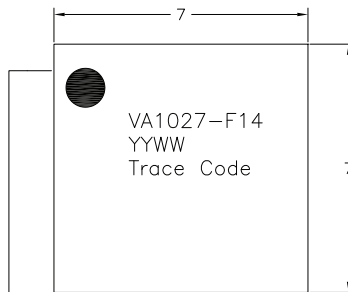


Package Drawing

(All dimensions in mm)



Branding Diagram



Pin 1 Indicator

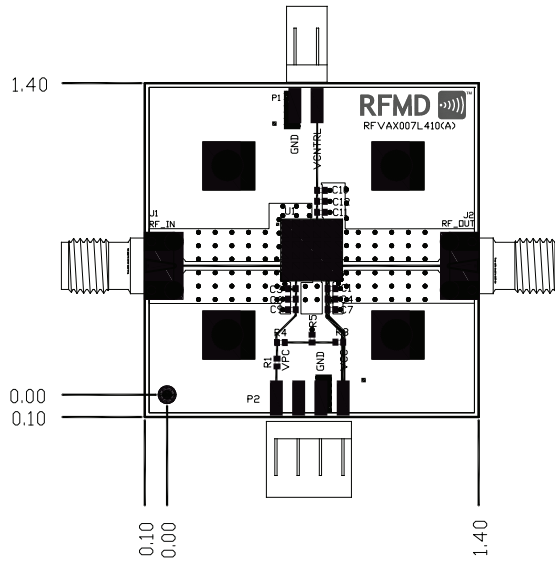
Fill in the YYWW Notation with the Date Code

YY = Year

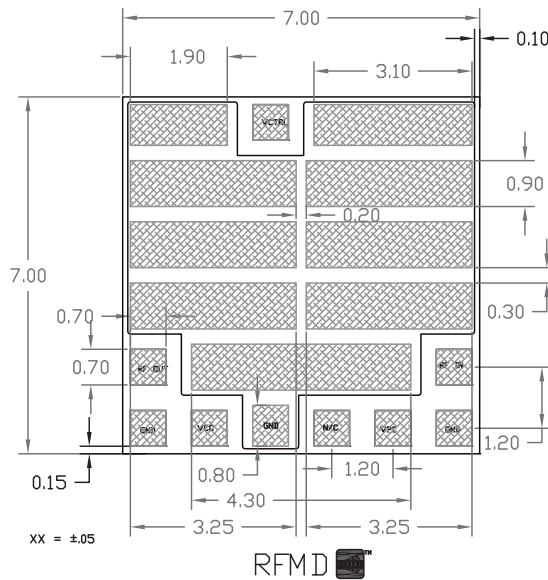
WW = Week

Trace Code to be assigned by SubCon

Evaluation Board Assembly Drawing



Required PCB Solder Stencil



Note: This solder stencil pattern is required to prevent solder voiding that may impact thermal dissipation.