TPS560200 采用高级 Eco-mode™ 的 4.5V 至 17V 输入、500mA 同步降压 转换器

1 特性

- 集成单片 0.95Ω 高侧和 0.33Ω 低侧 MOSFET
- 500mA 持续输出电流
- 输出电压范围：0.8V 至 6.5V
- 0.8V 基准电压，温度范围内的精度为 ±1.3%
- 高级自动跳跃 Eco-mode™用于在轻负载时实现高效率
- D-CAP2™模式启用快速瞬态响应
- 无需外部补偿
- 600kHz 开关频率
- 2ms 内部软启动
- 安全启动至预偏置 VOUT
- 热关断
- -40°C 至 125°C 的工作结温范围
- 采用 5 引脚小外形尺寸晶体管 (SOT)-23 封装

2 应用

- 机顶盒
- 调制解调器
- DTB
- ASDL

3 说明

TPS560200 是一款集成 MOSFET 的 17V、500mA、低 Iq 自适应导通时间 D-CAP2 模式同步单片降压转换器，采用简单易用的 5 引脚 SOT-23 封装。

TPS560200 有助于系统设计人员通过具备成本效益、所用组件较少并且待机电流较低的解决方案完成各种终端设备的电源总线调节器集。器件主控制回路采用 D-CAP2 模式控制，无需外部补偿元件即可实现快速瞬态响应。自适应导通时间控制支持器件在高负载条件下的 PWM 模式与轻负载条件下的高级 Eco-mode 工作模式之间实现无缝切换。

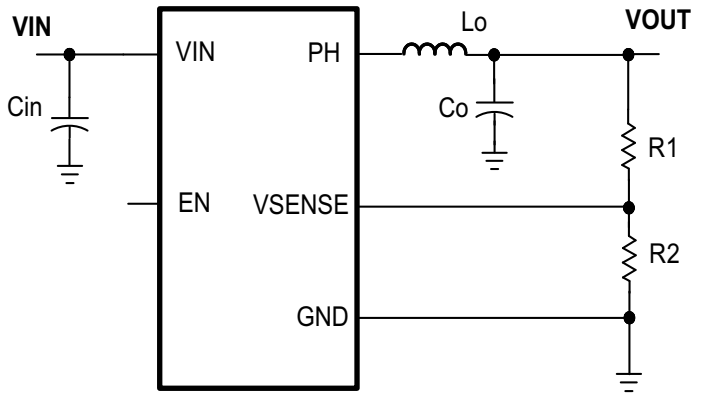
TPS560200 的专有电路还可使其适应低等效串联电阻 (ESR) 输出电容（如导电性聚合物钽固体电解电容 (POSCAP) 和导电性聚合物铝电解电容 (SP-CAP)）以及超低 ESR 陶瓷电容。该器件由 4.5V 至 17V 范围内的输入电压供电。输出电压可在 0.8 V 至 6.5V 范围内进行编程。该器件还 具有 2ms 固定软启动时间。该器件采用 5 引脚 SOT-23 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS560200	SOT (5)	2.90mm × 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

4 修订历史记录

Changes from Revision B (February 2015) to Revision C **Page**

- 从数据表标题删除了 SWIFT™ ... 1

Changes from Revision A (Janurary 2015) to Revision B **Page**

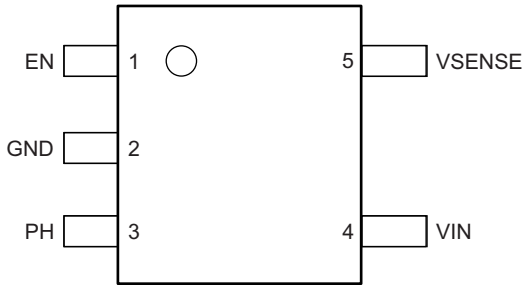
- Removed note from ENABLE (EN PIN) to indicate that the parameters are production tested ... 5

Changes from Original (September 2013) to Revision A **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Float to enable
GND	2	—	Return for control circuitry and low-side power MOSFET
PH	3	O	The switch node
VIN	4	I	Supplies the control circuitry of the power converter
VSENSE	5	I	Converter feedback input. Connect to output voltage with feedback resistor divider

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	20	V
	EN	–0.3	7	
	VSENSE	–0.3	3	
Output voltage	PH	–0.6	20	
	PH 10-ns transient	–2	20	
Source current	EN		±100	µA
	PH	Current limit		A
Sink current	PH	Current limit		A
Operating junction temperature		–40	125	°C
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage range	4.5	17	V
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS560200 DBV 5 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	166.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100	
$R_{\theta JB}$	Junction-to-board thermal resistance	75.5	
ψ_{JT}	Junction-to-top characterization parameter	29.2	
ψ_{JB}	Junction-to-board characterization parameter	3.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	28.7	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, VIN = 4.5 V to 17 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
VIN Operating input voltage		4.5		17	V
VIN Internal UVLO threshold	VIN Rising	3.9	4.35	4.5	V
VIN Internal UVLO hysteresis			200		mV

Electrical Characteristics (continued)

T_J = –40°C to 125°C, VIN = 4.5 V to 17 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN Shutdown supply current	EN = 0 V, VIN = 12 V	2.0	3.7	9	µA
VIN Operating– non switching supply current	VSENSE = 850 mV, VIN = 12 V	35	60	95	µA
ENABLE (EN PIN)					
Enable threshold	Rising		1.16	1.29	V
	Falling	1.05	1.13		V
Internal Soft-Start	VSENSE ramps from 0 V to 0.8 V		2		ms
OUTPUT VOLTAGE					
Voltage reference	25°C, VIN = 12 V, VOUT = 1.05 V, IOUT = 5 mA, Pulse-Skipping	0.796	0.804	0.812	V
	25°C, VIN = 12 V, VOUT = 1.05 V, IOUT = 100 mA, Continuous current mode	0.792	0.800	0.808	V
	VIN = 12 V, VOUT = 1.05 V, IOUT = 100 mA, Continuous current mode	0.789	0.800	0.811	V
MOSFET					
High-side switch resistance(1)(2)	VIN = 12 V	0.50	0.95	1.50	Ω
Low-side switch resistance(1)	VIN = 12 V	0.20	0.33	0.55	Ω
CURRENT LIMIT					
Low-side switch sourcing current limit	LOUT = 10 µH, Valley current, VOUT = 1.05 V	550	650	775	mA
THERMAL SHUTDOWN					
Thermal shutdown			170		°C
Thermal shutdown hysteresis			10		°C
ON-TIME TIMER CONTROL					
On time	VIN = 12 V	130	165	200	ns
Minimum off time	25°C, VSENSE = 0.5 V		250	400	ns
OUTPUT UNDERVOLTAGE PROTECTION					
Output UVP threshold	Falling	56	63	69	%VREF
Hiccup time			15		ms

(1) Not production tested
(2) Measured at pins

6.6 Typical Characteristics

V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

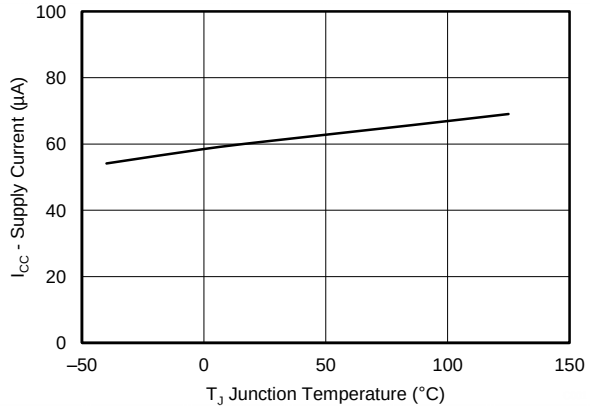


图 1. Supply Current vs Junction Temperature

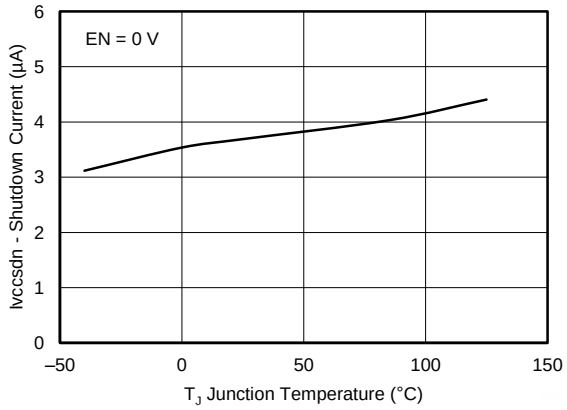


图 2. Shutdown Current vs Junction Temperature

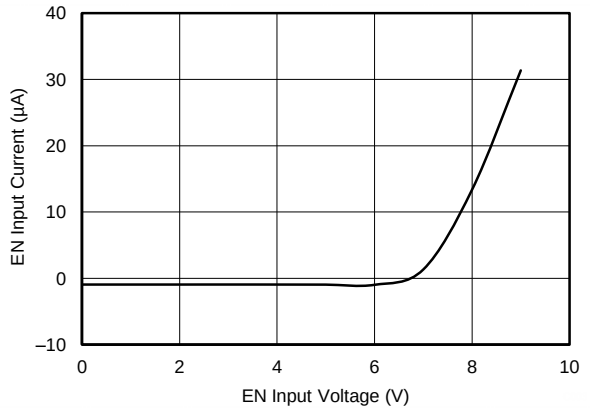


图 3. EN Input Current vs EN Input Voltage

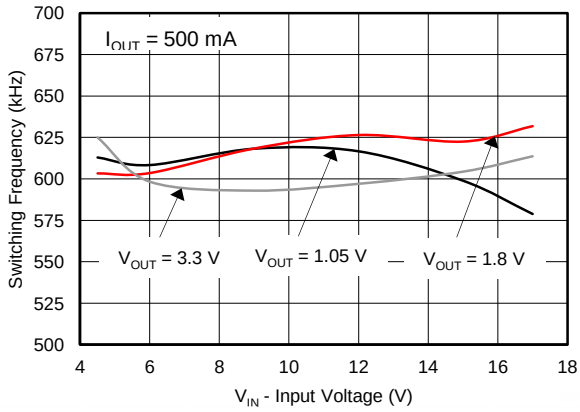


图 4. Switching Frequency vs Input Voltage

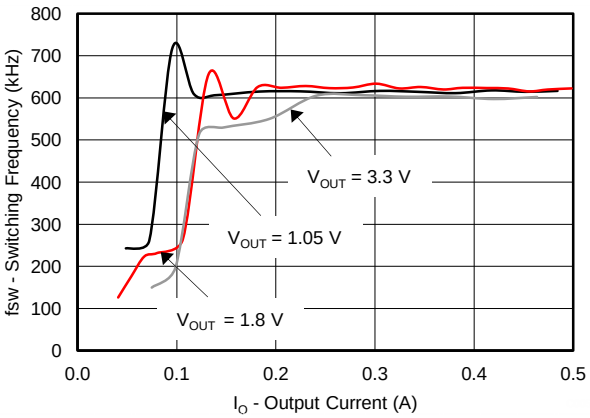


图 5. Switching Frequency vs Output Current

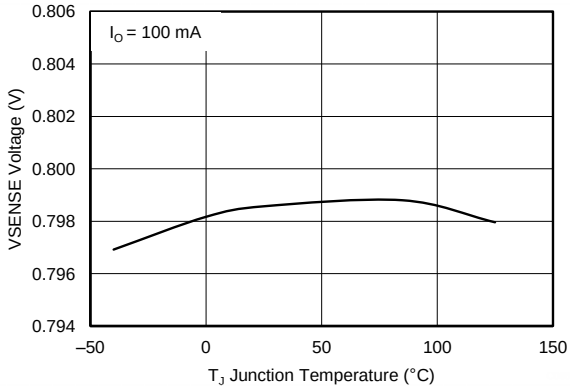


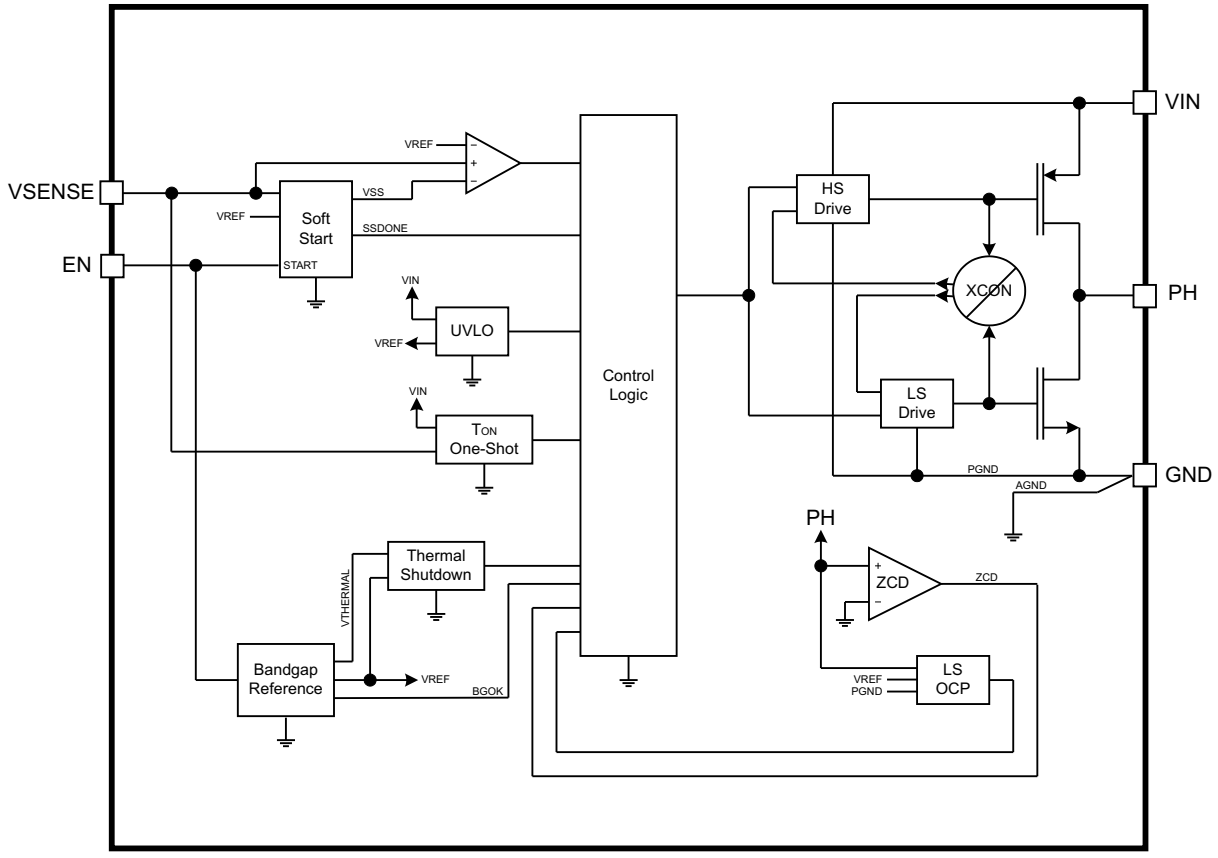
图 6. VSENSE Voltage vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS560200 is a 500-mA synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS560200 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VOUT, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

Feature Description (接下页)

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS560200 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS560200 runs with a pseudo-constant frequency of 600 kHz by using the input voltage and output voltage to set the on-time, one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

7.3.3 Advanced Auto-Skip Eco-Mode Control

The TPS560200 is designed with advanced auto-skip Eco-Mode to increase higher light-load efficiency. As the output current decreases from heavy-load condition, the inductor current is also reduced. If the output current is reduced enough, the inductor current ripple valley reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying low-side MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept approximately the same as is in continuous conduction mode. The off-time increases as it takes more time to discharge the output capacitor to the level of the reference voltage with smaller load current. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 公式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times fsw} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.4 Soft-Start and Prebiased Soft-Start

The TPS560200 has an internal 2-ms soft-start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS560200 contains a unique circuit to prevent current from being pulled from the output during start-up if the output is prebiased. When the soft-start commands a voltage higher than the prebias level (internal soft-start becomes greater than feedback voltage V_{VSENSE}), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, and ensure that the out voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from prebiased start-up to normal mode operation.

7.3.5 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the PH pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. The TPS560200 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each switching cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the overcurrent threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This protection is nonlatching. When the VSENSE voltage becomes lower than 63% of the target voltage, the UVP comparator detects it. After 7 µs detecting the UVP voltage, device shuts down and re-starts after hiccup time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

Feature Description (接下页)

7.3.6 Thermal Shutdown

TPS560200 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 170°C), the device is shut off. This is nonlatch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS560200 can operate in its normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS560200 operates at a quasi-fixed frequency of 600 kHz.

7.4.2 Eco-Mode Operation

When the TPS560200 is in the normal CCM operating mode and the switch current falls to 0 A, the TPS560200 begins operating in pulse-skipping Eco-Mode. Each switching cycle is followed by a period of energy-saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-Mode threshold voltage. As the output current decreases the perceived time between switching pulses increases.

7.4.3 Standby Operation

When the TPS560200 is operating in either normal CCM or Eco-Mode, it may be placed in standby by asserting the EN pin low.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS560200 is used as a step-down converter which converts a voltage of 4.5 V to 17 V to a lower voltage. WEBENCH® software is available to aid in the design and analysis of circuits.

8.2 Typical Application

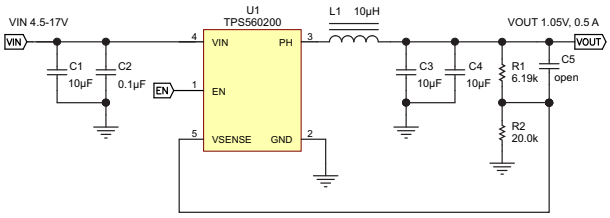


图 7. Typical Application Schematic

8.2.1 Design Requirements

For this design example, refer to the application parameters shown in 表 1.

表 1. Design Parameters

PARAMETER	VALUES
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	500 mA
Output voltage ripple	10 mV/pp

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using 公式 2 to calculate V_{OUT}.

To improve efficiency at light loads, consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VSENSE input current are more noticeable.

$$R2 = \frac{R1 \times 0.8\ V}{V_{OUT} - 0.8V} \quad (2)$$

8.2.2.2 Output Filter Selection

The output filter used with the TPS560200 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS560200. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of 公式 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 2.

表 2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C5 (pF)	L1 (µH)			C3 + C4 (µF)
				MIN	TYP	MAX	
1.0	4.99	20.0			10		10 + 10
1.05	6.19	20.0			10		10 + 10
1.2	10.0	20.0			10		10 + 10
1.5	17.4	20.0			10		10 + 10
1.8	24.9	20.0	optional		10		10 + 10
2.5	42.2	20.0	optional		10		10 + 10
3.3	61.9	20.0	optional		10		10 + 10
5.0	105	20.0	optional		10		10 + 10

Because the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. Additional phase boost can be achieved by adding a feed-forward capacitor (C5) in parallel with R1. The feed-forward capacitor is most effective for output voltages at or above 1.8 V.

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 公式 4, 公式 5, and 公式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 600 kHz for f_{SW}.

Use 600 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 公式 5 and the RMS current of 公式 6.

$$I_{LPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_{OUT} \times fsw} \quad (4)$$

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

$$I_{L_{OUT}(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{LPP}^2} \quad (6)$$

For this design example, the calculated peak current is 0.582 A and the calculated RMS current is 0.502 A. The inductor used is a Würth 744777910 with a peak current rating of 2.6 A and an RMS current rating of 2 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS560200 is intended for use with ceramic or other low-ESR capacitors. The recommended values are given in 表 2. Use 公式 7 to determine the required RMS current rating for the output capacitor.

$$I_{C_{OUT}(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times fsw} \quad (7)$$

For this design two MuRata GRM32DR61E106KA12L 10-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.047 A and each output capacitor is rated for 3 A.

8.2.2.3 Input Capacitor Selection

The TPS560200 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1-µF capacitor (C2) from pin 4 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.3 Application Curves

V_{IN} = 12 V, V_{OUT} = 1.05 V, T_A = 25°C (unless otherwise noted).

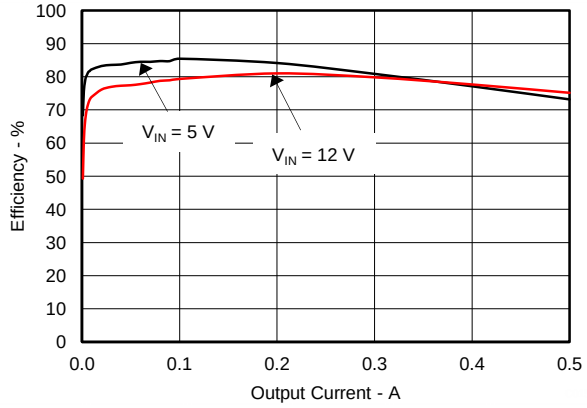


图 8. Efficiency

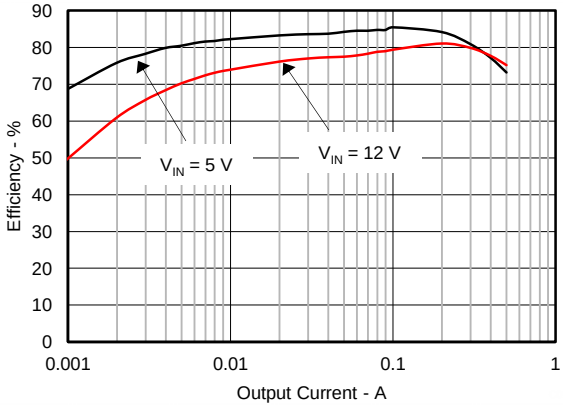


图 9. Light-Load Efficiency

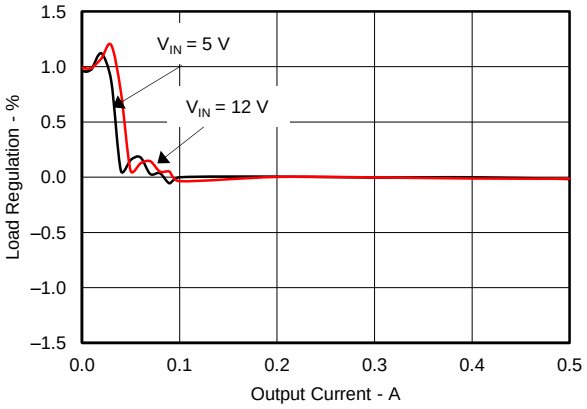


图 10. Load Regulation

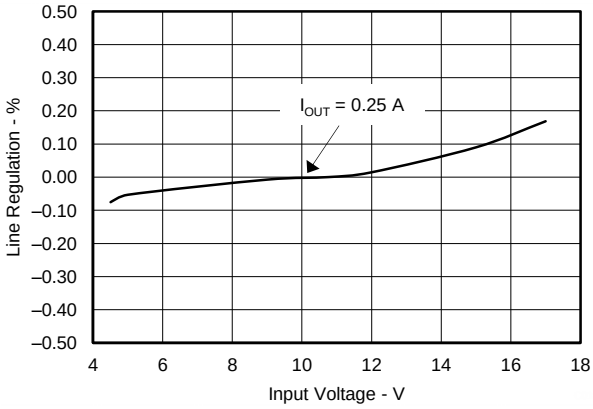


图 11. Line Regulation

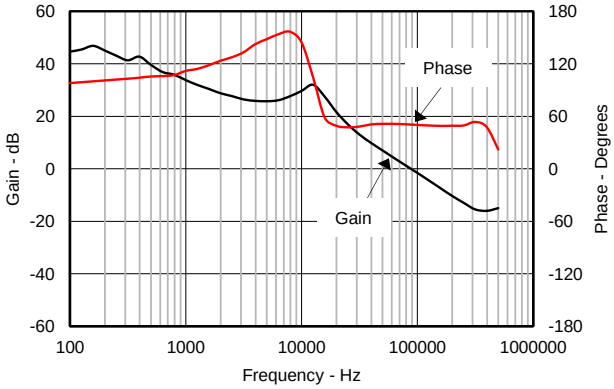


图 12. Loop Response, I_{OUT} = 0.25 A

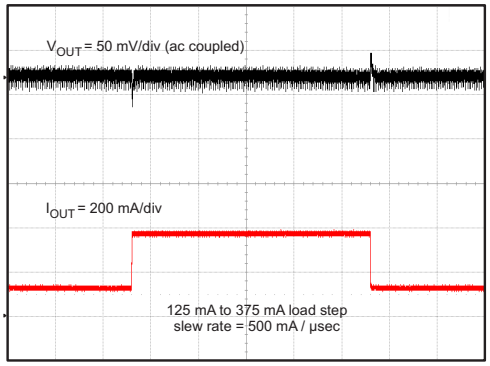
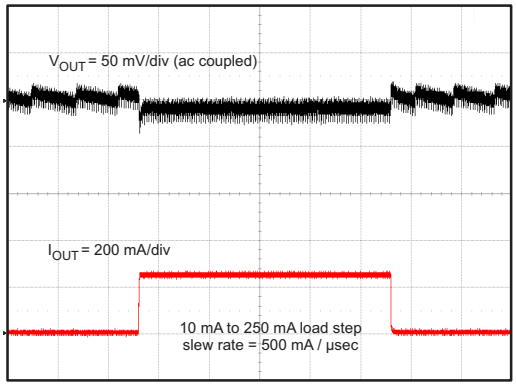
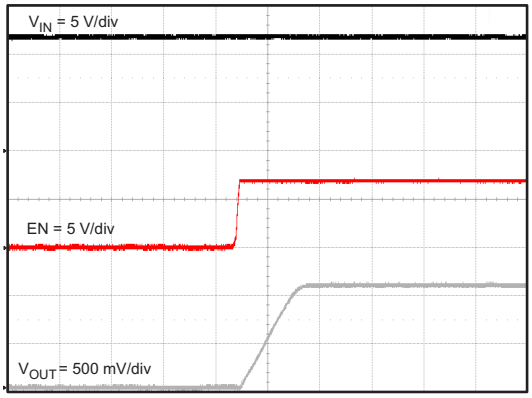


图 13. Transient Response, 25% to 75% Load Step



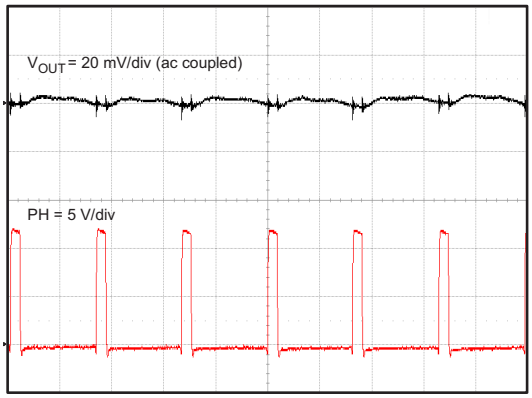
Time = 200 µs/div

图 14. Transient Response, 2% to 50% Load Step



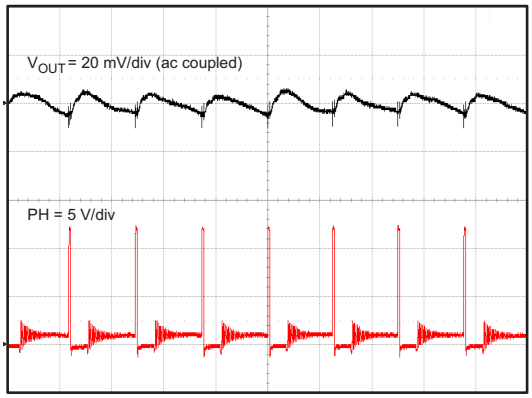
Time = 2 ms/div

图 15. Start-Up Relative to EN



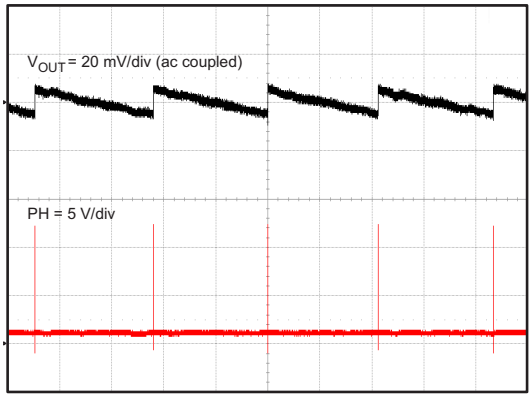
Time = 1 µs/div

图 16. Output Ripple, I_{OUT} = 500 mA



Time = 5 µs/div

图 17. Output Ripple, I_{OUT} = 30 mA



Time = 2 ms/div

图 18. Output Ripple, I_{OUT} = 0 mA

9 Power Supply Recommendations

The TPS560200 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is VO / 0.65.

10 Layout

10.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. Take care to minimize the loop area formed by the bypass capacitor connection, the VIN pin, and the GND pin of the IC. The typical recommended bypass capacitance is 10-μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN and GND pins of the device. An additional high-frequency bypass capacitor may be added. See 图 19 for a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. The PH pin should be routed to a small copper area directly adjacent to the pin. Make the circulating loop from PH to the output inductor, output capacitors and back to GND as tight as possible while preserving adequate etch width to reduce conduction losses in the copper. Connect the exposed thermal pad to bottom or internal layer ground plane using vias as shown. Additional vias may be used adjacent to the IC to tie top-side copper to the internal or bottom layer copper. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate layout schemes; however, this layout produced good results and is intended as a guideline.

10.2 Layout Example

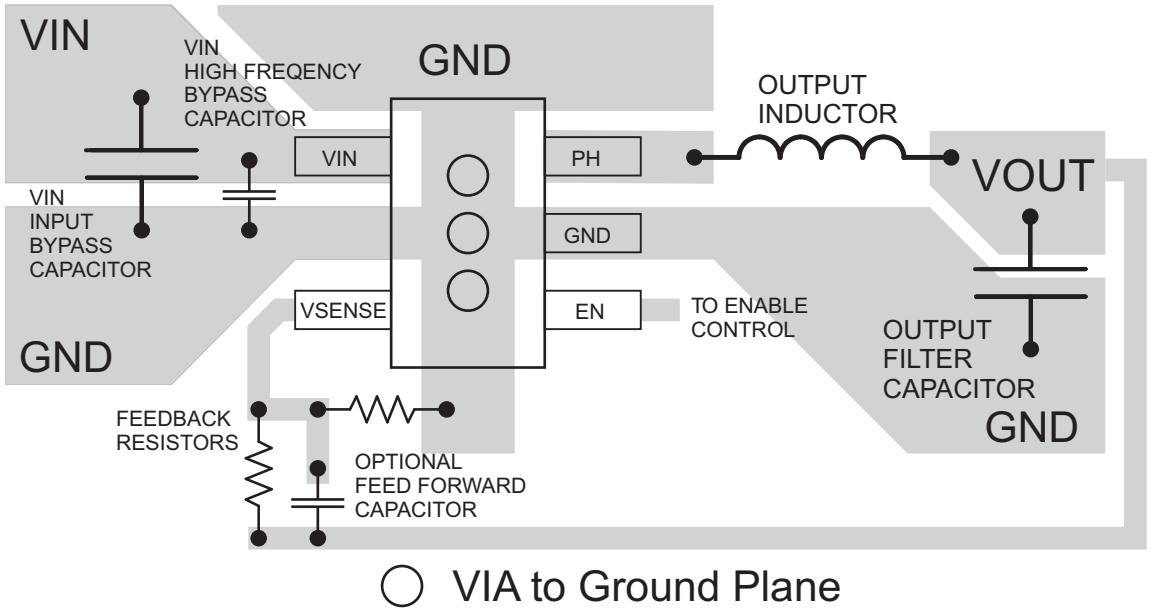


图 19. Layout Schematic

11 器件和文档支持

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11.2 静电放电警告

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11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS560200DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L562	Samples
TPS560200DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L562	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS560200 :

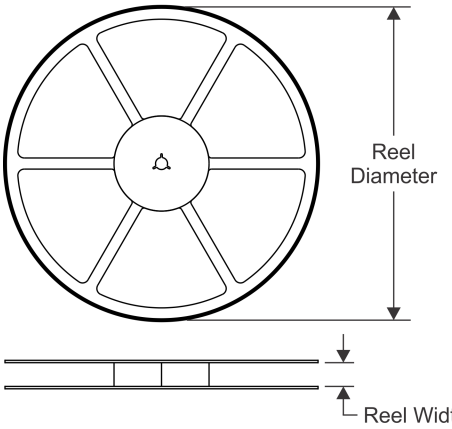
- Automotive: TPS560200-Q1

NOTE: Qualified Version Definitions:

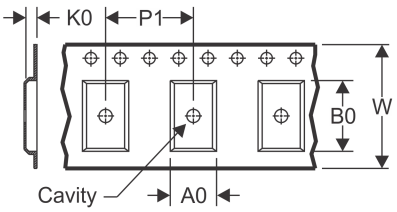
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

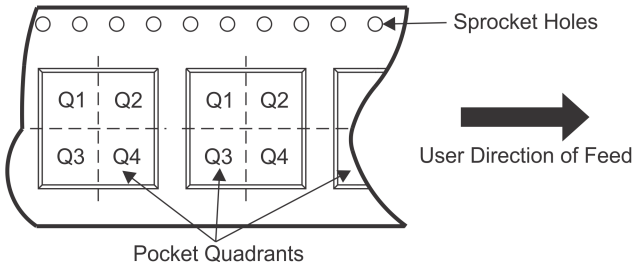


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

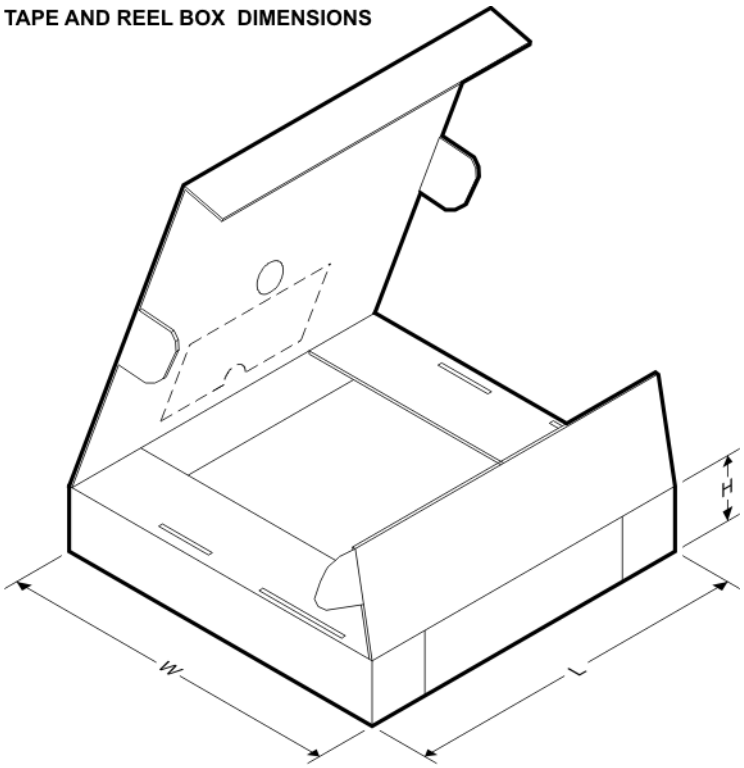
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS560200DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS560200DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

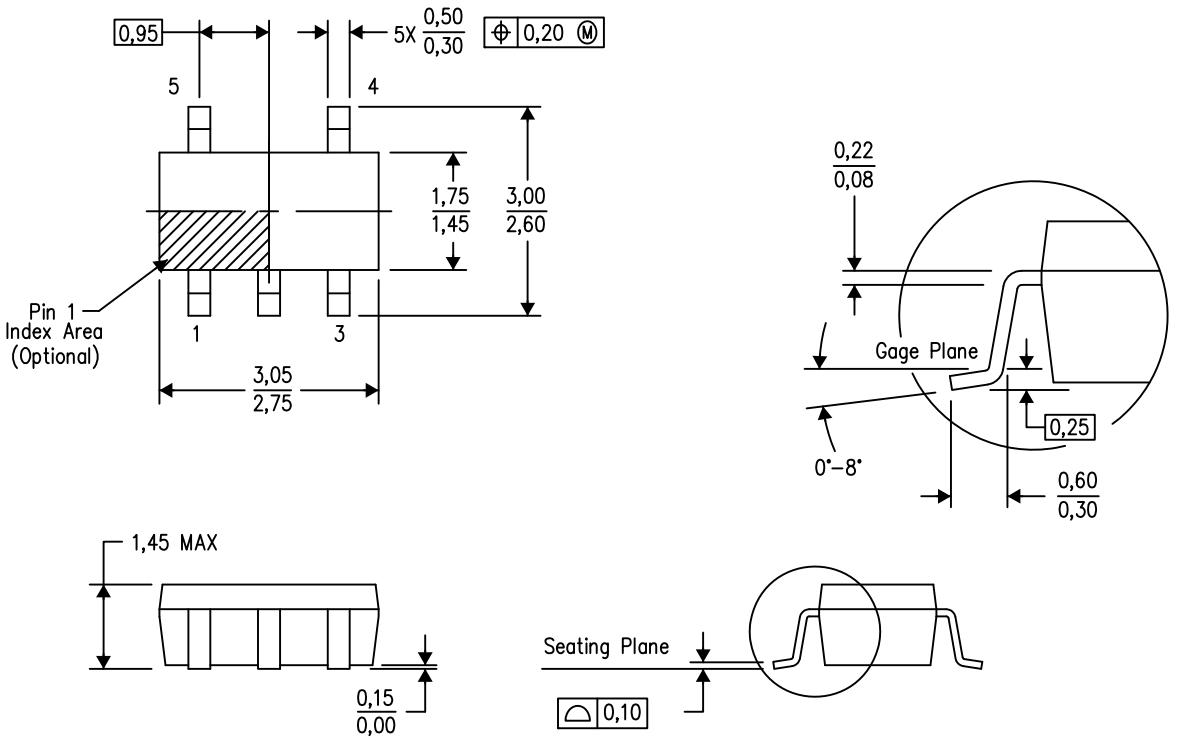
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS560200DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS560200DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

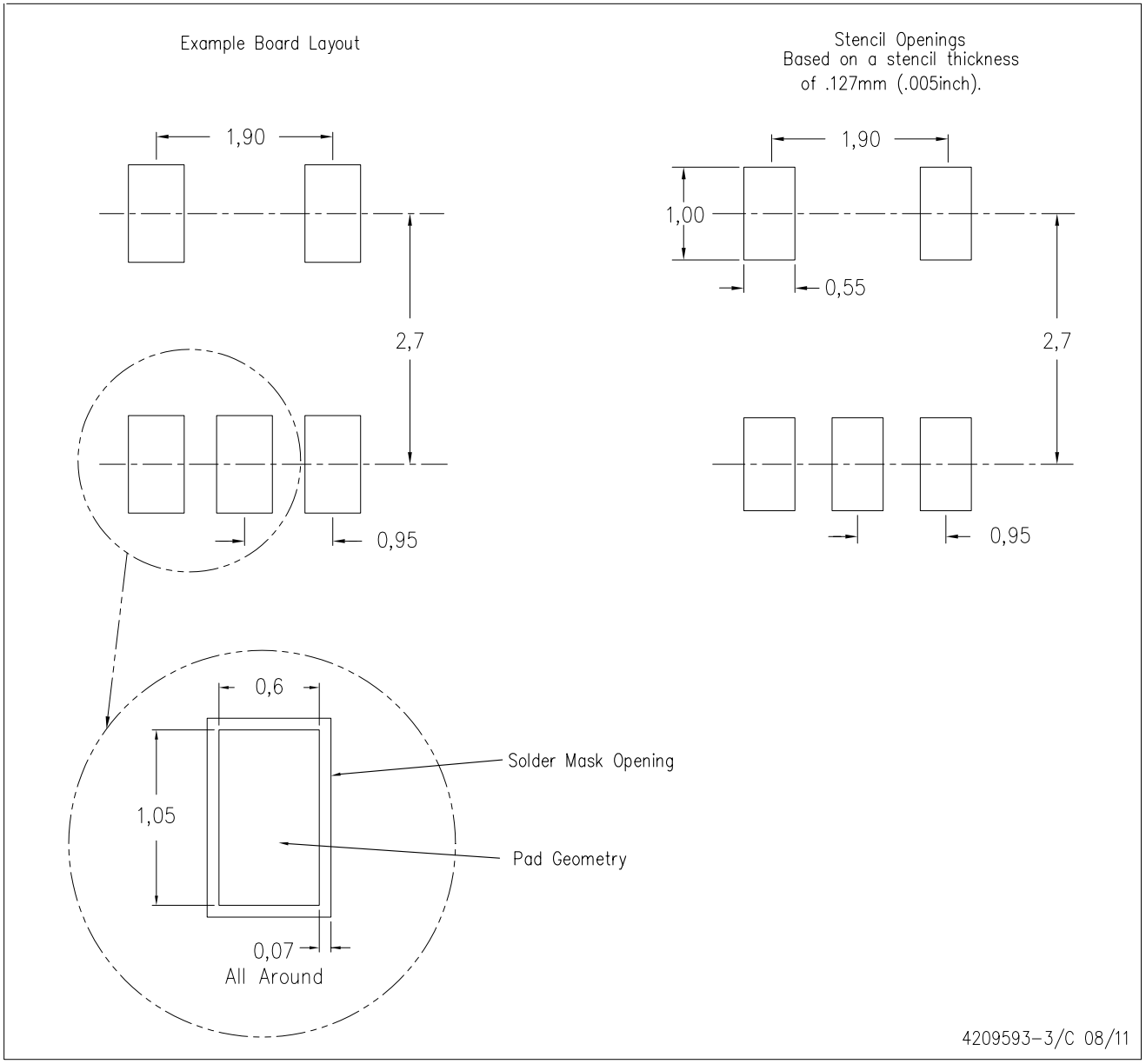
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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