OV8610 SINGLE-CHIP CMOS VGA COLOR DIGITAL CAMERA
OV8110 SINGLE-CHIP CMOS VGA B&W DIGITAL CAMERA

Description

The OV8610 (color) and OV8110 (black and white) CMOS Image sensors are single-chip video/imaging camera devices designed to provide a high level of functionality in a single, small-footprint package. The devices incorporate an 800 x 600 image array capable of operating at up to 60 frames per second. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions including exposure control, gamma, gain, white balance, color matrix, color saturation, hue control, windowing, and more, are programmable through the serial SCCB interface. The device can be programmed to provide image output in different 8-bit or 16-bit digital formats.

Features

- 480,000 pixels, 1/3" lens, SVGA/QSVGA format
- Data output formats include ITU-601 and ITU-656
- Choice of progressive scan/interlaced read
- Wide dynamic range, anti-blooming, zero smearing
- Electronic exposure/gain/white balance control
- Image Controls - brightness, contrast, gamma, saturation, sharpness, windowing, hue, etc.
- Internal & external synchronization
- Line exposure option
- 3.3-Volt operation, low power dissipation
  - < 30 mA active power at 30FPS with 10 mA load
  - < 10 µA in power-down mode
- Built in Gamma correction (0.45/0.55/1.00)
- SCCB programmable:
  - Color saturation, brightness, hue, white balance, exposure time, gain, etc.

Ordering Information

Product	Package	Description
OV8610	**48 LCC** **0.560 in^2**	**COLOR, SVGA, QSVGA, QCIF Digital, SCCB interface**
OV8110	**48 LCC** **0.560 in^2**	**SVGA, QSVGA, QCIF, Digital, SCCB interface**

Applications

. Cell Phone
. Digital Still Camera
. PC Multimedia
. PDAs
. Machine Vision

Key Specifications

Active Array Element (SVGA) (QSVGA)	800x600 (400x300)
Pixel Size	6.2µm x 6.2µm
Image Area	4.96mm x 3.72mm
Max Frames/Sec	Up to 120 FPS for QSVGA
Electronics Exposure	Up to 648:1 (for selected FPS)
Scan Mode	Progressive or Interlace
Gamma Correction	0.45/0.55/1.0
Min. Illumination (3000K)	OV8610 < 3 lux @ f1.2 OV8110 < 0.8 lux @ f1.2
S/N Ratio	> 48 dB (AGC off, Gamma=1)
FPN	< 0.03% V_{PP}
Dark Current	< .2 nA/cm^2
Dynamic Range	> 72 dB
Power Supply	3.0–3.6VDC
Power Requirements	< 30mA Active (w/10mA load) < 10µA Standby
Package	48 pin LCC

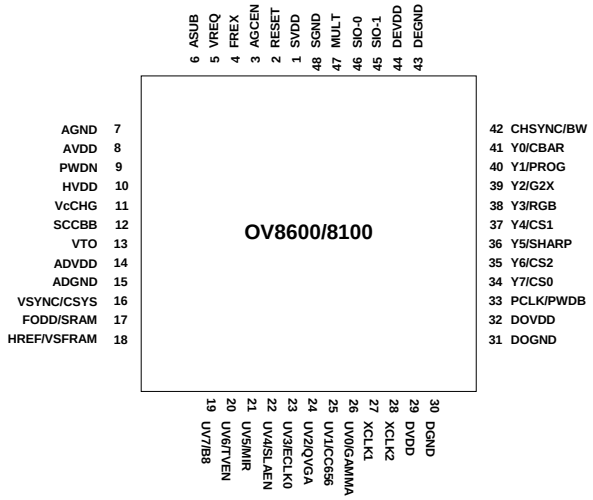


Figure 1. OV8610/OV8110 Pin Diagram

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Pin Description

Table 1. Pin Description

Pin No.	Name	Pin Type	Function/Description
01	SVDD	V_{IN}	Array power (+3.3VDC). Bypass to ground with a 0.1µF capacitor.
02	RESET	Function (Default=0)	Chip reset, active high. Resets all control registers to factory defaults.
03	AGCEN	Function (Default=0)	Automatic Gain Control (AGC) selection "0" – Disable AGC "1" – Enable AGC *Note: This function is disabled when OV8610/OV8110 sensor is configured in SCCB low mode. In SCCB low mode this pin is an SCCB chip select function.*
04	FREX	Function (Default=0)	Frame exposure control "0" – Disables frame exposure control "1" – Enables frame exposure control
05	VREQ	V_{REF} (1.5V)	Array reference. Connect to ground with a 0.1µF (min.) capacitor.
06	ASUB	V_{IN}	Analog substrate voltage
07	AGND	V_{IN}	Analog ground
08	AVDD	V_{IN}	Analog power supply (+3.3VDC). Bypass to ground with a 0.1µF capacitor.
09	PWDN	Function (Default=0)	Power-down mode selection. "0" – Operating mode "1" – Power-down mode
10	HVDD	V_{REF} (5.0V)	Charge pump out voltage. Doubler must be enabled.
11	V_CCHG	V_{REF} (2.7V)	Internal voltage reference. Bypass to ground with a 0.1µF capacitor.
12	SCCBB	Function (Default=0)	SCCB enable selection. "0" – Selects internal register setting control and enables SCCB interface "1" – Enables I/O input pin power on latch setting control
13	VTO	O	B&W CCIR analog composite signal output—for test purposes only
14	ADVDD	V_{IN}	Analog power supply (+3.3VDC). Bypass to ground with a 0.1µF capacitor.
15	ADGND	V_{IN}	Analog signal ground
16	VSYNC/CSYS	O	Vertical sync output. At power-up, read as CSYS.
17	FODD/SRAM	O	Field ID FODD output. At power-up, read as SRAM.
18	HREF/VSFRAM	O	HREF output. At power-up, read as VSFRAM
19	*UV7/B8	O	Bit 7 of U video component output. At power-up, sampled as B8.
20	*UV6/TVEN	O	Bit 6 of U video component output. At power-up, sampled as TVEN.
21	*UV5/MIR	O	Bit 5 of U video component output. At power-up, sampled as MIR.
22	*UV4/SLAEN	O	Bit 4 of U video component output. At power-up, sampled as SLAEN.
23	*UV3/ECLK0	O	Bit 3 of U video component output. At power-up, samples as ECLKO.
24	*UV2/QSVGA	O	Bit 2 of U video component output. At power-up, sampled as QSVGA.
25	*UV1/CC656	O	Bit 1 of U video component output. At power-up, sampled as CC656.
26	*UV0/GAMMA	O	Bit 0 of U video component output. At power-up, sampled as GAMMA.
27	XCLK1	I	Crystal clock input
28	XCLK2	O	Crystal clock output
29	DVDD	V_{IN}	Digital power supply (+3.3VDC). Bypass to ground with a 0.1µF capacitor.
30	DGND	V_{IN}	Digital ground
31	DOGND	V_{IN}	Digital interface output buffer ground
32	DOVDD	V_{IN}	Digital output buffer supply (+3.3VDC). Bypass to ground with a 0.1µF capacitor.
33	PCLK/PWDB	O	PCLK output. At power-up sampled as charge pump enable.
34	Y7	O	Bit 7 of Y video component output
35	Y6	O	Bit 6 of Y video component output
36	Y5/SHARP	O	Bit 5 of Y video component output. At power-up, sampled as SHARP.
37	Y4	O	Bit 4 of Y video component output

Pin No.	Name	Pin Type	Function/Description
38	Y3/RGB	O	Bit 3 of Y video component output. At power-up, sampled as RGB.
39	Y2/G2X	O	Bit 2 of Y video component output. At power-up, sampled as G2X.
40	Y1/PROG	O	Bit 1 of Y video component output. At power-up, samples as PROG
41	Y0/CBAR	O	Bit 0 of Y video component output. At power-up, sampled as CBAR.
42	CHSYNC/BW	O	CHSYNC output. At power-up, sampled as BW.
43	DEGND	V_{IN}	Decoder ground
44	DEVDD	V_{IN}	Decoder power supply (+3.3VDC). Bypass to ground with a 0.1µF capacitor.
45	SIO-1	I	SCCB serial interface clock input
46	SIO-0	I/O	SCCB serial interface data input and output
47	Reserved	Function (Default=0)	
48	SGND	V_{IN}	Array ground

** Note: Output is not available on the OV8110 sensor and one-port mode for OV8610.*

All I/O latch input pins are effective only when SCCB pin is high, otherwise all pin functions are regulated by the register settings.

Legend: (I=Input), (O=Output), (I/O=Bi-directional), (P=Power), (A=Analog)

Electrical and Mechanical Characteristics

Table 2. General Characteristics

Descriptions	Min	Max	Units
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 3. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
Supply					
V_{DD1}	Supply voltage (DEVDD, ADVDD, AVDD, DVDD, DOVDD)	3.6	3.3	3.0	V
I_{DD1}	Supply current (@ 30 fps and 3.3V digital I/O with 25pF plus ITTL loading on 16-bit data bus)	35	30		mA
I_{DD3}	Standby supply current	10	8		µA
Digital Inputs					
V_{IL}	Input voltage LOW	0.8			V
V_{IH}	Input voltage HIGH			2	V
C_{IN}	Input capacitance	10			PF
Digital Outputs (standard loading 25pF, 1.2KΩ to 3V)					
V_{OH}	Output voltage HIGH			2.4	V
V_{OL}	Output voltage LOW	0.6			V
SCCB Input					
V_{IL}	SIO-0 and SIO-1 (V_{DD2}=5V)	1.5		-0.5	V
V_{IH}	SIO-0 and SIO-1 (V_{DD2}=5V)	V_{DD}+0.5	3.3	3.0	V
V_{IL}	SIO-0 and SIO-1 (V_{DD2}=3V)	1	0	-0.5	V
V_{IH}	SIO-0 and SIO-1 (V_{DD2}=3V)	V_{DD}+0.5	3	2.5	V

Table 4. AC Characteristics (T_A=25°C, V_{DD}=3V)

Symbol	Descriptions	Max	Typ	Min	Units
RGB/YCrCb Output					
I_{SO}	Maximum sourcing current		15		mA
V_Y	DC level at zero signal Y_{PP} 100% amplitude (without sync) Sync amplitude		1.2 1 0.4		V
ADC Parameters					
B	Analog bandwidth		TBD		MHz
Φ_{DIFF}					
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB

Table 5. Timing Characteristics

Symbol	Descriptions	Max	Typ	Min	Units
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1)	40	20	10	MHz
t_r, t_f	Clock input rise/fall time	5			ns
	Clock input duty cycle	55	50	45	%
SCCB Timing (400Kbit/s)					
t_{BUF}	Bus free time between STOP and START			1.3	ms
$t_{HD:SAT}$	SIO-D change after START status			0.6	µs
t_{LOW}	SIO-D low period			1.3	µs
t_{HIGH}	SIO-D high period			0.6	µs
$t_{HD:DAT}$	Data hold time			0	µs
$t_{SU:DAT}$	Data setup time			0.1	µs
$t_{SU:STP}$	Setup time for STOP status			0.6	µs
Digital Timing					
t_{PCLK}	PCLK period (16-bit operation)		50		ns
t_{PCLK}	PCLK period (8-bit operation)		50		ns
t_r, t_f	PCLK rise/fall time	5			ns
t_{PDD}	PCLK to data valid	5			ns
t_{PHD}	PCLK to HREF delay	20	10	5	ns
Zoom Video Port AC Parameters					
t1	PCLK fall time	8		4	ns
t2	PCLK low time			21	ns
t3	PCLK rise time	8		4	ns
t4	PCLK high time			21	ns
t5	PCLK period			50	ns
t6	Y/UV/HREF setup time			5	ns
t7	Y/UV/HREF hold time			20	ns
t8	VSYNC setup/hold time to HREF			1	µs

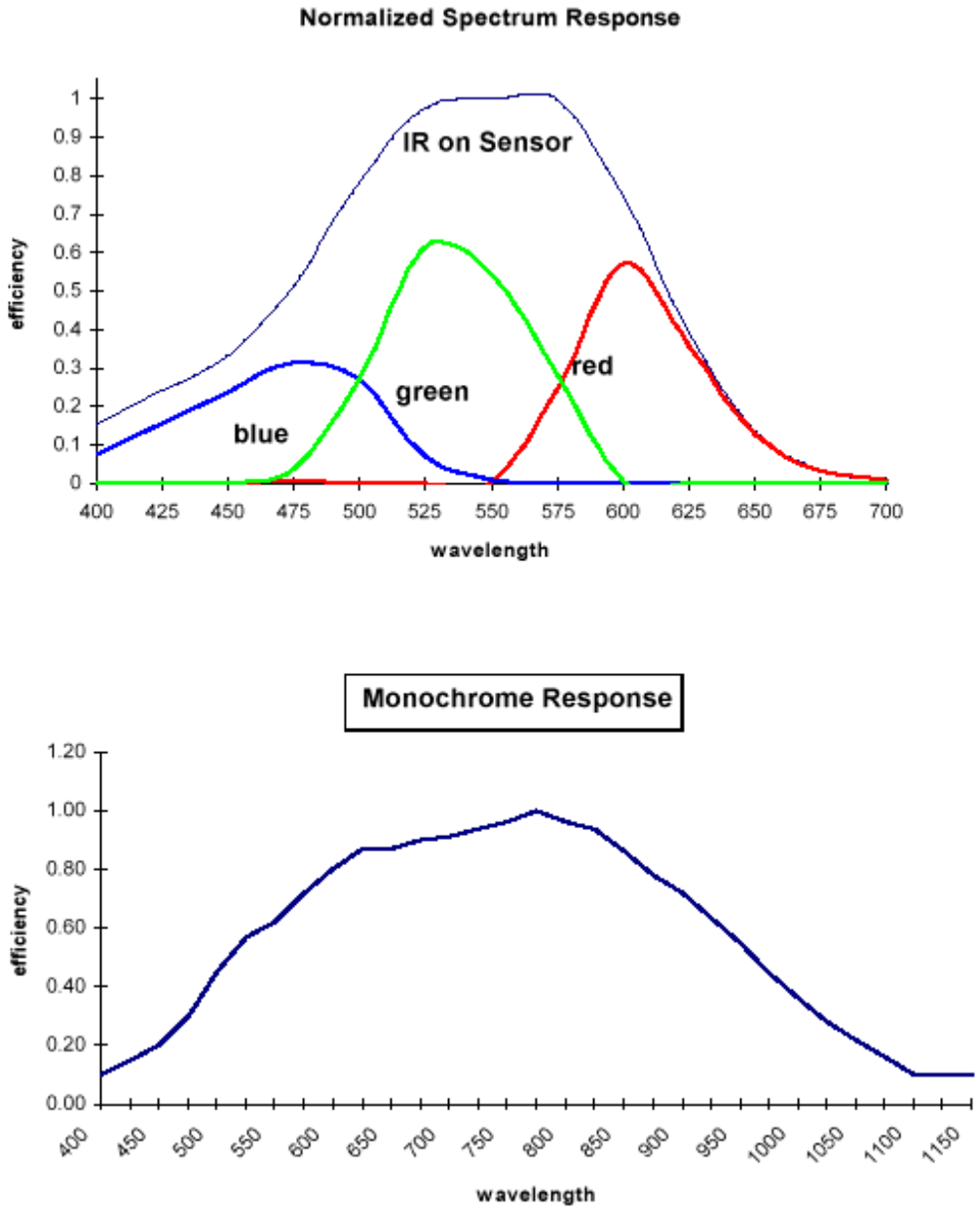


Figure 2. OV8610/8110 Light Response

Function Description

Overview

Referring to Figure 3 below, the OV8610/OV8110 sensor includes a 824 x 615 pixel image array, an analog signal processor, dual 10-bit A/D converters, analog video multiplexer, digital data formatter, video port, SCCB interface and control registers to control the timing block, exposure time, black level, white balance and a number of other parameters.

The OV8610/OV8110 sensor is a 1/3" CMOS imaging device. The sensor contains a total of 506,760 pixels (824x615). Its design is based on a field integration readout system with line-by-line transfer and an electronic rolling shutter with a synchronous pixel readout scheme. The color filter of the sensor consists of primary red, green, and blue filters arranged in the line-alternating Bayer pattern, RGRG/GBGB.

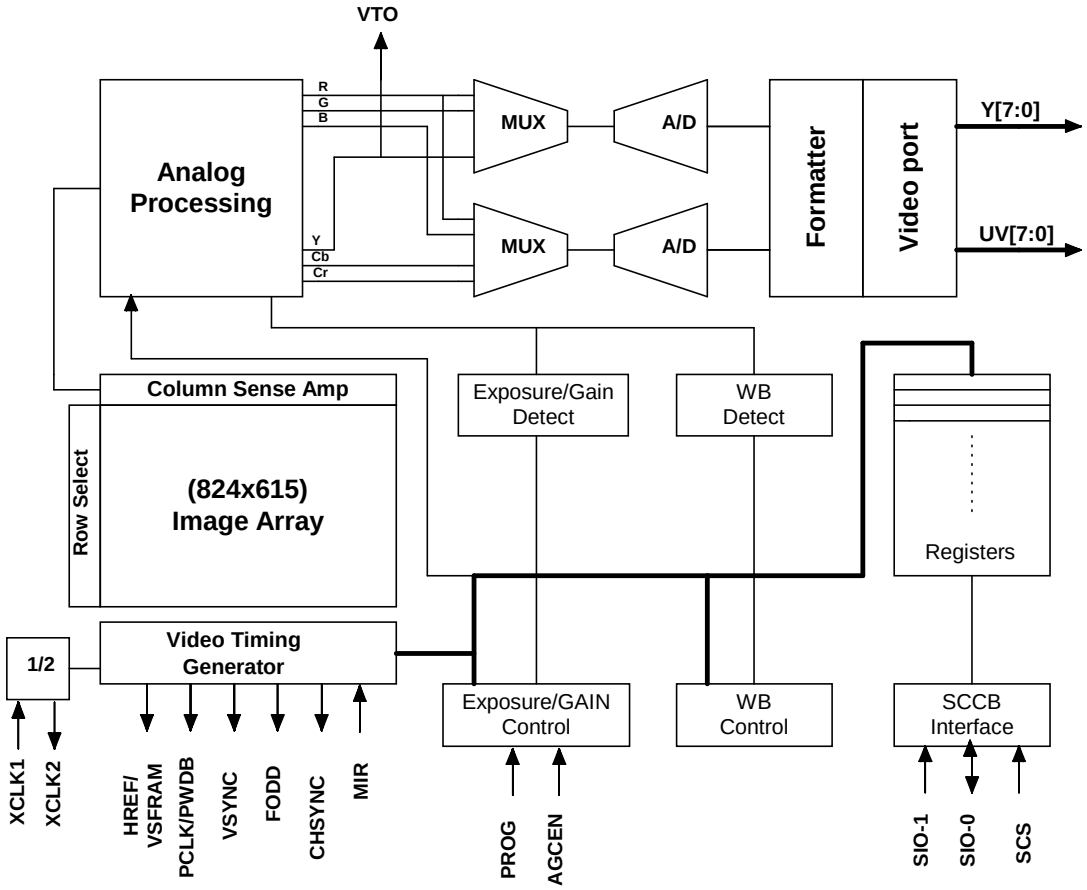


Figure 3. OV8610/OV8110 CMOS Image Sensor Block Diagram

Analog Processing Circuits

Overview

The image is captured by the 824 x 615 pixel image array and routed to the analog processing section where the majority of signal processing occurs. This block contains the circuitry that performs color separation, color correction, automatic gain control (AGC), gamma correction, color balance, black level calibration, "knee" smoothing, aperture correction, controls for picture luminance and chrominance, and hue control for color. The analog video signals are based on the following formula:

Y = 0.59G + 0.31R + 0.11B
U = R – Y
V = B – Y
Where R,G,B are the equivalent color components in each pixel.

YCrCb format is also supported, based on the formula below:

Y = 0.59G + 0.31R + 0.11B
Cr = 0.713 (R – Y)
Cb = 0.564 (B – Y)

The YcrCb or RGB data signal from the analog processing section is fed to two on-chip 10-bit analog-to-digital (A/D) converters: one for the Y/G channel and one shared by the CrCb/BR channels. The converted data stream is further conditioned in the digital formatter. The processed signal is delivered to the digital video port through the video multiplexer which routes the user-selected 8-, or 10-bit video data to the correct output pins.

The on-chip 10-bit A/D operates at up to 20 MHz, and is fully synchronous to the pixel rate. Actual conversion rate is related to the frame rate. A/D black-level calibration circuitry ensures:

- The black level of Y/RGB is normalized to a value of 16
- The peak white level is limited to 240
- CrCb black level is 128
- CrCb Peak/bottom is 240/16
- RGB raw data output range is 16/240
  (Note: Values 0 and 255 are reserved for sync flag)

Image Processing

The algorithm used for the electronic exposure control is based on the brightness of the full image. The exposure is optimized for a "normal" scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the automatic exposure control (AEC) white/black ratio may be adjusted to suit the needs of the application.

Additional on-chip functions include:

- AGC that provides a gain boost of up to 24dB
- White balance control that enables setting of proper color temperature and can be programmed for automatic or manual operation.
- Separate saturation, brightness, hue, and sharpness adjustments allow for further fine-tuning of the picture quality and characteristics.

The OV8610/OV8110 image sensor also provides control over the White Balance ratio for increasing/decreasing the image field Red/Blue component ratio. The sensor provides a default setting that may be sufficient for many applications.

Windowing

The windowing feature of the OV8610/OV8110 image sensors allows user-definable window sizing as required by the application. Window size setting (in pixels) ranges from 2 x 2 to 800 x 600, and can be positioned anywhere inside the 824 x 615 boundary. Note that modifying window size and/or position does not change frame or data rate. The OV8610 imager alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical region. The default output window is 800 x 600.

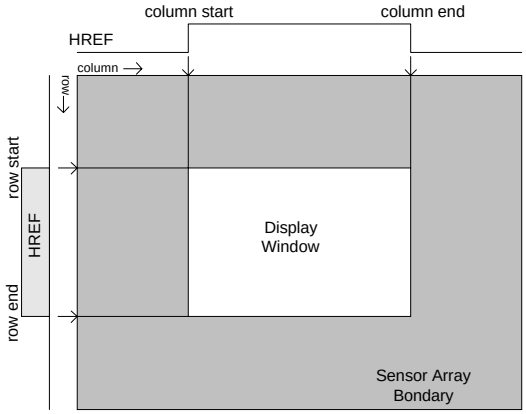
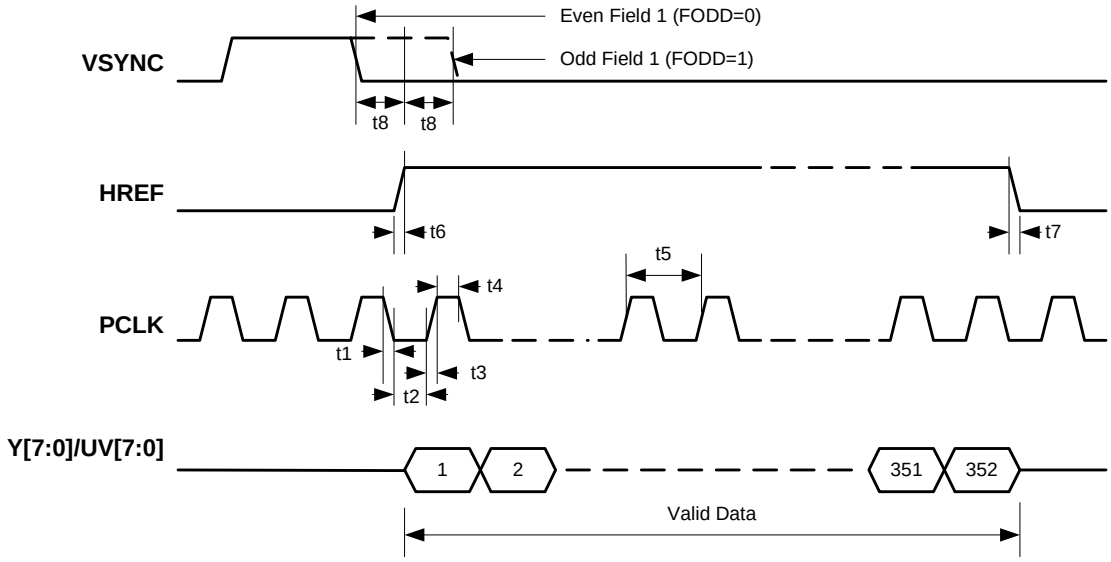


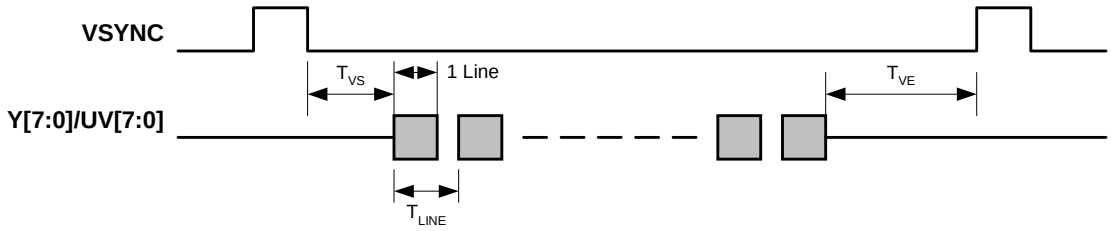
Figure 4. Windowing

Zoom Video Port (ZV)

The OV8610/OV8110 image sensor includes a Zoom Video (ZV) function that supports standard ZV port interface timing. Signals available include VSYNC, CHSYNC, PCLK and 16-bit data bus: Y[7:0] and UV[7:0]. The rising edge of PCLK clocks data into the ZV port. See Figure 5. Zoom Video Port Timing below.



Horizontal Timing



Vertical Timing

Figure 5. Zoom Video Port Timing

Note:

Zoom Video Port format output signal includes:

VSYNC: Vertical sync pulse.
HREF: Horizontal valid data output window.
PCLK: Pixel clock used to clock valid data and CHSYNC into Zoom V Port. Default frequency is 20MHz when use 20MHz as system clock plus 2X PLL implemented on chip. Rising edge of PCLK is used to clock the 16 Bit data.
Y[7:0]: 8 Bit luminance data bus.
UV[7:0]: 8 Bit chrominance data bus.

QSVGA

A QSVGA mode is available for applications where higher resolution image capture is not required. Only half of the pixel rate is required when programmed in same frame rate with sub-sampling method. If you keep the same pixel rate with skip method, the maximum frame rate is 120. Default resolution is 400 x 300 pixels and can be programmed for other resolutions. Refer to Table 11. QSVGA Digital Output Format (YUV beginning of line) and Table 12. RGB Data Format for further information.

QCIF

A QCIF mode is available for further resolution decrease. Two method used to get this mode, sub-sampling and skip. The first one can get better quality than the second one and the second approach can have higher frame rate. The maximum frame rate is 240 for QCIF. The default resolution is 200 x 150.

Video Output

The video output port of the OV8610/OV8110 image sensors provides a number of output format/standard options to suit many different application requirements. Table 6, Digital Output Format indicates the output formats available. These formats are user-programmable through the SCCB interface.

YUV Output

The OV8610/OV8110 supports ITU-656 and ITU-601 output formats, providing VSYNC, HREF, and PCLK as standard output video timing signals.

ITU-601/ITU-656

The OV8610/OV8110 imager supports both ITU-601 and ITU-656 output formats in the following configurations (See Table 7. 4:2:2 16-bit Format and Figure 6. Pixel Data Bus (YUV Output) for further details):

- 16-bit, 4:2:2 format

  (This mode complies with the 60/50 Hz ITU-601 timing standard. See Table 7. 4:2:2 16-bit Format*)*

- 8-bit data mode

  (In this mode, video information is output in Cb Y Cr Y order using the Y port only and running at twice the pixel rate during which the UV port is inactive. See Table 8. 4:2:2 8-bit Format*).*

The OV8610/OV8110 imager provides VSYNC, HREF, PCLK, FODD, and CHSYNC as standard video timing signals**.**

In ITU-656 modes, the OV8610/OV8110 imager asserts SAV (Start of Active Video) and EAV (End of Active Video) to indicate the beginning and the ending of the HREF window. As a result, SAV and EAV change with the active pixel window.

The OV8610/OV8110 imager offers flexibility in YUV output format. The device may be programmed to standard YUV 4:2:2. The device may also be configured to “swap” the UV sequence. When swapped, the UV channel output sequence in the 16-bit configuration becomes:

- V U V U···.

The 8-bit configuration becomes:

- V Y U Y···.

The third format available in the 8-bit configuration is the Y/UV sequence swap:

Y U Y V···.

RGB Raw Data Output

The OV8610/OV8110 imager can also be programmed to provide 8-bit RGB raw data output. The output sequence is matched to the OV8610 color filter pattern.

The video output appears in Y channel only and the UV channel is disabled in 8-bit RGB raw data. The output sequence is B G R G.

B/W Output

The single-chip camera can be configured for use as a black and white image device. The vertical resolution is higher than in color mode. Video data output is provided at the Y port and the UV port is tri-stated. The data (Y/RGB) rate is equivalent to 16-bit in color mode.

The MSB and LSB of Y/UV or RGB output can be reversed. Y7 is MSB and Y0 is LSB in the default setting. Y7 becomes LSB and Y0 becomes MSB in the reverse order configuration. Y2-Y6 is also reversed appropriately.

Table 6. Digital Output Format

Resolution	Pixel Clock	800 X 600	400 X 300	200 X 150
YUV 4:2:2	16-bit	Y	Y	Y
	8-bit	Y	Y	Y
	ITU-656	Y	Y	Y
RGB	16-bit	Y	Y	Y
	8-bit	Y	Y	Y
	ITU-656[1]	Y	Y	Y
Y/UV swap[2]	16-bit			
	8-bit	Y	Y	Y
U/V swap	YUV[3]	Y	Y	Y
	RGB[4]	Y	Y	Y
YG	16-bit	Y	Y	Y
	8-bit			
Single-Line RGB	16-bit			
Raw Data	8-bit	Y	Y	Y
MSB/LSB swap		Y	Y	Y

Note:

("Y" indicates mode/combination is supported by OV8610/OV8110)

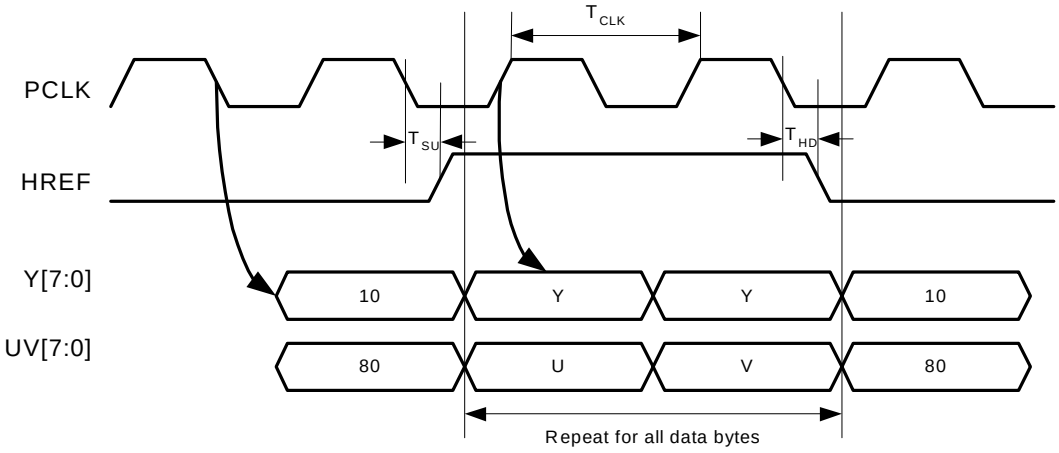
1. Output is 8-bit in RGB ITU-656 format. SAV and EAV are inserted at the beginning and ending of HREF, which synchronize the acquisition of VSYNC and HSYNC. 8-bit data bus configuration (without VSYNC and CHSYNC) can provide timing and data in this format.
2. Y/UV swap is valid in 8-bit only. Y channel output sequence is Y U Y V ···
3. U/V swap means UV channel output sequence swaps in YUV format, i.e., V U V U ··· for 16 bit and V Y U Y ··· for 8-bit.
4. U/V swap means neighbor row B R output sequence swap in RGB format. Refer to RGB raw data output format for further details.

Table 7. 4:2:2 16-bit Format

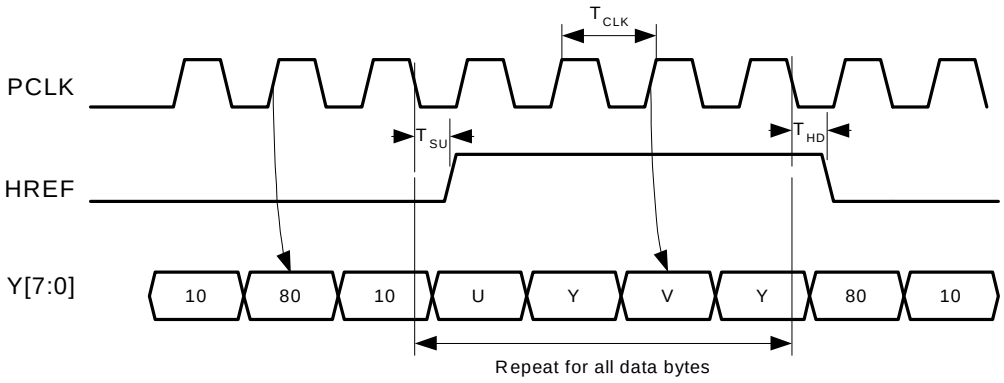
Data Bus	Pixel Byte Sequence					
Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	UV7	UV7	UV7	UV7	UV7	UV7
UV6	UV6	UV6	UV6	UV6	UV6	UV6
UV5	UV5	UV5	UV5	UV5	UV5	UV5
UV4	UV4	UV4	UV4	UV4	UV4	UV4
UV3	UV3	UV3	UV3	UV3	UV3	UV3
UV2	UV2	UV2	UV2	UV2	UV2	UV2
UV1	UV1	UV1	UV1	UV1	UV1	UV1
UV0	UV0	UV0	UV0	UV0	UV0	UV0
Y Frame	0	1	2	3	4	5
UV Frame	01		23		45	

Table 8. 4:2:2 8-bit Format

Data Bus	Pixel Byte Sequence							
Y7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
Y6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
Y5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
Y4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
Y3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
Y2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
Y1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
Y0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
Y Frame	0		1		2		3	
UV Frame	0 1				2 3			



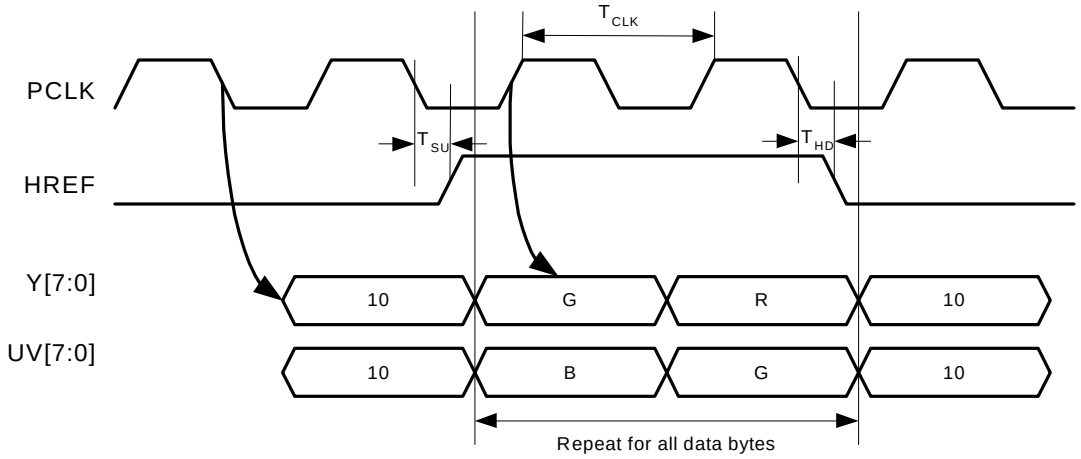
Pixel Data 16-bit Timing
(PCLK rising edge latches data bus)



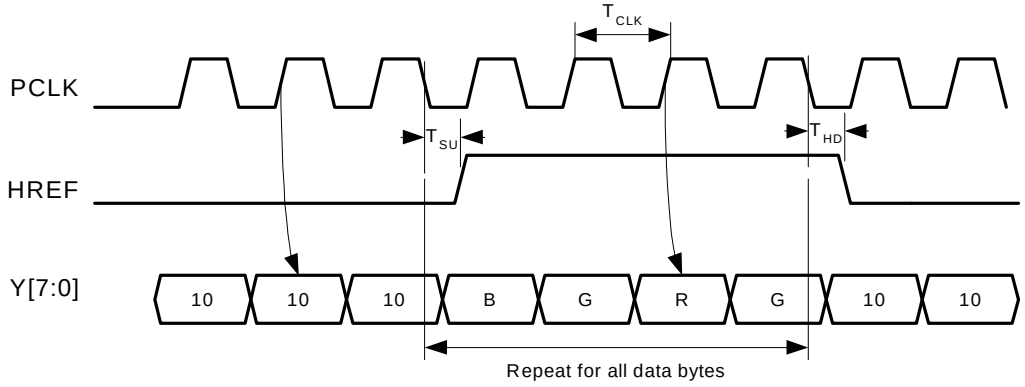
Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

Note: *T_{CLK} is pixel clock period.. T_{CLK}=50ns for 16-bit output and T_{CLK}=25ns for 8-bit output if the system clock is 20MHz with on chip 2X PLL . T_{SU} is the setup time of HREF. The maximum is 15ns. T_{HD} is the hold time of HREF. The maximum is 15ns.*

Figure 6. Pixel Data Bus (YUV Output)



Pixel Data 16-bit Timing
(PCLK rising edge latches data bus)



Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

Note: *T_{CLK} is pixel clock period.. T_{CLK}=50ns for 16-bit output and T_{CLK}=25ns for 8-bit output if the system clock is 20MHz with on chip 2X PLL. T_{SU} is the setup time of HREF. The maximum is 15ns. T_{HD} is the hold time of HREF. The maximum is 15ns.*

Figure 7. Pixel Data Bus (RGB Output)

The default U/UV channel output port relation before an MSB/LSB swap:

Table 9. Default Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The relation after an MSB/LSB swap changes to:

Table 10. Swapped MSB/LSB Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7

Table 11. QSVGA Digital Output Format (YUV beginning of line)

Pixel #	1	2	3	4	5	6	7	8
Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
UV	U0, V0	U1, V1	U2, V2	U3, V3	U4, V4	U5, V5	U6, V6	U7, V7

- Y channel output U2Y2V3 Y3U6 Y6V7 Y7 U10Y10 V11Y11 ···
- Every other (total 400) pixels and every other line (total 300 lines) is output in each frame.

Table 12. RGB Data Format

The pixel pattern is as following:

R\C	1	2	3	4	···	821	822	823	824
1	$B_{1,1}$	$G_{1,2}$	$B_{1,3}$	$G_{1,4}$		$B_{1,821}$	$G_{1,821}$	$B_{1,823}$	$G_{1,824}$
2	$G_{2,1}$	$R_{2,2}$	$G_{2,3}$	$R_{2,4}$		$G_{2,821}$	$R_{2,821}$	$G_{2,823}$	$R_{2,824}$
3	$B_{3,1}$	$G_{3,2}$	$B_{3,3}$	$G_{3,4}$		$B_{3,821}$	$G_{3,642}$	$B_{3,823}$	$G_{3,824}$
4	$G_{4,1}$	$R_{4,2}$	$G_{4,3}$	$R_{4,4}$		$G_{4,821}$	$R_{4,642}$	$G_{4,823}$	$R_{4,824}$
613	$B_{613,1}$	$G_{613,2}$	$B_{613,3}$	$G_{613,4}$		$B_{613,821}$	$G_{613,822}$	$B_{613,823}$	$G_{613,824}$
614	$G_{614,1}$	$R_{614,2}$	$G_{614,3}$	$R_{614,4}$		$G_{614,821}$	$R_{614,822}$	$G_{614,823}$	$R_{614,824}$

- RGB full resolution progressive scan mode. (Total 614 HREFs)
  - 1st HREF Y channel output unstable data
  - 2nd HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{13}G_{23}$ R_{24} G_{14}···
  - 3rd HREF Y channel output B_{31} G_{21} R_{22} G_{32} B_{33} G_{23} R_{24} G_{34} ···
  - Every line of data is output twice for each frame.
  - PCLK is double
- RGB QSVGA resolution progressive scan mode. (Total 300 HREFs)
  - 1st HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{15}G_{25}$ R_{26} G_{16}···
  - 2nd HREF Y channel output $B_{31}G_{41}$ R_{42} G_{32} $B_{35}G_{45}$ R_{46} G_{36}···
  - 3rd HREF Y channel output B_{51} G_{61} R_{62} G_{52} B_{55} G_{65} R_{66} G_{56} ···
  - Every line of data is output once for each frame.
  - Max frame rate is 60FPS
- RGB full resolution raw data one line format. (Total 600 HREFs)
  - 1st HREF Y channel output B_{11} G_{12} B_{13} G_{14} ···
  - 2nd HREF Y channel output G_{21} R_{22} G_{23} R_{24} ···
  - 3rd HREF Y channel output B_{31} G_{32} B_{33} G_{34} ···
  - PCLK rising edge latch data bus.
- RGB QSVGA resolution raw data one line format. (Total 246 HREFs)
  - 1st HREF Y channel output B_{11} G_{12} B_{15} G_{16} ···
  - 2nd HREF Y channel output G_{21} R_{22} G_{25} R_{26} ···
  - 3rd HREF Y channel output B_{51} G_{52} B_{55} G_{56} ···
  - 3rd HREF Y channel output G_{61} R_{62} G_{65} R_{66} ···
  - PCLK rising edge latch data bus.

Frame Exposure Mode

OV8610/OV8110 supports frame exposure mode when FREX is set high. PWDN is asserted by an external master device to set exposure time at this mode. The pixel array is quickly pre-charged when PWDN is set to "1". OV8610/OV8110 captures the image in the time period when PWDN remains high. The video data stream is delivered to output port in a line-by-line manner after PWDN switches to "0".

It should be noted that PWDN must remain high long enough to ensure the entire image array has been pre-charged.

Reset

OV8610/8110 includes a RESET pin (pin 2) that forces a complete hardware reset when it is pulled high (VCC). OV8610/8110 clears all registers and resets to their default values when a hardware reset occurs. Reset can also be initiated through the SCCB interface.

Power Down Mode

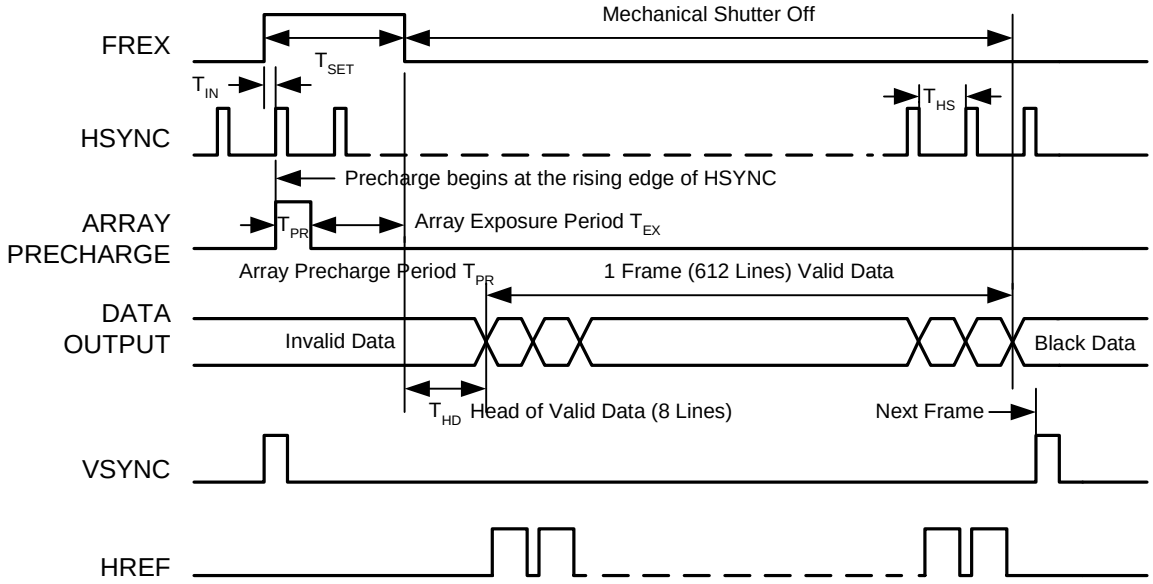
Two methods are available to place OV8610 into power-down mode: hardware power-down and SCCB software power-down.

To initiate hardware power-down, the PWDN pin (9) must be tied to high (+3.3VDC). When this occurs, the OV8610 internal device clock is halted and all internal counters are reset. The current draw is less than 10µA in this standby mode.

Executing a software power-down through the SCCB interface suspends internal circuit activity, but does not halt the device clock. The current requirements drop to less than 1mA in this mode.

Configure OV8610/OV8110

The method to configure OV8610/OV8110 is to use its on-chip SCCB register programming capability. The SCCB interface provides access to all of the device's programmable internal registers.



Note:

- *T_{PR}=824 x 4 x T_{CLK} or T_{PR}=858xT_{clk} depends on mode selecton. T_{CLK} is internal pixel period. T_{CLK}=50ns if the system clock is 20MHz . T_{CLK} will increase with the clock divider CLK[5:0].*
- *T_{EX} is array exposure time which is decided by external master device.*
- *T_{IN} is uncertain time due to the using of HSYNC rising edge to synchronize FREX. T_{IN} < T_{HS}.*
- *There are 8 lines data output before valid data after FREX=0. T_{HD}=4 THS. Valid data is output when HREF=1.*
- *T_{SET}=T_{IN} + T_{PR} + T_{EX}. T_{SET} > T_{PR} + T_{IN}. The exposure time setting resolution is T_{HS} (one line) due to the uncertainty of T_{IN}.*

Figure 8. Frame Exposure Timing

Register Set

The table below provides a list and description of available SCCB registers contained in the OV8610/8110 image sensor.

Table 13. SCCB Registers

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
00	GAIN	00	RW	AGC gain control GC[7:6] – Unimplemented. GC[5:0] – The current gain setting. *This register is updated automatically if AGC is enabled. The internal controller stores the optimal gain value in this register. The current value is stored in this register if AGC is not enabled.*
01	BLUE	80	RW	Blue gain control BLU[7:0] – blue channel gain balance value. “FFh” is highest and “00h” is lowest ***Note:*** *This function is not available on the OV8110 image sensor.*
02	RED	80	RW	Red gain control RED[7:0] – red channel balance value. “FFh” is highest and “00h” is lowest ***Note:*** *This function is not available on the OV8110 image sensor.*
03	SAT	80	RW	Color saturation control SAT[7:4] – Saturation adjustment. “F8h” is highest and “00h” is lowest. SAT[3:0] – Unimplemented. ***Note:*** *This function is not available on the OV8110 image sensor.*
04	HUE	10	RW	Color hue control HUE[7:6] – Unimplemented. HUE[5] – Enable HUE control HUE[4:0] – HUE control, range -30°~30°
05	Rvsd	xx	-	Reserved
06	BRT	80	RW	Brightness control BRT[7:0] – Brightness adjustment. “FFh” is highest and “00h” is lowest.
07-09	Rsvd 07-09	xx	–	Reserved
0A	PID	86	R	Product ID number read only
0B	VER	B0	R	Product version number, read only
0C	ABLU	20	RW	White balance background: Blue channel ABLU[7:6] – Rsvd ABLU[5:0] - White balance blue ratio adjustment, “3Fh” is most blue. ***Note:*** *This function is not available on the OV8110 image sensor.*
0D	ARED	20	RW	White balance background: Red channel ARED[7:6] – Rsvd ARED[4:0] - White balance red ratio adjustment, “3Fh” is most red. ***Note:*** *This function is not available on the OV8110 image sensor.*
0E-0F	Rsvd 0E-0F	xx	-	Reserved
10	AEC	A2	RW	Automatic exposure control AEC[7:0] - Set exposure time $T_{EX} = 4 \times T_{LINE} \times AEC[7:0]$

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
11	CLKRC	00	RW	Clock rate control CLKRC[7:6] – Sync output polarity selection "00" – HSYNC=Neg, CHSYNC=Neg, VSYNC=Pos "01" – HSYNC=Neg, CHSYNC=Neg, VSYNC=Neg "10" – HSYNC=Pos, CHSYNC=Neg, VSYNC=Pos "11" – HSYNC=Pos, CHSYNC=Pos, VSYNC=Pos CLKRC[5:0] – Clock pre-scalar CLK = (MAIN_CLOCK / ((CLKRC[5:0] + 1) × 2)) / n Where n=1 if register [15], COMD[5] is set to "1" and n=2 otherwise.
12	COMA	24	RW	Common control A COMA[7] – SRST, "1" initiates soft reset. All registers are set to default values and chip is reset to known state and resumes normal operation. COMA[6] – MIRR, "1" selects mirror image COMA[5] – AGCEN, "1" enables AGC, COMA[4] – Digital output format, "0" selects 8-bit: U Y V Y U Y V Y "1" selects 8-bit: Y U Y V Y U Y V COMA[3] – Select video data output: "1" - select RGB, "0" - select YCrCb COMA[2] – Auto white balance "1" - Enable AWB, "0" - Disable AWB COMA[1] – Color bar test pattern: "1" - Enable color bar test pattern COMA[0] – ADC BLC method : "1" – precise, "0" more stable but less precise
13	COMB	01	RW	Common control B COMB[7] – VSYNC output selection, "1" – no VSYNC when no valid data, "0" – VSYCN always output. COMB[6] – AGC/AWB register SCCB update option. "1" – updated immediately after SCCB input, "0" – updated after VSYNC COMB[5] - Select data format. "1" - select 8-bit format, Y/CrCb and RGB is multiplexed to 8-bit Y bus, UV bus is tri-stated, "0" - select 16-bit format COMB[4] – "1" - enable digital output in ITU-656 format COMB[3] – CHSYNC output. "0" - horizontal sync, "1" - composite sync COMB[2] – "1" – Tri-state Y and UV bus. "0" - enable both bus COMB[1] – "1" - Initiate single frame transfer. COMB[0] – "1" - Enable auto adjust mode. ***Note:*** *COMB[5] is not programmable on the OV8110 image sensor.*
14	COMC	00	RW	Common control C COMC[7] – AWB threshold selection. "1" - More stable and less accurate, "0" – more accurate but less stable. COMC[6] – UV option. "1" – UV always zero. "0" – normal color mode COMC[5] – QSVGA digital output format selection. "1" - 400x300; "0" - 800x 600. COMC[4] – Field/Frame vertical sync output in VSYNC port selection: "1" - frame sync, only ODD field vertical sync; "0" - field vertical sync, effect in Interlaced mode COMC[3] – HREF polarity selection: "0" - HREF positive effective, "1" - HREF negative. COMC[2] – gamma selection: "1" - RGB Gamma on ; "0" - RGB gamma is 1. COMC[1:0] – reserved

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
15	COMD	01	RW	Common Control D COMD[7] – ADC clock 50% duty cycle selection. “1” – 50% duty cycle, “0” – non 50%. COMD[6] – PCLK polarity selection. “0” - OV8610/OV8110 output data at PCLK falling edge and data bus will be stable at PCLK rising edge; “1” - rising edge output data and stable at PCLK falling edge. COMD[5] – Digital 2x PLL disable. “1” – disable. “0” – enable. COMD[4] – Array vertical 2nd stage skip mode enable. Frame rate will double and only effective at progressive scan and 1st stage sub-sampling disable. COMD[3] – AGCEN pin option. “1” – AGCEN as data output enable/disable pin control, “0” – normal AGCEN pin. COMD[2] – Reserved COMD[1] – Enable NTSC timing. Only part of full resolution output. COMD[0] – U V digital output sequence exchange control. 1 - UV UV ··· for 16-bit, U Y V Y ··· for 8-bit; 0 - V U V U ··· for 16-bit and V Y U Y ··· for 8-bit. ***Note:*** *COMD[0] is not programmable on the OV8110 image sensor.*
16	FSD	03	RW	Field slot division FSD[7:2] – Field interval selection. It has functional in EVEN and ODD mode defined by FSD[1:0]. It is disabled in OFF and FRAME mode. The purpose of FSD[7:2] is to divide the video signal into programmed number of time slots, and allows HREF to be active only one field in every FSD[7:2] fields. It does not affect the video data or pixel rate. FSD[7:2]=1 outputs one field every field. FSD[7:2]=2 outputs one field every two fields. All other fields output black reference. FSD[1:0] – field mode selection. Each frame consists of two fields: Odd and Even, FSD[1:0] define the assertion of HREF in relation to the two fields. “00” – OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register 13) “01” – Interlace mode: ODD mode; HREF is asserted in odd field only. Progressive mode: HREF is asserted in frame according FD[7:2] “10” – Interlace mode: EVEN mode; HREF is asserted in even field only. Progressive mode: HREF is asserted in frame according FD[7:2]. “11” – FRAME mode; HREF is asserted in both odd field and even field. FSD[7:2] disabled.
17	HREFST	38	RW	Horizontal HREF start HS[7:0] – selects the starting point of HREF window, each LSB represents four pixels for SVGA resolution mode, two pixels for QVGA resolution mode, one pixel for QCIF mode. This value is set based on an internal column counter. The default value corresponds to 800 horizontal windows. Maximum window size is 824. HS[7:0] should be less than HE[7:0].
18	HREFEND	EA	RW	Horizontal HREF end HE[7:0] – selects the ending point of HREF window, each LSB represents four pixels for full resolution and two pixels for QSVGA resolution, one pixel for QCIF mode. This value is set based on an internal column counter, the default value corresponds to the last available pixel. HE[7:0] should be larger than HS[7:0]. See window description below.
19	VSTRT	03	RW	Vertical line start VS[7:0] – selects the starting row of vertical window, in full resolution mode, each LSB represents 2 scan line in one field for Interlaced Scan Mode, 4 scan line in one frame for Progressive Scan Mode. In QSVGA mode, each LSB represents 1 scan line in one field for Interlaced Mode, 2 scan line in one frame for Progressive Scan Mode. See window description below. Min. is [02], max. is [98] and should less than VE[7:0].

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
1A	VEND	92	RW	Vertical line end VE[7:0] – selects the ending row of vertical window, in full resolution mode, each LSB represents 2 scan line in one field for Interlaced Scan Mode, 4 scan line in one frame for Progressive Scan Mode. In QSVGA mode, each LSB represents 1 scan line in one field for interlaced Mode, 2 scan line in one frame for Progressive Scan Mode. See window description below. Min. is [03], max. is [98] and should larger than VS[7:0].
1B	PSHFT	00	RW	Pixel shift PS[7:0] – to provide a way to fine tune the output timing of the pixel data relative to that of HREF, it physically shifts the video data output time late in unit of pixel clock. This function is different from changing the size of the window as defined by HS[7:0] and HE[7:0] in registers 17 and 18. It just delays the output pixels relative tp HREF and does not change the window size. The highest number is "FF" and the maximum shift number is delay 256 pixels.
1C	MIDH	7F	R	Manufacture ID byte: High MIDH[7:0] – read only, always returns "7F" as manufacturer's ID no.
1D	MIDL	A2	R	Manufacture ID byte: Low MIDL[7:0] – read only, always returns "A2" as manufacturer's ID no.
1E-1F	Rsvd 1E-1F	xx	RW	Reserved
20	COME	00	RW	Common control E COME[7] – Reserved COME[6] – Enables Field/Frame luminance average value calculations. Value is stored in Reg. [7C], AVG [7:0]. COME[5] – PCLK output option. "1" enables PCLK output during Sleep Mode. "0" disables PCLK during Sleep Mode. COME[4] – "1" Aperture correction enable. Correction strength and threshold value will be decided by COMF[7] ~ COMF[4]. COME[3] – AWB smart mode enable. 1 – do not count pixels that their luminance level are not in the range defined in register [66]. 0 - count all pixels to get AWB result. Valid only when COMB[0]=1 and COMA[2]=1. COME[2] – Aperture correction mode selection. "1" - Correction only when luminance average level larger than preset level. "0" – Correction always same in whole range luminance. COME[1] – AWB fast/slow mode selection. "1" - AWB is always fast mode, that is register [01] and [02] is changed every field. "0" AWB is slow mode, [01] and [02] change every 16/ 64 field decided by COMK[1]. When AWB enable, COMA[2]=1, AWB is working as fast mode until it reaches stable, than as slow mode. COME[0] – Digital output driver capability increase selection: "1" Double digital output driver current; "0" low output driver current status. ***Note:*** *COME[3] and COME[1] are not programmable on the OV8110 image sensor.*
21	YOFF	80	RW	Y channel offset adjustment YOFF[7] – Offset adjustment direction 0 - Add Y[6:0]; 1 -Subtract Y[6:0]. YOFF[6:0] –Y channel digital output offset adjustment. Range: +127 ~ -127. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through SCCB has no effect. COMG[2]=1, Y channel offset adjustment will use the stored value which can be changed through SCCB. This register has no effect to ADC output data if COMF[1]=0. If output RGB raw data, this register will adjust G channel data.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
22	UOFF	80	RW	U Channel offset adjustment UOFF[7] – Offset adjustment direction: 0 - Add U[6:0]; 1 - Subtract U[6:0]. UOFF[6:0] – U channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through SCCB has no effect. COMG[2]=1, U channel offset adjustment will use the stored value which can be changed through SCCB. This register has no effect to ADC output data if COMF[1]=1. If output RGB raw data, this register will adjust B channel data. ***Note:*** *This function is not available on the OV8110 image sensor.*
23	CLKC	04	RW	Oscillator circuit and common mode control CLKC[7:6] – Select different crystal circuit power level (“11” = minimum). CLKC[5] – ADC current control, “1” – half current, “0” full current. CLKC[4] – Output data polarity selection. “1” – negative, “0” – positive. CLKC[3] – Horizontal array skip mode. “1” – only read out half of horizontal pixel (400) and frame rate will double. “0” – full pixel read out CLKC[2] – Vertical array 1st stage skip mode. “1” – only read out half of vertical lines (200) and frame rate will double. CLKC[1] – System clock output selection. “1” half frequency of system clock, “0” – system clock. Only effective when FODD is set to output system clock. CLKC[0] – Aperture correction mode selection. “1” enable threshold relative to current gain faction. “0” – disable this function.
24	AEW	33	RW	Automatic exposure control: Bright pixel ratio adjustment AEW[7:0] – Used as calculate bright pixel ratio. OV8610/OV8110 AEC algorithm is count whole field bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is on the range of the ratio defined by the register [24] and [25], image stable. This register is used to define bright pixel ratio, default is 25%, each LSB represent step: 1.3% for interlace and 0.7% for progressive scan. Change range is: [01] ~ [65]; Increase AEW[7:0] will increase bright pixel ratio. For same light condition, the image brightness will increase if AEW[7:0] increase. ***Note:*** *AEW[7:0] must combine with register [25] AEB[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] > [65].*
25	AEB	97	RW	Automatic Exposure Control: Black pixel ratio adjustment AEB[7:0] – used as calculate black pixel ratio. OV8610/OV8110 AEC algorithm is count whole field/ frame bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is in the range of the ratio defined by the register [24] and [25], image stable. This register is used to define black pixel ratio, default is 75%, each LSB represent step: 1.3% for interlace and 0.7 for progressive scan. Change range is: [01] ~ [65]; Increase AEB[7:0] will increase black pixel ratio. For same light condition, the image brightness will decrease if AEB[7:0] increase. ***Note:*** *AEB[7:0] must e combined with register [24] AEW[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] > [65].*

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
26	COMF	B0	RW	Common control F COMF[7:6] – Aperture correction threshold selection. Range is 1% to 6.4% of difference of neighbor pixel luminance. COMF[5:4] – Aperture correction strength selection. Range is 0 to 200% of difference of neighbor pixel luminance. COMF[3] – Reserved. COMF[2] – Digital data MSB/LSB swap. “1” LSB→bit7, MSB→bit0; “0” normal. COMF[1] – “1” digital offset adjustment enable. “0” disable. COMF[0] – “1” Output first 4/8 line black level before valid data output according Interlace/Progressive scan mode. HREF number will increase 4/8 lines relatively. “0” no black level output.
27	COMG	A0	RW	Common control G COMG[7:6] – reserved COMG[5] – Select smart AWB algorithm control condition. “1” – if strong color component is more than 60%, AWB stop. “0” – 40%. COMG[4] – reserved. COMG[3] – Enable ADC black level calibration offset define by register [78]~[7A]. COMG[2] – “1” digital offset adjustment manually mode enable. Digital data will be add/subtract a value defined by register [21], [22] and [2E], the contents are programmed through SCCB. “0” - digital data will be added/subtract a value defined by register [21], [22] and [2E], which are updated by internal circuit. COMG[1] – Digital output full range selection. OV8610/OV8110 default output data range is [10] - [F0]. The output range changes to [01] - [FE] with signal overshoot and undershoot level if COMG[1]=1. COMG[0] – SRAM interface on/off. “1”=enabled, “0” = disabled
28	COMH	01	RW	Common control H COMH[7] – “1” selects one-line RGB raw data output format, “0” selects normal two-line RGB raw data output. COMH[6] – “1” enables black/white mode. The vertical resolution will be higher than color mode when the imager works as B/W mode. OV8610/OV8110 outputs data from Y port. UV port will be tri-state. COMB[5] and COMB[4] will be set to “0”. “0” =normal color mode. COMH[5] – Progressive scan mode selection. “0” – Interlace, “1” Progressive. COMH[4] – Freeze AEC/AGC value, effective only at COMB[0]=1. “1” - register [00] and [10] will not be updated and hold latest value. “0” - AEC/AGC normal working status. COMH[3] – AGC disable. “1” - when COMB[0]=1 and COMA[5]=1, internal circuit will not update register [00], register [00] will kept latest updated value. “0” - when COMB[0]=1 and COMA[5]=1, register [00] will be updated by internal algorithm. COMH[2] – RGB raw data output YG format: “1” - Y channel G, UV channel B R; “0” - Y channel: G R G R ···, UV channel B G B G ··· COMH[1] – Gain control bit. “1” channel gain increases 6dB. “0” no change to the channel gain. COMH[0] – Change AGCEN input pin to FSIN input when this resister is “1”. ***Note:*** *COMH[2] is not programmable on the OV8110 image sensor.*

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
29	COMI	00	RW	Common control I COMI[7] – AEC disable. “1” If COMB[0]=1, AEC stop and register [10] value will be held at last AEC value and not be updated by internal circuit. “0” - if COMB[0]=1, register [10] value will be updated by internal circuit COMI[6] – Slave mode selection. “1” slave mode, use external SYNC and VSYNC; “0” master mode. COMI[5] – ADC data latch 10ns delay option. COMI[4] – Reserved COMI[3] – Central 1/4 image area rather whole image used to calculate AEC/AGC. “0” use whole image area to calculate AEC/AGC. COMI[2] – reserved COMI[1:0] – Version flag. For version A, value is [00], these two bits are read only.
2A	FRARH	84	RW	Frame rate adjust high FRARH[7] – Frame rate adjustment enable bit. “1” Enable. FRARH[6:5] – Highest 2 bit of frame rate adjust control byte. FRARH[4] – Output range selection. “1” – 01 ~ FE, “0” -- 00 ~ FF. FRARH[3] –Y brightness adjustment by manual. Effective only COMF[1]=”1”. FRARH[2] – Enable HSYNC latched by PCLK FRARH[1] – “1” When in Frame exposure mode, only One frame data output. FRARH[0] – Fast AGC mode. “1” – Speed double. “0” – Smooth but slow AGC mode.
2B	FRARL	5E	RW	Frame rate adjust low FRARL[7:0] – Frame rate adjust control byte. Frame rate adjustment resolution is 0.12%. Control byte is 10 bit. Every LSB equal decrease frame rate 0.12%. Range is 0.12% - 112%. IF frame rate adjustment enable, COME[7] must set to “0”.
2C	Rsvd 2C	88	RW	Reserved
2D	COMJ	03	RW	Common control J COMJ[7:5] – reserved COMJ[4] – Enable auto black expanding mode. COMJ[3] – Reserved COMJ[2] – Band filter enable. This bit enables a different exposure algorithm to cut light band induced by fluorescent light. COMJ[1] – Reverse output frame division. “1” – Change drop frame to output frame COMJ[0] –Reserved.
2E	VCOFF	80	RW	V channel offset adjustment VCOFF[7] – Offset adjustment direction: “0” = Add V[6:0]; “1” = Subtract V[6:0]. VCOFF[6:0] – V channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write to this register through SCCB has no effect. If COMG[2] =1, V channel offset adjustment will use the stored value which can be changed through SCCB. Only effective when COMF[1] =0. If output RGB raw data, this register will adjust R channel data. ***Note:*** *This function is not available on the OV8110 image sensor.*
2F	REF1	19	RW	Internal voltage reference control
30 – 4B	Rsvd 30–4B	××	–	Reserved
4C	MEDC	00	RW	Medium filter option control MEDC[7] – AWB step and range x1.5 when this register is “1”. MEDC[6:0] – Reserved.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
4D	ADDC	10	RW	ADC converter option control ADDC[7:6] – Reserved ADDC[5] – Reserved ADDC[4] – Reserved ADDC[3:2]—UV delay selection. “00” – no delay. “01” – no delay. “10” – 2tp delay. “11” 4tp delay. ADDC[1:0] Reserved
4E—5F	Rsvd 4E—5F	xx	-	Reserved
60	SPCA	20	RW	Signal process control A SPCA[7] – Channel 1.5x preamplifier gain enable. SPCA[6] – Analog half current selection. SPCA[5] – Gev/God switch instead of average for G in RGB and UV channel. SPCA[4] – Gev/God switch instead of average for Y channel in YUV mode SPCA[3:2] – Red channel preamplifier gain selection. “00” –1x, “01” –1.2x, “10” –1.4x, “11”-1.6x. SPCA[1:0] – Blue channel preamplifier gain selection. Same as above.
61	SPCB	80	RW	Signal process control B SPCB[7] – AGC/AEC feedback loop using Y channel. RGB output must set it to “0”. SPCB[6:5] – Reserved SPCB[4] – Anti-aliasing 2X option SPCB[3] – Enable RGB brightness control. SPCB[2] – Brightness control BRT[7:0] range and step half. SPCB[1:0] – Auto brightness reference level. “00” – 0IRE, “01” – 6IRE, “10” 10IRE, “11” 20IRE.
62~64	Rsvd 62--64	xx	-	Reserved register for internal use.
65	SPCC	02	RW	Signal process control C SPCC[7:3] – Reserved for internal use. SPCC[2] – ADC mode selection. Increase range by 1.5x. SPCC[1:0] – ADC reference selection. Use recommended value only.
66	AWBC	55	RW	AWB process control. AWBC[7:6] – Selectable highest luminance level to be available in AWB control. AWBC[5:4] – Selectable lowest luminance level to be available in AWB control. Effective only when COME[3]=1 in AWBC[7:4] AWBC[3:2] – Selectable U level to be available in AWB control. AWBC[1:0] – Selectable V level to be available in AWB control. Effective only when COMM[7]=1 in AWBC[3:0].
67	YMXB	55	RW	YUV matrix control. YMXB[7:6] – UV coefficient selection, u=B-Y, v=R-Y “00” - U=u. V=v. “01” – U=0.938u, V=0.838v “10” – U=0.563u, V=0.613v “11” – U=0.5u, V=0.877v YMXB[5] – Reserved. YMXB[4] – UV signal with 3 points average. YMXB[3:2] – Y delay selection. 0tp to 3tp. YMXB[1:0] – Reserved.
68	ARL	AC	RW	AEC/AGC reference level ARL[7:5] – Voltage reference selection (Higher voltage = brighter final stable image) “000” = Lowest reference level “111” = Highest reference level ARL[4:0] – Reserved
69-6E	Rvsd 69-6F	xx	-	Reserved.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
70	COMK	80	RW	Common mode control K COMK[7] – HREF edge latched by PCLK falling edge. COMK[6] – Output port drive current 2x larger option. COMK[5] – Aperture correction option. COMK[4] – ZV port vertical timing selection. “1” VSYNC output ZV port vertical sync signal. “0” normal TV vertical sync signal. COMK[3] – Reserved. COMK[2] – Double Aperture correction strength. COMK[1] – 4x stable time less when in AWB slow mode. COMK[0] – Disable output pin internal 100K pull down resistor
71	COMJ	00	RW	Common control J COMJ[7] – Auto brightness update rate selection. “1” slow, “0” fast. COMJ[6] – PCLK output gated by HREF. COMJ[5] – Change HREF output port to CHSYNC. COMJ[4] – Change CHSYNC output port to HREF. COMJ[3:2] – Highest 2 bit for HSYNC rising edge shift control. See register [72]. COMJ[1:0] – Highest 2 bit for HSYNC falling edge shift control. See register [73].
72	HSDY	14	RW	Horizontal SYNC rising edge shift COMJ[3:2], HSDY[7:0], HSYNC rising edge shift control. Range 000 to 3FF, step 1 pixel.
73	HEDY	54	RW	Horizontal SYNC falling edge shift COMJ[1:0]&HEDY[7:0], HSYNC falling edge shift control. Range 000 to 3FF.
74	COMM	20	RW	Common mode control M COMM[7] – Enable UV smart AWB threshold controlled by COMG[5]. COMM[6:5] – AGC maximum gain boost control. “00” – 6db, “01” – 12db, “10” – 6db, “11” – 18db COMM[4:0] – Reserved.
75	COMN	0E	RW	Common mode control N COMN[7] – AWB control mode selection. “1” – AWB stop when field/frame average level less than threshold. “0” always do AWB. COMN[6:4] – Reserved for internal test mode. COMN[3] – Drop one field/frame when exposure line change is bigger than a fixed number. COMN[2] – Enable exposure go down to less than 1/120” or 1/60” in smooth AEC mode. COMN[1:0] – Reserved.
76	COMO	00	RW	Common mode control O COMO[7] – Output main clock at FODD pin. COMO[6] – Reserved. COMO[5] – Software power down mode. COMO[4] – ITU-656 timing. COMO[3] – Reserved. COMO[2] – Tri-state all timing output except data line. COMO[1] – SCCB writing bit synchronized by VSYNC. COMO[0] – Reserved.
77	Rvsd 77	××	-	Reserved
78	YBAS	80	RW	Y/G ADC offset YBAS[7:0] – Fixed offset to final Y/G data, range –128 to 128
79	UBAS	80	RW	U/B ADC offset UBAS[7:0] – Fixed offset to final U/B data, range –128 to 128
7A	VBAS	80	RW	V/R ADC offset VBAS[7:0] – Fixed offset to final V/R data, range –128 to 128.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
7B	REF2	D8	RW	Internal reference control.
7C	AVG	00	RW	Field/Frame average level storage. Only effective COME[6]=1.
7D	COMP	08	RW	Common mode control P COMP[7] – 10-bit output in one port output, less 2 bit come from UV1 and UV0. COMP[6] – 10-bit output in one port output, less 2 bit come from FODD and HREF. COMP[5] – Reserved. COMP[4] – Flip vertical sate read out. Only for YUV mode. COMP[3] – ADC BLC level option. “1”=10-bit ADC BLC level “10” (H), “0”=10-bit ADC BLC Level “40” (H). COMP[2:0] – Reserved.
7E—81	Rsvd7E—81	xx	-	Reserved
82	VB	23	RW	AEC/AGC fast mode low threshold control. Same as AEB[7:0].
83	VW	0B	RW	AEC/AGC fast mode high threshold control. Same as AEW[7:0].
84	COMS	00	RW	Common mode control S COMS[7] – Reserved. COMS[6] – Average AGC/AEC algorithm COMS[5:3] –Reserved. COMS[2] – 1-line ADC option COMS[1] – Reserved. COMS[0] – Reserved.
85-86	Rsvd85-86	xx	-	Reserved.
87-88	Rsvd 87-88	xx	-	Reserved.
89	COMV	00	RW	Common mode control V COMV[7] – Auto frame rate adjustment selection. “1” – 1 time every 2 fields/frames. “0” – 1time every 1 field/frame. COMV[6] – Double output pixel clock. COMV[5] – Output true black line. COMV[4] – CIF 1 line clock phase selection. COMV[3] – Enable ZV timing HSYC option. COMV[2] – By pass RGB matrix. COMV[1] – Change highest bit AGC to clock down 2. COMV[0] – Reserved.
8A	RAVE	00	RW	R channel average values
8B	BAVE	00	RW	B channel average values

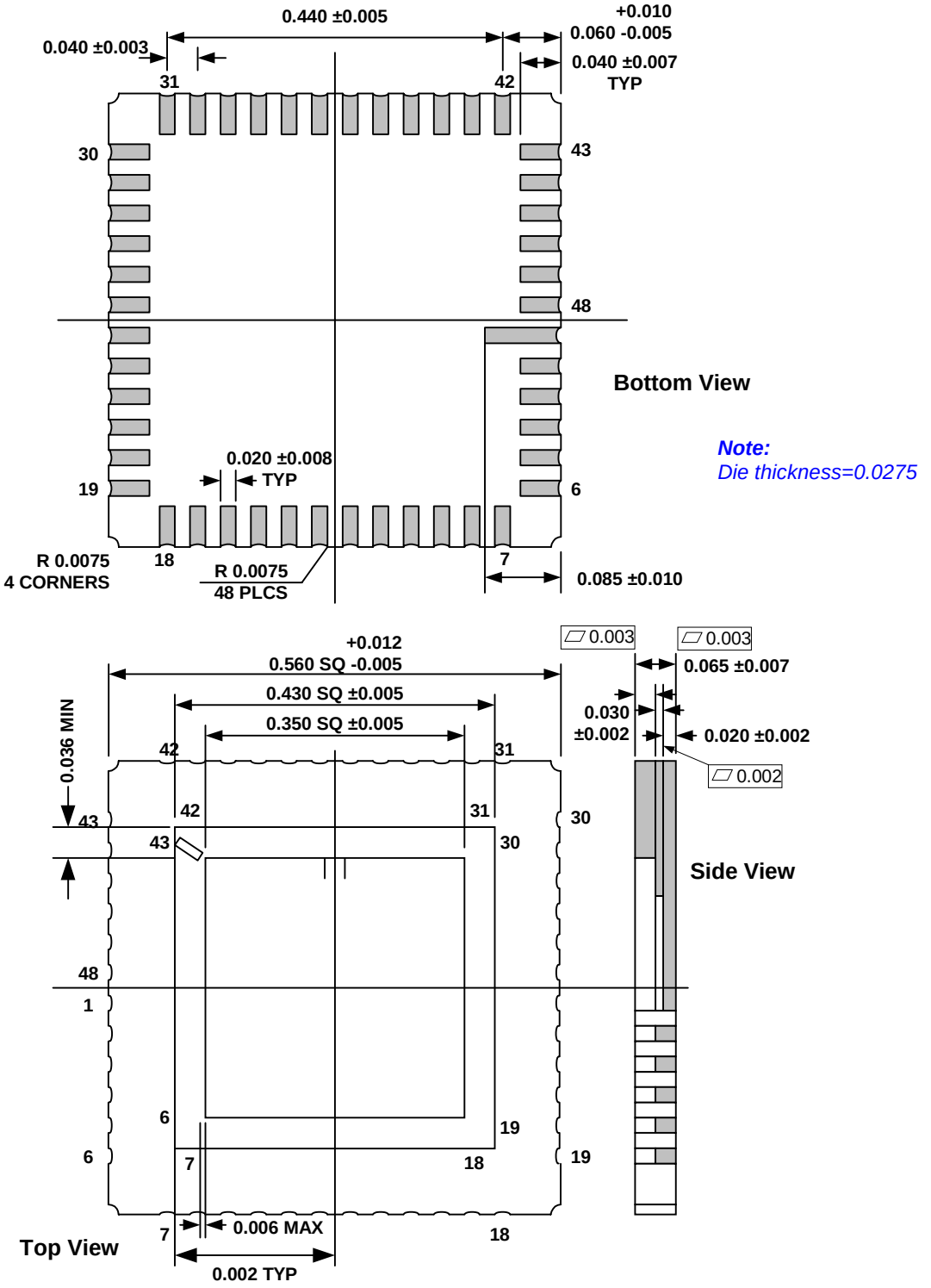


Figure 9. OV8610/OV8110 Package Diagram

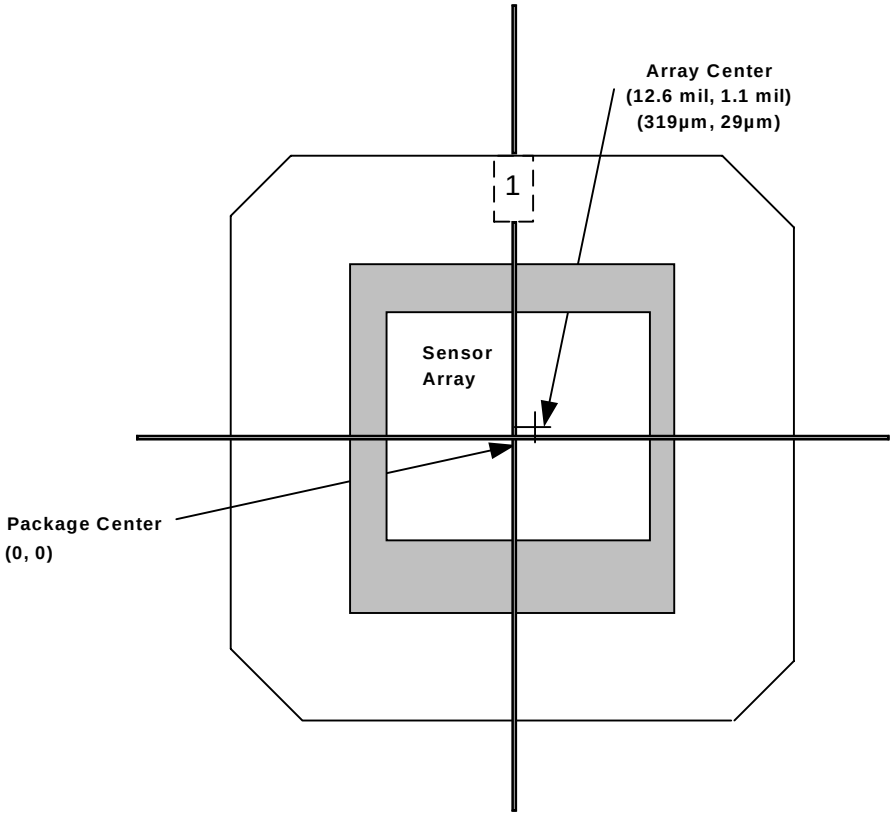


Figure 10. OV8610/8110 Sensor array center location

Note: *Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin one down.*

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