QN908x

Ultra low power Bluetooth 5 system-on-chip solution

Rev. 1.2 — 19 April 2018 Product data sheet

1. Introduction

QN908x is an ultra low power Bluetooth Low Energy wireless MCU with on-chip memory, USB 2.0 full-speed compliant device interface, and 16-bit ADC for Bluetooth Smart applications.

QN9080 integrates a 32-bit ARM Cortex-M4F core with Bluetooth Low Energy (v5.0) compliant radio, link controller, host stack and GATT profiles. The 32-bit ARM Cortex-M4F MCU and on-chip memory provides additional signal processing and scope to run applications for a true single-chip Bluetooth Low Energy (v5.0) solution.

The QN908x uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner. It optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

2. General description

The QN908x is a single chip, 10 mW peak power, high performance Bluetooth Low Energy SoC platform. It facilitates the development of end products such as wearables, health, and sport and fitness trackers. The end products also include retail beacons, connected smart home appliances, smart remote controls, HID devices, asset trackers, and home automation.

QN9080 provides single-chip solution for Bluetooth Smart applications by integrating a Bluetooth Low Energy (v5.0) compliant radio, link controller, host stack and GATT profiles. The integrated 32-bit ARM Cortex-M4F MCU with on-chip flash memory and a mix of analogue and digital peripherals provides the most efficient data fusion engine. The feature makes it a superior solution for applications requiring significant sensor fusion computation.

Additional system features include a fully integrated DC-to-DC converter, LDO, low-power sleep timer, battery monitor, high resolution ADC, and GPIO. These features reduce overall system cost and size.

The QN908x operates with a power supply range of 1.62 V to 3.6 V. The best in-class active current, with ultra-low power sleep modes, give excellent battery life allowing operation from a coin cell battery.

3. Features and benefits

- True single-chip Bluetooth Low Energy (v5.0) SoC solution
  - Integrated Bluetooth LE radio, protocol stack and application profiles
  - Supports central and peripherals roles
  - Supports master/slave concurrency
  - Supports 16 simultaneous links
  - Supports secure connections
  - Supports data packet length extension
  - Wifi/Bluetooth LE coexistence interface
  - 48-bit unique bluetooth device address
- RF
  - –95dBm RX sensitivity in 1Mbps mode, -92dBm RX sensitivity in 2Mbps mode (LDO mode)
  - –94dBm RX sensitivity in 1Mbps mode, -91.5dBm RX sensitivity in 2Mbps mode (DC-to-DC converter mode)
  - Fast and reliable RSSI in 1dB step
  - TX output power from –20 dBm to 2 dBm
  - Single-ended RF port with integrated balun
  - Generic FSK modulation with programmed data rate from 250Kbps to 2Mbps
  - Compatible with worldwide radio frequency regulations
- Very low power consumption
  - Single 1.62 V to 3.6 V power supply
  - Integrated DC-to-DC buck converter and LDO
  - 1.0 μA power-down 1 mode, to wake up by GPIO
  - 2.5 μA power-down 0 mode, to wake up by 32 kHz sleep timer, RTC and GPIO
  - 3.5 mA RX current with DC-to-DC convertor enabled at 3 V supply in 1Mbps mode
  - 5.0 mA RX current with DC-to-DC convertor enabled at 3 V supply in 2Mbps mode
  - 3.5 mA TX current @0 dBm TX power with DC-to-DC converter enabled at 3 V supply in both 1Mbps and 2Mbps mode
- ARM Cortex-M4 core (version r0p1)
  - ARM Cortex-M4 processor, running at a frequency of up to 32 MHz
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU)
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC)
  - Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points, including serial wire output for enhanced debug capabilities
  - System tick timer
- On-chip memory
  - 512 kB on-chip flash program memory and 2 kB page erase and write
  - 128 kB SRAM
  - 256 kB ROM
- ROM API support
  - Flash In-System Programming (ISP)
- Serial interfaces
  - Four Flexcomm serial peripherals

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- USART protocol supported by Flexcomm0, USART and I2C by Flexcomm1, SPI and I2C by Flexcomm2, and SPI by Flexcomm3
- Each Flexcomm includes a FIFO
- I^2C-bus interfaces support fast mode and with multiple address recognition and monitor mode
- USB 2.0 (full speed) device interface
- Two quadrature decoders
- SPI Flash Interface (SPIFI) uses a SPI bus superset with four data lines to access off-chip quad SPI flash memory at a much higher rate than is possible using standard SPI or SSP interfaces
- Supports SPI memories with 1 or 4 data lines

- Digital peripherals
  - DMA controller with 20 channels, able to access memories and DMA capable peripherals
  - Up to 35 General Purpose Input Output (GPIO) pins, with configurable pull-up or pull-down resistors
  - GPIO registers are located on the AHB for fast access
  - 32 GPIOs can be selected as Pin INTerrupts (PINT), triggered by rising, or falling input edges
  - AES-128 security coprocessor
  - Random Number Generator (RNG)
  - CRC engine
  - Fusion Signal Processor (FSP) for data fusion and machine learning algorithms resulting in low power consumption compared to software processing
- Analog peripherals
  - 16-bit ADC with 8 external input channels, with sample rates of up to 32k sample per second, and with multiple internal and external trigger inputs
  - Integrated temperature sensor, connected to one internal dedicated ADC channel
  - Integrated battery monitor connected to one internal dedicated ADC channel
  - General-purpose 8-bit 1M sample per second DAC
  - Integrated capacitive sense up to 8 channels, able to wake up the MCU from low power states.
  - Two ultra low-power analog comparators, able to wake up the MCU from low power states.
- Timers
  - Four 32-bit general-purpose timers or counters, support capture inputs and compare outputs, PWM mode, and external count input
  - Sleep timer, which can work in power-down mode and wake up MCU
  - 32-bit Real Time Clock (RTC) with 1 second resolution running in the always-on power domain; can be used for wake-up from all low power modes including power-down
  - Watchdog Timer.
  - SC Timer or PWM.
- Clock generation
  - 32 MHz internal RC oscillator, which can be used as a system clock

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  - 16 MHz or 32 MHz crystal oscillator, which can be used as a system and RF reference
  - 32 kHz on-chip RC oscillator
  - 32.768 kHz crystal oscillator
- Power control
  - Programmable Power Management Unit (PMU) to minimize power consumption
  - Reduced power modes: sleep, and power-down
  - Power-On Reset (POR)
  - Brown-Out Detection (BOD) with separate thresholds for interrupt and forced reset
- Single power supply 1.62 V to 3.6 V
- Operating temperature range −40 °C to +85 °C
- Available as 6 × 6 HVQFN48 and 3.28 × 3.20 mm WLCSP packages

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4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
QN9080	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 × 6 × 0.85 mm	SOT778-7
QN9083	WLCSP47	wafer level chip-scale package; 47 bumps; 3.28 × 3.20 × 0.365 mm, 0.40 mm pitch	SOT1882-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Silicon revision[1]	Flash (kB)	Total SRAM (kB)	Cortex-M4 with FPU	FSP	USB FS	GPIO
QN9080	QN9080CHN	C	512	128	1	1	1	35
	QN9080DHN	D	512	128	1	1	1	35
QN9083	QN9083CUK	C	512	128	1	1	1	28
	QN9083DUK	D	512	128	1	1	1	28

[1] For details of Silicon revision, please refer to Errata sheet.

5. Marking

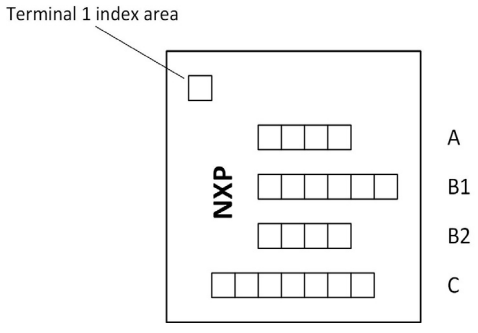

Fig 1. HVQFN48 package marking

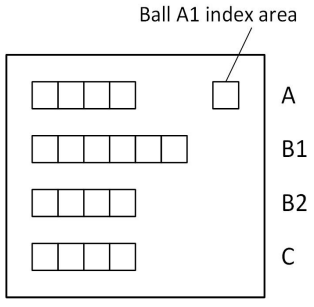

Fig 2. WLCSP47 package marking

The HVQFN package has the following top-side marking:

- Line A: “9080” for QN9080
- Line B1: xxxxxx
- Line B2: xxxx
- Line C: xxYYWW[R]
  - YY: year code, 17 for 2017
  - WW: week code
  - R = Chip revision

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The WLCSP package has the following top-side marking:

- Line A: “9083”
- Line B1: xxxxxx
- Line B2: xxWW
  - WW: week code
- Line C: YY[R]x
  - YY: year code, 17 for 2017
  - R = Chip revision

Table 3. Device revision table

Revision identifier (R)	Revision description
‘D’	Current revision
‘C’	Second metal fix revision

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6. Block diagram

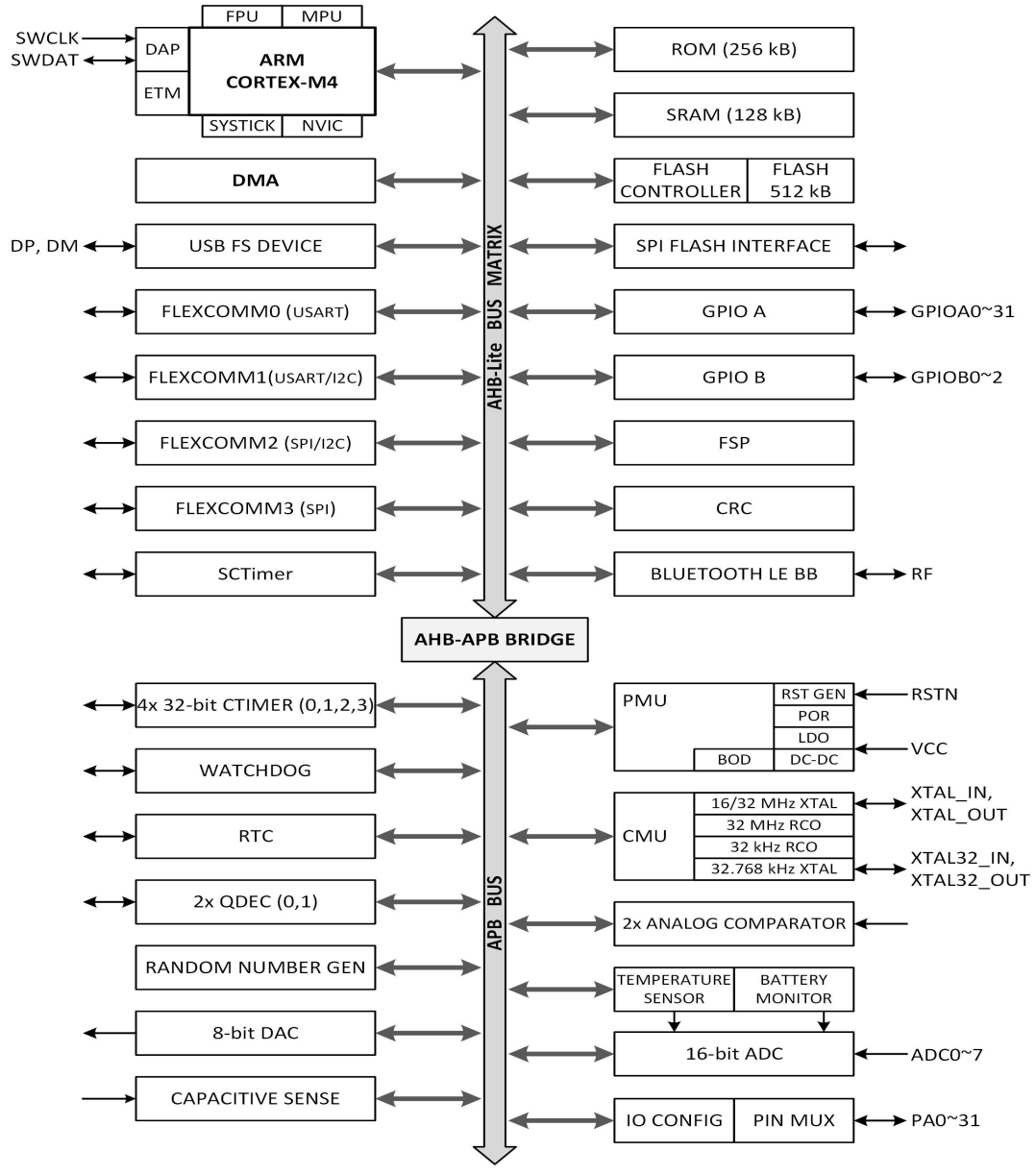

Fig 3. QN908x block diagram

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7. Pinning information

7.1 Pinning

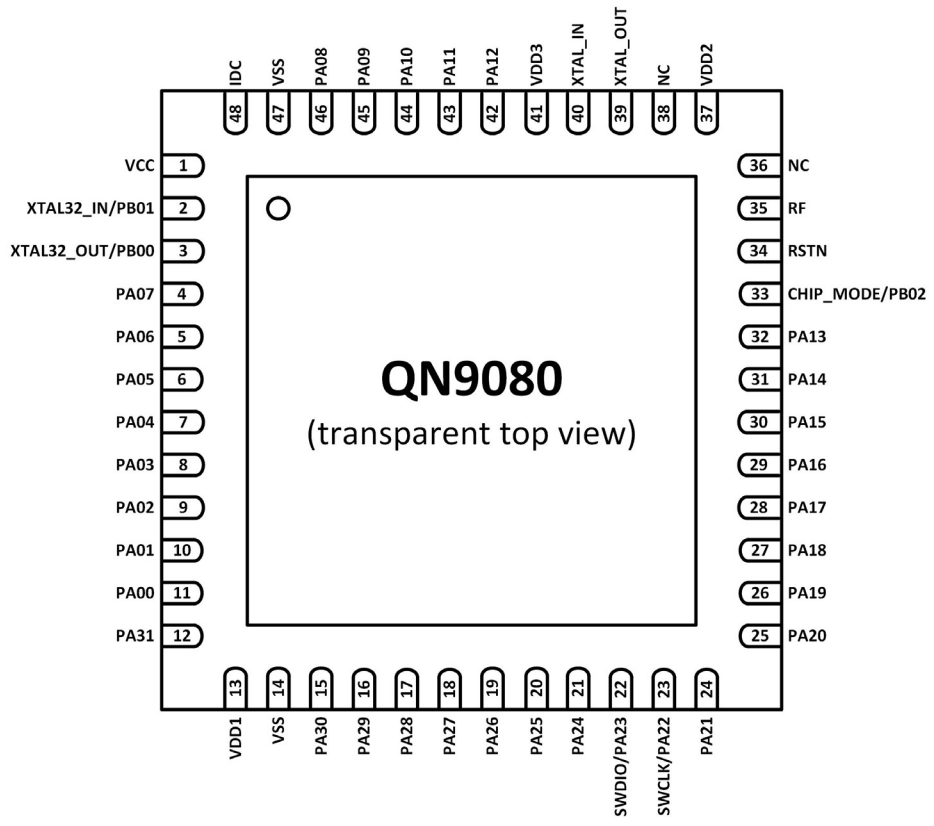

Fig 4. HVQFN48 pin configuration

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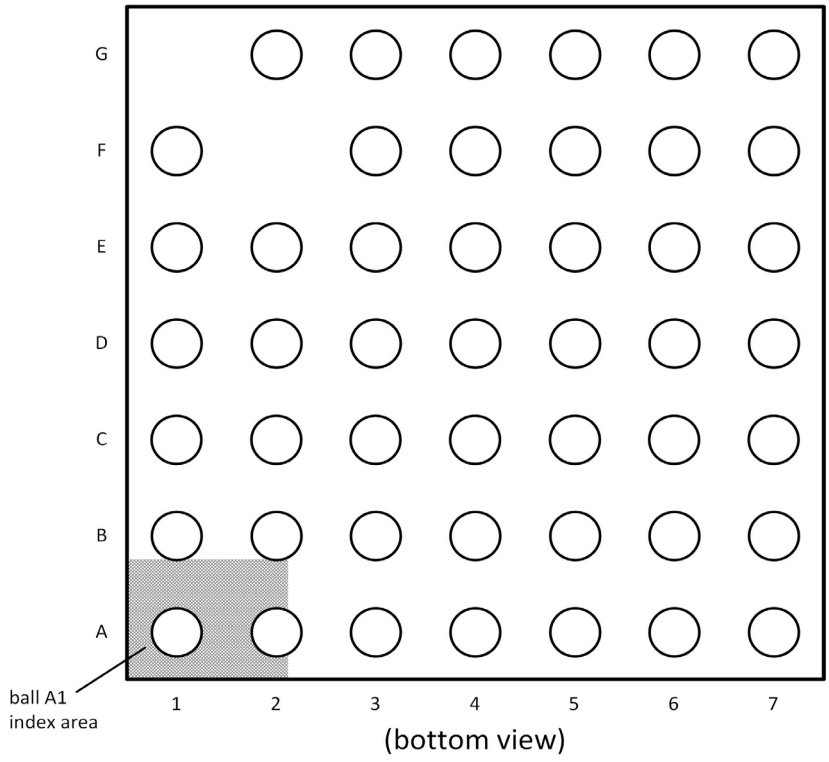

Fig 5. WLCSP pin configuration

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7.2 Pin description

In QN908x, each pin can support up to eight different digital or analog functions, including General Purpose Input Output (GPIO).

Table 4. Pin description

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA00	11	6B	PU	GPIOA0	I/O	general-purpose digital input output pin
				ADC0	AI	ADC external input 0
				SCT0_OUT0	O	SCTimer output 0
				CTIMER0_CAP0	I	32-bit CTimer 0 capture input 0
				FC0_RTS	I/O	flexcomm 0: USART RTS
				FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
				WLAN_TX	I	WLAN active high TX active indicator for coexistence
PA01	10	6A	PU	GPIOA1	I/O	general-purpose digital input output pin
				ADC1	AI	ADC external input 1
				SCT0_OUT1	O	SCTimer output 1
				CTIMER0_CAP1	I	32-bit CTimer 0 capture input 1
				FC0_CTS	I/O	flexcomm 0: USART CTS
				FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
				WLAN_RX	I	WLAN active high RX active indicator for coexistence
PA02	9	-	PU	GPIOA2	I/O	general-purpose digital input output pin
				QDEC0_A	I	quadrature decoder 0 input channel A
				SCT0_OUT2	O	SCTimer output 2
				CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
				R	I/O	reserved
				FC2_SCL_SSEL1	I/O	flexcomm 2: I2C SCL, SPI SSEL1
				RFE_RX_EN	O	RX enable for external RF front-end
PA03	8	-	PU	GPIOA3	I/O	general-purpose digital input output pin
				QDEC0_B	I	quadrature decoder 0 input channel B
				SCT0_OUT3	O	SCTimer output 3
				CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
				R	O	reserved
				FC2_SDA_SSEL0	I/O	flexcomm 2: I2C SDA, SPI SSEL0
				RFE_TX_EN	O	TX enable for external RF front-end
PA04	7	5B	PU	GPIOA4	I/O	general-purpose digital input output pin
				ADC2	AI	ADC external input 2
				SCT0_OUT4	O	SCTimer output 4
				CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
				FC0_TXD	I/O	flexcomm 0: USART TXD
				FC2_SDA_MOSI	I/O	flexcomm 2: I2C SDA, SPI MOSI
				SPIF_IO0	I/O	data bit 0 for the SPI flash interface

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Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA05	6	5A	PU	GPIOA5	I/O	general-purpose digital input output pin
				ADC3	AI	ADC external input 3
				SCT0_OUT5	O	SCTimer output 5
				CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
				FC0_RXD	I/O	flexcomm 0: USART RXD
				FC2_SCL_MISO	I/O	flexcomm 2: SCL, SPI MISO
				SPIF_IO1	I/O	data bit 1 for the SPI flash interface
PA06	5	4B	PU	GPIOA6	I/O	general-purpose digital input output pin
				ADC_EX_CAP	A	connected with ADC external capacitor
				SCT0_OUT3	O	SCTimer output 3
				CTIMER0_MAT2	O	32-bit CTimer 0 match output 2
				FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I2C SCL
				BLE_PTI0	O	BLE packet traffic information bit 0
				SPIFI_CLK	O	clock output for the SPI flash interface
PA07	4	3B	PU	GPIOA7	I/O	general-purpose digital input output pin
				ADC_VREFI	AI	ADC external reference voltage input
				SCT0_OUT2	O	SCTimer output 2
				CTIMER1_CAP0	I	timer 1 input capture 0
				FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
				BLE_PTI1	O	BLE packet traffic information 1
				SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA08	46	2B	PU	GPIOA8	I/O	general-purpose digital input output pin
				ADC4	AI	ADC external input 4
				SCT0_IN0	I	SCTimer input 0
				CTIMER1_CAP1	I	timer 1 input capture 1
				FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I2C SCL
				BLE_PTI2	O	BLE packet traffic information 2
				SPIFI_IO2	I/O	data bit 2 for the SPI flash interface
PA09	45	1B	PU	GPIOA9	I/O	general-purpose digital input output pin
				ADC5	AI	ADC external input 5
				SCT0_IN1	I	SCTimer input 1
				CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
				FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
				BLE_PTI3	O	BLE packet traffic information bit 3
				SPIFI_IO3	I/O	data bit 3 for the SPI flash interface

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Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA10	44	2C	PU	GPIOA10	I/O	general-purpose digital input output pin
				ADC6	AI	ADC external input 6
				SCT0_IN2	I	SCTimer input 2
				CTIMER1_MAT1	O	32-bit CTimer 1 match output 1
				FC1_SCK	I/O	flexcomm 1: USART clock
				ACMP0_OUT	O	analog comparator 0 output
				BLE_TX	O	BLE transmit indicator for coexistence
PA11	43	2D	PU	GPIOA11	I/O	general-purpose digital input output pin
				ADC7	AI	ADC external input 7
				SCT0_IN3	I	SCTimer input 3
				CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
				FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
				ACMP1_OUT	O	analog comparator 1 output
				BLE_RX	O	BLE reception indicator for coexistence
PA12	42	-	PU	GPIOA12	I/O	general-purpose digital input output pin
				R	O	reserved
				SCT0_OUT5	O	SCTimer output 5
				ACMP0_OUT	O	analog comparator 0 output
				FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I2C SCL
				SD_DAC	O	sigma-delta modulator DAC output
				ANT_SW	O	external antenna switch for diversity
PA13	32	-	PU	GPIOA13	I/O	general-purpose digital input output pin
				R	I/O	reserved
				SCT0_OUT4	O	SCTimer output 4
				ACMP1_OUT	O	analog comparator 1 output
				FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
				FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
				RFE_EN	O	enable for external RF front-end
PA14	31	5G	PU	GPIOA14	I/O	general-purpose digital input output pin
				CS0	AI	capacitive touch sense button input 0
				ANT_SW	O	external antenna switch for diversity
				CTIMER2_CAP0	I	timer 2 input capture 0
				FC0_RTS	I/O	flexcomm 0: USART RTS
				FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
				QDEC1_A	I	quadrature decoder 1 input channel A

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Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA15	30	4G	PU	GPIOA15	I/O	general-purpose digital input output pin
				CS1	AI	capacitive touch sense button input 1
				SCT0_OUT0	O	SCTimer output 0, PWM output 0
				CTIMER2_CAP1	I	timer 2 input capture 1
				FC0_CTS	I/O	flexcomm 0: USART CTS
				FC3_SCK	I/O	flexcomm 3: SPI clock
				QDEC1_B	I	quadrature decoder 1 input channel B
PA16	29	4F	PU	GPIOA16	I/O	general-purpose digital input output pin
				CS2	AI	capacitive touch sense button input 2
				SCT0_OUT1	O	SCTimer output 1, PWM output 1
				CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
				FC0_TXD	I/O	flexcomm 0: USART TXD
				FC3_MOSI	I/O	flexcomm 3: SPI MOSI
				QDEC0_A	I	quadrature decoder 0 input channel A
PA17	28	6G	PU	GPIOA17	I/O	general-purpose digital input output pin
				CS3	AI	capacitive touch sense button input 3
				SD_DAC	O	sigma-delta modulator DAC output
				CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
				FC0_RXD	I/O	flexcomm 0: USART RXD
				FC3_MISO	I/O	flexcomm 3: SPI MISO
				QDEC0_B	I	quadrature decoder 0 input channel B
PA18	27	5F	PU	GPIOA18	I/O	general-purpose digital input output pin
				CS4	AI	capacitive touch sense button input 4
				SCT0_OUT3	O	SCTimer output 3, PWM output 3
				CTIMER2_MAT2	O	32-bit CTimer 2 match output 2
				FC0_SCK	I/O	flexcomm 0: USART clock
				FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
				BLE_SYNC	O	BLE sync pulse
PA19	26	7G	PU	GPIOA19	I/O	general-purpose digital input output pin
				CS5	AI	capacitive touch sense button input 5
				SCT0_OUT2	O	SCTimer output 2, PWM output 2
				RFE_EN	O	enable for external RF front-end
				FC0_SCK	I/O	flexcomm 0: USART clock
				FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
				BLE_IN_PROC	O	BLE event in process indicator for coexistence

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Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA20	25	-	PU	GPIOA20	I/O	general-purpose digital input output pin
				QDEC1_A	I	quadrature decoder 1 input channel A
				SCT0_OUT1	O	SCTimer output 1, PWM output 1
				CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
				SWO	I/O	serial wire trace output
				FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I2C SCL
				SPIFI_CLK	O	clock output for the SPI flash interface
PA21	24	-	PU	GPIOA21	I/O	general-purpose digital input output pin
				QDEC1_B	I	quadrature decoder 1 input channel B
				SCT0_OUT0	O	SCTimer output 0, PWM output 0
				CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
				FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
				FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
				SPIFI_CSN	O	active low chip select output for the SPI flash interface
SWCLK /PA22	23	7F	PU	SWCLK	I/O	serial wire clock; it is the default function after reset
				GPIOA22	I/O	general-purpose digital input output pin
				SCT0_IN2	I	SCTimer input 2
				CTIMER3_MAT0	O	32-bit CTimer 3 match output 0
				FC2_SDA_SSEL0	I/O	flexcomm 2: I2C SDA, SPI SSEL0
				FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
				QDEC1_A	I	quadrature decoder 1 input channel A
SWDIO/ PA23	22	6F	PU	SWDIO	I/O	serial wire debug I/O; it is the default function after booting
				GPIOA23	I/O	general-purpose digital input output pin
				SCT0_IN3	I	SCTimer input 3
				CTIMER3_MAT1	O	32-bit CTimer 3 match output 1
				FC2_SCL_SSEL1	I/O	flexcomm 2: I2C SCL, SPI SSEL1
				FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
				QDEC1_B	I	quadrature decoder 1 input channel B
PA24	21	6E	PU	GPIOA24	I/O	general-purpose digital input output pin
				ACMP0N/CS6	AI	analog comparator 0 negative input, or capacitive touch sense button input 6
				ETM_TRACEDAT0	O	ETM trace data output bit 0
				CTIMER3_CAP0	I	timer 3 input capture 0
				RFE_RX_EN	O	RX enable for external RF front-end
				FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
				SPIFI_IO0	I/O	data bit 0 for the SPI flash interface

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Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA25	20	7E	PU	GPIOA25	I/O	general-purpose digital input output pin
				ACMP0P/CS7	AI	analog comparator 0 positive input, or capacitive touch sense button input 7
				ETM_TRACEDAT1	O	ETM trace data output bit 1
				CTIMER3_CAP1	I	timer 3 input capture 1
				RFE_TX_EN	O	TX enable for external RF front-end
				FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
				SPIFI_IO1	I/O	data bit 1 for the SPI flash interface
PA26	19	6D	PU	GPIOA26	I/O	general-purpose digital input output pin
				USB_DP	I/O	USB0 bidirectional D+ line
				SCT0_IN0	I	SCTimer input 0
				CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
				FC2_SDA_MOSI	I/O	flexcomm 2: I2C SDA, SPI MOSI
				QDEC0_A	I	quadrature decoder 0 input channel A
				BLE_SYNC	O	BLE sync pulse
PA27	18	7D	PU	GPIOA27	I/O	general-purpose digital input output pin
				USB_DM	I/O	USB0 bidirectional D- line
				SCT0_IN1	I	SCTimer input 1
				CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
				FC2_SCL_MISO	I/O	flexcomm 2: I2C SCL, SPI MISO
				QDEC0_B	I	quadrature decoder 0 input channel B
				BLE_IN_PROC	O	BLE event in process indicator for coexistence
PA28	17	-	PU	GPIOA28	I/O	general-purpose digital input output pin
				CLK_AHB	O	AHB clock output
				ETM_TRACECLK	O	ETM trace clock output
				RTC_CAP	I	RTC capture input
				FC1_SCK	I/O	flexcomm 1: USART clock
				SD_DAC	O	sigma-delta modulator DAC output
				SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA29	16	6C	PU	GPIOA29	I/O	general-purpose digital input output pin
				ACMP1N	AI	analog comparator 1 negative input
				ETM_TRACEDAT2	O	ETM trace data output bit 2
				CTIMER3_MAT0	O	timer 3 match output 0
				FC2_SCK	I/O	flexcomm 2: SPI clock
				FC3_MISO	I/O	flexcomm 3: SPI MISO
				SPIFI_IO2	I/O	data bit 2 for the SPI flash interface

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Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
PA30	15	7C	PU	GPIOA30	I/O	general-purpose digital input output pin
				ACMP1P	AI	analog comparator 1 positive input
				ETM_TRACEDAT3	O	ETM trace data output bit 3
				CTIMER3_MAT1	O	timer 3 match output 1
				FC2_SCK	I/O	flexcomm 2: SPI clock
				FC3_MOSI	I/O	flexcomm 3: SPI MOSI
				SPIFI_IO3	I/O	data bit 3 for the SPI flash interface
PA31	12	7B	PU	GPIOA31	I/O	general-purpose digital input output pin
				DAC	AO	DAC analog output
				RTC_CAP	I	RTC capture input
				CTIMER3_MAT2	O	Timer 3 match output 2
				SWO	I/O	serial wire trace output
				FC3_SCK	I/O	flexcomm 3: SPI clock
				SPIFI_CLK	O	clock output for the SPI flash interface
XTAL32_OUT/PB00	3	4A	-	XTAL32_OUT	AO	32.768 kHz crystal oscillator output **Remark:** leave it unconnected or used as GPIO when the LFXO is not used.
				GPIOB00	I/O	general-purpose digital input output pin
XTAL32_IN/PB01	2	3A	-	XTAL32_IN	AI	32.768 kHz crystal oscillator input **Remark:** external input clock can be injected when the LFXO is not used.
				GPIOB01	I/O	general-purpose digital input output pin
CHIP_MODE/PB02	33	3C	PU	CHIP_MODE	I	boot selection with pull-up by default; it should be pulled low to go through the normal ISP process for firmware programming, otherwise the ISP process is escaped to jump to flash
				GPIOB02	I/O	general-purpose digital input output pin
				ANT_SW	O	external antenna switch for diversity
RSTN	34	4E	PU	-	I	active low reset input
XTAL_OUT	39	1D	-	-	AO	16/32 MHz crystal oscillator output **Remark:** leave it unconnected if not used for crystal oscillator
XTAL_IN	40	1C	-	-	AI	16/32 MHz crystal oscillator input **Remark:** this can be used as external clock input, without using internal crystal oscillator
RF	35	2G	-	-	RF	RF input output port with Tx or Rx switch integrated on chip
VCC	1	2A	-	-	-	power supply (1.62 V to 3.6 V)
VDD1	13	7A	-	-	-	digital power supply
VDD2	37	1E	-	-	-	RF power supply
VDD3	41	2E	-	-	-	analog power supply

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Table 4. Pin description *...continued*

Symbol	HVQFN48	WLCSP	Reset state[1]	Alternate function	Type	Description
VSS	14,47	1F,3D,3E,3F,3G,4C,4D,5C,5D,5E	-	-	-	ground
IDC	48	1A	-	-	AO	DC-to-DC converter output; refer to reference design circuit when DC-to-DC is used; leave it open when DC-to-DC is not used
NC	36,38	-	-	-	-	not connected

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{CC}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, AO = analog output, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 7.2.2. For termination on unused pins, see Section 7.2.1.

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7.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function can be left unconnected and are configured as input with their internal pull-up or pull-down enabled. Enabling pull-down is preferred.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as inputs, with their internal pull-up or pull-down enabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
PAnm	I; PU	unconnected if driven LOW and configured as GPIO output with pull-up disabled by software
XTAL32_IN	-	unconnected
XTAL32_OUT	-	unconnected

[1] I = Input, PU = Pull-up enabled

7.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Power-down
PAnm pins	As configured in the SYSCON[1]. Default: input with internal pull-up enabled		
RSTN	Reset function enabled. Default: input, internal pull-up enabled		

[1] Default and programmed pin states are retained in sleep and power down mode

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8. Functional description

8.1 Architectural overview

The ARM Cortex-M4 includes one AHB-Lite bus, one system bus, and I-code and D-code buses. Separate buses are dedicated for instruction fetch (I-code) and data access (D-code).

The QN908x uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner. It optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

8.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general-purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, and interruptable or continuable multiple load and store instructions. It also provides automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is executed, its successor is decoded, and a third instruction is fetched from memory.

8.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE standard 754-2008. The IEEE standard for binary floating-point arithmetic is referred as the IEEE 754 standard.

8.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data. Access to memory regions can be disabled and also be defined as read-only. It detects unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions, each of which is divided into eight sub-regions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will trigger memory management fault exception.

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8.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The NVIC supports 52 external interrupt input sources, each with eight levels of priority. The processor supports both level and edge interrupts. External interrupt signals are connected to the NVIC, and the NVIC prioritizes the interrupts. Software is used to set the priority of each interrupt. The NVIC and the Cortex-M4F processor core are closely coupled, providing low-latency interrupt processing and efficient processing of late arriving interrupts.

The Wake-up Interrupt Controller (WIC) supports ultra-low power sleep mode. It enables the processor and NVIC to be put into a very low-power sleep mode leaving the WIC to identify and prioritize the interrupts. The processor implements the Wait-For-Interrupt (WFI), Wait-For-Event (WFE) and the Send EVent (SEV) instructions. In addition, the processor also supports use of SLEEPONEXIT, which causes the processor core to enter sleep mode when it returns from an exception handler to thread mode.

8.5.1 Features

- Controls system exceptions and peripheral interrupts
- 52 external interrupt input sources
- Eight programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table using Vector Table Offset Register (VTOR)
- Software interrupt generation

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. There are 52 interrupt sources in total.

8.6 System Tick timer (SysTick)

The ARM Cortex-M4 core includes a System Tick timer (SysTick) that generates a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

8.7 On-chip static RAM

QN908x supports 128 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

The 128 kB SRAM is divided into ten memory blocks, each with separate power control, to refine the power consumption according to application requirements.

Table 7. SRAM memory blocks

SRAM block	SIze	Start address offset
9	4k × 32 bit	0x0001 C000
8	4k × 32 bit	0x0001 8000
7	4k × 32 bit	0x0001 4000
6	4k × 32 bit	0x0001 0000

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Table 7. SRAM memory blocks

SRAM block	Slze	Start address offset
5	4k × 32 bit	0x0000 C000
4	4k × 32 bit	0x0000 8000
3	4k × 32 bit	0x0000 4000
2	2k × 32 bit	0x0000 2000
1	1k × 32 bit	0x0000 1000
0	1k × 32 bit	0x0000 0000

8.8 On-chip flash

The QN908x supports 512 kB of on-chip flash memory, to store code and data. The MCU accesses the flash via flash controller.

- 256 equal pages with 2 kB each; any page can be erased individually
- Greater than 10 years of data retention at 85°C
- Endurance: minimum 10,000 cycles

8.9 On-chip ROM

The 256 kB on-chip ROM contains boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) support for flash programming

8.10 Memory mapping

QN908x incorporates several distinct memory regions. The APB peripheral area is 64 kB in size and is divided to allow for multiple peripherals. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

QN908x integrates four types of memories: embedded flash, ROM, SRAM, and external SPIFI memory interface. To provide enough flexibility, the flash, ROM and RAM can be mapped to different regions of the memory map, depending on the register bits remap. The remap is 0 after reset and ROM is remapped to the address 0x0000 0000.

Table 8. Memory map options

Memory	Primary space	Alias	Memory remap option
ROM (256 kB)	0x0300 0000 to 0x0304 0000	N/A	0x0000 0000 to 0x0004 0000 (remap=0)
flash (512 kB)	0x0100 0000 to 0x0108 0000	0x2100 0000 to 0x2108 0000; 0x3100 0000 to 0x3108 0000	0x0000 0000 to 0x0008 0000 (remap=1)
SRAM (128 kB)	0x0400 0000 to 0x0402 0000	0x2000 0000 to 0x2002 0000	0x0000 0000 to 0x0002 0000 (remap=2)
SPIFI flash memory	0x1000 0000 to 0x1800 0000	0x8000 0000 to 0x8800 0000	N/A

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Figure 6 shows the overall map of the entire address space from the user program viewpoint.

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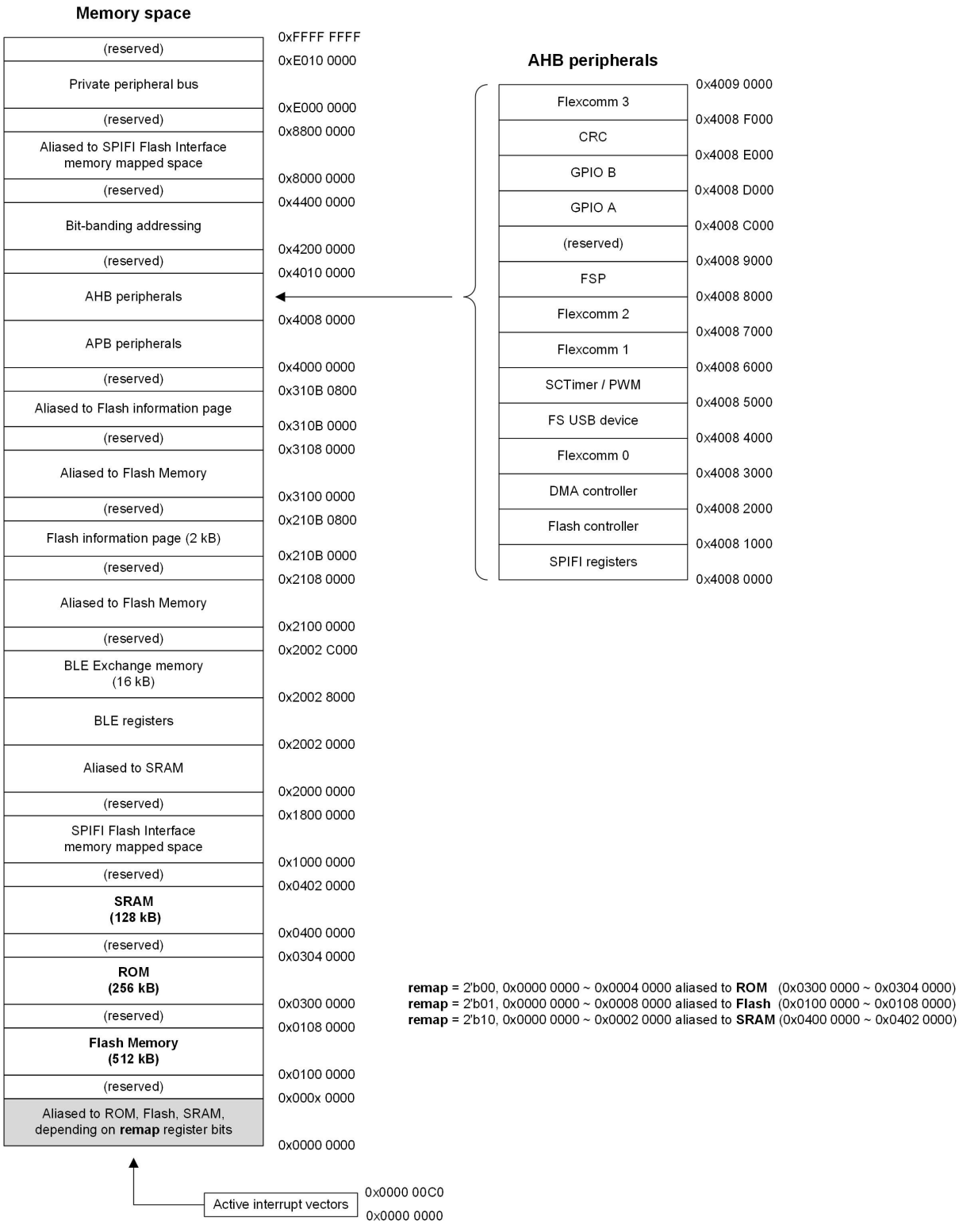

The private peripheral bus includes CPU peripherals such as the NVIC, SysTick, and the core control registers.

Fig 6. QN908x memory mapping

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Fig 7. QN908x APB memory map

8.11 Power management

To minimize system power consumption, the QN908x supports a variety of power modes and power management features.

8.11.1 Power supply

QN908x integrates both LDO and DC-to-DC converter. When the device is powered at a higher supply voltage like 3 V, DC-to-DC converter can be used to reduce current consumption.

When in the LDO mode without using DC-to-DC converter, users should make sure the VDD1, VDD2 and VDD3 never ramp-up before VCC. A simple way is to connect them together. Refer to the reference schematic for more information.

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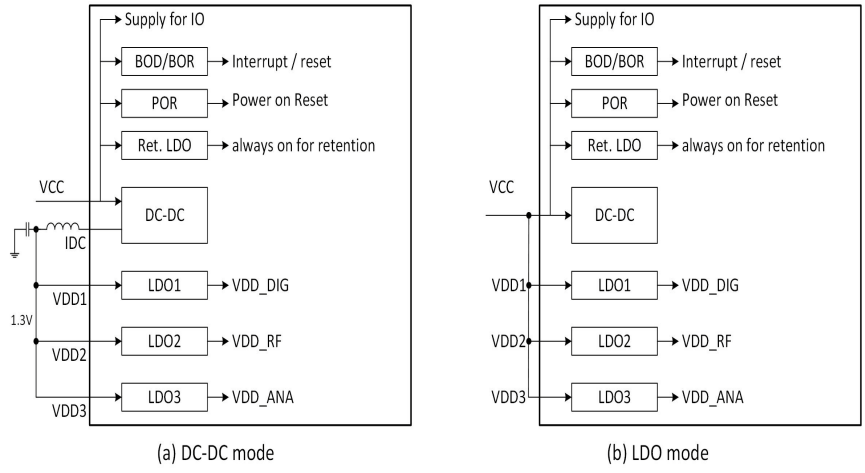

Fig 8. QN908x power supply

8.11.2 Power modes

A variety of power modes are supported for the optimization of power consumption, including active, sleep, power-down 0 and power-down 1 mode. Upon power-up or reset, the device enters active mode. After processing is complete, the software puts the chip into sleep mode or power-down mode, to save power consumption. The device is woken up either by a reset or an interrupt trigger like a GPIO interrupt, timer timeout, or other wake-up sources.

8.11.2.1 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked, can continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

8.11.2.2 Power-down 0 mode

In power-down 0 mode, power is shut off to the entire chip except for the always-on PMU domain, 32.768 kHz crystal oscillator, 32k RC oscillator, sleep timer, RTC, and the RSTN pin. All peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock running. In addition, all analog blocks and flash are shut down. In power down mode, the application can keep the analog comparator circuit running to monitor external voltage input, which wakes up the device if external voltage is higher than the reference voltage.

The QN908x wakes up from power-down 0 mode via a reset, digital pins selected as inputs to the pin interrupt block, sleep timer timeout interrupt, RTC interrupt, BOD forced reset, analog comparator interrupt, or cap sense interrupt.

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In power-down 0 mode, the processor state, registers, and SRAM values can be maintained, and the logic levels of the pins remain static. Power-down mode reduces power consumption compared to sleep mode, at the expense of longer wake-up times.

8.11.2.3 Power-down 1 mode

In power-down 1 mode, 32k clock source is powered off too. The capacitive sensor, RTC or BLE's low power domain does not work either. Only external IO, analog comparator can wake up system from this mode.

Table 9 shows the peripheral configuration in reduced power modes.

Table 9. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Power-down 0 mode	Power-down 1 mode
Flash	Software configured	Off	Off
SRAM blocks	Software configured	Software configured	Software configured
Sleep timer	Software configured	Software configured	Off
RTC	Software configured	Software configured	Off
Other digital peripherals	Software configured	Off	Off
Analog comparator	Software configured	Software configured	Software configured
32 kHz RCO	Software configured	Software configured	Off
32.768 kHz crystal oscillator	Software configured	Software configured	Off
BOD	Software configured	Software configured	Software configured
Capacitive sense	Software configured	Software configured	Software configured
Other analog peripherals	Software configured	Off	Off

8.11.3 Brown-Out Detection (BOD)

The QN908x includes a monitor for the voltage level on pin VCC. If this voltage falls below a fixed level, the BOD sets a flag that can cause an interrupt. In addition, separate threshold levels can be selected to cause chip reset and interrupt. By default, the BOD is disabled.

8.12 General-Purpose Input Output (GPIO)

The QN908x has two GPIO ports with a total of 35 GPIO pins. Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. The current level of a port pin can be read back, no matter what peripheral is selected for that pin. See Table 4 for the default state on reset.

8.12.1 Features

- Accelerated GPIO functions
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved
  - All GPIO registers are word, half-word, and byte addressable
  - Entire port value can be written in one instruction
- Direction control of individual bits
- All I/O default to inputs after reset

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- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request

8.13 Pin interrupt

The pin interrupt block configures up to four pins from all digital pins to provide four external interrupts connected to the NVIC. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt. The registers that control the pin interrupt are located on the I/O+ bus for fast single-cycle access.

8.13.1 Features

- Pin interrupts:
  - All pins of GPIO A can be selected as edge sensitive or level sensitive interrupt requests, each request creates a separate interrupt in the NVIC
  - Edge sensitive interrupt pins can interrupt on rising or falling edges or both
  - Level sensitive interrupt pins can be active HIGH or active LOW
  - Pin interrupts can wake up the device from sleep mode, but not in power-down mode

8.14 AHB peripherals

8.14.1 DMA controller

The DMA controller allows peripheral to memory, memory to peripheral, and memory to memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

8.14.1.1 Features

- 20 channels, 15 of which are connected to peripheral DMA requests, these DMA requests come from the Flexcomm (USART, SPI, I2C), and SPIFI interfaces
- DMA operations can be triggered by on-chip or off-chip events
- Priority is user-selectable for each channel (up to eight priority levels)
- Continuous priority arbitration
- Address cache with four entries
- Efficient use of data bus
- Supports single transfers of up to 1024 words
- Address increment options allow packing and/or unpacking data

8.15 Digital serial peripherals

8.15.1 USB 2.0 (full-speed) device controller

8.15.1.1 Features

- USB 2.0 (full-speed) device controller operating at 12Mbit/s
- Supports ten physical (five logical) endpoints including one control endpoint

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- Single- and double buffering supported
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types
- Supports wake-up from deep sleep mode on USB activity and remote wake-up
- Link Power Management (LPM) supported

8.15.2 SPI Flash Interface (SPIFI)

The SPI Flash Interface (SPIFI) allows low-cost serial flash memories to be connected to CPU, with little performance penalty compared to parallel flash devices with higher pin count. A driver API handles setup, programming, and erasure. After an initialization call to the SPIFI driver, the flash content is accessible as normal memory using byte, half word, and word accesses by the processor and/or DMA.

8.15.2.1 Features

- SPI flash interface to external flash
- Transfer rates of up to SPIFI_CLK/2 bytes per second
- Code in the serial flash memory can be executed as if it was in the internal memory space of the CPU. It is accomplished by mapping the external flash memory directly into the CPU memory space

  Remark: the SPIFI implemented on QN908x devices is intended for data access. The cache size is reduced and therefore direct execution from off-chip SPI flash is not recommended.
- Supports 1-bit, 2-bit, and 4-bit bidirectional serial protocols
- Half-duplex protocol compatible with various vendors and devices
- A driver library available from NXP Semiconductors to assist in using the SPIFI

8.15.3 Flexcomm serial communication (0,1,2,3)

Each Flexcomm provides a choice of peripheral functions, one of which the user must choose before the function can be configured and used.

8.15.3.1 Features

- USART with asynchronous operation or synchronous master or slave operation
- SPI-bus master or slave, with up to four slave selects
- I^2C-bus, including separate master, slave, and monitor functions
- Data for USART, and SPI traffic uses the Flexcomm FIFO. The I^2C function does not use the FIFO
- Flexcomm 0: USART
- Flexcomm 1: USART and I2C-bus
- Flexcomm 2: SPI-bus and I2C-bus
- Flexcomm 3: SPI-bus

8.15.4 I2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter

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with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus and can be controlled by more than one bus master connected to it.

8.15.4.1 Features

- Independent master and slave functions
- Bus speeds supported:
  - Standard mode, up to 100 kbits/s
  - Fast mode, up to 400 kbits/s
- Supports both multi-master and multi-master with slave functions
- Programmable I2C-bus slave addresses
- No chip clocks are required to receive and compare an address as a slave; so this event can wake up the device from sleep mode

8.15.5 USART

8.15.5.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option
- Maximum bit rates of 1 Mbit/s in asynchronous mode
- Maximum data rates of 1 Mbit/s in synchronous master and slave modes for USART functions
- Multiprocessor/multidrop (9-bit) mode with software address compare
- RS-485 transceiver output enable
- Auto-baud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode
- One transmit and one receive data buffer
- RTS/CTS for hardware signaling for automatic flow control; software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output
- Received data and status can optionally be read from a single register
- Break generation and detection
- Receive data is 2 of 3 sample "voting"; status flag set when one sample differs
- Built-in baud rate generator with auto-baud function
- Fractional rate divider shared among all USARTs
- Interrupts available for FIFO receive level reached, FIFO transmit level reached, transmit idle, change in receiver break detect, framing error, parity error, overrun, underrun, delta CTS detect, and receiver sample noise detected
- Loopback mode for testing of data and flow control
- USART transmit and receive functions work with the system DMA controller

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8.15.6 SPI serial I/O controller

8.15.6.1 Features

- Master and slave operation
- Maximum data rates of 16 Mbit/s in master mode for SPI functions
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up
- Master and slave operation
- Data can be transmitted to a slave without the need to read incoming data; useful while setting up an SPI memory
- Control information can optionally be written along with data; allows very versatile operation, including “any length” frames
- Three slave select input/outputs with selectable polarity and flexible usage

8.16 Timers

8.16.1 Standard timer/counter (CTIMER0 to 3)

The QN908x includes four general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system-derived clock or an externally supplied clock. It optionally generates interrupts, timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs, to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.16.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler
- Counter or timer operation
- Up to three 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions; a capture event may also generate an interrupt
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Up to four external outputs per timer corresponding to match registers with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match

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- Up to two match registers can be used to generate timed DMA requests
- PWM mode using up to three match channels for PWM output

8.16.2 SCTimer/PWM

The SCTimer/PWM is a flexible timer module capable of creating complex PWM waveforms. It can also perform other advanced timing and control operations with minimal or no CPU intervention.

The SCTimer/PWM can operate as a single 32-bit counter or as two independent, 16-bit counters in uni-directional or bi-directional mode. It supports a selection of match registers against which the count value can be compared. It also has capture registers where the current count value can be recorded when some pre-defined condition is detected.

The SCTimer/PWM module supports multiple separate events. The events can be defined by the user based on some combination of parameters including a match on one of the match registers, and/or a transition on one of the SCTimer/PWM inputs or outputs, the direction of count, and other factors.

Every action that the SCTimer/PWM block can perform occurs in direct response to one of these user-defined events without any software overhead. Any event can be enabled to:

- Start, stop, or halt the counter
- Limit the counter which means to clear the counter in unidirectional mode or change its direction in bi-directional mode
- Set, clear, or toggle any SCTimer/PWM output
- Force a capture of the count value into any capture registers
- Generate an interrupt of DMA request

8.16.2.1 Features

- The SCTimer/PWM supports:
  - Five inputs
  - Six outputs
  - Ten match/capture registers
  - Ten events
  - Ten states
- Counter/timer features
  - Each SCTimer/PWM is configurable as two 16-bit counters or one 32-bit counter
  - Counters clocked by system clock or selected input
  - Configurable number of match and capture registers. Up to five match and capture registers total
  - Ten events
  - Ten states
  - Upon match and/or an input or output transition create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs; change the state
  - Counter value can be loaded into capture register triggered by a match or input/output toggle

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- Each SCTimer/PWM is configurable as two 16-bit counters or one 32-bit counter
- Counters clocked by system clock or selected input
- Configurable number of match and capture registers. Up to five match and capture registers total
- Ten events
- Ten states
- Upon match and/or an input or output transition create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs; change the state
- Counter value can be loaded into capture register triggered by a match or input/output toggle

- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals
  - Up to eight single-edge or four dual-edge PWM outputs with independent duty cycle and common PWM cycle length
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as an rising or falling edge or level, a combination of match and/or input/output condition
  - Selected events can limit, halt, start, or stop a counter or change its direction
  - Events trigger state changes, output toggles, interrupts, and DMA transactions
  - Match register 0 can be used as an automatic limit
  - In bi-directional mode, events can be enabled based on the count direction
  - Match events can be held until another qualifying event occurs
- State control features:
  - A state is defined by events that can happen in the state while the counter is running
  - A state changes into another state as a result of an event
  - Each event can be assigned to one or more states
  - State variable allows sequencing across multiple counter cycles

8.16.3 WatchDog Timer (WDT)

The Watchdog timer (WDT) is a 32-bit timer clocked by 32 kHz clock. It is intended as a recovery method in situations where the CPU is subjected to software upset. The WDT resets the system when software fails to clear the WDT within the selected time interval. The WDT is configured as either a watchdog timer or as a timer for general-purpose use. If the watchdog function is not required in an application, it is possible to configure the watchdog timer as an interval timer that can be used to generate interrupts at selected time intervals. The maximum timeout interval is 1.5 days.

8.16.3.1 Features

- Programmable 32-bit timer

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- Internally resets chip if not reloaded during the programmable time-out period
- Flag to indicate Watchdog reset

8.16.4 RTC timer

The RTC block has three counters:

- 15-bit counter running of 32 kHz clock, to generate second
- 32-bit second counter to count seconds
- 32-bit free running counter with associated match registers to generate interrupt and forced reset

8.16.4.1 Features

- 15-bit counter, to generate second:
  - Operate on 32 kHz clock
  - Programmable 1second interrupt
  - Calibration function to compensate clock inaccuracy
- 32-bit second counter to count seconds generated by the 15-bit counter
  - Support configuration of second register on the fly
- 32-bit free running counter and associated match register:
  - Operate on 32 kHz clock
  - Match register for interrupt generation
  - Match register to generate reset, to be used as watchdog function
- Can wake up MCU from sleep mode and power down mode
- Can capture edge of input pins, to generate interrupts on either rising edge or falling edge

8.17 Analog peripherals

8.17.1 16-bit Analog-to-Digital Converter (ADC)

The ADC is a 16-bit general-purpose Sigma-Delta (SD) type ADC that can sample up to 32 kilo sample per second, using up to eight different external input channels, with multiple trigger sources.

8.17.1.1 Features

- 16-bit sigma-delta analog to digital converter
- 14-bit ENOB at 32 kHz sampling rate
- Integrated filter with 256 decimation rate. Additional software filtering by user can achieve higher resolution
- Up to eight external single-ended inputs, which can be configured as differential mode
- Supports both single or burst mode
- Supports scan mode
- Multiple trigger resources
- A temperature sensor is connected as an alternative input of ADC

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- A battery monitor is connected as an alternative input of ADC
- ADC output buffer
- ADC done interrupt with DMA capability

8.17.2 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a Complement To Absolute Temperature (VCTAT) voltage. The output voltage varies inversely with device temperature with an absolute accuracy of better than ±2°C over the full temperature range (-40°C to 85°C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

8.17.3 Battery monitor

The battery monitor is used to monitor the V_{CC} supply. A voltage divider (V_{CC}/4) is integrated and connected to an ADC internal channel.

8.17.4 Analog comparators (ACMP0, ACMP1)

The QN908x integrates two analog voltage comparators. The analog comparator is used to compare the voltage of two analog inputs. It generates a digital output to indicate the higher input voltage. The positive input is always from the external pin. The negative input can either be one of the selectable internal references or from an external pin. The ultra-low power analog comparator triggers an interrupt and wakes up the devices from power-down mode.

8.17.4.1 Features

- External negative input or configurable internal reference
- Comparator output can be read via register, or output to GPIO pins
- Configurable output polarity
- Can trigger an interrupt
- Can wake up the device from power-down mode

8.17.5 Digital-to-Analog Converter (DAC)

The DAC supports two modes:

- 1 MHz 8-bit digital-to-analog conversion
- Sigma-delta modulated digital output with 20-bit digital input

8.17.5.1 Features

- 1 MHz 8-bit Digital-to-analog conversion mode
- Sigma-delta modulation of 20-bit digital input data
  - 8-bit or 20-bit digital input from MCU or DMA, with gain control
  - Internal generated 20-bit sin-wave with configurable frequency and amplitude
- Eight entry input data FIFO

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- Input FIFO status indication with DMA capability
- Multiple trigger sources to start conversion:
  - Timer timeout
  - GPIO
  - Software trigger

8.17.6 Capacitive sense

The QN908x integrates a capacitive sense module, by monitoring the frequency change of the RC ring oscillator induced changing capacitance on external input pins. The monitored output is stored in FIFO for further software processing, to realize flexible user interface design. Smaller capacitance leads to higher frequency with bigger output data, and vice versa.

8.17.6.1 Features

- Up to eight input channels
- Support hardware continuous detection to reduce power consumption
- Scan mode among selected channels
- Eight entry output data FIFO, with interrupt to MCU
- Output data with channel index for easy software processing
- Programmable frequency range with trade off for current consumption
- Low power mode, operating on 32 kHz clock allows one selected channel to wake up the device from power down mode, with pre-defined threshold

8.18 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.

8.19 Random Number Generator (RNG)

QN908x integrates a random number generator for security purpose. The Random Number Generator (RNG) generates true non-deterministic random numbers for generating keys, initialization vectors and other random number requirements.

8.20 Advanced Encryption Standard (AES) coprocessor

The Advanced Encryption Standard (AES) coprocessor allows encryption/decryption to be performed with minimal CPU usage. The coprocessor supports 128-bit key.

8.21 Quadrature DECoder (QDEC)

The QN908x integrates two quadrature decoders.The decoder supports decoding of quadrature encoded sensor signals. It provides a pulse train with 90 degrees phase difference depending on whether the reference signal is leading or lagging, to determine the direction of rotation. It is suitable for mechanical or optical sensors with optional input debounce filter. The sample period and accumulation are configurable to provide flexibility for application.

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8.22 Fusion Signal Processor (FSP)

The QN908x integrates a co-processor (FSP) as hardware accelerator to offload the MCU from routine computations in data fusion and machine learning algorithms. The FSP is on the AHB bus. Once it is programmed and the input data is ready, it starts working and generates interrupt once the operation is complete. The interrupt triggers the MCU or DMA engine to fetch output data. To reduce current consumption for data transfers, the FSP has direct access to system memory to read input data and write the resultant output.

8.22.1 Features

- Matrix operations: inverse, add, multiplication, dot multiplication, transpose
  - Maximum size of matrix is 9×9
  - Floating point operation
- Transform engine supports FFT, IFFT, DCT, IDT operations
  - Configurable 64, 128, or 256 points operation
  - Supports real/complex, and fixed point/floating point input data
  - Supports real/complex, and fixed point/floating point output result
- Linear operation: FIR filter and correlation
  - Up to 9 parallel FIR filters
  - Each FIR filter has up to 15 taps with programmable coefficients. Supports both fixed point and floating point operation
  - Correlation between two sequences with length up to 256. Supports both fixed point and floating point operation
- Non-linear operations include Sine, Cosine, Log, Sqrt, Cordic
  - Supports both fixed point and floating point operation
- Statistics include Min, Max, Sum, Power Sum
  - Supports both fixed-point and floating-point operation
  - Supports up to 256 samples

8.23 Clock management

8.23.1 Clock sources

The QN908x supports two external and two internal clock sources:

- Internal 32 MHz oscillator
- Internal 32 kHz RC oscillator
- External high frequency crystal oscillator (32 MHz or 16 MHz)
- External 32.768 kHz crystal oscillator

8.23.1.1 Internal 32 MHz oscillator

The internal 32 MHz oscillator can be used as a clock that drives the CPU. Upon power-up, or any chip reset, the QN908x uses the internal oscillator as the clock source. Software switches to one of the available clock sources later.

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8.23.1.2 Internal 32 kHz oscillator

The 32 kHz oscillator is a low-power internal oscillator. It can be used to provide a clock to the sleep timer, RTC and to the entire chip. After proper calibration, the peripherals including RTC and sleep timer can achieve the accuracy of ±500 ppm.

8.23.1.3 External high frequency crystal oscillator

QN908x has 16/32 MHz external crystal with ±50 ppm accuracy. The high frequency crystal oscillator provides reference frequency for the radio transceiver. The load capacitance is integrated to reduce BOM cost, configurable by software.

8.23.1.4 External 32.768 kHz crystal oscillator

A 32.768 kHz crystal oscillator is used to replace the internal 32 kHz oscillator where accurate timing is needed. The 32 kHz clock with higher accuracy reduces power consumption of Bluetooth Low Energy operation.

8.23.2 Clock generation

The system control block facilitates the clock generation. Many clocking variations are possible. Figure 9 gives an overview of the potential clock options.

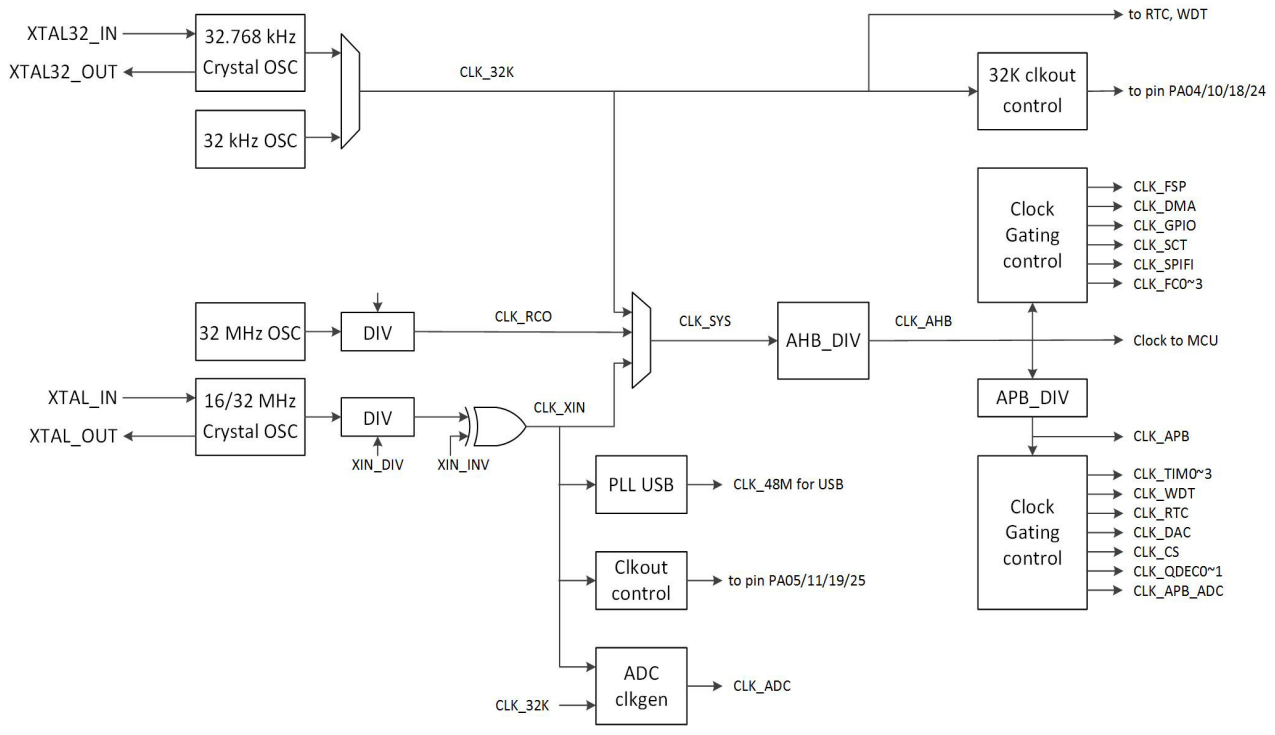

Fig 9. QN908x clock generation

8.24 Code security

This feature of the QN908x allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) is restricted.

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8.25 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

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9. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage	on pin VCC	[2]	-0.3	3.6	V
V_{DD1}	digital supply voltage	on pin VDD1	[2]	-0.3	3.6	V
V_{DD2}	RF supply voltage	on pin VDD2	[2]	-0.3	3.6	V
V_{DD3}	analog supply voltage	on pin VDD3	[2]	-0.3	3.6	V
V_I	input voltage		[6]	-0.3	3.6	V
V_I	input voltage	RF pin		-0.3	1.3	V
V_I	input voltage	USB_DM, USB_DP pins		-0.3	3.6	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[7]	-0.3	3.6	V
I_{CC}	total supply current	per supply pin	[3]	-	50	mA
I_{SS}	total ground current	per ground pin	[3]	-	50	mA
I_{latch}	I/O latch-up current	$-(0.5V_{CC}) < V_I < (1.5V_{CC})$; $T_j < 125$ °C		-	100	mA
$V_{i(HFXO)}$	32/16 MHz oscillator input voltage		[2]	-0.3	3.6	V
$V_{i(LFXO)}$	32.768 kHz oscillator input voltage		[2]	-0.3	3.6	V
T_{stg}	storage temperature		[8]	-65	150	°C
$T_{j(max)}$	maximum junction temperature			-	+150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model; all pins	[4]	-	2	kV
		Charged Device Model; all pins				
		HVQFN48	[5]		500	V
		WLCSP	[5]	-	400	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 18.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 18) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kOhm series resistor.

[5] Charged device model.

[6] Including the voltage on outputs in 3-state mode.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[8] Dependent on package type.

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10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
HVQFN64 package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	28±15%	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		4±15%	°C/W
WLCSP47 package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	53±15%	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		1±15%	°C/W

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11. Static characteristics

11.1 General operating conditions

Table 12. General operating conditions

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	32	MHz
V_{CC}	supply voltage			1.62	-	3.6	V
V_{DD1}	digital supply voltage			1.3	-	3.6	V
V_{DD2}	RF supply voltage			1.3	-	3.6	V
V_{DD3}	analog supply voltage			1.3	-	3.6	V
V_{ref}	ADC reference voltage	External reference		1.2	-	V_{CC}	V
External 32.768 kHz crystal oscillator pins							
V_i	32.768 kHz oscillator input voltage	on pin XTAL32_IN		0	-	3.6	V
V_o	32.768 kHz oscillator output voltage	on pin XTAL32_OUT		0	-	3.6	V
External high frequency crystal oscillator pins							
V_i	16 / 32 MHz oscillator input voltage	on pin XTAL_IN		0	-	3.6	V
V_o	16 / 32 MHz oscillator output voltage	on pin XTAL_OUT		0	-	3.6	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

11.2 CoreMark data

Table 13. CoreMark score

T_{amb} = 25 °C, V_{CC} = 3.0V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode				
CoreMark score	CoreMark code executed from SRAM	[1][2]	2.3	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash	[1][2]	2.3	(Iterations/s) / MHz

[1] Characterized through bench measurements using typical samples.

[2] Compiler settings: Keil µVision v.5.14., optimization level 3, optimized for time on.

11.3 Power consumption

Power measurements in active, sleep, power down modes were performed under the following conditions:

- All peripherals disabled
- Analog peripherals (ADC/DAC/ACMP/Capacitive Sense) powered down
- RF off
- Internal 32 MHz HFRCO powered down

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Table 14. Static characteristics: Power consumption in active modes

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
16 MHz crystal oscillator; DC-to-DC converter enabled, V_{cc} = 3.0 V							
I_{CC}	supply current	CoreMark code executed from RAM; flash powered down					
		CLK_AHB = 16 MHz	[2]	-	670	-	µA
		CLK_AHB = 8 MHz	[2]	-	480	-	µA
		CoreMark code executed from flash					
		CLK_AHB = 16 MHz	[2]	-	870	-	µA
		CLK_AHB = 8 MHz	[2]	-	590	-	µA
32 MHz crystal oscillator; DC-to-DC converter enabled, V_{cc} = 3.0 V							
I_{CC}	supply current	CoreMark code executed from RAM; flash powered down					
		CLK_AHB = 32 MHz	[2]	-	1080	-	µA
		CLK_AHB = 16 MHz	[2]	-	750	-	µA
		CLK_AHB = 8 MHz	[2]	-	560	-	µA
		CoreMark code executed from flash					
		CLK_AHB = 32 MHz	[2]	-	1410	-	µA
		CLK_AHB = 16 MHz	[2]	-	900	-	µA
		CLK_AHB = 8 MHz	[2]	-	640	-	µA
16 MHz crystal oscillator; DC-to-DC converter disabled, V_{cc} = V_{DD1} to V_{DD3} = 3.0 V							
I_{CC}	supply current	CoreMark code executed from RAM; flash powered down					
		CLK_AHB = 16 MHz	[2]	-	1140	-	µA
		CLK_AHB = 8 MHz	[2]	-	760	-	µA
		CoreMark code executed from flash;					
		CLK_AHB = 16 MHz	[2]	-	1450	-	µA
		CLK_AHB = 8 MHz	[2]	-	920	-	µA
32 MHz crystal oscillator; DC-to-DC converter disabled, V_{cc} = V_{DD1} to V_{DD3} = 3.0 V							
I_{CC}	supply current	CoreMark code executed from RAM; flash powered down					
		CLK_AHB = 32 MHz	[2]	-	2070	-	µA
		CLK_AHB = 16 MHz	[2]	-	1370	-	µA
		CLK_AHB = 8 MHz	[2]	-	980	-	µA
		CoreMark code executed from flash					
		CLK_AHB = 32 MHz	[2]	-	2660	-	µA
		CLK_AHB = 16 MHz	[2]	-	1650	-	µA
		CLK_AHB = 8 MHz	[2]	-	1120	-	µA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

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Table 15. Static characteristics: Bluetooth LE power consumption in active modes

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
32 MHz crystal oscillator, CLK_AHB = 16 MHz. Transmitter mode: f_c = 2440 MHz, 1Mbps mode							
I_{CC}	supply current	DC-to-DC converter enabled, V_{cc} = 3 V					
		Tx power = 0 dBm		-	3.5	-	mA
		Tx power = –4 dBm		-	2.5	-	mA
		DC-to-DC converter disabled, V_{cc} = 3 V					
		Tx power = 0 dBm		-	7.1	-	mA
		Tx power = –4 dBm		-	5.0	-	mA
32 MHz crystal oscillator, CLK_AHB = 32 MHz. Transmitter mode: f_c = 2440 MHz, 2Mbps mode[4]							
I_{CC}	supply current	DC-to-DC converter enabled, V_{cc} = 3 V					
		Tx power = 0 dBm		-	3.5	-	mA
		DC-to-DC converter disabled, V_{cc} = 3 V					
		Tx power = 0 dBm		-	7.1	-	mA
32 MHz crystal oscillator, CLK_AHB = 16 MHz. Receiver mode: f_c = 2440 MHz, 1Mbps mode							
I_{CC}	supply current	DC-to-DC converter enabled, V_{cc} = 3 V					
		–94 dBm RX sensitivity		-	3.5	-	mA
		DC-to-DC converter disabled, V_{cc} = 3 V					
		–95 dBm RX sensitivity		-	7.2	-	mA
32 MHz crystal oscillator, CLK_AHB = 32 MHz. Receiver mode: f_c = 2440 MHz, 2Mbps mode[4]							
I_{CC}	supply current	DC-to-DC converter enabled, V_{cc} = 3 V					
		–91.5 dBm RX sensitivity		-	5.0	-	mA
		DC-to-DC converter disabled, V_{cc} = 3 V					
		–92dBm RX sensitivity		-	10.3	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples, with 50 ohm loading on RF port.

[3] Guaranteed by characterization, not tested in production.

[4] 2Mbps mode is only supported when AHB clock is 32MHz.

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Table 16. Static characteristics: Power consumption in sleep, and power-down modes

T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{CC}	supply current	Sleep mode: all SRAM on. Flash in standby mode. DC-to-DC converter enabled, V_{cc} = 3 V.					
		32 MHz crystal oscillator					
		CLK_AHB = 8 MHz		-	350	-	µA
		CLK_AHB = 16 MHz		-	420	-	µA
		Sleep mode: all SRAM on. Flash in standby mode. DC-to-DC converter disabled, V_{cc} = 3 V.					
		32 MHz crystal oscillator					
		CLK_AHB = 8 MHz		-	600	-	µA
		CLK_AHB = 16 MHz		-	750	-	µA
		Power down 1 mode; all clocks off. Flash is powered down. DC-DC disabled, V_{cc} = 3 V. T_{amb} = 25 °C.					
		32 KB SRAM powered		-	1.0	-	µA
		64 KB SRAM powered		-	1.2	-	µA
		128 KB SRAM powered		-	1.8	-	µA
		Power down 0 mode; 32.768 kHz crystal oscillator on. Flash is powered down. DC-DC disabled, V_{cc} = 3 V. T_{amb} = 25 °C.					
		32 KB SRAM powered		-	2.5	-	µA
		64 KB SRAM powered		-	2.8	-	µA
		128 KB SRAM powered		-	3.4	-	µA
		Power down 0 mode; 32kHz on-chip RC oscillator on. Flash is powered down. DC-DC disabled, V_{cc} = 3 V. T_{amb} = 25 °C.					
		32 KB SRAM powered		-	2.2	-	µA
		64 KB SRAM powered		-	2.3	-	µA
		128 KB SRAM powered		-	2.9	-	µA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

[3] Guaranteed by characterization, not tested in production.

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Table 17. Static characteristics: ADC power consumption

T_{amb} = −40 °C to +85 °C, unless otherwise specified.1.62 V ≤ V_{CC} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{CC}	analog supply current	2 MHz sampling clock					
		Internal reference		-	200	-	μA
		PGA, gain = 1		-	330	-	μA
		PGA, gain = 16		-	660	-	μA
		Modulator		-	270	-	μA
		500 kHz sampling clock					
		Internal reference		-	140	-	μA
		PGA, gain = 1		-	220	-	μA
		PGA, gain = 8		-	880	-	μA
		Modulator		-	100	-	μA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), nominal supply voltages.

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11.4 Pin characteristics

Table 18. Static characteristics: pin characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified. 1.62 V ≤ V_{CC} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RSTN pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{CC}	-	3.6	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{CC}	V
V_{hys}	hysteresis voltage			0.05 × V_{CC}	-	-	V
Standard I/O pins							
Input characteristics							
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{CC} < 3.6 V		0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{CC} < 3.6 V		-	-	0.3 × V_{CC}	V
V_{hys}	hysteresis voltage		[2]	0.1 × V_{CC}	-	-	V
Output characteristics							
V_O	output voltage	output active		0	-	V_{CC}	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA[3]; 1.62 V ≤ V_{CC} < 3.6 V		V_{CC}-0.3	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA[3]; 1.62 V ≤ V_{CC} < 3.6 V		-	-	0.45	V
I_{OH}	HIGH-level output current	1.62 V ≤ V_{CC} < 3.6 V		4	-	-	mA
I_{OL}	LOW-level output current	1.62 V ≤ V_{CC} < 3.6 V		4	-	-	mA
R_{PD}	Pull-down register	1.62 V ≤ V_{CC} < 3.6 V		-	170	-	kΩ
R_{PU}	Pull-up resistor	1.62 V ≤ V_{CC} < 3.6 V		-	90	-	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Guaranteed by design, not tested in production.

[3] Pin's settings DRV_CTRL must be set to high to drive 4mA output.

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12. Dynamic characteristics

12.1 Start-up behavior

Table 19. Start-up characteristics

T_{amb} = −40 °C to +85 °C; 1.62 V ≤ V_{CC} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_a	32MHz RCO start-up		[1][2]			10	µs
t_b	POR ready		[1][2]			10	µs
t_c	VDD1~3 ramp up		[1][2]			10	µs
t_d	PMU supply ramp up		[1][2]			1	ms
t_e	RSTN delay		[1][2]		1		ms
t_f	boot time		[1][2]		218		µs

[1] See Figure 10.

[2] Based on characterization, not tested in production.

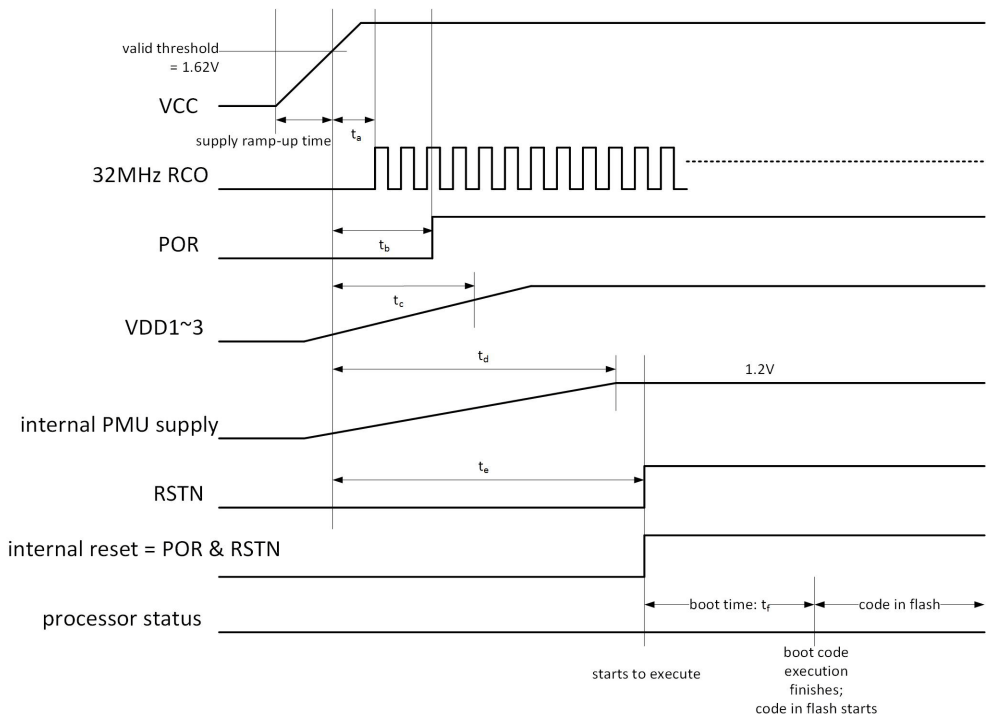

Fig 10. Start-up timing

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12.2 Flash memory

Table 20. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified. 1.62 V ≤ V_{CC} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	page erase/program	[1]	10000	-	-	cycles
		mass erase/program		10000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page/mass		-	-	100	ms
t_{prog}	programming time	word		-	-	20	ms

[1] Number of erase/program cycles.

12.3 I/O pins

Table 21. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 1.62 V ≤ V_{CC} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins							
t_r	rise time	pin configured as output; standard mode	[2][3]	-	-	2.4	ns
		pin configured as output; high drive mode	[2][3]	-	-	1.6	ns
t_f	fall time	pin configured as output; standard mode	[2][3]	-	-	4.2	ns
		pin configured as output; high drive mode	[2][3]	-	-	1.6	ns
t_r	rise time	pin configured as input	[4]	-	-	2	ns
t_f	fall time	pin configured as input	[4]	-	-	2	ns

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured by register. See the QN9080 user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

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12.4 Wake-up process

Table 22. Dynamic characteristic: Typical wake-up times from low power modes

V_{CC} = 3.0 V;T_{amb} = 25 °C; using 32MHz Oscillator as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode, waked up by GPIO interrupt, to code executing in flash	[2][5]	-	3		µs
		from power down mode, waked up by GPIO interrupt, to code executing in flash	[2][5]	-	10		µs
		from power down mode, waked up by GPIO interrupt, to Bluetooth advertising	[3][6]	-	7		ms
		from RSTN pin deasserted, to code executing in flash	[4][5]	-	218		µs
		from power-up, to code executing in flash	[5][5]		1.2		ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages. Based on characterization. Not tested in production.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] The time measured is the time between when a GPIO input pin is triggered to when a peripheral starts advertising.

[4] The wake-up time measured is the time between when the RSTN pin is de-asserted to wake the device up and when a GPIO output pin is set in the reset handler.

[5] The wake-up time measured is the time between power on and when a GPIO output pin is set in the reset handler.

[6] 16 MHz HFXO enabled, all peripherals off; CLK_AHB=16 MHz.

12.5 Internal 32MHz oscillator

Table 23. Dynamic characteristic: internal 32MHz oscillator

T_{amb} = 25 °C; 1.62 V ≤ V_{CC} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(HFRCO)}$	oscillator frequency		-	32	-	MHz
TC	temperature coefficient		-	0.04	-	%/°C
$\Delta f_{osc}/\Delta V_{CC}$	oscillator frequency variation with supply voltage		-	3	-	%/V
t_{start}	start-up time		-	-	2	µs
Icc	current consumption		-	60	-	µA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

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12.6 External high frequency crystal oscillator

Table 24. Dynamic characteristic: external high frequency crystal oscillator
T_{amb} = 25 °C; 1.62 V ≤ V_{CC} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{xtal}	crystal frequency		-	16	-	MHz
			-	32	-	MHz
Δf_{xtal}	crystal frequency accuracy		–50	-	+50	ppm
ESR	equivalent serial resistance	16 MHz, 9 pF load	-	-	100	Ω
		32 MHz, 9 pF load	-	-	100	Ω
C_L	load capacitance		5		12	pF
t_{start}	start-up time	16 MHz, 9 pF load	-	-	700	µs
		32 MHz, 9 pF load	-	-	400	µs
Icc	current consumption	16 MHz, 9 pF load	-	100	-	µA
		32 MHz, 9 pF load	-	200	-	µA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

12.7 External 32.768 kHz crystal oscillator

See Section 13.5 for connecting the 32.768 kHz oscillator to an external clock source.

Table 25. Dynamic characteristic: LFXO
T_{amb} = –40 °C to +85 °C; 1.62 ≤ V_{CC} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{xtal}	input frequency	-		-	32.768		kHz
Δf_{xtal}	Frequency tolerance			-50	-	+50	ppm
ESR	Equivalent serial resistance	9 pF load		-	-	100	kΩ
C_L	Load capacitance			5		12	pF
t_{start}(LFXO)	Start-up time	9 pF load		-	-	1	S
Icc(LFXO)	Current consumption	9 pF load		-	1	-	µA

[1] Parameters are valid over operating temperature range unless otherwise specified.

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12.8 Internal 32 kHz oscillator

Table 26. Dynamic characteristics: internal 32 kHz oscillator

T_{amb} = –40 °C to +85 °C; 1.62 ≤ V_{CC} ≤ 3.6[1]

Symbol	Parameter		Min	Typ[1]	Max	Unit
f_{osc}	oscillator frequency	[2]	-	32	-	kHz
$f_{osc(acc)}$	clock accuracy after calibration		-500		+500	ppm
TC	temperature coefficient		-	0.04	-	%/°C
$\Delta f_{osc}/\Delta V_{CC}$	oscillator frequency variation with supply voltage		-	3	-	%/V
t_{start}	start-up time		-	-	1	mS
Icc	current consumption		-	1	-	μA

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = -40 °C to +85 °C) is ±40 %.

12.9 SPI interfaces

In master mode, the maximum supported bit rate is 16 Mbit/s. In slave mode, assuming a set-up time of 4 ns for the external device and neglecting any PCB trace delays, the maximum supported bit rate is 16 Mbit/s. The actual bit rate depends on the delays introduced by the external trace and the external device.

Table 27. SPI dynamic characteristics[1]

T_{amb} = –40 °C to 85 °C; V_{CC} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master						
t_{DS}	data set-up time			5	-	ns
t_{DH}	data hold time			5	-	ns
$t_{v(Q)}$	data output valid time			–4	7	ns
SPI slave						
t_{DS}	data set-up time			7	-	ns
t_{DH}	data hold time			5	-	ns
$t_{v(Q)}$	data output valid time			–2	16	ns

[1] Based on simulated values.

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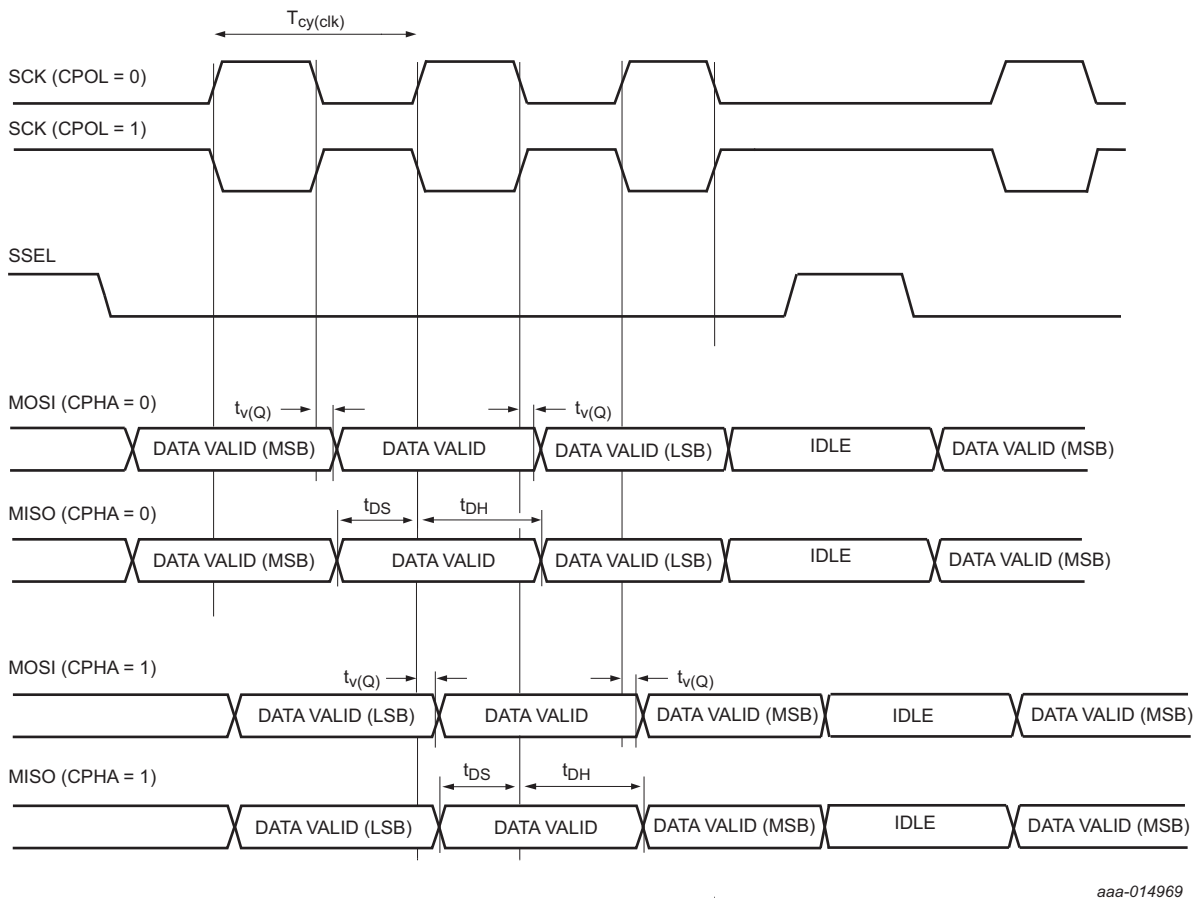

$T_{cy(clk)}$ = CLK_AHB/DIVVAL with CLK_AHB = AHB bus clock frequency. DIVVAL is the SPI clock divider. See the QN908x *User manual*.

Fig 11. SPI master timing

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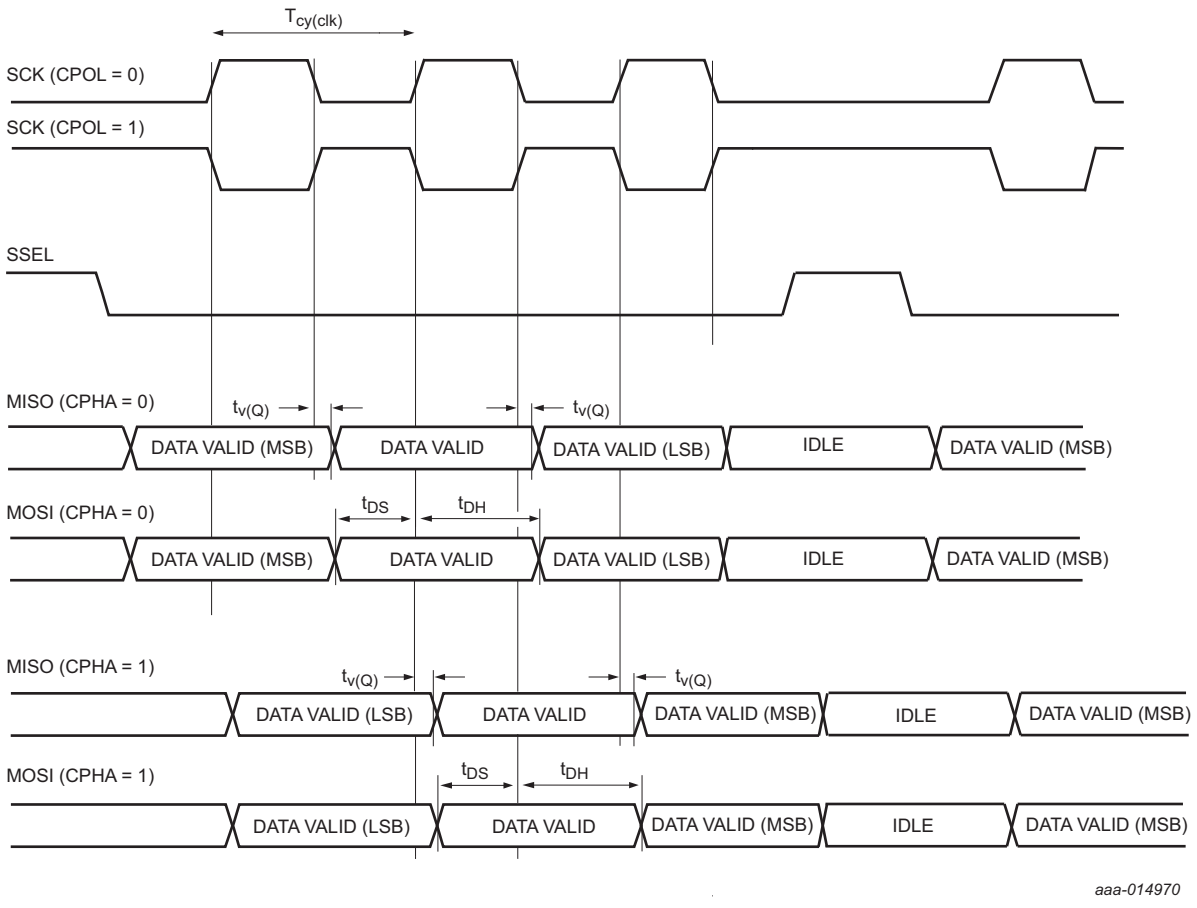

Fig 12. SPI slave timing

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12.10 USART interface

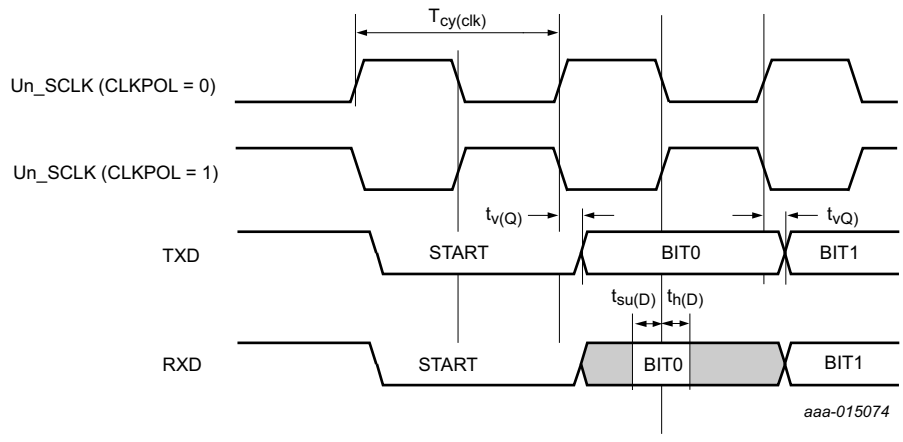
In master and slave synchronous modes, the maximum supported bit rate is 1 Mbit/sec.The actual bit rate depends on the delays introduced by the external trace, the external device, and capacitive loading.

Table 28. USART dynamic characteristics[1]

T_{amb} = –40 °C to 85 °C; V_{CC} = 1.62V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time		21	-	ns
$t_{h(D)}$	data input hold time		2	-	ns
$t_{v(Q)}$	data output valid time		–5	12	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		6	-	ns
$t_{h(D)}$	data input hold time		6	-	ns
$t_{v(Q)}$	data output valid time		–2	21	ns

[1] Based on simulated values.



In master mode, $T_{cy(clk)}$ = CLK_AHB/BRGVAL. See the QN908x *user manual*.

Fig 13. USART timing

12.11 SPIFI

Table 29. Dynamic characteristics: SPIFI[1]

T_{amb} = –40 °C to 85 °C; V_{CC} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time		-	62.5	-	ns
SPIFI						
t_{DS}	data set-up time		11	-	-	ns
t_{DH}	data hold time		4	-	-	ns
$t_{v(Q)}$	data output valid time		-5	-	7	ns

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[1] Based on simulated values.

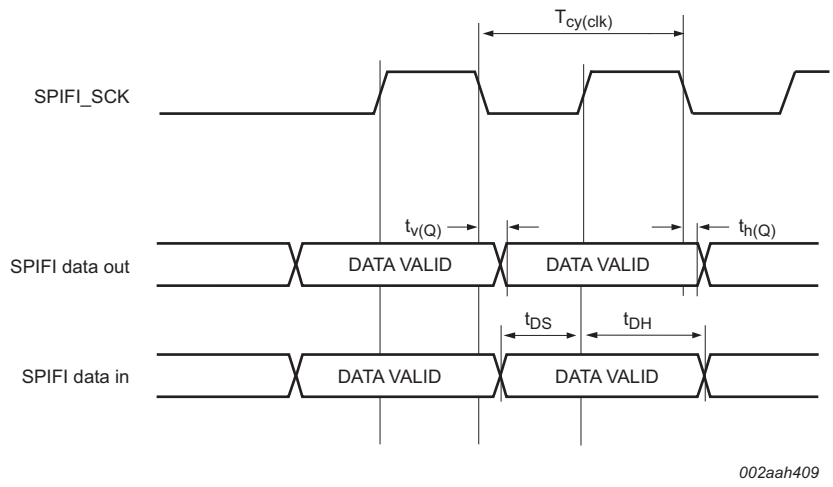

Fig 14. SPI flash interface timing (mode 0)

12.12 SCTimer output timing

Table 30. SCTimer output dynamic characteristics

T_{amb} = −40 °C to 85 °C; 1.62 V ≤ V_{CC} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at 10 % and 90 % of the signal level; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	1.1	ns

12.13 USB interface characteristics

Table 31. Dynamic characteristics: USB pins (full speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{CC}, unless otherwise specified; 3.0 V ≤ V_{CC} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	C_L=50pF, 10 % to 90 %		4	-	20	ns
t_f	fall time	C_L=50pF, 10 % to 90 %		4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90	-	111	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 15		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 15		-2	-	+5	ns
t_{JR1}	receiver jitter to next transition			-18.5	-	+18.5	ns

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Table 31. Dynamic characteristics: USB pins (full speed) *...continued*

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{CC}, unless otherwise specified; 3.0 V ≤ V_{CC} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		-9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 15	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 15	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

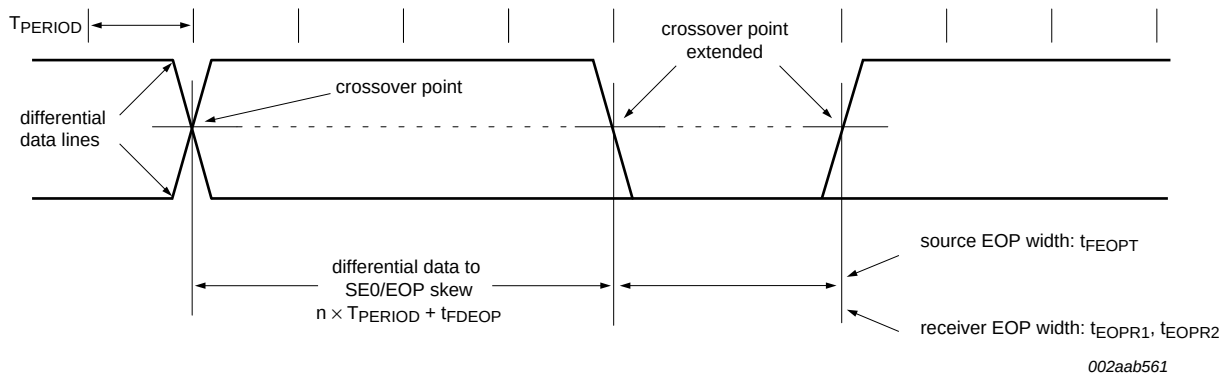

Fig 15. Differential data-to-EOP transition skew and EOP width

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13. RF characteristics

13.1 Receiver

Table 32. Receiver characteristics

T_{amb} = 25 °C; based on characterization; not tested in production. V_{CC} = 3 V; f_c = 2440 MHz; BER < 0.1 %

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S_{RX}	RX sensitivity	high performance mode with DC-to-DC converter disabled	-	–95	-	dBm
		low power mode with DC-to-DC converter	-	–94	-	dBm
S_{RX2M}	RX sensitivity (2Mbps)	DC-to-DC converter disabled	-	-92	-	dBm
		DC-to-DC converter enabled	-	-91.5	-	dBm
S_{GFSK}	GFSK RX sensitivity	250kbps, GFSK-BT=0.5, h=0.5	-	–95	-	dBm
$P_{i(max)}$	maximum input power		-	0	-	dBm
C/I	carrier-to-interference ratio	co-channel	-	6	-	dB
		adjacent channel @ ±1 MHz	-	–4	-	dB
		alternate channel @ ±2 MHz	-	–41	-	dB
α_{image}	image rejection		-	–41	-	dB
$\alpha_{sup(oob)}$	out-of-band suppression	30 MHz to 2000 MHz	–1	-	-	dBm
		2003 MHz to 2399 MHz	–10	-	-	dBm
		2484 MHz to 2997 MHz	–10	-	-	dBm
		3 GHz to 12.75 GHz	–10	-	-	dBm

Table 33.Receiver specification with GFSK modulations (Data Rate <= 1Mbps)

T_{amb} = 25 °C; based on characterization; not tested in production. V_{CC} = 3 V; f_c = 2440 MHz; BER < 0.1 %

GFSK BT=0.5,h=0.5		Adjacent/Alternate Channel Selectivity (dB)					
Data Rate (kbps)	Typical Sensitivity (dBm)	Desired signal level (dBm)	Interferer at -/+1* channel BW offset[1]	Interferer at -/+2* channel BW offset	Interferer at -/+3* channel BW offset	Interferer at -/+4* channel BW offset	Co-channel
1000	-95	-67	-6	-43	-46	-49	5
500	-95	-67	-5	-31	-33	-35	4
250	-95	-67	-9	-32	-36	-42	0

[1]Channel BW offset equals to 1MHz.

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Table 34.Receiver specification with GFSK modulations (Data Rate = 2Mbps)

T_{amb} = 25 °C; based on characterization; not tested in production. V_{CC} = 3 V; f_c = 2440 MHz; BER < 0.1 %

GFSK BT=0.5, h=0.5		Adjacent/Alternate Channel Selectivity (dB)					
Data Rate (kbps)	Typical Sensitivity (dBm)	Desired signal level (dBm)	Interferer at -/+2* channel BW offset[1]	Interferer at -/+4* channel BW offset	Interferer at -/+6* channel BW offset	Interferer at -/+8* channel BW offset	Co-channel
2000	-92	-67	-8	-44	-46	-51	5

[1]Channel BW offset equals to 1MHz.

13.2 Transmitter

Table 35. Transmitter characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.V_{CC} = 3 V; f_c = 2440 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(RF)}$	RF output frequency		2400	-	2483.5	MHz
α_{CS}	channel separation		-	2	-	MHz
P_o	output power	TX power	–20	-	+2	dBm

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14. Analog characteristics

14.1 BOD

Table 36. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		-	2.05	-	V
		de-assertion		-	2.35	-	V
		reset level 0					
		assertion		-	1.50	-	V
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.45	-	V
		de-assertion		-	2.80	-	V
		reset level 1					
		assertion		-	1.85	-	V
V_{th}	threshold voltage	interrupt level 2					
		assertion		-	2.70	-	V
		de-assertion		-	3.10	-	V
		reset level 2					
		assertion		-	2.0	-	V
V_{th}	threshold voltage	interrupt level 3					
		assertion		-	3.05	-	V
		de-assertion		-	3.45	-	V
		reset level 3					
		assertion		-	2.35	-	V

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14.2 ADC

Table 37.16-bit ADC static characteristics

T_{amb} = −40 °C to +85 °C; 1.62 V ≤ V_{CC} ≤ 3.6 V; VREFP = V_{DDA}; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage range (V_{INP}-V_{INN})	V_{REF} = 1.2 V		-	0.8 × VREF/(PGA_GAIN × ADC_GAIN)	-	
		V_{REF} = V_{CC}		-	0.5 × VREF/(PGA_GAIN × ADC_GAIN)	-	
C_i	input capacitance			-	10	-	pF
Z_i	input impedance	DC signal, PGA enabled		>10		-	MΩ
		DC signal, PGA bypassed, 2MHz sampling clock		-	50	-	kΩ
$f_{clk(ADC)}$	ADC sampling clock frequency			-	-	2	MHz
f_c	output date rate?			-	-	31.25	ksps
ENOB	Effective number	500 kHz sampling clock, over-sampling rate = 256, data rate = 1.9 kHz, all gains, all temperature, all Vcc		14.2	15.2	-	bit
		2 MHz sampling clock, over-sampling rate = 256, data rate = 7.8 kHz, all gains, all temperature, all Vcc		12.9	14.4	-	bit
INL	integral non-linearity	PGA enabled		-	+/-30[1]	+/-200	ppm
		PGA bypassed		-	+/-60[1]	+/-250	ppm
E_O	gain error			-	2	4	%
CMRR	common mode rejection	at DC	[2]	20	50	-	dB
PSRR	power-supply rejection	at DC		-40	-50	-	dB
V_{BG} (*25 °C*)	1.2V Bandgap voltage reference	T_{amb} = *25 °C*	[3][4]	1.216	1.222	1.227	V
V_{BG} (*-40~85 °C*)	1.2V Bandgap voltage reference	T_{amb} = *-40~85 °C*	[3][4]	1.211	-	1.232	V
	BG_SEL steps		[4]	-	3	-	mV

[1] Characterized but not implemented as production test. Guaranteed by design.

[2] CMRR degrades severely if Vcc < 3V

[3] BG_SEL = 0x08

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[4] All values are obtained at Vcc = 3V

14.3 Temperature sensor

Table 38. Temperature sensor static and dynamic characteristics
V_{DD} = V_{DDA} = 1.62 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_m (°C)	range	T_{amb} = –40 °C to +85 °C	-40	-	+85	°C
dT_m (°C)	error	with 1-point calibration	-	1	3	°C
		without calibration		3	5	°C

[1] Typical value is obtained at T_{amb} =25°C, V_{CC} / V_{DD} =3V

14.4 DAC

Table 39. DAC static and dynamic characteristics
V_{CC} = 1.62 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	resolution		-	8	-	bits
DNL	differential nonlinearity	[1]	-	0.2	-	LSB
INL	integral nonlinearity	[1]	-	0.2	-	LSB
	bandwidth of the internal low pass filter		-	150	-	kHz
V_{out}	output voltage range		0.7	-	V_{CC} – 0.7	V
	full scale output voltage swing step size		40	-	197	mV
	capacitive load stability	RL=1 kΩ	-	10	-	pF
	frequency of sample		-	-	1	MHz

[1] Characterized but not implemented as production test. Guaranteed by design.

14.5 Analog comparator

Table 40.Analog comparator static and dynamic characteristics
V_{CC} = 1.62 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_i	input voltage		0	-	V_{CC}	V
$I_{CC(int)A}$	analog internal supply current		-	0.3	-	µA
V_{hys}	hysteresis	use VBG as reference voltage (register bit ACMP_VREF_SEL=1,ACM_REF=8)	35	40	55	mV

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14.5.1 Capacitive sense

Table 41. Capacitive sense static and dynamic characteristics

V_{DD} = 1.62 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current		-	2.6	-	μA
	noise level		-	0.2%	-	/base cap
	temperature coefficient		-	0.02	-	%/°C
	input cap range		-	-	100	pF

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15. Application information

15.1 Schematic for QN9080 with DC-to-DC converter

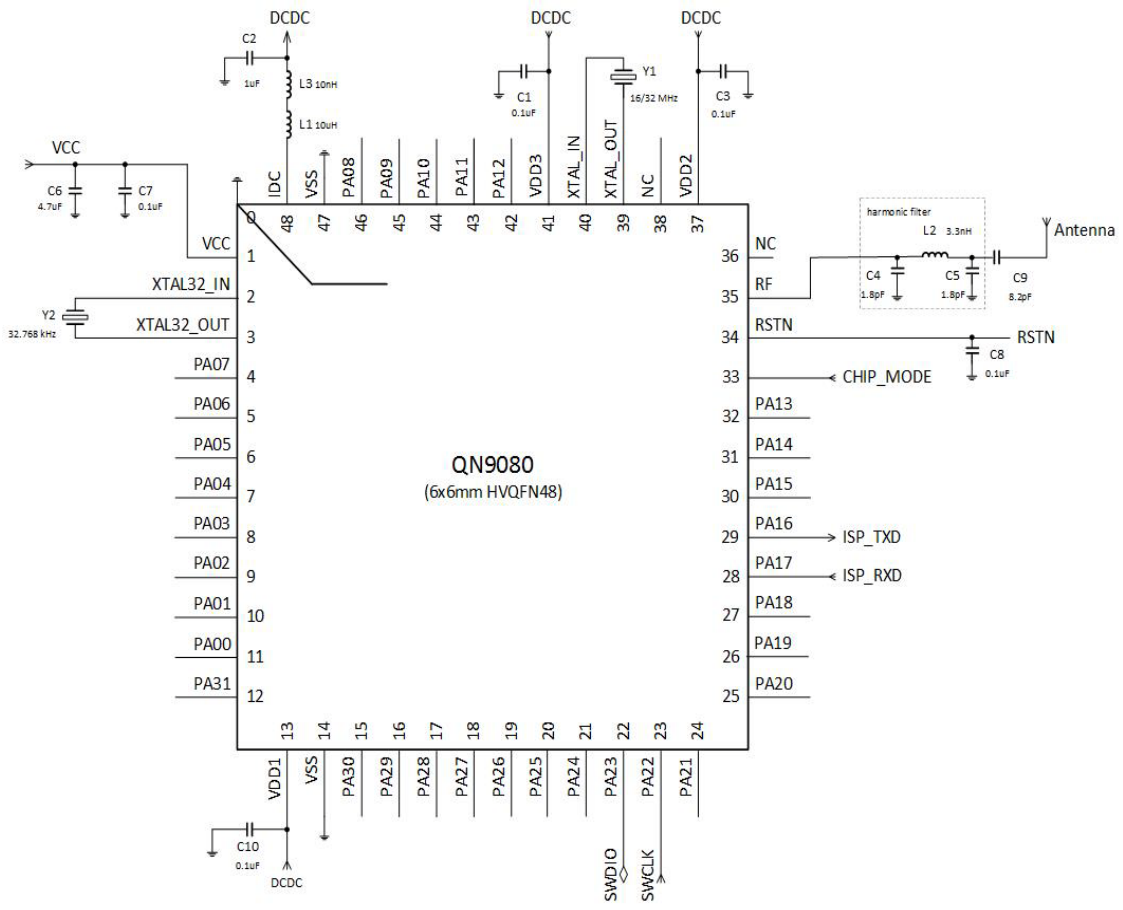

Fig 16. QN9080 typical application schematic with DC-to-DC converter

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15.2 Schematic for QN9080 without DC-to-DC converter

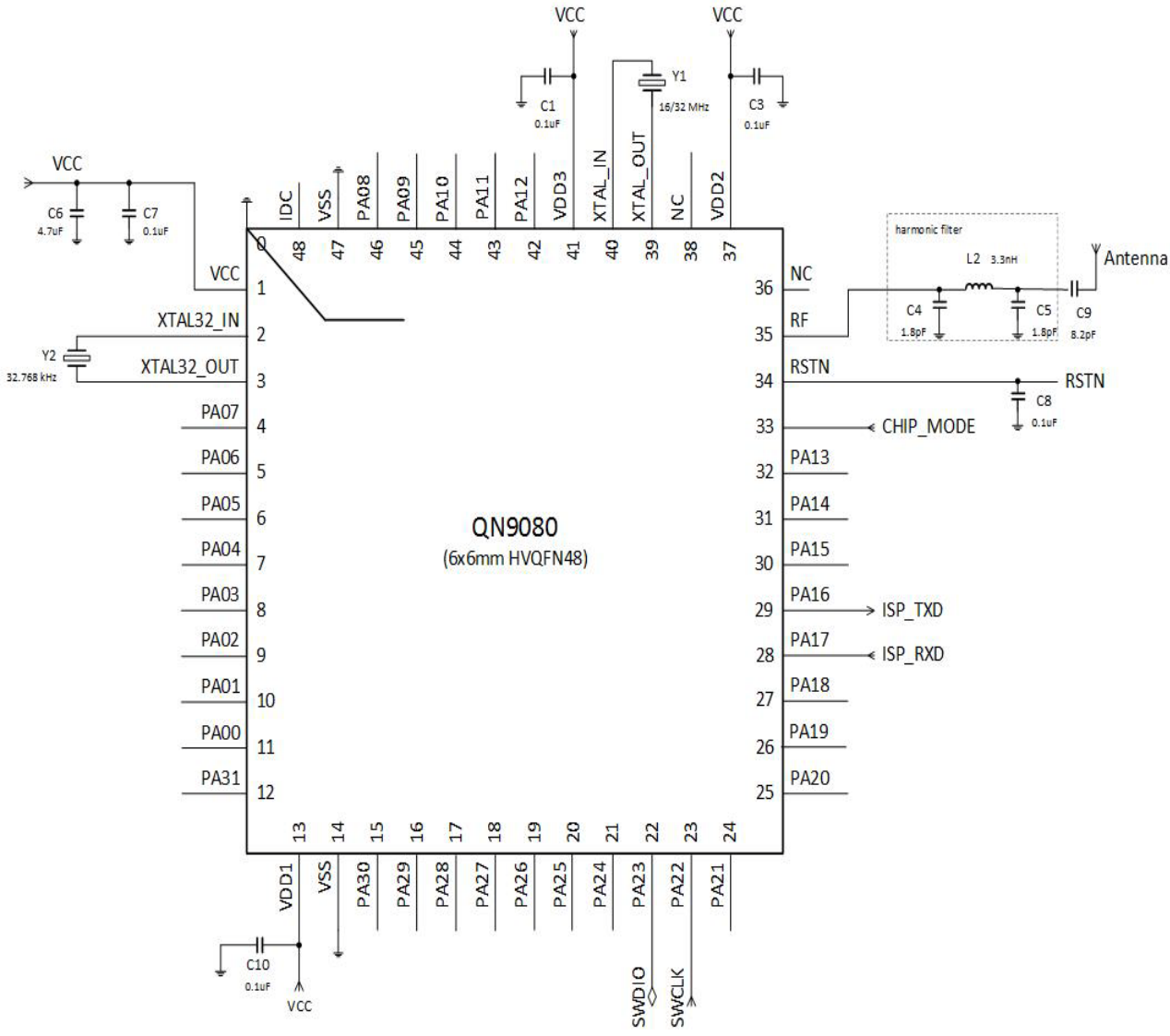

Fig 17. QN9080 typical application schematic without DC-to-DC converter

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15.3 Schematic for QN9083 with DC-to-DC converter

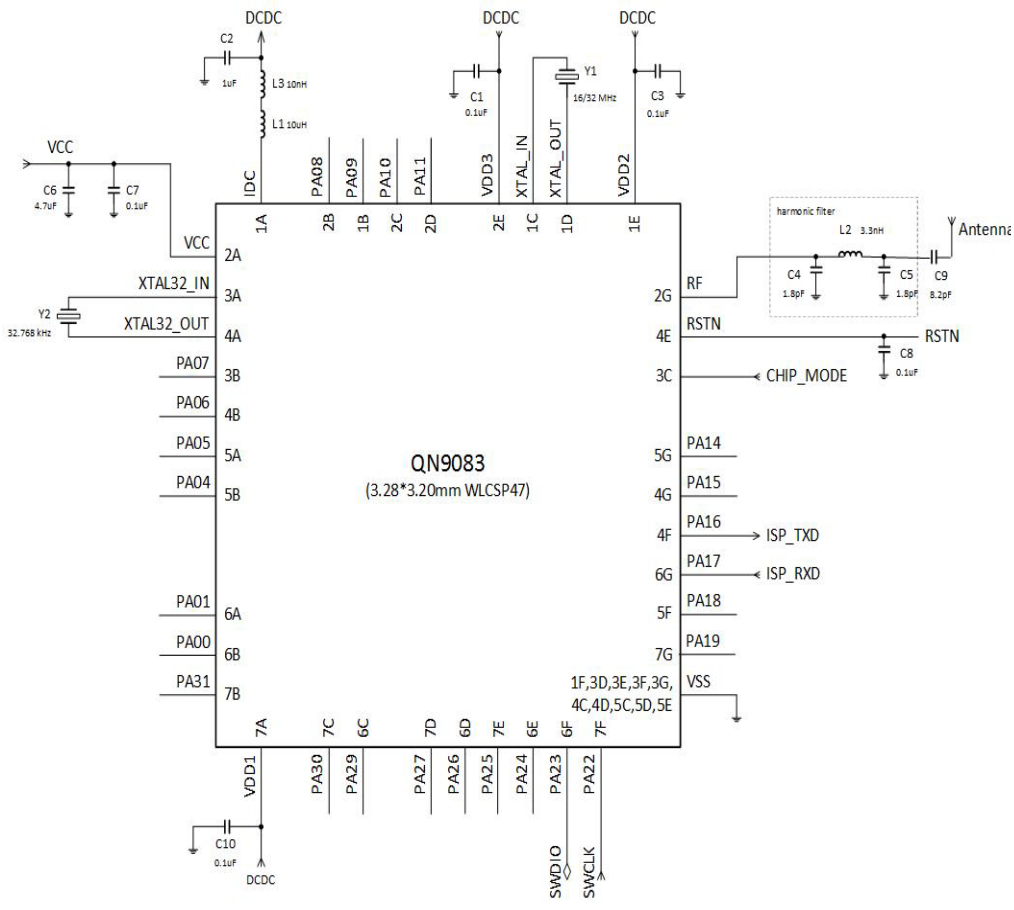

Fig 18. QN9083 typical application schematic with DC-to-DC converter

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15.4 Schematic for QN9083 without DC-to-DC converter

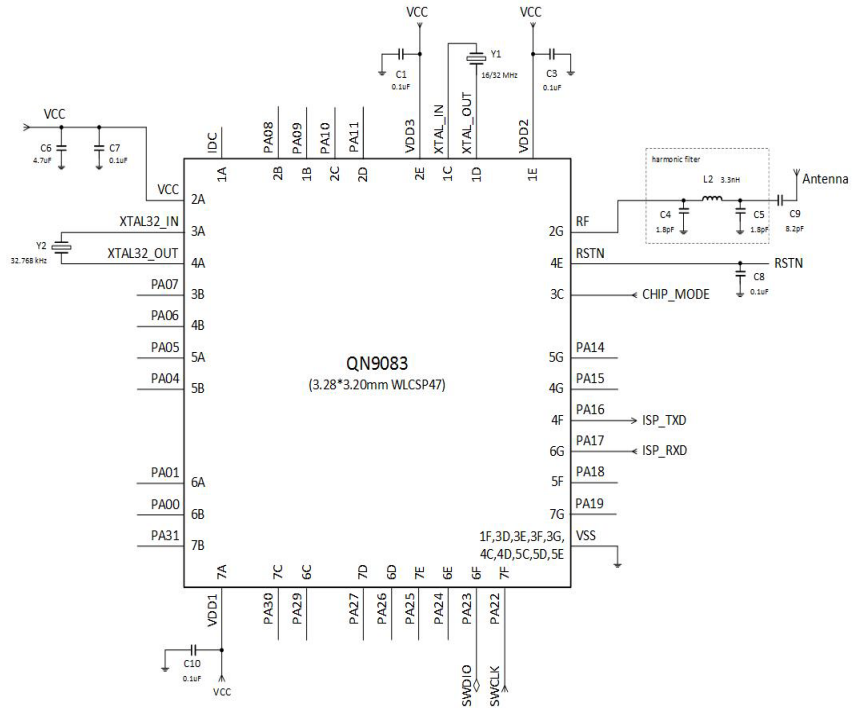

Fig 19. QN9083 typical application schematic without DC-to-DC converter

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15.5 QN908x external component list

Table 42. External component list

Component	Description	Value
C4	capacitor for RF harmonic filter	1.8 pF
C5	capacitor for RF harmonic filter	1.8 pF
C1, C3, C7, C10	supply decoupling capacitors	100 nF, X5R, ±10 %, 6.3 V, 0402
C6	supply decoupling capacitor	4.7 μF, X5R, ±10 %, 6.3 V, 0402
C2	supply decoupling capacitor	1 μF, X7R, ±5 %, 6.3 V, 0402
C8	capacitor used for reset	0.1 μF, ±5 %, 6.3 V, 0402
C9	capacitor used for RF front-end	8.2 pF, C0G, ±0.5pF, 50V, 0402
L2	inductor for RF harmonic filter	3.3 nH
L1	chip inductor for DC-to-DC converter	10 μH
L3	chip inductor for DC-to-DC converter	10 nH
Y1	crystal	16 MHz or 32 MHz
Y2	crystal	32.768 kHz

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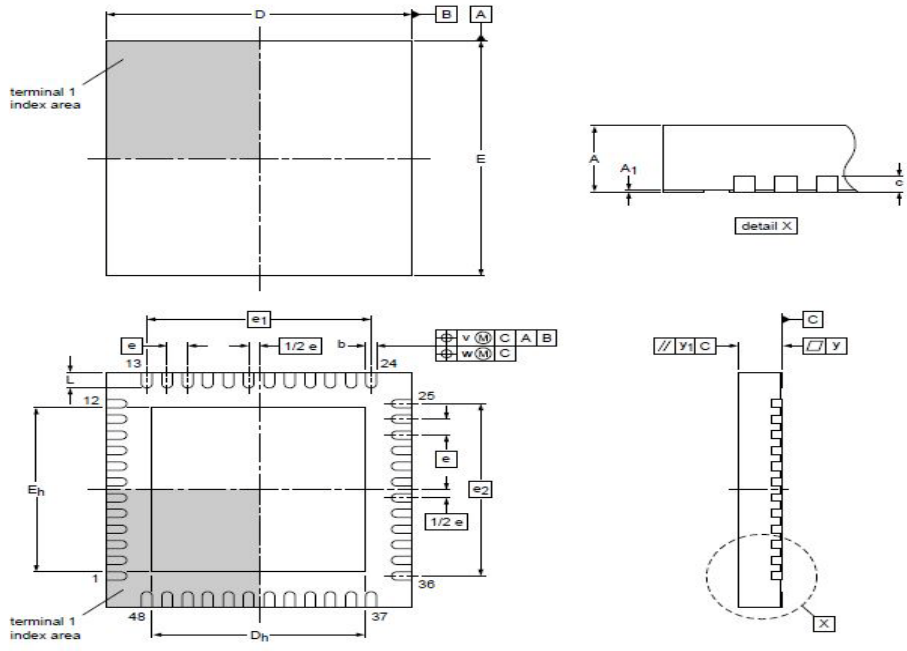
16. Package outline

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 x 6 x 0.85 mm — **SOT778-7**



Dimensions: (mm are the orginal dimensons)

Unit		$A^{(1)}$	A_1	b	c	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.90	0.05	0.26		6.1	4.25	6.1	4.25				0.45				
	nom	0.85	0.02	0.21	0.2	6.0	4.20	6.0	4.20	0.4	4.4	4.4	0.40	0.1	0.1	0.05	0.1
	min	0.80	0.00	0.16		5.9	4.15	5.9	4.15				0.35				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot778-7_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT778-7		- - -				~~15-12-03~~ 15-12-17

Fig 20. HVQFN48 package outline

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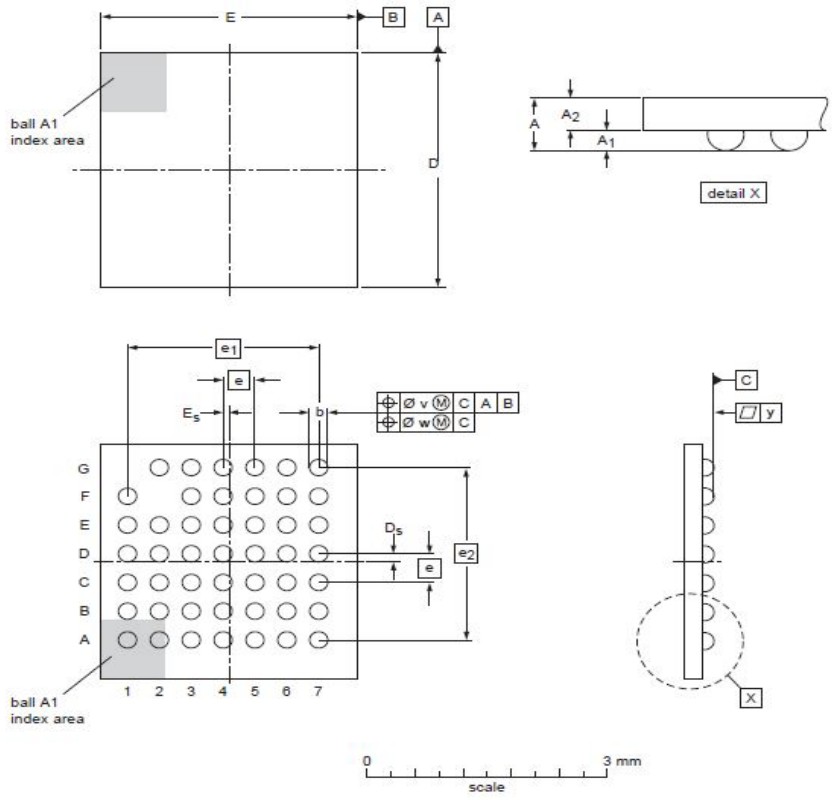
WLCSP47: wafer level chip-scale package; 47 bumps; 3.28 x 3.20 x 0.365 mm

SOT1882-1



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_s	E	E_s	e	e_1	e_2	v	w	y
mm	max	0.395	0.155	0.250	0.26	3.31		3.23							
	nom	0.365	0.140	0.225	0.23	3.28	0.115	3.20	0.075	0.4	2.4	2.4	0.05	0.015	0.03
	min	0.335	0.125	0.200	0.20	3.25		3.17							

sot1882-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1882-1		- - -				~~16-07-27~~ 16-08-01

Fig 21. WLCSP Package outline

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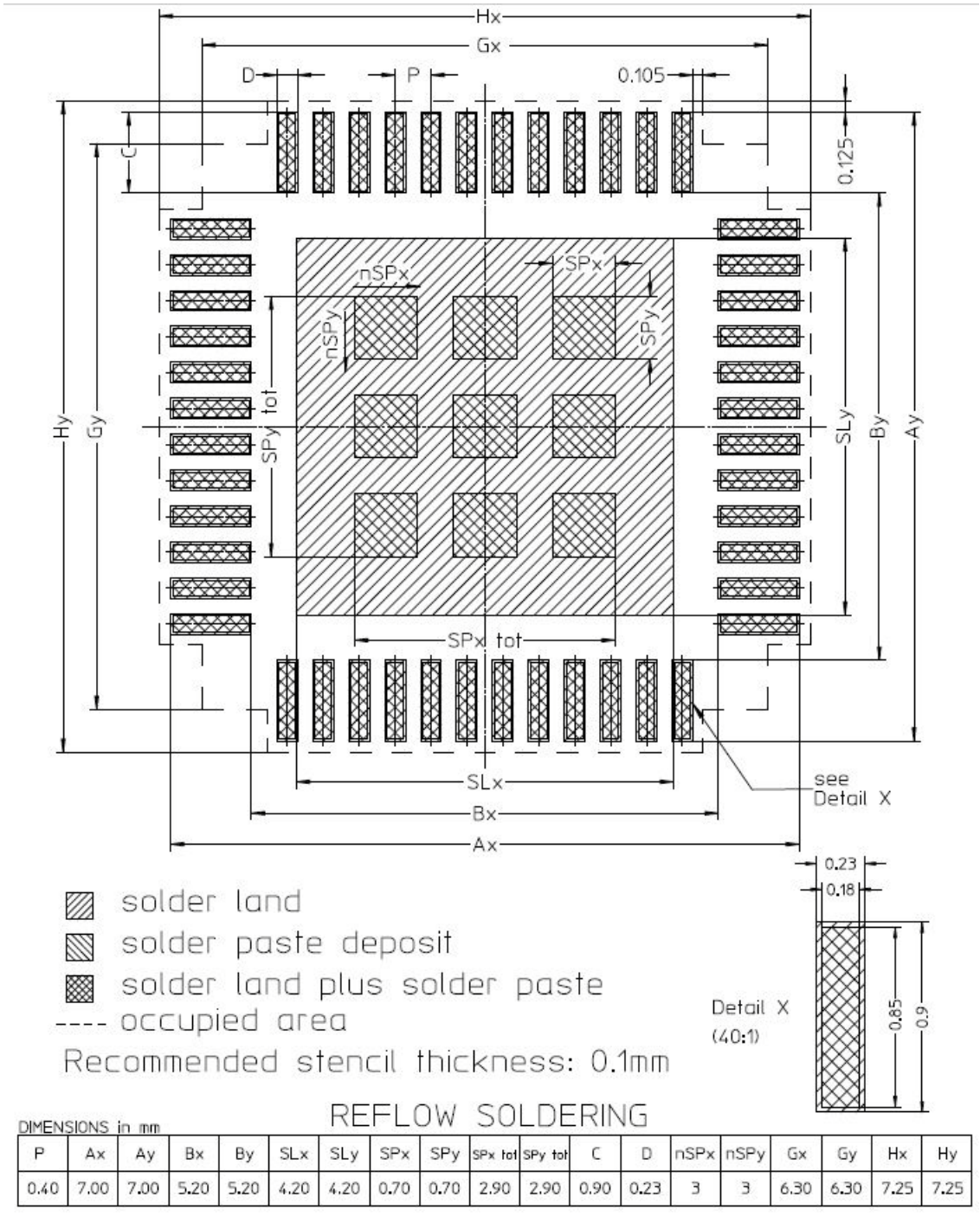
17. Soldering



P	Ax	Ay	Bx	By	SLx	SLy	SPx	SPy	SPx tot	SPy tot	C	D	nSPx	nSPy	Gx	Gy	Hx	Hy
0.40	7.00	7.00	5.20	5.20	4.20	4.20	0.70	0.70	2.90	2.90	0.90	0.23	3	3	6.30	6.30	7.25	7.25

Fig 22. HVQFN48 Soldering footprint

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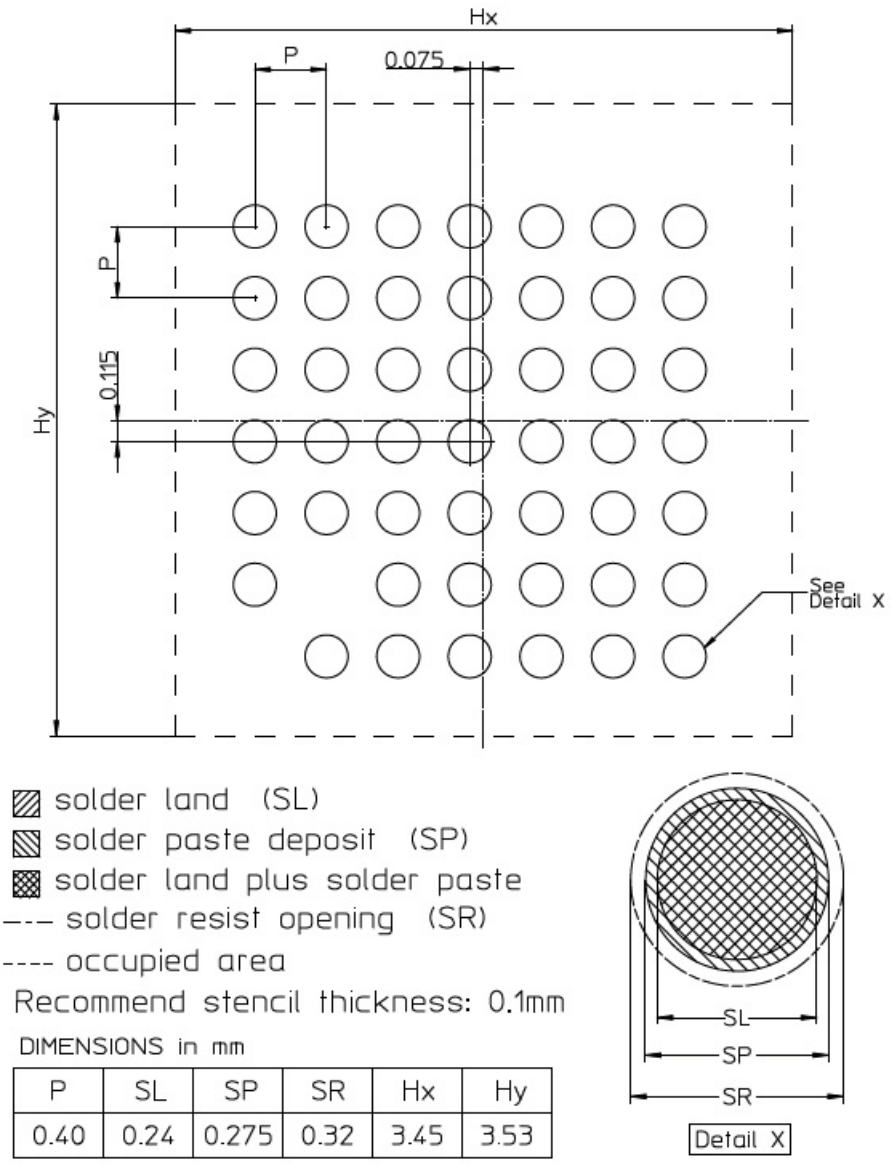

P	SL	SP	SR	Hx	Hy
0.40	0.24	0.275	0.32	3.45	3.53

Fig 23. WLCSP Soldering footprint

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18. Abbreviations

Table 43. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
GPIO	General-Purpose Input Output
LSB	Least Significant Bit
MCU	MicroController Unit
SPI	Serial Peripheral Interface
USART	Universal Asynchronous Receiver/Transmitter
TTL	Transistor-Transistor Logic
ENOB	Equivalent Number of Bits

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19. Revision history

Table 44. Revision history

Document ID	Release date	Substantial changes	Supersedes
QN908x Rev.1.2	04/2018	Add Silicon revision in Table 2.	QN908x v.1.1
QN908x Rev.1.1	02/2018	Append characteristics data	QN908x v.1.0
QN908x Rev.1.0	07/2017	Initial Release	-

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[2] The term 'short data sheet' is explained in section "Definitions".

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