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1. General Description

The KD125 is a member of LCD driver IC series developed by King Billion Electronics Co. It's a 120-output common/segment LCD driver IC suitable for driving small/medium scale dot matrix LCD panels, used in PDA or electronic dictionary. The KD125 is good as a segment driver, common driver or common/segment driver, and it can create a low power consuming, high-resolution LCD. The KD125 have eight modes can selected to set common and segment numbers by control register. The KD125 also has built-in analog regulator and DC/DC converter and they can be enabled or disabled to use external LCD power system for larger LCD panel.

2. Features

- Number of LCD drive outputs: 120 COM/SEG
- Supply voltage for LCD drive: **Max +16V**
- Supply voltage for the logic system: +2.4 to +4 V
- LCD display duty selectable by control register
- 8 LCD Configurations: 0COM/120SEG, 32COM/88SEG, 48COM/72SEG, 64COM/56SEG, 80COM/40SEG, 96COM/24SEG, 112COM/8SEG, 120COM/0SEG.
- Low power consumption and low output impedance
- Built-in LCD voltage regulator and booster circuit (with Boost ratio of 2X/3X/4X/5X/6X)
- Bias configuration: 1/6 ~ 1/12 bias.
- Bus width selectable: 1-bit series / 4-bit parallel modes.
- Package: 154-pin COB (Pad Size:80um×80um, Pad Pitch: 95um×95um).

(Segment mode)

- Shift clock frequency

  15 MHz (MAX.): VDD = +3.0 to + 4 V

  12 MHz (MAX.): VDD = +2.4 to + 3.0 V
- 4-bit parallel / serial input modes are selectable with a mode (P/S) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 88、72、56 、40、24、8 or 120 bits of input data
- Line latch circuits are reset when XDISPOFF active

(Common mode)

- Shift clock frequency: 4 MHz (MAX.)

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- Built-in X-bit shift register
- Available in a single mode
- Y_1->Y_X Single mode

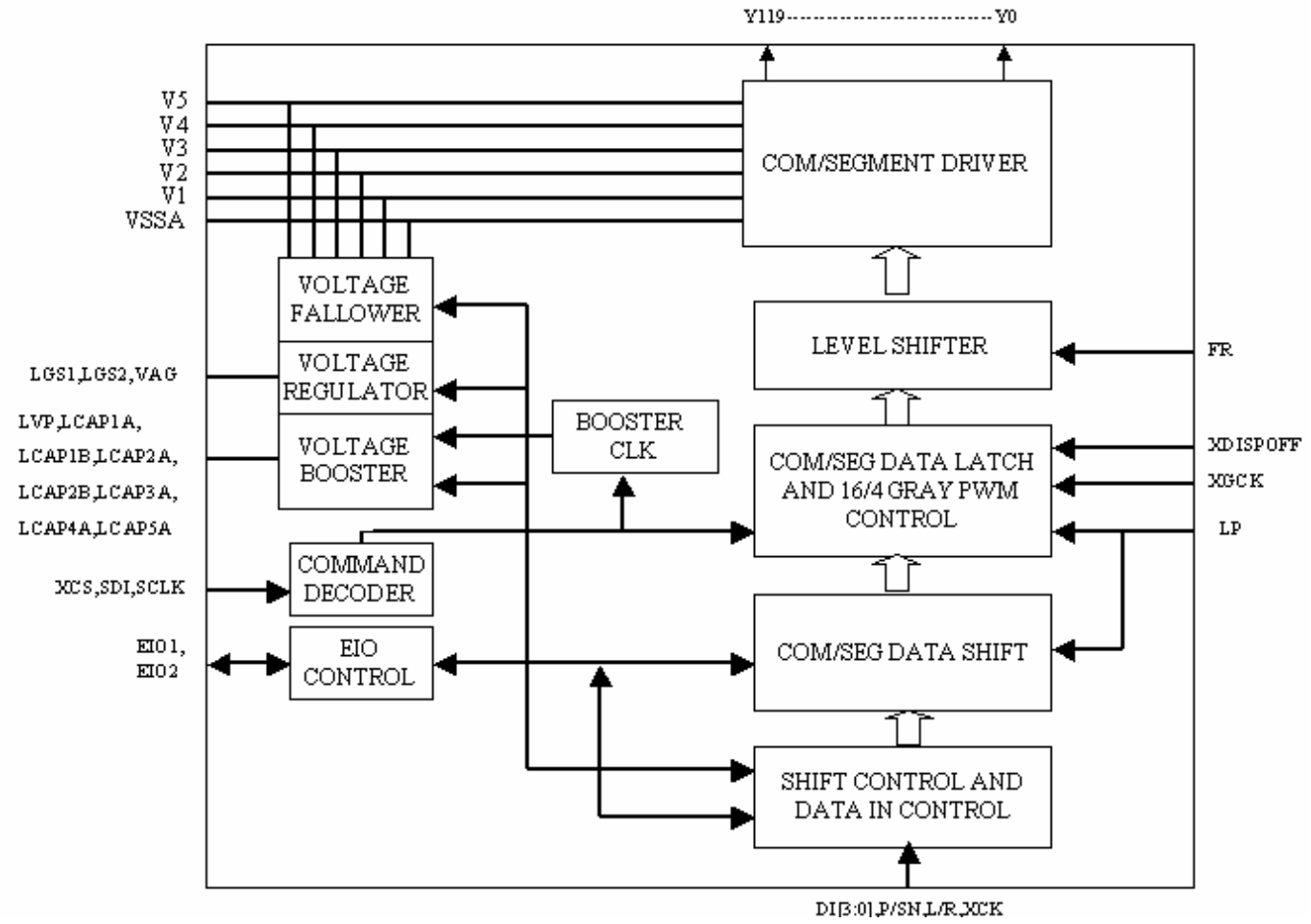
  Y_X->Y_1 Single mode

  X=32、48、64、80、96、112、120
- Shift register circuits are reset when XDISPOFF active

(16 Levels Gray Display)

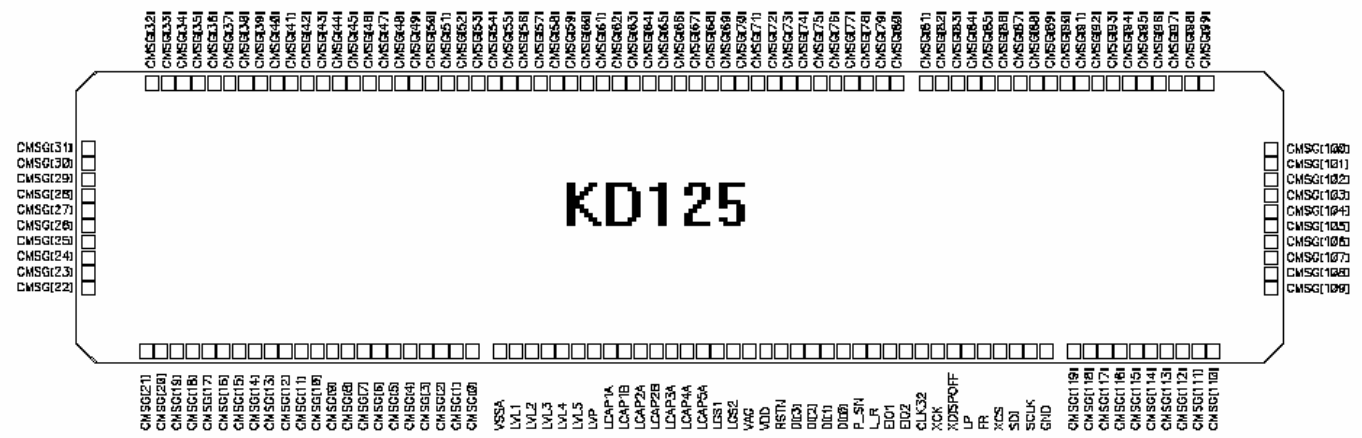
- B/W, 4 and 16 gray levels can be displayed by the pulse width modulation.

3. Block Diagram



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4. Pin Description



Pin Name	I/O	Description
Y[119..0]/CMSG[119:0]	O	LCD driver Common/Segment outputs
V[5:1]	P	Power supply for LCD driver, Connect a capacitor between this terminal and GND.V5 ≧ V4 ≧ V3 ≧ V2 ≧ V1 ≧ GND.
LVP	P	DC/DC charge pump voltage, connect a capacitor between this terminal and GND. .LVP ≧ V5
LCAP1A	O	DC/DC charge pump converter pad.
LCAP1B	O	DC/DC charge pump converter pad.
LCAP2A	O	DC/DC charge pump converter pad.
LCAP2B	O	DC/DC charge pump converter pad.
LCAP3A	O	DC/DC charge pump converter pad.
LCAP4A	O	DC/DC charge pump converter pad.
LCAP5A	O	DC/DC charge pump converter pad.
LGS1	I	Regulator voltage setting pin(adjust V5 voltage)
LGS2	I	Regulator voltage setting pin(adjust V5 voltage)
VAG	O	Internal reference voltage.
VDD	P	Positive Power Input. Adding 0.1 μF capacitor as by-pass capacitor on power pins is necessary.(within 1 cm distance)
RSTn	**I**	**System Reset pin .When low level active.** **The XRST L PULSE timing min value is 200us and max value is 0.5s**

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Pin Name	I/O	Description
GND x2	P	Power ground pads.
DI[3:0]	B	Command/Data I/O port. All these pins are in push-pull mode DIO[3:0] pin is used for nibble mode data transferring.
P/Sn	B	This is the parallel data input/serial data input switch terminal. P/S="H": Parallel data input. P/S="L": Serial data input.
L/R	I	Input pin for selecting the reading direction of display data When set to GND level "L", data is read sequentially from Y119 to Y0. When set to VDD level "H", data is read sequentially from Y0 to Y119.
EIO2, EIO1	I/O	Input/output for chip selection at segment mode and FLM input output function at COM/SEG mix mode or common mode.
XGCK	I	Clock input for 16 level clock source
XCK	I	Clock input for taking display data at segment mode
XDISPOFF	I	Control input for output of non-select level
LP	**I**	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
FR	**I**	AC-converting signal input for LCD drive waveform
XCS	I	This is the command mode select pin. When XCS="L" then write command to the LCD.
SDI	I	The series command data input pin.
SCLK	I	The series command clock input pin.

5. Control Registers

There are 97 control bits used to configure the KD125. The charge-pump and current follower bias circuit are included in KD125. These 97 control bits are written by the series interface of XCS, SDI, SCLK. The timing is shown as below diagram, and the function descriptions of control bits are summarized in following table.

Bit[14:13]	Bit12	Bit11	Bit10	Bit9	Bit[8:6]	Bit[5:3]	Bit[2:0]	Reset Value

Gray[1:0]	BLANK	BUFE	CPUMPE	PDOWN	VADJ[2:0]	Bias[2:0]	COM[2:0]	0000_0000_0000

Bit[39:35]	Bit[34:30]	Bit[29:25]	Bit[24:20]	Bit[19:15]	Reset Value
GRAY4[4:0]	GRAY3[4:0]	GRAY2[4:0]	GRAY1[4:0]	GRAY0[4:0]	0000_0000_0000

Bit[64:60]	Bit[59:55]	Bit[54:50]	Bit[49:45]	Bit[44:40]	Reset Value
GRAY9[4:0]	GRAY8[4:0]	GRAY7[4:0]	GRAY6[4:0]	GRAY5[4:0]	0000_0000_0000

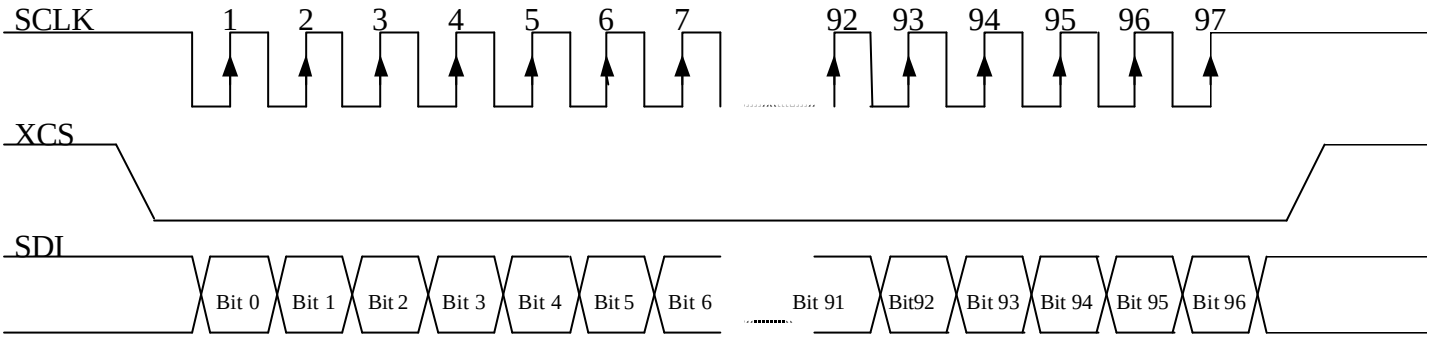
Bit[89:85]	Bit[84:80]	Bit[79:75]	Bit[74:70]	Bit[69:65]	Reset Value
GRAY14[4:0]	GRAY13[4:0]	GRAY12[4:0]	GRAY11[4:0]	GRAY10[4:0]	0000_0000_0000

Bit[96:95]	Bit[94:90]	Reset Value
CPCK[1:0]	GRAY15[4:0]	0000_0000_0000

Name	Description
Cpck[1:0]	Charge pump clock select 00:32k 01:64k 10:128k 11:256k
GRAY0[4:0] ~ GRAY15[4:0]	The mapping register between the levels selected in shift data and the real gray scale if the content of GRAY1 is 0x01, when value of a certain pixel is 1 the displayed effect will correspond to actual gray level 1, the 16 gray scale display use all 16 registers GRAY0 ~ GRAY15 to select among 32 available gray levels to correspond to level 0 ~ 15, when 4 gray scale display utilizes registers GRAY0 ~ GRAY3 to select among 32 gray levels to correspond to level 0 ~ 15.
Gray[1:0]	“00”: Black/White display. “01”: 4 levels gray display. “10”:16 levels gray display. “11”:Reserved
BLANK	0: Normal Display 1: LCD display blanked. The COM signals of LCD driver output inactive levels (V4

Name	Description
	and V1) while SEG signals output normal display patterns.
PDOWN	1:LCD charge pump disable 0:LCD charge pump enable
BUFE	1: Disable internal bias network buffer, LV1~5 are provided externally. 0: Enable internal bias network buffer.
CPUMPE	1: Internal charge-pump is disabled and LCD power is supplied externally. 0: Internal charge-pump is enabled.
VADJ[2:0]	LCD Contrast Adjustment (±0%) "111":-10% Darkest, "110":-7% "101":-4% "100":-1% "011":+1% "010::+4% "001":+7% "000": +10% Lightest.
Bias[2:0]	LCD Power System Bias Configuration **"000": Reserved** "001": 1/6 Bias "010": 1/7 Bias "011": 1/8 Bias "100": 1/9 Bias "101": 1/10 Bias "110": 1/11 Bias "111":1/12 Bias
COM[2:0]	LCD COM/SEG Output Configuration Mode "000": 128 SEG "001": 32 COM × 88 SEG "010": 48 COM × 72 SEG "011": 64 COM × 56 SEG "100": 80 COM × 40 SEG

Name	Description
	"101": 96 COM × 24 SEG "110": 112 COM × 8 SEG "111": 120 COM



Control Register Write Timing

6. LCD Power System

The internal regulator, charge-pump and current follower bias circuits are built in to provide the LCD power system, when the internal LCD power system is used by set CPUMPE and BUFE bits. If the external LCD power is provided, the internal LCD power system shall be disabled by clear the CPUMPE bit. The following table shows the relationship of LCD power system.

Bit[14:13]	Bit12	Bit11	Bit10	Bit9	Bit[8:6]	Bit[5:3]	Bit[2:0]	Reset Value
Gray[1:0]	BLANK	BUFE	CPUMPE	PDOWN	VADJ[2:0]	Bias[2:0]	COM[2:0]	0000_0000_0000

PDOWN	CPUMPE	BUFE	Function
0	0	0	Internal charge-pump and current follower Bias circuit are enabled to supply the LCD display power.
0	0	1	Internal charge-pump system is enabled, but the current follower Bias circuit is disabled, and the external power sources are applied LV5~LV1.
0	1	0	Internal charge-pump system is disabled, but the current follower Bias circuit

			is enabled. The single external power is applied to LVP, and internal bias circuit will generate the LV5~LV1 voltages.
0	1	1	Internal charge-pump and current follower Bias circuit are disabled, and the external power sources are applied to LVP and LV5~LV1 pads.
1	0	0	The lcd power system is disable, but the LVP is applied to VDD and LV5~LV1 is applied to high impedance.
1	0	1	The lcd power system is disable, but the LVP is applied to VDD and LV5~LV1 is applied to high impedance.
1	1	0	The lcd power system is disable, but the LVP and LV5~LV1 is applied to high impedance.
1	1	1	The lcd power system is disable, but the LVP and LV5~LV1 is applied to high impedance.

The boost circuit charge pump regulated voltage to LCD highest voltage LVP (3~6 times of VDD voltage).The set-up voltage generated at LVP output the V5 through the voltage regulator circuit.

The LCD voltage(V5) can also be fine-tuned (in ±10% range) through the VADJ[2:0] bits. The LCD voltage levels V1~V5 shall be configured properly by the Bias[2:0] bits based on the LCD duty and LCD highest voltage. The following table is a general configuration relationship for the LCD duty and bias.

Duty	Bias
1/32	1/6 or 1/7
1/48	1/7 or 1/8
1/64	1/8 or 1/9
1/80	1/8 or 1/9
1/96	1/9 or 1/10
1/112	1/10 or 1/11
1/120	1/11 or 1/12

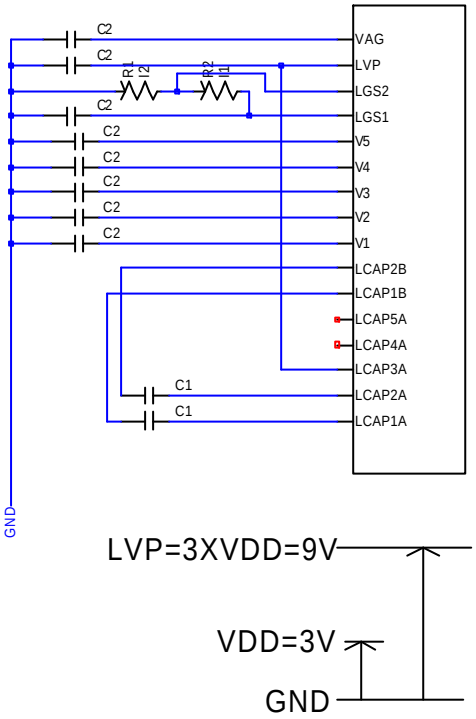
Voltage charge pump: The VDD voltage is then boosted up by 3, 4, 5, or 6 times to generate LVP, depending on external capacitors configurations as shown below. Please note that LVP must be lower than maximum operation voltage to prevent chip from break-down. The capacitance of capacitors connected to LVP and V1~V5 shall be increased in an appropriate amount based on the LCD panel size. For small size

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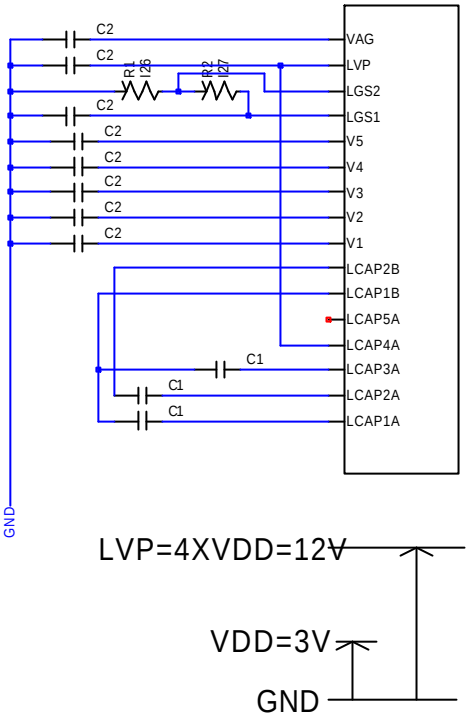
LCD panel, the **0.1uF** capacitors are enough, but **(1uF~10uF)** or bigger capacitors may be necessary for larger LCD size application..

.The setup-up voltage circuits

3X set-up voltage circuit

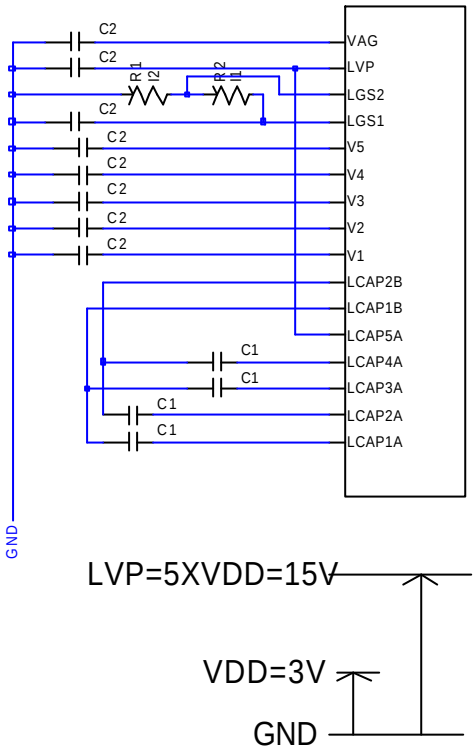


4X set-up voltage circuit

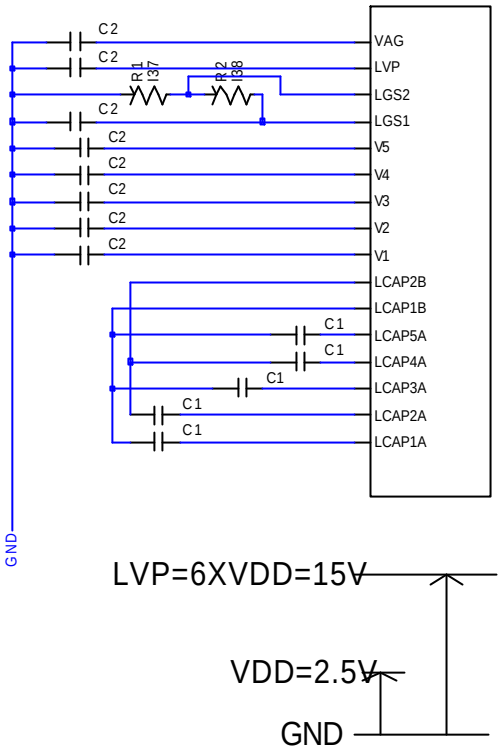


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5X set-up voltage circuit



6X set-up voltage circuit



C1 and C2 are determined by the size of the LCD being driven (0.1u~10u)

.The voltage regulator circuit:

VADJ[2:0]	ADJ
000	+10%
001	+7%
010	+4%
011	+1%
100	-1%
101	-4%
110	-7%
111	-10%

V5=(1+R2/R1)*(1V±Vref*ADJ)

Charge pump times	Vref	Condition : VDD = 3.3V
6X	1.7	
5X	1.2	
4X	1.2	

3X	1.2	
Use LVP (external power)	0.9	

The R1 resistor is connected between LGS2 and ground and R2 is connected to LGS1 and LGS2. LGS1 pin is sensitive to noise. Vref will change if LGS1 pin is coupled with noise. Please take care in PCB layout. The metal wire between LGS1 to R1 R2 resistor is as short as possible.

7. Relationship between Display Data and LCD Driver Pins

16-level Gray Scale Display with PWM

DISPLAY DATA				
DI[3]	DI[2]	DI[1]	DI[0]	GRAY SCALE REGISTER
0	0	0	0	GRAY0(GRAY LEVEL0)
0	0	0	1	GRAY1(GRAY LEVEL1)
0	0	1	0	GRAY2(GRAY LEVEL2)
0	0	1	1	GRAY3(GRAY LEVEL3)
0	1	0	0	GRAY4(GRAY LEVEL4)
0	1	0	1	GRAY5(GRAY LEVEL5)
0	1	1	0	GRAY6(GRAY LEVEL6)
0	1	1	1	GRAY7(GRAY LEVEL7)
1	0	0	0	GRAY8(GRAY LEVEL8)
1	0	0	1	GRAY9(GRAY LEVEL9)
1	0	1	0	GRAY10(GRAY LEVEL10)
1	0	1	1	GRAY11(GRAY LEVEL11)
1	1	0	0	GRAY12(GRAY LEVEL12)
1	1	0	1	GRAY13(GRAY LEVEL13)
1	1	1	0	GRAY14(GRAY LEVEL14)
1	1	1	1	GRAY15(GRAY LEVEL15)

4-level Gray Scale Display with PWM

DISPLAY DATA		
DI[3]/DI[1]	DI[2]/DI[0]	GRAY SCALE REGISTER
0	0	GRAY0(GRAY LEVEL0)
0	1	GRAY1(GRAY LEVEL1)
1	0	GRAY2(GRAY LEVEL2)
1	1	GRAY3(GRAY LEVEL3)

-Gray Scale REGISTER of 32 PWM (Pulse Width Modulate)

DEC	GRAY SCALE REGISTER(5 BIT)	PWM	NOTE
0	00000	0	BRIGHTER
1	00001	2/32	
2	00010	3/32	
3	00011	4/32	
4	00100	5/32	
5	00101	6/32	
….	…….		

….	…….		
….	…….		
….	…….		
28	11100	29/32	
29	11101	30/32	
30	11110	31/32	
31	11111	1	DARKER

Segment Mode

Black/White Display (4-bit Parallel Input Mode)

L/R	EIO_1	EIO_2	Data Input	Number of Clocks						
				30 CLOCK	29 CLOCK	28 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI[0]	Y0	Y4	Y8	…	Y108	Y112	Y116
			DI[1]	Y1	Y5	Y9	…	Y109	Y113	Y117
			DI[2]	Y2	Y6	Y10	…	Y110	Y114	Y118
			DI[3]	Y3	Y7	Y11	…	Y111	Y115	Y119
H	Input	Output	DI[0]	Y119	Y115	Y111	…	Y11	Y7	Y3
			DI[1]	Y118	Y114	Y110	…	Y10	Y6	Y2
			DI[2]	Y117	Y113	Y109	…	Y9	Y5	Y1
			DI[3]	Y116	Y112	Y108	…	Y8	Y4	Y0

Black/White Display (1-bit Series Input Mode)

L/R	EIO_1	EIO_2	Data Input	Number of Clocks						
				120 CLOCK	119 CLOCK	118 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI[0]	Y0	Y1	Y2	…	Y117	Y118	Y119
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x
H	Input	Output	DI[0]	Y119	Y118	Y117	…	Y2	Y1	Y0
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x

x: Don't care, should be fixed to "H" or "L", avoiding floating.

4 Levels Gray Display (4-bit Parallel Input Mode)

L/R	EIO_1	EIO_2	Data Input	Number of Clocks						
				60 CLOCK	59 CLOCK	58 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI[0]	Y0 (0)*	Y2 (0)	Y4 (0)	…	Y114 (0)	Y116 (0)	Y118 (0)
			DI[1]	Y0 (1)*	Y2 (1)	Y4 (1)	…	Y114 (1)	Y116 (1)	Y118 (1)

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			DI[2]	Y1 (0)	Y3 (0)	Y5 (0)	…	Y115 (0)	Y117 (0)	Y119 (0)
			DI[3]	Y1 (1)	Y3 (1)	Y5 (1)	…	Y115 (1)	Y117 (1)	Y119 (1)
H	Input	Output	**DI[0]**	Y119 (0)	Y117 (0)	Y115 (0)	…	Y5 (0)	Y3 (0)	Y1 (0)
			DI[1]	Y119 (1)	Y117 (1)	Y115 (1)	…	Y5 (1)	Y3 (1)	Y1 (1)
			DI[2]	Y118 (0)	Y116 (0)	Y114 (0)	…	Y4 (0)	Y2 (0)	Y0(0)
			DI[3]	Y118 (1)	Y116 (1)	Y114 (1)	…	Y4 (1)	Y2 (1)	Y0(1)

(1): 2nd bit, msb; (0): 1st bit, lsb.

4 Levels Gray Display (1-bit Series Input Mode)

L/R	**EIO_1**	**EIO_2**	**Data Input**	**Number of Clocks**						
				240 CLOCK	**239 CLOCK**	**238 CLOCK**	**…**	**3 CLOCK**	**2 CLOCK**	**1 CLOCK**
L	Output	Input	**DI[0]**	Y0 (0)*	Y0 (1)*	Y1 (0)	…	Y118 (1)	Y119 (0)	Y119 (1)
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x
H	Input	Output	**DI[0]**	Y119 (0)	Y119 (1)	Y118 (0)	…	Y1 (1)	Y0 (0)	Y0 (1)
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x

(1): 2nd bit, msb; (0): 1st bit, lsb. x: Don't care, should be fixed to "H" or "L", avoiding floating.

16 Levels Gray Display (4-bit Parallel Input Mode)

L/R	**EIO_1**	**EIO_2**	**Data Input**	**Number of Clocks**						
				120 CLOCK	**119 CLOCK**	**118 CLOCK**	**…**	**3 CLOCK**	**2 CLOCK**	**1 CLOCK**
L	Output	Input	**DI[0]**	Y0 (0)*	Y1 (0)	Y2 (0)	…	Y117 (0)	Y118 (0)	Y119 (0)
			DI[1]	Y0 (1)*	Y1 (1)	Y2 (1)	…	Y117 (1)	Y118 (1)	Y119 (1)
			DI[2]	Y0 (2)*	Y1 (2)	Y2 (2)	…	Y117 (2)	Y118 (2)	Y119 (2)
			DI[3]	Y0 (3)*	Y1 (3)	Y2 (3)	…	Y117 (3)	Y118 (3)	Y119 (3)
H	Input	Output	**DI[0]**	Y119 (0)	Y118 (0)	Y117 (0)	…	Y2 (0)	Y1 (0)	Y0 (0)
			DI[1]	Y119 (1)	Y118 (1)	Y117 (1)	…	Y2 (1)	Y1 (1)	Y0 (1)
			DI[2]	Y119 (2)	Y118 (2)	Y117 (2)	…	Y2 (2)	Y1 (2)	Y0 (2)
			DI[3]	Y119 (3)	Y118 (3)	Y117 (3)	…	Y2 (3)	Y1 (3)	Y0 (3)

(3): 4th bit, msb; (2): 3rd bit; (1): 2nd bit; (0): 1st bit, lsb.

16 Levels Gray Display (1-bit Series Input Mode)

L/R	**EIO_1**	**EIO_2**	**Data Input**	**Number of Clocks**						
				480 CLOCK	**479 CLOCK**	**478 CLOCK**	**…**	**3 CLOCK**	**2 CLOCK**	**1 CLOCK**

L	Output	Input	**DI[0]**	Y0 (0)*	Y0 (1)*	Y0 (2)*	…	Y119 (1)	Y119 (2)	Y119 (3)
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x
H	Input	Output	**DI[0]**	Y119 (0)	Y119 (1)	Y119(2)	…	Y0 (1)	Y0 (2)	Y0 (3)
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x

(3): 4th bit, msb; (2): 3rd bit; (1) 2nd bit; (0): 1st bit, lsb. x: Don't care, should be fixed to "H" or "L", avoiding floating.

Common Mode

L/R	Data Transfer Direction	EIO1	EIO2
L	$Y_{119} \rightarrow Y_0$	Output	Input
H	$Y_0 \rightarrow Y_{119}$	Input	Output

Mixed Mode (Common/Segment Mode)

For example: When (SEL2, SEL1, SEL0) = (0, 0, 1), Select the 32 COM/88 SEG MODE, then segment side of mixed mode.

Black/White Display (4-bit Parallel Input Mode)

L/R	**EIO_1**	**EIO_2**	**Data Input**	**Number of Clocks**						
				22 CLOCK	**21 CLOCK**	**20 CLOCK**	**…**	**3 CLOCK**	**2 CLOCK**	**1 CLOCK**
L	Output	Input	**DI[0]**	Y0	Y4	Y8	…	Y76	Y80	Y84
			DI[1]	Y1	Y5	Y9	…	Y77	Y81	Y85
			DI[2]	Y2	Y6	Y10	…	Y78	Y82	Y86
			DI[3]	Y3	Y7	Y11	…	Y79	Y83	Y87
H	Input	Output	**DI[0]**	Y119	Y115	Y111	…	Y43	Y39	Y35
			DI[1]	Y118	Y114	Y110	…	Y42	Y38	Y34
			DI[2]	Y117	Y113	Y109	…	Y41	Y37	Y33
			DI[3]	Y116	Y112	Y108	…	Y40	Y36	Y32

Black/White Display (1-bit Series Input Mode)

L/R	**EIO_1**	**EIO_2**	**Data Input**	**Number of Clocks**						
				88 CLOCK	**87 CLOCK**	**86 CLOCK**	**…**	**3 CLOCK**	**2 CLOCK**	**1 CLOCK**

L	Output	Input	**DI[0]**	Y0	Y1	Y2	…	Y85	Y86	Y87
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x
H	Input	Output	**DI[0]**	Y119	Y118	Y117	…	Y34	Y33	Y32
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x

x: Don't care, should be fixed to "H" or "L", avoiding floating.

4 Levels Gray Display (4-bit Parallel Input Mode)

L/R	**EIO_1**	**EIO_2**	**Data Input**	**Number of Clocks**						
				44 CLOCK	**43 CLOCK**	**42 CLOCK**	**…**	**3 CLOCK**	**2 CLOCK**	**1 CLOCK**
L	Output	Input	**DI[0]**	Y0 (0)*	Y2 (0)	Y4 (0)	…	Y82 (0)	Y84 (0)	Y86 (0)
			DI[1]	Y0 (1)*	Y2 (1)	Y4 (1)	…	Y82 (1)	Y84 (1)	Y86 (1)
			DI[2]	Y1 (0)	Y3 (0)	Y5 (0)	…	Y83 (0)	Y85 (0)	Y87 (0)
			DI[3]	Y1 (1)	Y3 (1)	Y5 (1)	…	Y83 (1)	Y85 (1)	Y87 (1)
H	Input	Output	**DI[0]**	Y119 (0)	Y117 (0)	Y115 (0)	…	Y37 (0)	Y35 (0)	Y33 (0)
			DI[1]	Y119 (1)	Y117 (1)	Y115 (1)	…	Y37 (1)	Y35 (1)	Y33 (1)
			DI[2]	Y118 (0)	Y116 (0)	Y114 (0)	…	Y36 (0)	Y34 (0)	Y32 (0)
			DI[3]	Y118 (1)	Y116 (1)	Y114 (1)	…	Y36 (1)	Y34 (1)	Y32 (1)

(1): 2^{nd} bit, msb; (0): 1^{st} bit, lsb.

4 Levels Gray Display (1-bit Series Input Mode)

L/R	**EIO_1**	**EIO_2**	**Data Input**	**Number of Clocks**						
				176 CLOCK	**175 CLOCK**	**174 CLOCK**	**…**	**3 CLOCK**	**2 CLOCK**	**1 CLOCK**
L	Output	Input	**DI[0]**	Y0 (0)*	Y0 (1)*	Y1 (0)	…	Y86 (1)	Y87 (0)	Y87 (1)
			DI[1]	X	x	x	x	X	x	x
			DI[2]	X	x	x	x	X	x	x
			DI[3]	X	x	x	x	X	x	x
H	Input	Output	**DI[0]**	Y119 (0)	Y119 (1)	Y118 (0)	…	Y33 (1)	Y32 (0)	Y32 (1)
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x

(1): 2^{nd} bit, msb; (0): 1^{st} bit, lsb. x: Don't care, should be fixed to "H" or "L", avoiding floating.

16 Levels Gray Display (4-bit Parallel Input Mode)

L/R	EIO_1	EIO_2	Data Input	Number of Clocks						
				88 CLOCK	87 CLOCK	86 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI[0]	Y0 (0)*	Y1 (0)	Y2 (0)	…	Y85 (0)	Y86 (0)	Y87 (0)
			DI[1]	Y0 (1)*	Y1 (1)	Y2 (1)	…	Y85 (1)	Y86 (1)	Y87 (1)
			DI[2]	Y0 (2)*	Y1 (2)	Y2 (2)	…	Y85 (2)	Y86 (2)	Y87 (2)
			DI[3]	Y0 (3)*	Y1 (3)	Y2 (3)	…	Y85 (3)	Y86 (3)	Y87 (3)
H	Input	Output	DI[0]	Y119 (0)	Y118 (0)	Y117 (0)	…	Y34 (0)	Y33 (0)	Y32 (0)
			DI[1]	Y119 (1)	Y118 (1)	Y117 (1)	…	Y34 (1)	Y33 (1)	Y32 (1)
			DI[2]	Y119 (2)	Y118 (2)	Y117 (2)	…	Y35 (2)	Y33 (2)	Y32 (2)
			DI[3]	Y119 (3)	Y118 (3)	Y117 (3)	…	Y35 (3)	Y33 (3)	Y32 (3)

(3): 4^{th} bit, msb; (2): 3^{rd} bit; (1): 2^{nd} bit; (0): 1^{st} bit, lsb.

16 Levels Gray Display (1-bit Series Input Mode)

L/R	EIO_1	EIO_2	Data Input	Number of Clocks						
				352 CLOCK	351 CLOCK	350 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI[0]	Y0 (0)*	Y0 (1)*	Y0 (2)*	…	Y87 (1)	Y87 (2)	Y87 (3)
			DI[1]	x	x	X	x	x	x	x
			DI[2]	x	x	X	x	x	x	x
			DI[3]	x	x	X	x	x	x	x
H	Input	Output	DI[0]	Y119 (0)	Y119 (1)	Y119(2)	…	Y32 (1)	Y32 (2)	Y32 (3)
			DI[1]	x	x	x	x	x	x	x
			DI[2]	x	x	x	x	x	x	x
			DI[3]	x	x	x	x	x	x	x

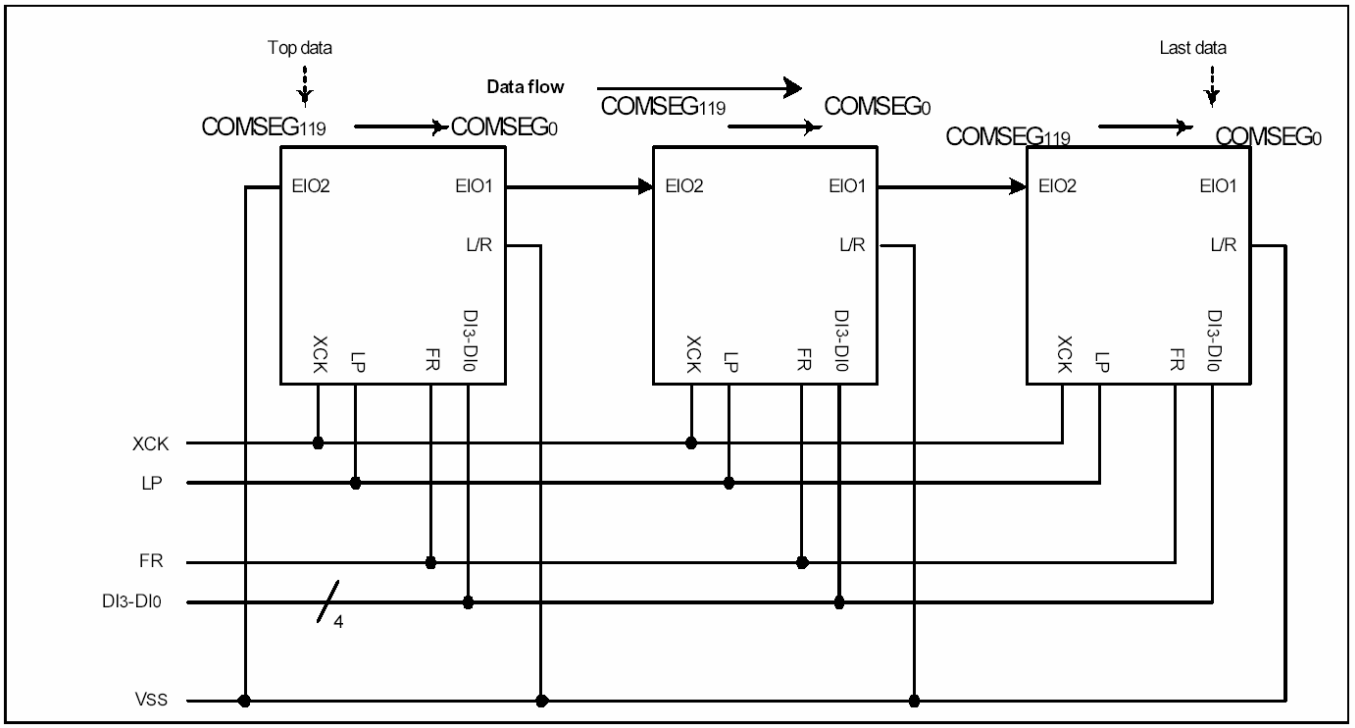
(3): 4^{th} bit, msb; (2): 3^{rd} bit; (1) 2^{nd} bit; (0): 1^{st} bit, lsb. x: Don't care, should be fixed to "H" or "L", avoiding floating.

Common Side of Mixed Mode

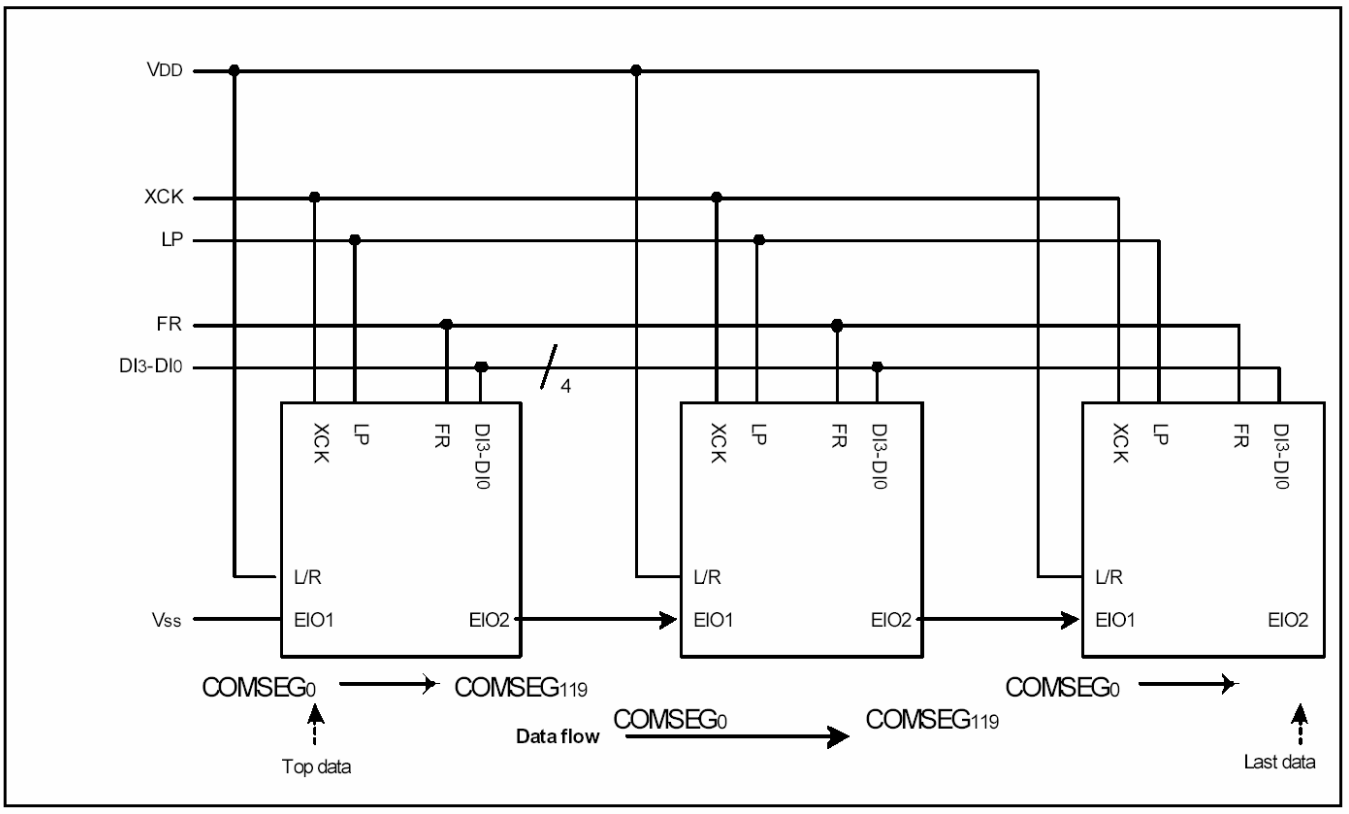
L/R	Data Transfer Direction	EIO_1	EIO_2
L	$Y_{119} \rightarrow Y_{88}$	Seg_end output	Input
H	$Y_0 \rightarrow Y_{119}$	Input	Seg_end output

8. Multi-Chip Connection

(c) When L/R = "L"



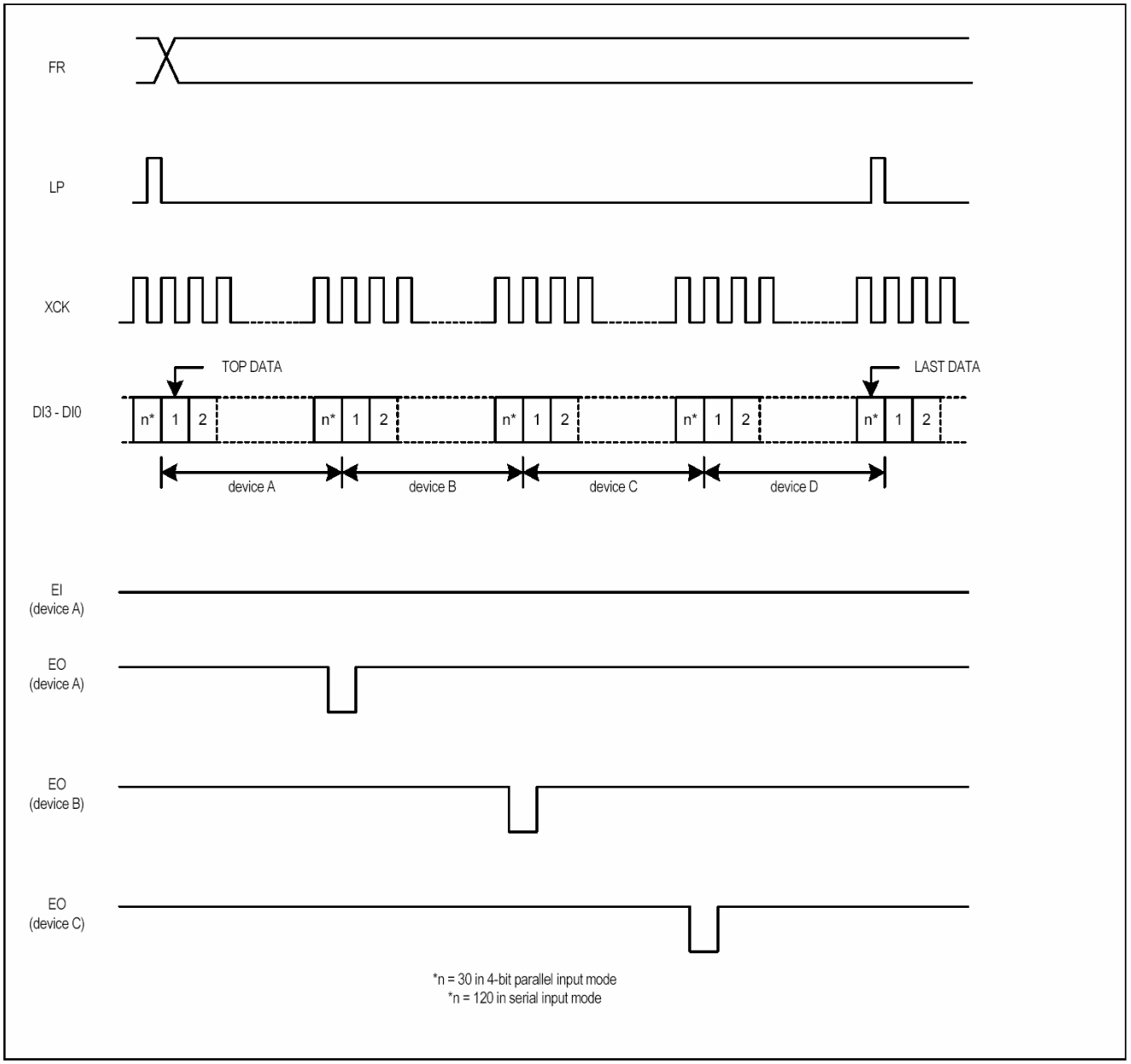
(d) When L/R = "H"



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9. Timing Chart of Cascade Connection

Timing chart of 4-device cascade connection of segment drivers

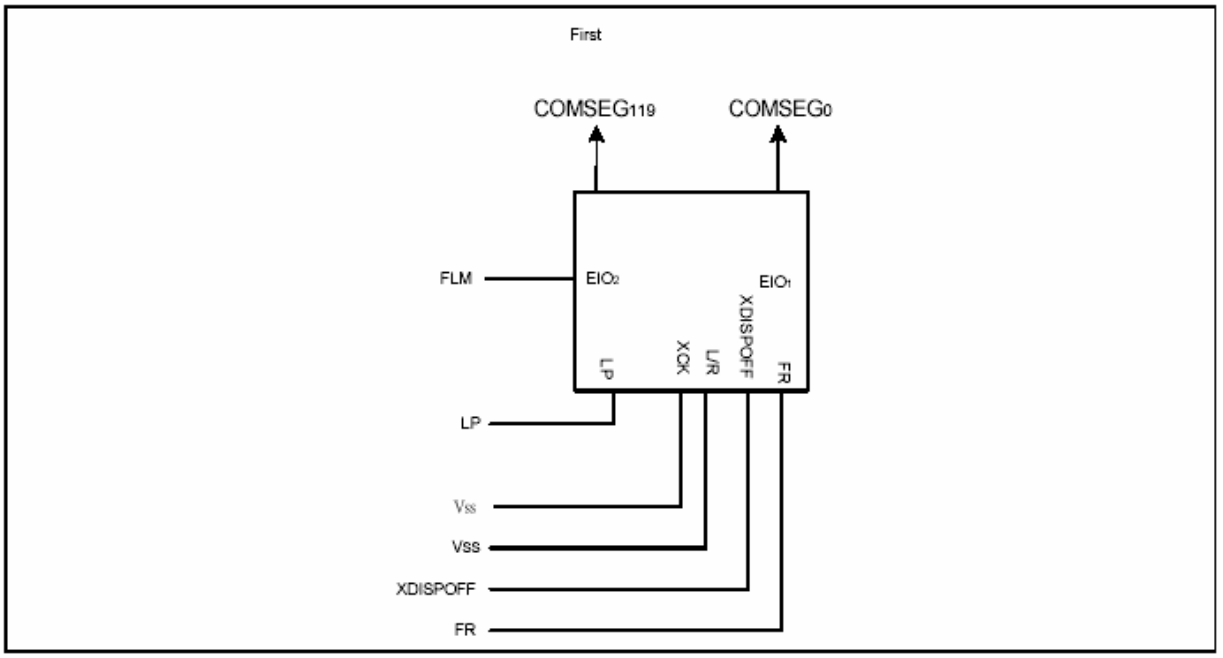


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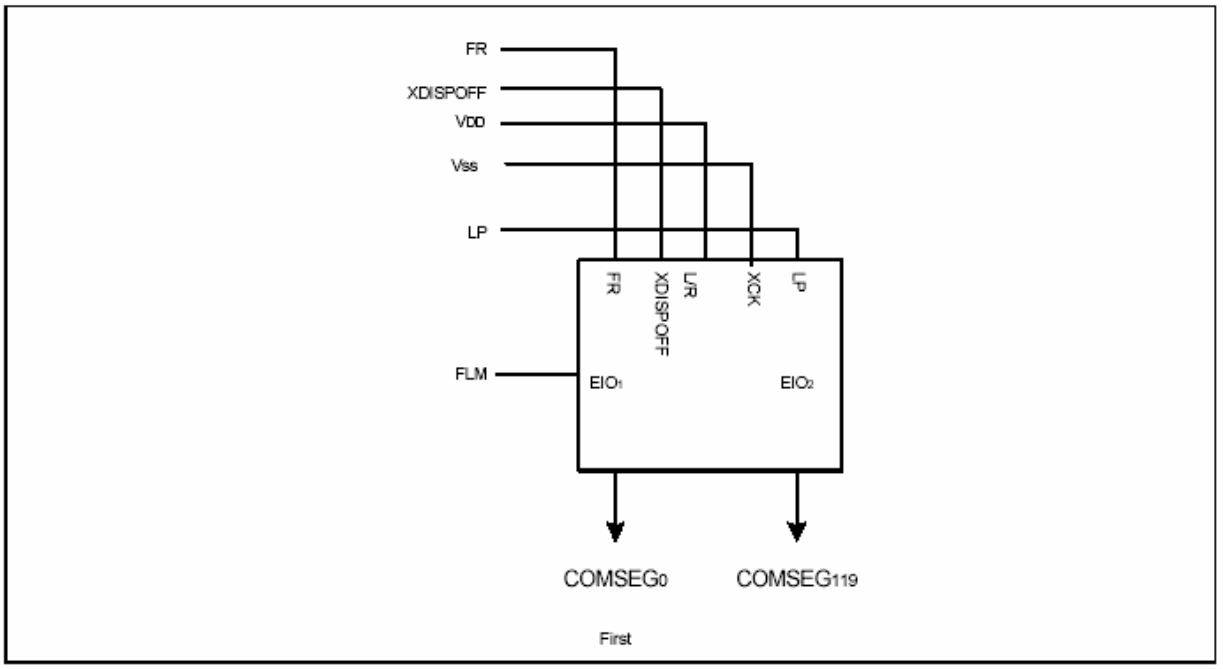
10. Common Connection

Connection examples for signal common drivers (120 common)

(e) L/R = "L"



(f) L/R = "H"



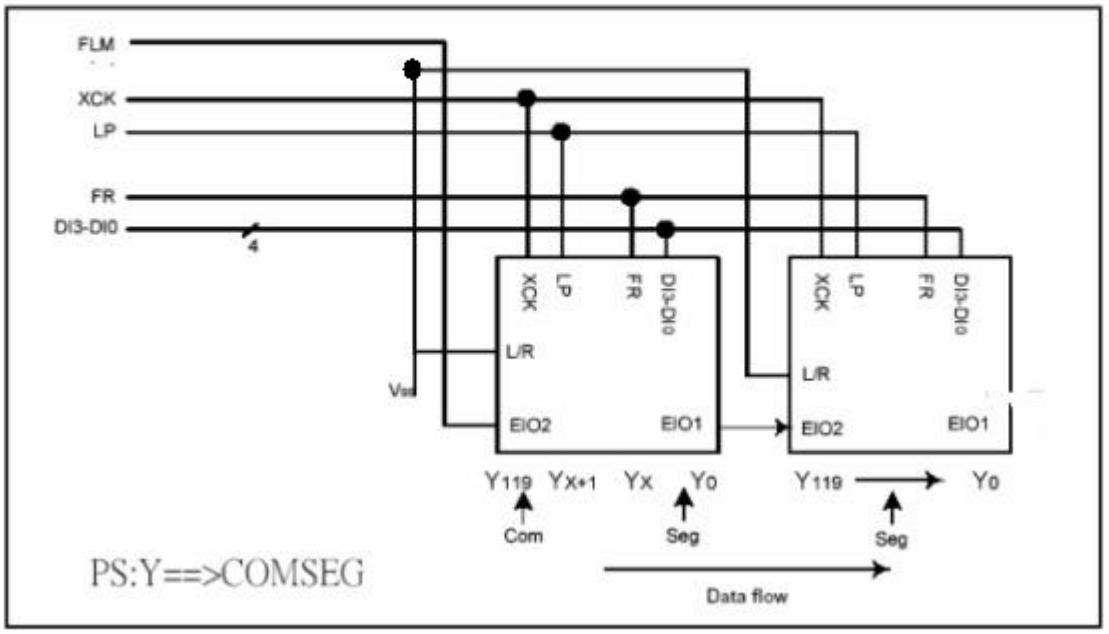
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11. Mixed Mode Connection

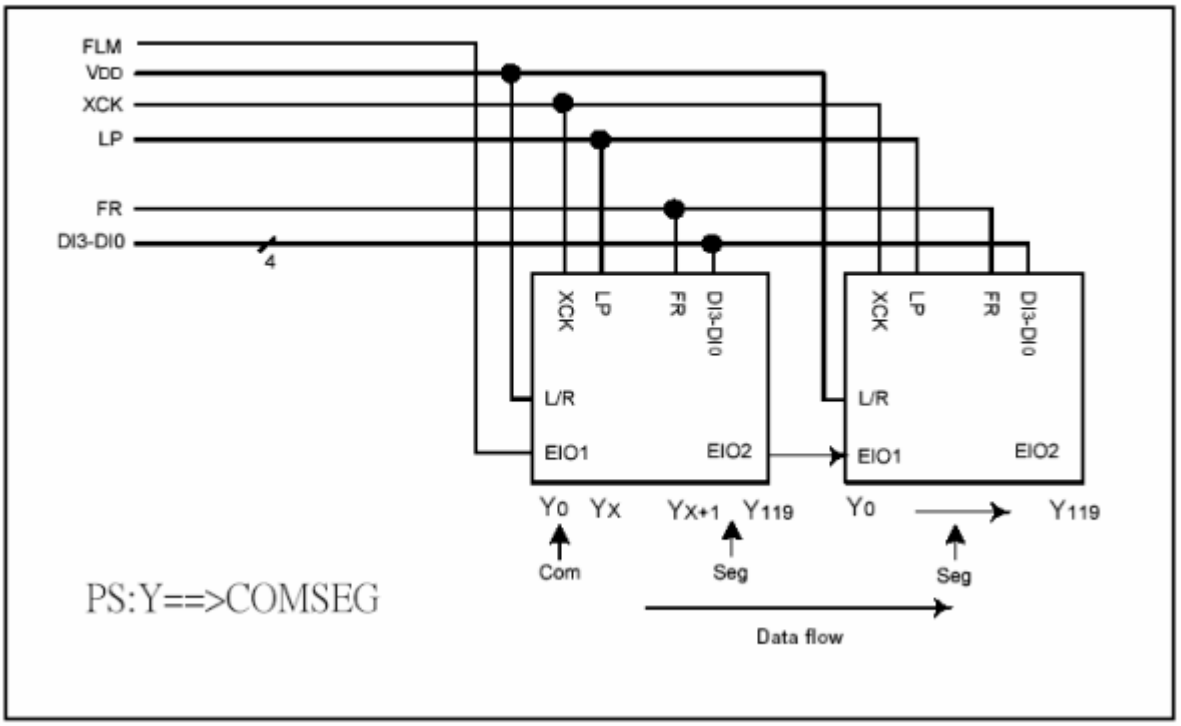
Connection examples for plural common/segment(mix mode) drivers

The mix mode is 1/32,1/48,1/64,1/80,1/96,1/112 duty mode

L/R = "L"



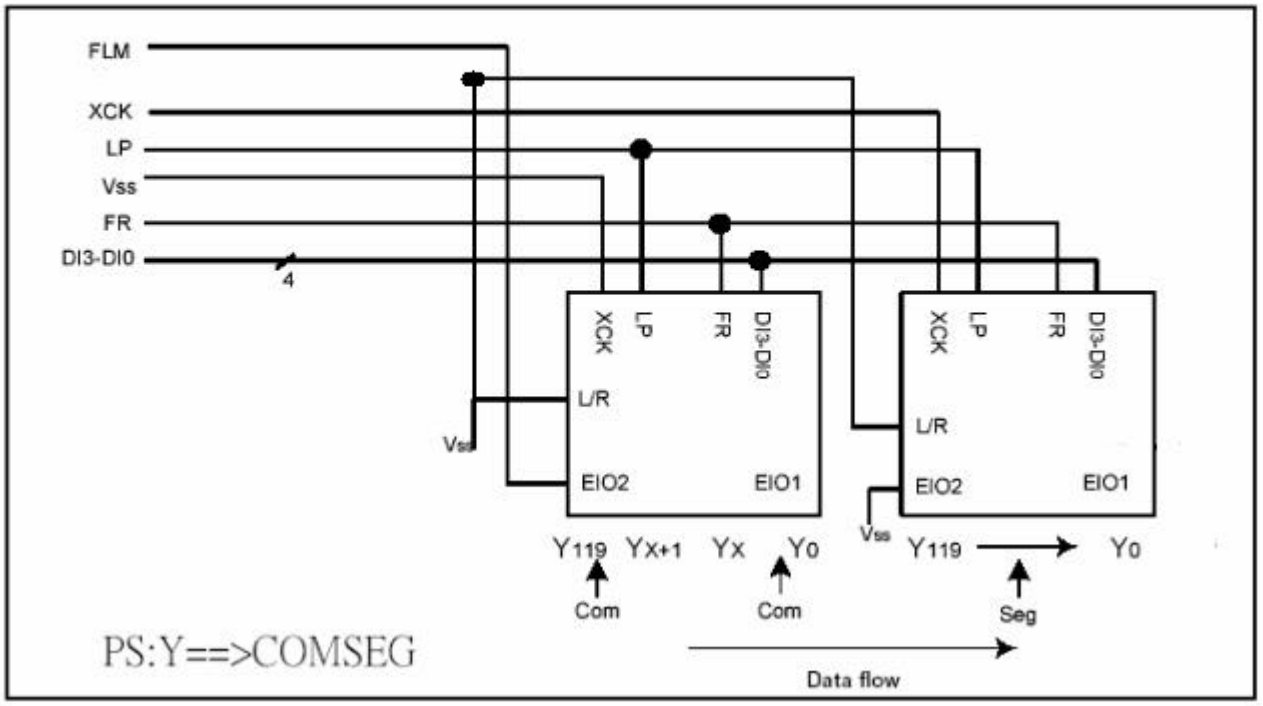
L/R="H"



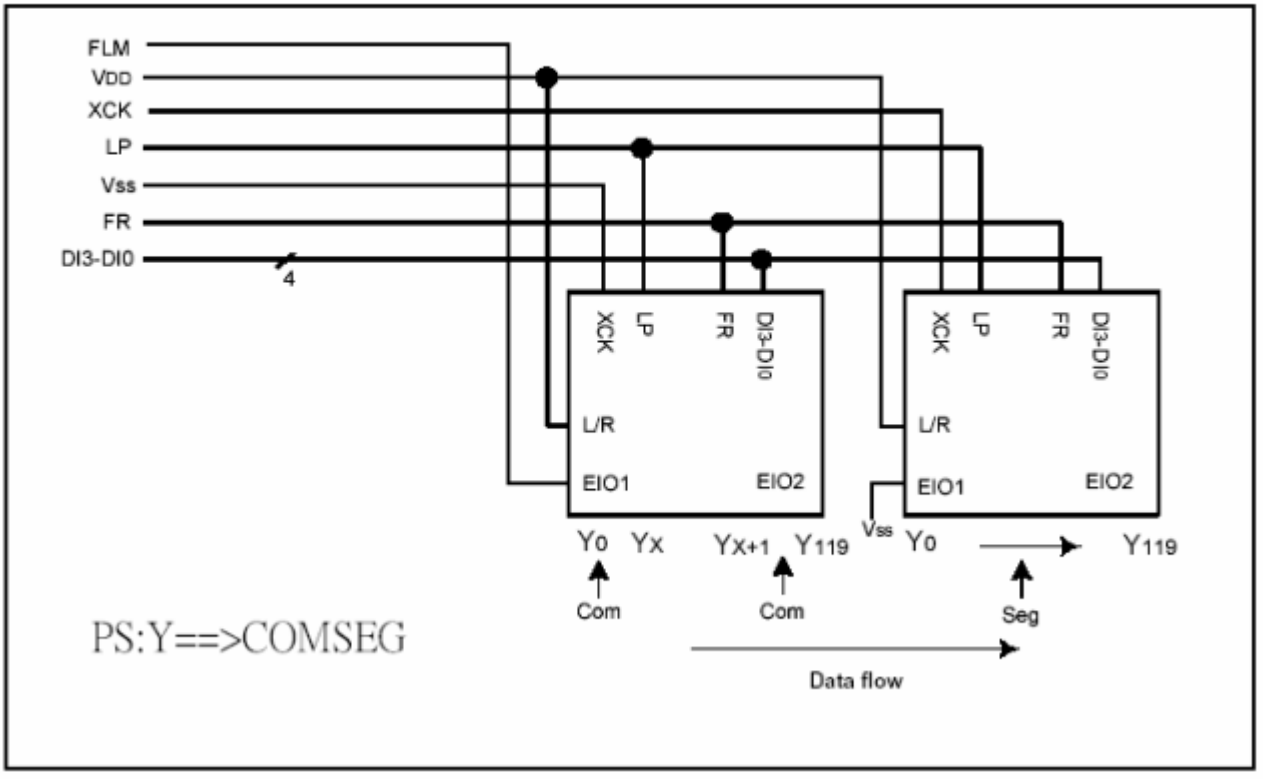
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Connection examples for 120 com &120 seg (for 1/120 duty)

L/R = "L"



L/R = "H"



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12. Precautions

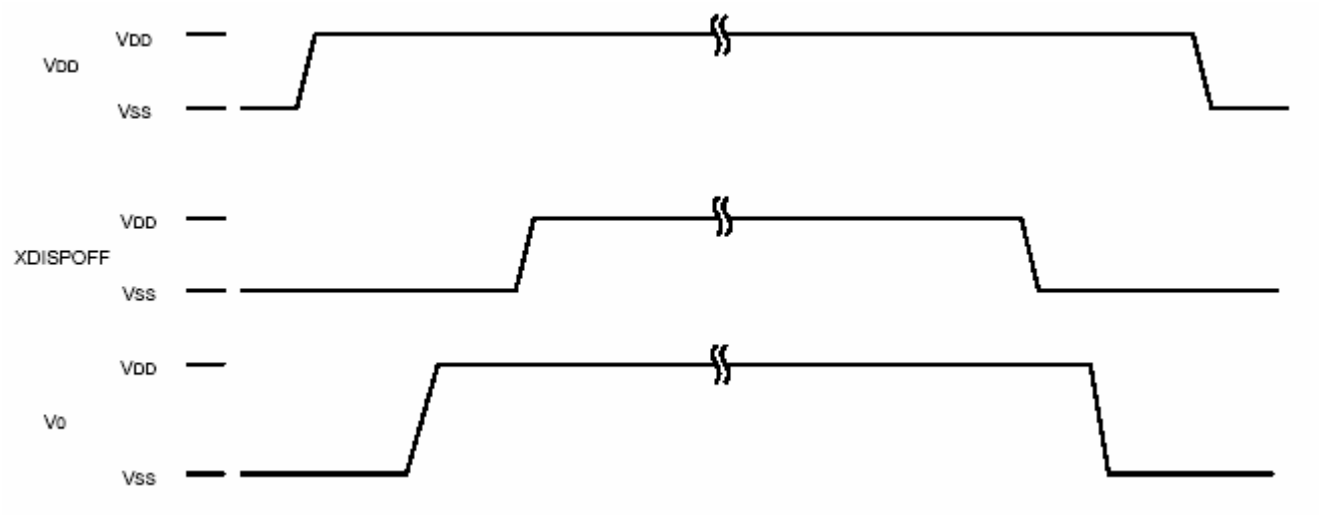
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows, when connecting the power supply, connect the LCD drive power after connecting the logic system power.

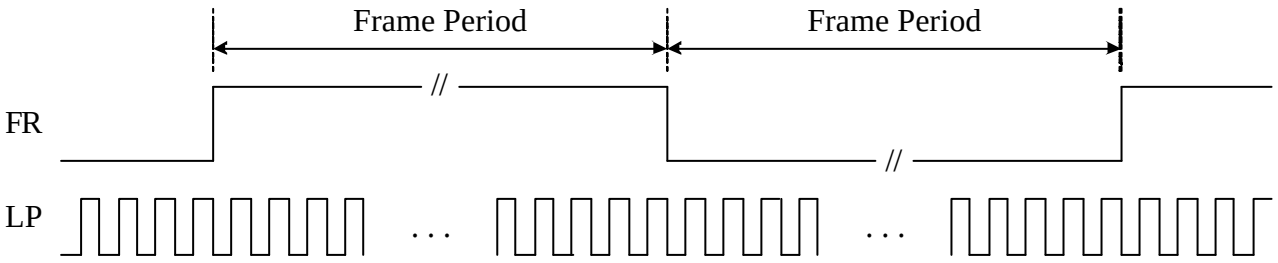
Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power and when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function.

After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level Vss on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here

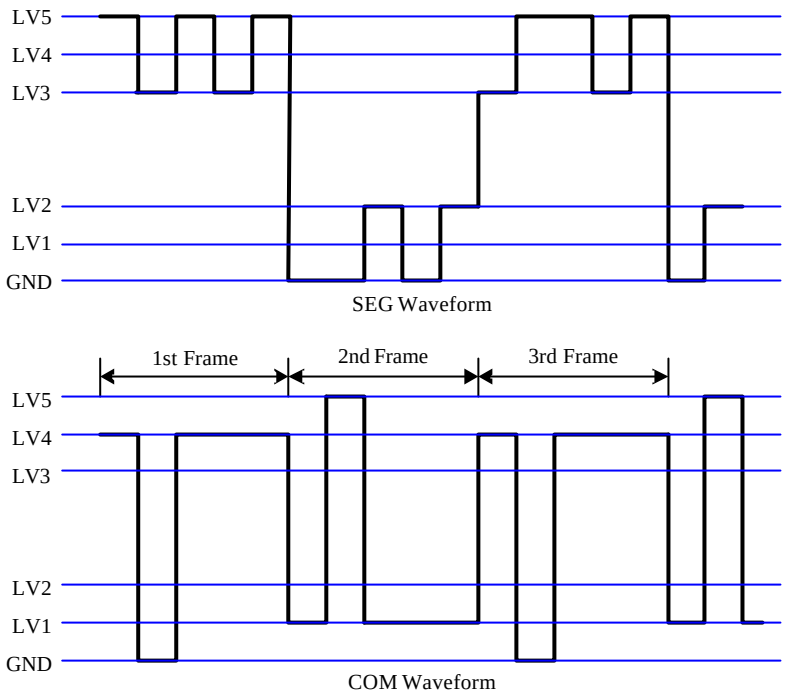


13. LCD Waveform

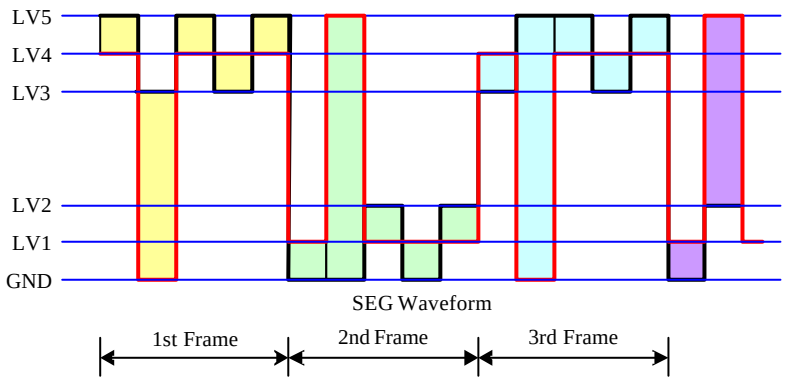


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Type B LCD COM and SEG waveform



Type B LCD COM/SEG waveform



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14. Pin Locations

1	CMSG[31]	X=	-3618	Y=	420	79	CMSG[109]	X=	3618.05	Y=	-437
2	CMSG[30]	X=	-3618	Y=	325	80	CMSG[108]	X=	3618.05	Y=	-342
3	CMSG[29]	X=	-3618	Y=	230	81	CMSG[107]	X=	3618.05	Y=	-247
4	CMSG[28]	X=	-3618	Y=	135	82	CMSG[106]	X=	3618.05	Y=	-152
5	CMSG[27]	X=	-3618	Y=	39.5	83	CMSG[105]	X=	3618.05	Y=	-57
6	CMSG[26]	X=	-3618	Y=	-55.5	84	CMSG[104]	X=	3618.05	Y=	38
7	CMSG[25]	X=	-3618	Y=	-151	85	CMSG[103]	X=	3618.05	Y=	133
8	CMSG[24]	X=	-3618	Y=	-246	86	CMSG[102]	X=	3618.05	Y=	228
9	CMSG[23]	X=	-3618	Y=	-341	87	CMSG[101]	X=	3618.05	Y=	323
10	CMSG[22]	X=	-3618	Y=	-436	88	CMSG[100]	X=	3618.05	Y=	418
11	CMSG[21]	X=	-3264.9	Y=	-819	89	CMSG[99]	X=	3219.9	Y=	819
12	CMSG[20]	X=	-3169.9	Y=	-819	90	CMSG[98]	X=	3124.9	Y=	819
13	CMSG[19]	X=	-3074.9	Y=	-819	91	CMSG[97]	X=	3029.9	Y=	819
14	CMSG[18]	X=	-2979.9	Y=	-819	92	CMSG[96]	X=	2934.9	Y=	819
15	CMSG[17]	X=	-2884.9	Y=	-819	93	CMSG[95]	X=	2839.9	Y=	819
16	CMSG[16]	X=	-2789.9	Y=	-819	94	CMSG[94]	X=	2744.9	Y=	819
17	CMSG[15]	X=	-2694.9	Y=	-819	95	CMSG[93]	X=	2649.9	Y=	819
18	CMSG[14]	X=	-2599.9	Y=	-819	96	CMSG[92]	X=	2554.9	Y=	819
19	CMSG[13]	X=	-2504.9	Y=	-819	97	CMSG[91]	X=	2459.9	Y=	819
20	CMSG[12]	X=	-2409.9	Y=	-819	98	CMSG[90]	X=	2364.9	Y=	819
21	CMSG[11]	X=	-2314.9	Y=	-819	99	CMSG[89]	X=	2269.9	Y=	819
22	CMSG[10]	X=	-2219.9	Y=	-819	100	CMSG[88]	X=	2174.9	Y=	819
23	CMSG[9]	X=	-2124.9	Y=	-819	101	CMSG[87]	X=	2079.9	Y=	819
24	CMSG[8]	X=	-2029.9	Y=	-819	102	CMSG[86]	X=	1984.9	Y=	819
25	CMSG[7]	X=	-1934.9	Y=	-819	103	CMSG[85]	X=	1889.9	Y=	819
26	CMSG[6]	X=	-1839.9	Y=	-819	104	CMSG[84]	X=	1794.9	Y=	819
27	CMSG[5]	X=	-1744.9	Y=	-819	105	CMSG[83]	X=	1699.9	Y=	819
28	CMSG[4]	X=	-1649.9	Y=	-819	106	CMSG[82]	X=	1604.9	Y=	819
29	CMSG[3]	X=	-1554.9	Y=	-819	107	CMSG[81]	X=	1509.9	Y=	819
30	CMSG[2]	X=	-1459.9	Y=	-819	108	CMSG[80]	X=	1332.9	Y=	819
31	CMSG[1]	X=	-1364.9	Y=	-819	109	CMSG[79]	X=	1237.9	Y=	819
32	CMSG[0]	X=	-1269.9	Y=	-819	110	CMSG[78]	X=	1142.9	Y=	819
33	VSSA	X=	-1101.4	Y=	-819	111	CMSG[77]	X=	1047.9	Y=	819
34	LVL1	X=	-1001.1	Y=	-819	112	CMSG[76]	X=	952.9	Y=	819
35	LVL2	X=	-906.12	Y=	-819	113	CMSG[75]	X=	857.9	Y=	819
36	LVL3	X=	-811.12	Y=	-819	114	CMSG[74]	X=	762.9	Y=	819
37	LVL4	X=	-716.12	Y=	-819	115	CMSG[73]	X=	667.9	Y=	819
38	LVL5	X=	-621.12	Y=	-819	116	CMSG[72]	X=	572.9	Y=	819

39	LVP	X=	-526.12	Y=	-819	117	CMSG[71]	X=	477.9	Y=	819
40	LCAP1A	X=	-431.12	Y=	-819	118	CMSG[70]	X=	382.9	Y=	819
41	LCAP1B	X=	-336.12	Y=	-819	119	CMSG[69]	X=	287.9	Y=	819
42	LCAP2A	X=	-241.12	Y=	-819	120	CMSG[68]	X=	192.9	Y=	819
43	LCAP2B	X=	-146.12	Y=	-819	121	CMSG[67]	X=	97.9	Y=	819
44	LCAP3A	X=	-51.12	Y=	-819	122	CMSG[66]	X=	2.9	Y=	819
45	LCAP4A	X=	43.88	Y=	-819	123	CMSG[65]	X=	-92.1	Y=	819
46	LCAP5A	X=	138.88	Y=	-819	124	CMSG[64]	X=	-187.1	Y=	819
47	LGS1	X=	233.88	Y=	-819	125	CMSG[63]	X=	-282.1	Y=	819
48	LGS2	X=	328.88	Y=	-819	126	CMSG[62]	X=	-377.1	Y=	819
49	VAG	X=	423.88	Y=	-819	127	CMSG[61]	X=	-472.1	Y=	819
50	VDD	X=	525.13	Y=	-819	128	CMSG[60]	X=	-567.1	Y=	819
51	RSTN	X=	620.13	Y=	-819	129	CMSG[59]	X=	-662.1	Y=	819
52	DI[3]	X=	715.13	Y=	-819	130	CMSG[58]	X=	-757.1	Y=	819
53	DI[2]	X=	810.13	Y=	-819	131	CMSG[57]	X=	-852.1	Y=	819
54	DI[1]	X=	906.38	Y=	-819	132	CMSG[56]	X=	-947.1	Y=	819
55	DI[0]	X=	1000.13	Y=	-819	133	CMSG[55]	X=	-1042.1	Y=	819
56	P_SN	X=	1095.13	Y=	-819	134	CMSG[54]	X=	-1137.1	Y=	819
57	L_R	X=	1190.13	Y=	-819	135	CMSG[53]	X=	-1232.1	Y=	819
58	EIO1	X=	1285.13	Y=	-819	136	CMSG[52]	X=	-1327.1	Y=	819
59	EIO2	X=	1380.13	Y=	-819	137	CMSG[51]	X=	-1422.1	Y=	819
60	CLK32	X=	1480.6	Y=	-819	138	CMSG[50]	X=	-1517.1	Y=	819
61	XCK	X=	1575.6	Y=	-819	139	CMSG[49]	X=	-1612.1	Y=	819
62	XDISPOFF	X=	1670.6	Y=	-819	140	CMSG[48]	X=	-1707.1	Y=	819
63	LP	X=	1765.6	Y=	-819	141	CMSG[47]	X=	-1802.1	Y=	819
64	FR	X=	1860.6	Y=	-819	142	CMSG[46]	X=	-1897.1	Y=	819
65	XCS	X=	1955.6	Y=	-819	143	CMSG[45]	X=	-1992.1	Y=	819
66	SDI	X=	2050.6	Y=	-819	144	CMSG[44]	X=	-2087.1	Y=	819
67	SCLK	X=	2145.6	Y=	-819	145	CMSG[43]	X=	-2182.1	Y=	819
68	GND	X=	2240.6	Y=	-819	146	CMSG[42]	X=	-2277.1	Y=	819
69	CMSG[119]	X=	2409.1	Y=	-819	147	CMSG[41]	X=	-2372.1	Y=	819
70	CMSG[118]	X=	2504.1	Y=	-819	148	CMSG[40]	X=	-2467.1	Y=	819
71	CMSG[117]	X=	2599.1	Y=	-819	149	CMSG[39]	X=	-2562.1	Y=	819
72	CMSG[116]	X=	2694.1	Y=	-819	150	CMSG[38]	X=	-2657.1	Y=	819
73	CMSG[115]	X=	2789.1	Y=	-819	151	CMSG[37]	X=	-2752.1	Y=	819
74	CMSG[114]	X=	2884.1	Y=	-819	152	CMSG[36]	X=	-2847.1	Y=	819
75	CMSG[113]	X=	2979.1	Y=	-819	153	CMSG[35]	X=	-2942.1	Y=	819
76	CMSG[112]	X=	3074.1	Y=	-819	154	CMSG[34]	X=	-3037.1	Y=	819
77	CMSG[111]	X=	3169.1	Y=	-819	155	CMSG[33]	X=	-3132.1	Y=	819
78	CMSG[110]	X=	3264.1	Y=	-819	156	CMSG[32]	X=	-3227.1	Y=	819

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15. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{DD}	-0.5V ~ 4V	
Input Voltage	V_{IN}	-0.5V ~ V_{DD}+0.5V	
Output Voltage	V_O	-0.5V ~ V_{DD}+0.5V	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

16. Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{DD}	2.4V ~ **4V**	
LCD operating voltage	V_{V5}	< 16V	
Input Voltage	V_{IH}	0.9 V_{DD} ~ V_{DD}	
	V_{IL}	0.0V ~ 0.1V_{DD}	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

This specification is subject to change without notice. Please contact sales person for the latest version before use.

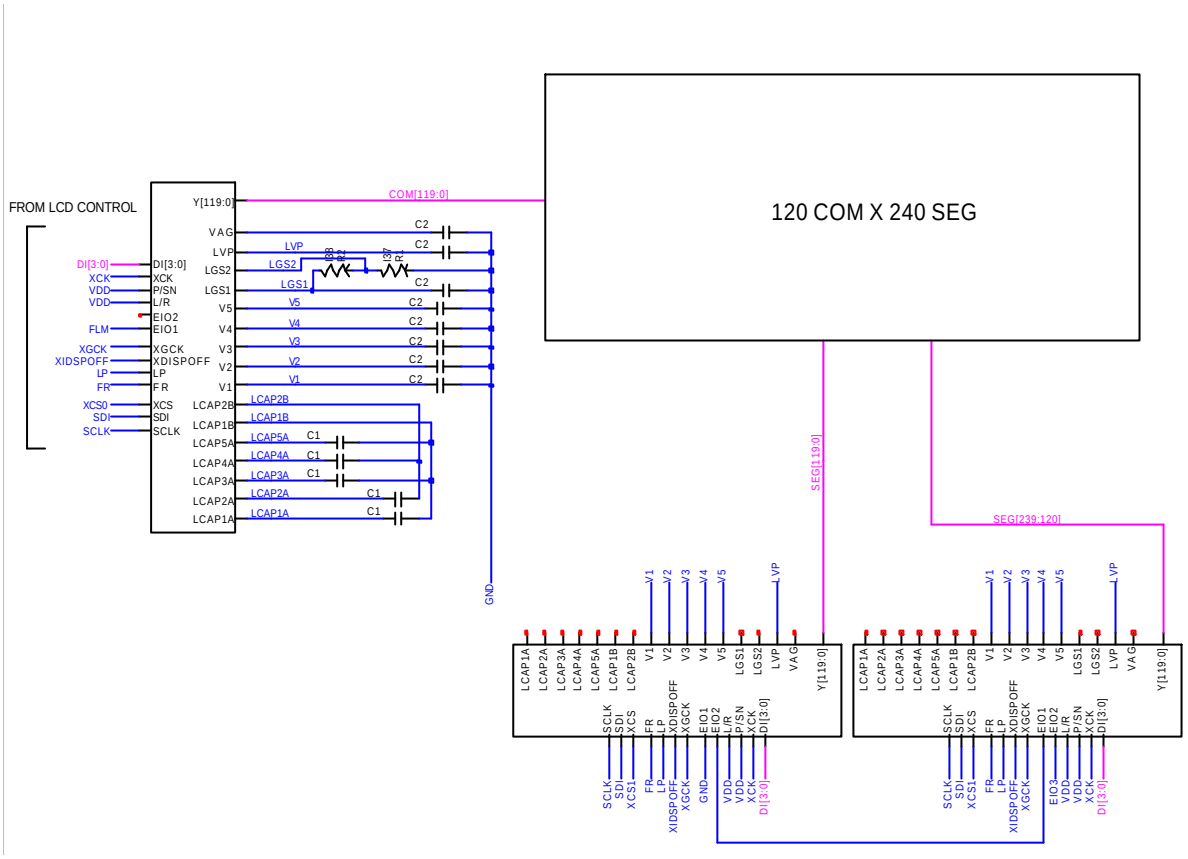
17. AC/DC Characteristics

Test Condition: Temperature: 25℃, VDD: 3V±10%

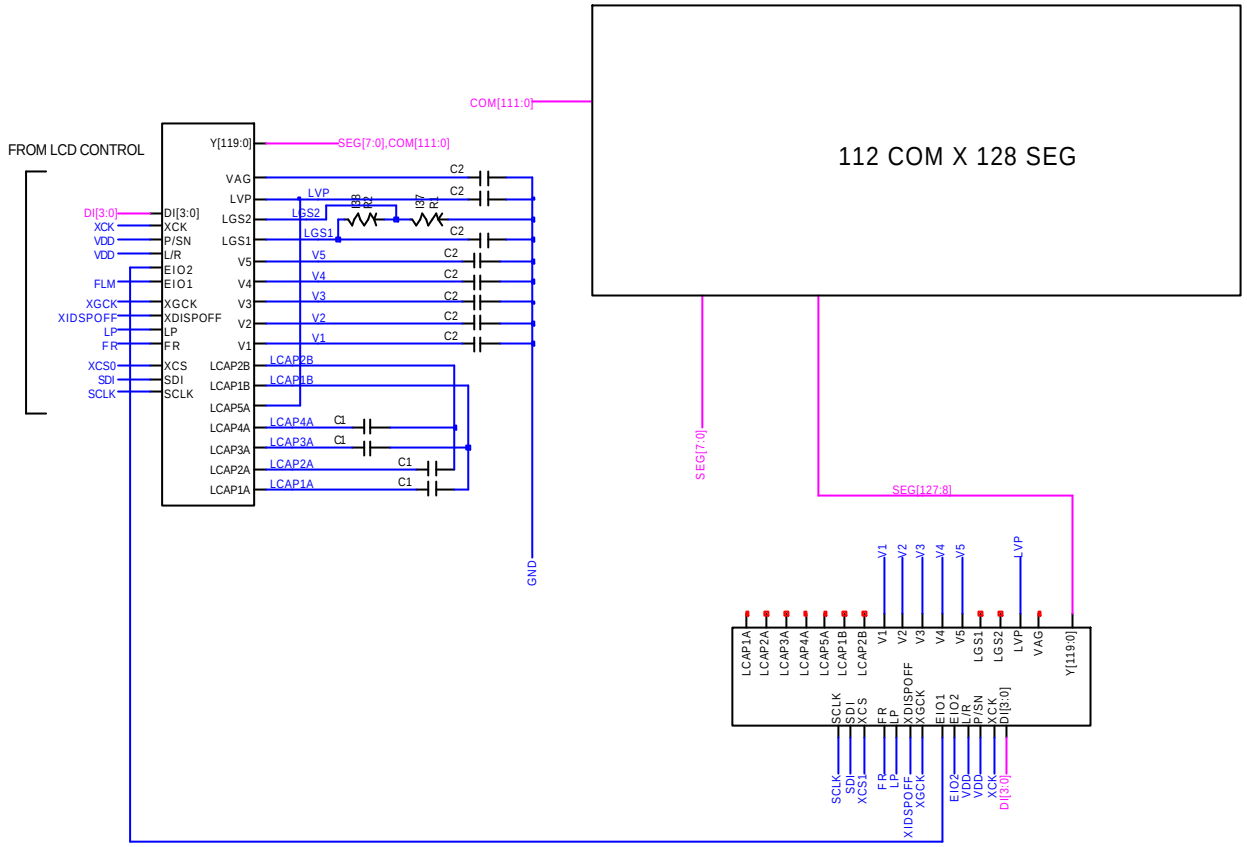
Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Current	I_{DD}		300	350	μA	
Standby mode current	I_{STBY}			1	μA	
Input high voltage	V_{IH}	0.8			V_{DD}	Input pins
Input low voltage	V_{IL}			0.2	V_{DD}	Input pins
Input leakage current	I_{IL}		20		μA	V_{IL} = GND, VDD
Input hysteresis width	V_{HYS}		1/3		V_{DD}	Input pins Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)
Output source current	I_{OH}	2.0			mA	RD[7..0], V_{OL}=2.0V
Output sink current	I_{OL}	2.0			mA	RD[7..0], V_{OL}=0.4V

18. Application Circuit for module

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19. Updated Record

Version	Date	Update History
V1.0	12/9/2004	First release version
V1.1	19/1/2005	Modify setup-up voltage circuits and application circuit. Add a capacitor between LGS1 and GND.