XD1008-BD

Receiver
30 kHz-40 GHz

Rev. V1

Features

- 15 dB Gain
- 22.5 dBm P1dB at 22 GHz
- 4.5 dB Noise Figure at 26 GHz
- Unconditional Stability over Temperature Range
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

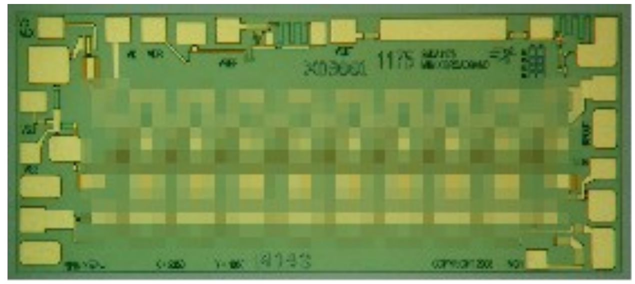
Description

M/A-COM Tech's 30 kHz - 40 GHz GaAs MMIC distributed amplifier has a gain of 15 dB with a 4.5 dB noise figure at 26 GHz. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for microwave, millimeter-wave, military, wideband and instrumentation applications.

Ordering Information

Part Number	Package
XD1008-BD-000V	"V" - vacuum release gel paks
XD1008-BD-EV1	evaluation module

Chip Device Layout



Absolute Maximum Ratings[1]

Parameter	Min.	Max.
Supply Voltage (Vd)		+10.0 V
Supply Current (Id)		340 mA
Gate Bias Voltage (Vg1)	-9.5 V	
Gate Current (Ig1)	-38 mA	+1 mA
Gate Bias Voltage (Vg2)	-3.5 V	+4.0 V
Gate Current (Ig2)	-20 mA	
CW Input Power (Pin)		17 dBm
Storage Temperature (Tstg)	-65 ºC	+165 ºC
Operating Temperature (Ta)	-55 ºC	
Channel Temperature (Tch)		+150 ºC

(1) Absolute maximum ratings for continuous operation unless otherwise noted.

Bias Settings

Parameter	Units	Min.	Typ.	Max.	Function
Drain Current (Id), V=7 V, VG1=-2.5 V*, VG2=open circuit	mA	9.0	-		
Drain Current (Id), V=4 V, VG1=-2.5 V*, VG2=open circuit	mA	DC	2.0		
Drain Voltage (Vd)	V	-	15.0		Supply drain current to device
Gate Bias (Vg1)	V	10.0	13.5		Adjusted to set drain current
Gate Bias (Vg2)	V	-	+3.0		Adjusted for gain control

*approximate

Electrical Specifications: High Power Applications[2]
Vdd=7 V, Idd(Q)=200 mA, Zin=Zo=50Ω

Parameter and Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB		15	
Gain Flatness (ΔS21)	dB		+/-0.75	
Input Return Loss RF (S11)	dB		16	
Output Return Loss (S22)	dB		16	
Reverse Isolation (S12)	dB		28	
Output Power for 1 dB Compression (P1dB) @ 22 GHz	dBm		22	
Saturated RF Power (Psat) @ 22 GHz	dBm		24.5	
Output 3rd Order Intercept Point (OIP3) @ 22 GHz	dBm		27	
Noise Figure (NF) @ 26 GHz	dB		4.5	
Noise Figure (NF) @ 40 GHz	dB		6.5	

Electrical Specifications[2]
Vdd=6 V, Idd(Q)=187 mA, Zin=Zo=50Ω

Parameter and Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB	14.0[3]	15.5	
Gain Flatness (ΔS21)	dB		+/-0.75	
Input Return Loss RF (S11)	dB		16	
Output Return Loss (S22)	dB		16	
Reverse Isolation (S12)	dB		28	
Output Power with 7 dB Input Power (Pout)	dBm	20[3]	22	
Output Power for 1 dB Compression (P1dB) @ 22 GHz	dBm		22.5	
Saturated RF Power (Psat) @ 22 GHz	dBm		24.5	
Output 3rd Order Intercept Point (OIP3) @ 22 GHz	dBm		27	
Noise Figure (NF) @ 26 GHz	dB		4.5	
Noise Figure (NF) @ 40 GHz	dB		6.5	

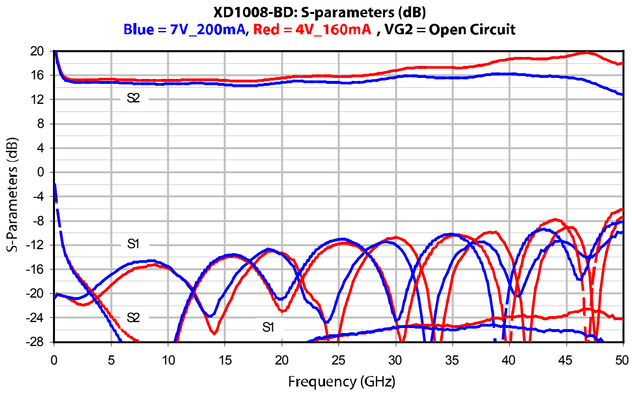
(2) Data measured in wafer form with backside temperature T = 25°C unless otherwise noted.
(3) 100% on-wafer RF test at 5, 25 and 40 GHz

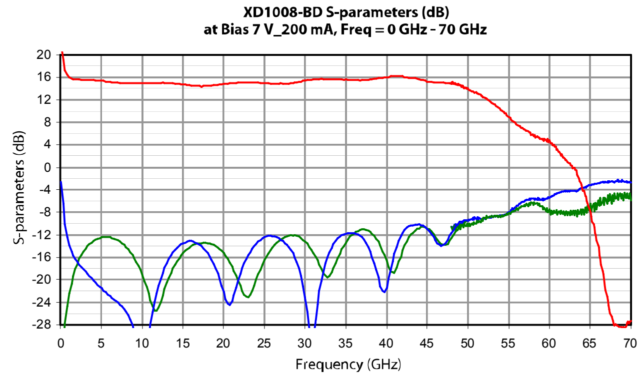
Electrical Specifications: High Gain, Low Noise Applications[4]
Vdd=4 V, Idd(Q)=160 mA, Zin=Zo=50Ω

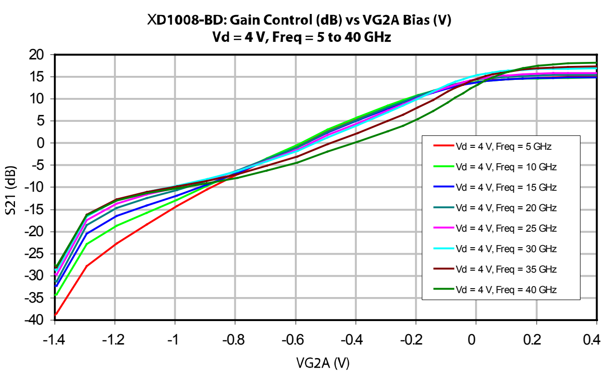
Parameter and Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB		16	
Gain Flatness (ΔS21)	dB		+/-0.75	
Input Return Loss RF (S11)	dB		16	
Output Return Loss (S22)	dB		16	
Reverse Isolation (S12)	dB		28	
Output Power for 1 dB Compression (P1dB) @ 22 GHz	dBm		18	
Saturated RF Power (Psat) @ 22 GHz	dBm		22	
Output 3rd Order Intercept Point (OIP3) @ 22 GHz	dBm		30	
Noise Figure (NF) @ 26 GHz	dB		3.5	
Noise Figure (NF) @ 40 GHz	dB		5.5	

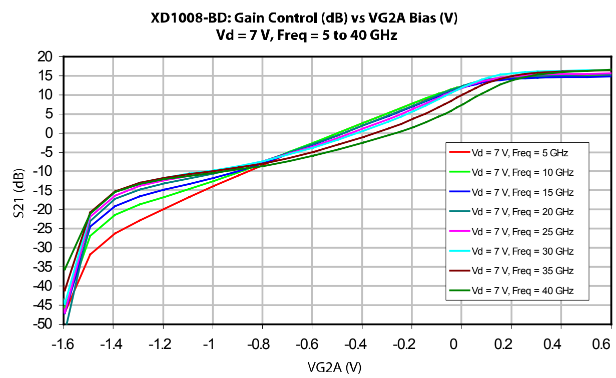
(4) Data measured in wafer form with backside temperature T = 25°C unless otherwise noted.

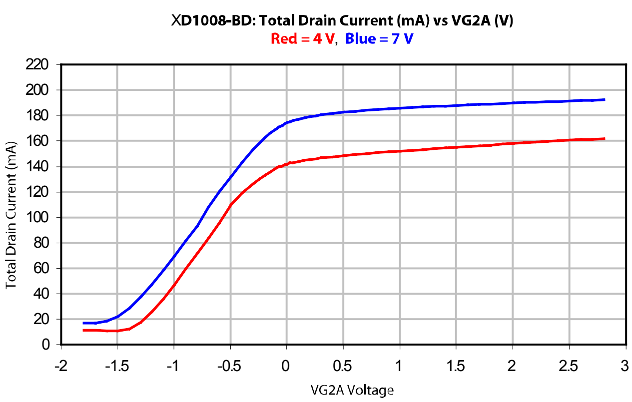
Typical Performance Curves

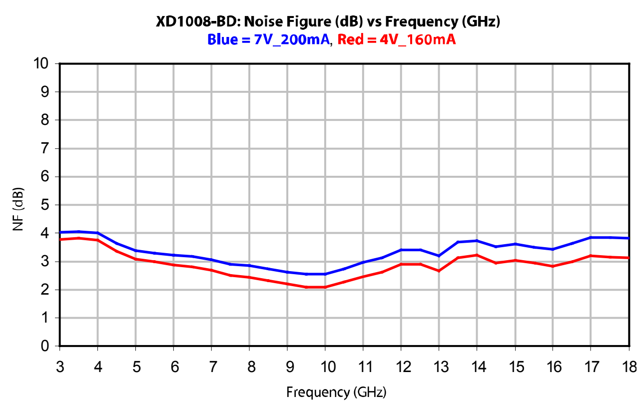




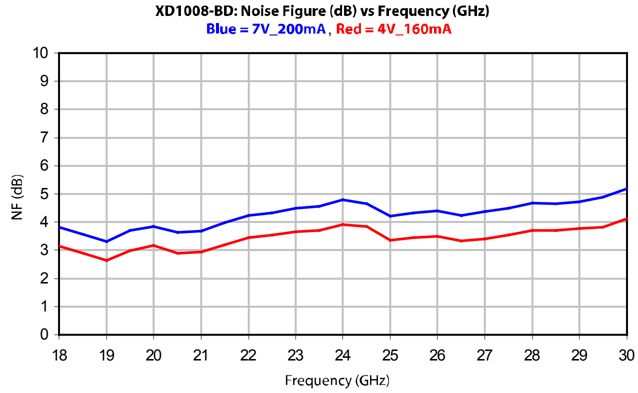


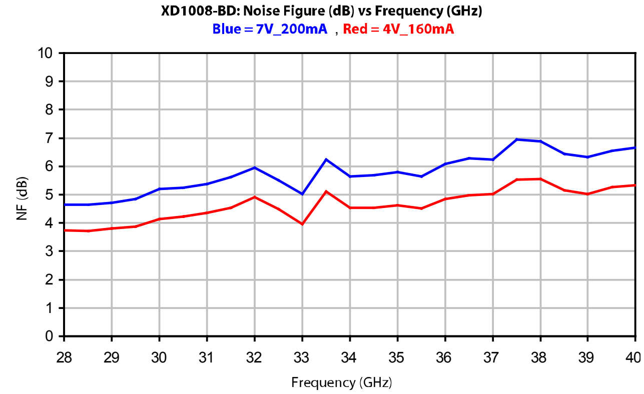


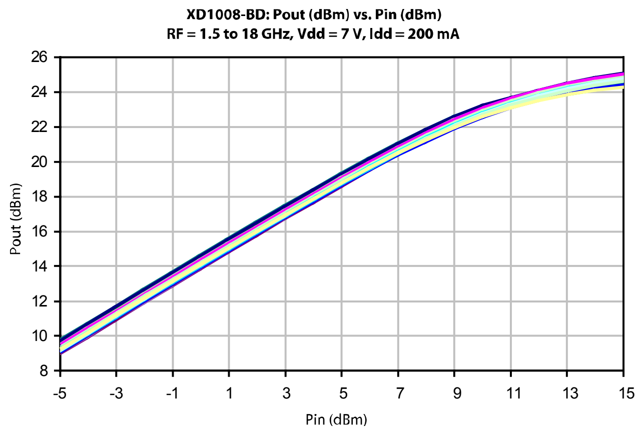


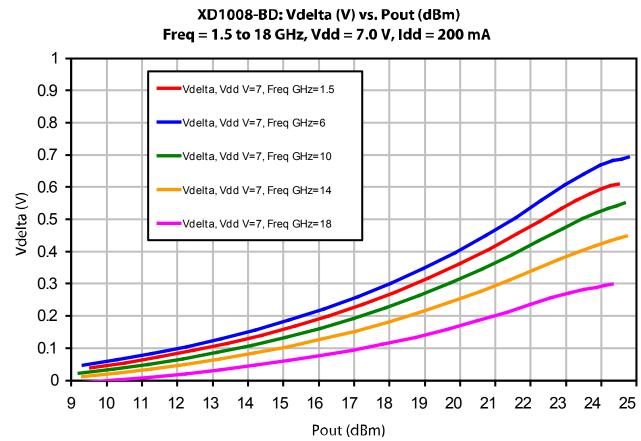


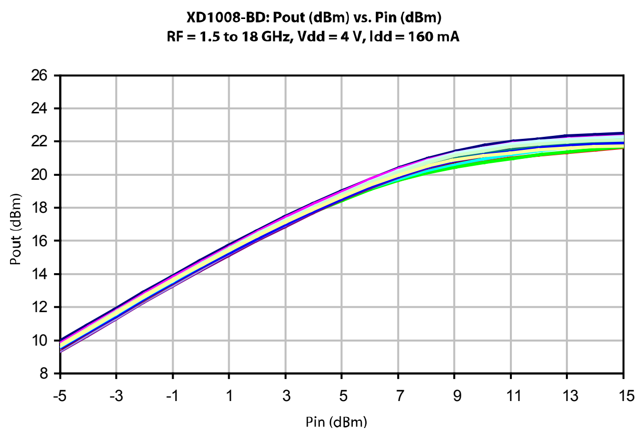
Typical Performance Curves (cont.)

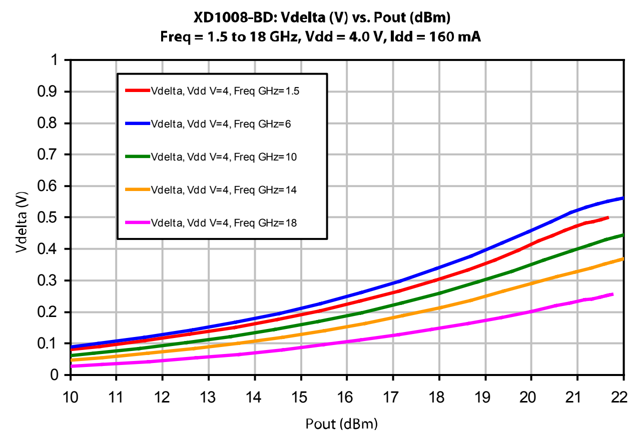






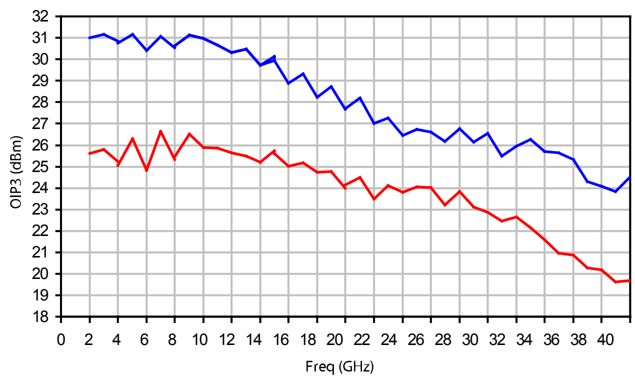




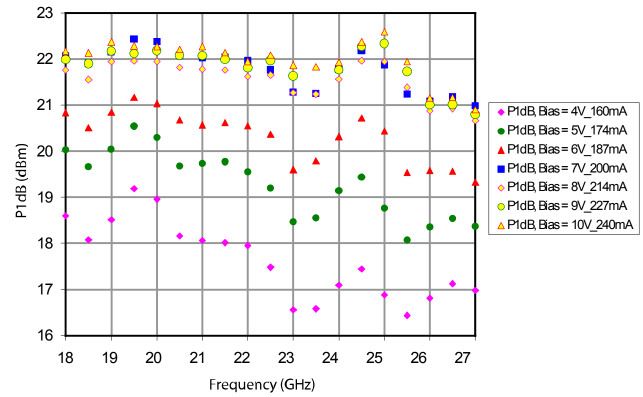


Typical Performance Curves (cont.)

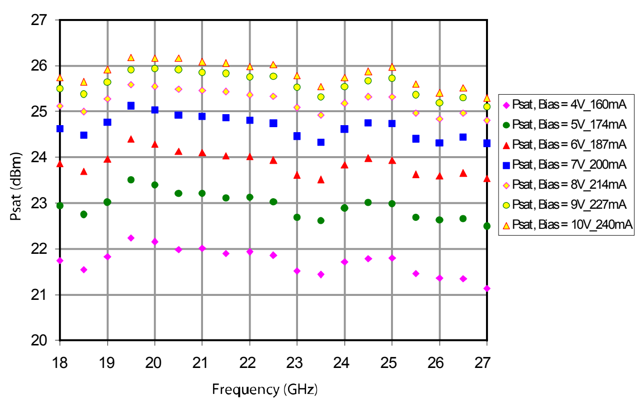
XD1008-BD: OIP3 (dBm) vs Freq (GHz)
Pin = 2 dBm, Blue = 7V_200mA , Red = 4V_160mA



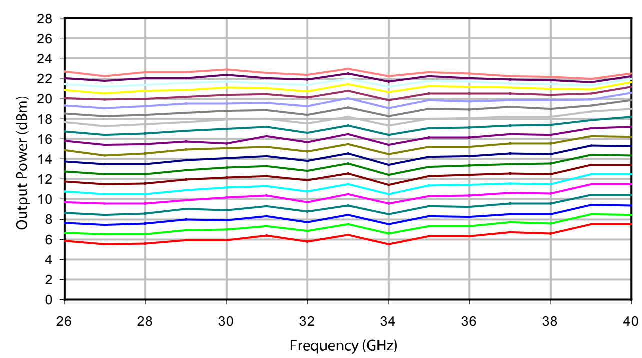
XD1008-BD: P1dB (dBm) vs Freq (GHz)



XD1008-BD: Psat (dBm) vs Freq (GHz)

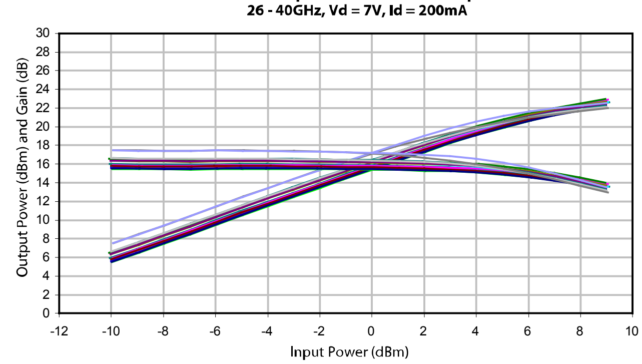


XD1008-BD: Output Power at Vd= 7V, Id = 200mA,
26-40 GHz with Pin -10 to +9 dBm

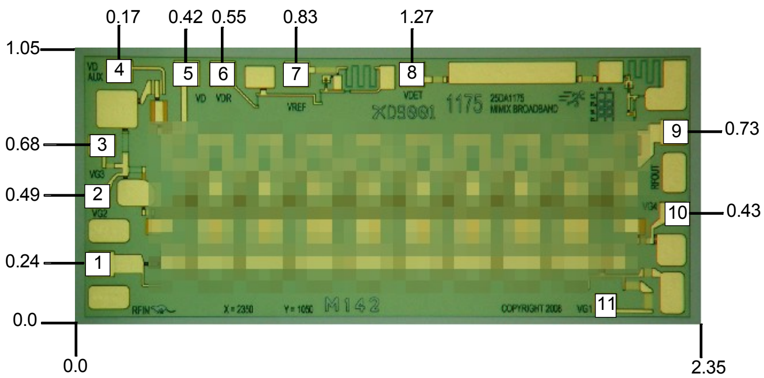


XD1008-BD: Output Power vs Input Power.
26 - 40 GHz, Vd = 7V, Id = 200mA

XD1008-BD: Output Power and Gain vs Input Power.
26 - 40GHz, Vd = 7V, Id = 200mA

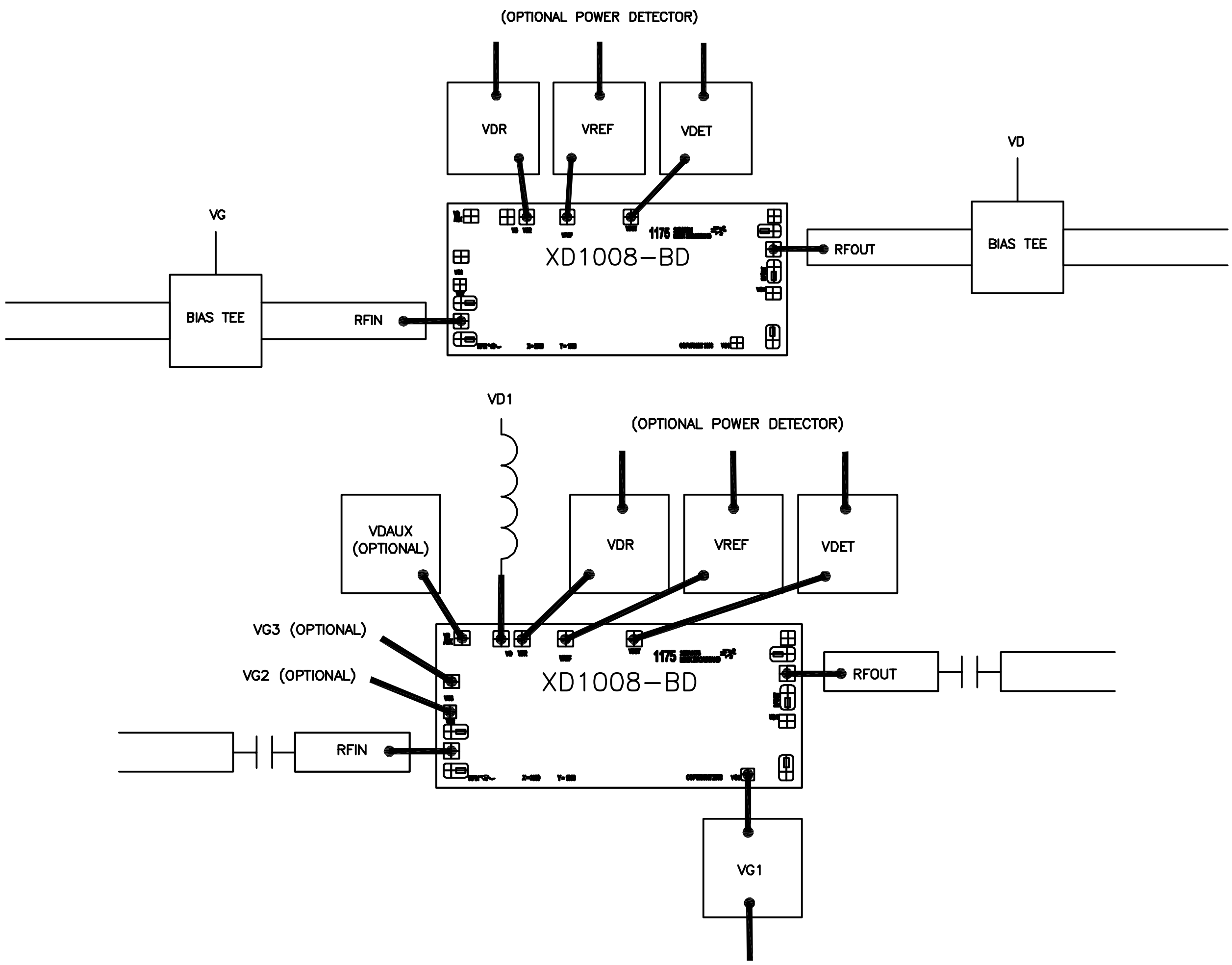


Layout Dimensions



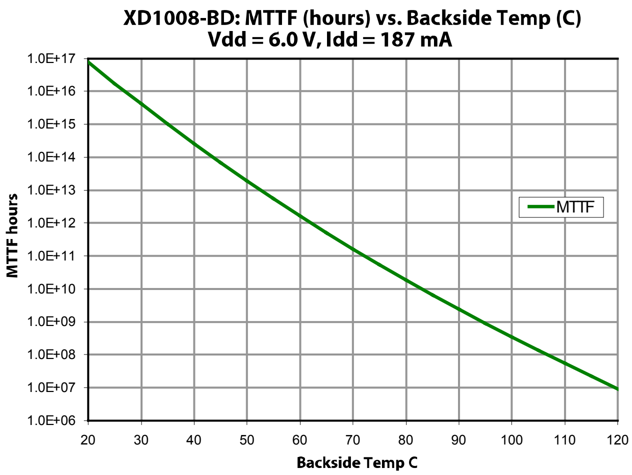
Pin1: RF IN
Pin2: VG2, not connected for basic application, but can be used for gain control (VG2 = 2V to -2V)
Pin3: VG3, not connected for basic application, can be used for gain peaking
Pin4: VD Aux, not connected, but can be used for capacitive bypass for operation at frequencies lower than 2 GHz
Pin5: VD – detector bias, the same as VD for the amplifier
Pin6: VDR – bias voltage for reference diode (see application note)
Pin7: VDREF – detector reference (see application note)
Pin8: VDET – detector diode (see application note)
Pin9: RFOUT
Pin10: VG4, not connected
Pin11: VG1, first gate bias typically bias at -2.5V to get -0.5V on the device.

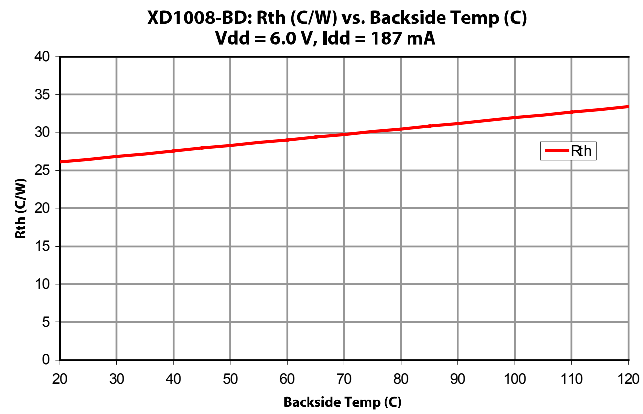
Bonding Diagram

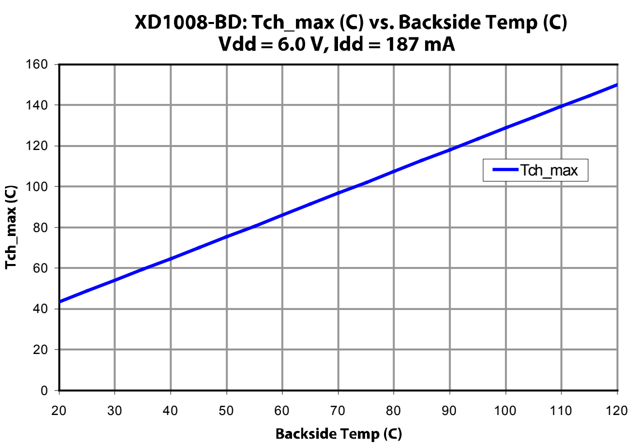


MTTF

These numbers were calculated based upon accelerated life test information received from the fabricating foundry and extensive thermal modeling/finite element analysis done at Mimix Broadband. The values shown here are only to be used as a guideline against the end application requirements and only represent reliability information under one bias condition. Ultimately bias conditions and resulting power dissipation along with the practical aspects, i.e. thermal material stack-up, attach method of die placement are the key parts in determining overall reliability for a specific application, see previous pages. If the data shown below does not meet your reliability requirements or if the bias conditions are not within your operating limits please contact technical sales for additional information.

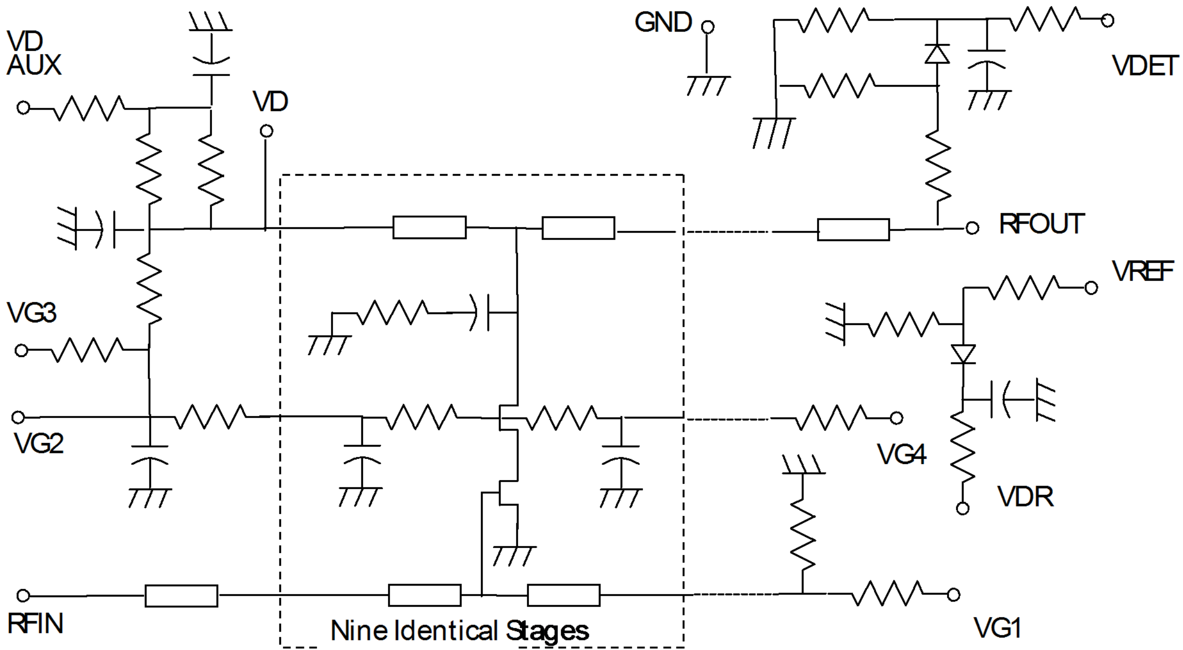






App Note [1] Biasing - The detector diode can be used to measure output power over a broad bandwidth. The detector diode is biased through the PA drain supply and the output voltage is measured at VDET with a high impedance voltage measurement device. A reference diode is also included which may be used to compensate for temperature and manufacturing process variation. The reference diode is biased through pin VDR with the same voltage as the PA drain supply and the voltage difference Vdelta = VDET – VREF is used to measure output power with temperature and manufacturing process compensation.

Biasing Schematic



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.