NB6L72M

2.5V / 3.3V Differential 2 X 2 Crosspoint Switch with CML Outputs

Multi−Level Inputs w/ Internal Termination

ON Semiconductor®

http://onsemi.com

Description

The NB6L72M is a high−bandwidth fully differential 2 x 2 Crosspoint Switch with internal source termination and CML output structure, optimized for low skew and minimal jitter.. The differential inputs incorporate internal 50 Ω termination resistors and will accept LVPECL, CML, LVDS, LVCMOS, or LVTTL logic levels. The SELECT inputs are single−ended and can be driven with LVCMOS/LVTTL.

The 16 mA differential CML outputs provide matching internal 50 Ω terminations and 400 mV output swings when externally terminated with a 50 Ω resistor to V_{CC}.

The device is offered in a small 3 mm x 3 mm 16−pin QFN package.

The NB6L72M is a member of the ECLinPS MAX™ family of high performance products.

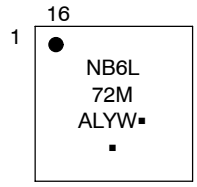
Features

- Maximum Input Clock Frequency > 3.0 GHz
- Maximum Input Data Rate > 5 Gb/s
- 360 ps Typical Propagation Delay
- 65 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV peak−to−peak, typical
- Operating Range: V_{CC} = 2.375 V to 3.63 V with GND = 0 V
- Internal Input and Output Termination Resistors, 50 Ω
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices



QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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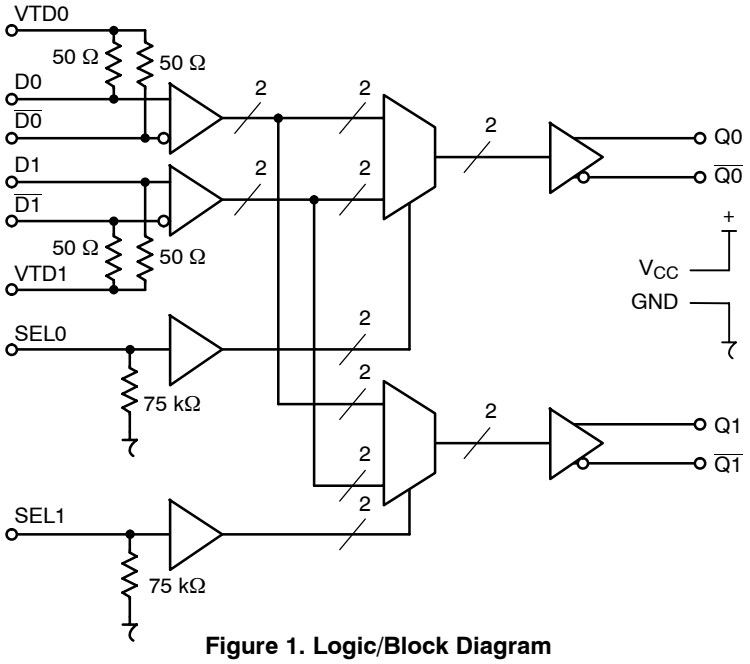


Figure 1. Logic/Block Diagram

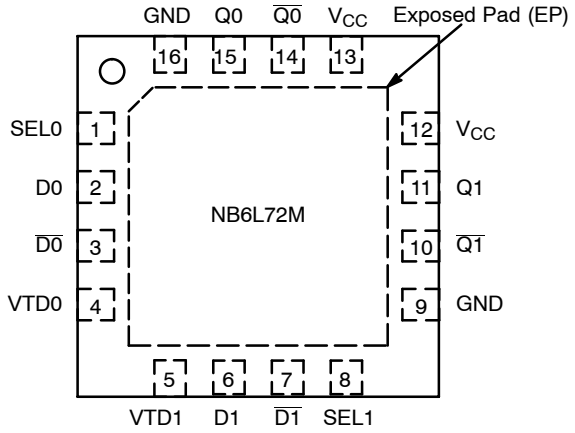


Figure 2. Pin Configuration (Top View)

Table 1. INPUT/OUTPUT SELECT TRUTH TABLE

SEL0*	SEL1*	Q0	Q1
L	L	D0	D0
H	L	D1	D0
L	H	D0	D1
H	H	D1	D1

*Defaults LOW when left open

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	SEL0	LVTTL,LVCMOS Input	Select Logic Input control that selects D0 or D1 to output Q0. See Table 1, Select Input Function Table. Pin defaults LOW when left open
2	D0	LVPECL, CML, LVDS, LVTTL, LVCMOS, Input	Noninverted Differential Input. Note 1
3	$\overline{D0}$	LVPECL, CML, LVDS, LVTTL, LVCMOS, Input	Inverted Differential Input. Note 1
4	VTD0	–	Internal 50 Ω Termination Pin. Note 1.
5	VTD1	–	Internal 50 Ω termination pin. Note 1.
6	D1	LVPECL, CML, LVDS, LVTTL, LVCMOS, Input	Noninverted Differential Input. Note 1.
7	$\overline{D1}$	LVPECL, CML, LVDS, LVTTL, LVCMOS, Input	Inverted Differential Input. Note 1
8	SEL1	LVTTL,LVCMOS Input	Select Logic Input control that selects D0 or D1 to output Q1. See Table 1, Select Input Function Table. Pin defaults LOW when left open
9	GND	–	Negative Supply Voltage
10	$\overline{Q1}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
11	Q1	CML Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
12	V_{CC}	–	Positive Supply Voltage
13	V_{CC}	–	Positive Supply Voltage
14	$\overline{Q0}$	CML Output	Inverted Differential Reset Input. Typically Terminated with 50 Ω Resistor to V_{CC}.
15	Q0	CML Output	Noninverted Differential Reset Input. Typically Terminated with 50 Ω Resistor to V_{CC}.
16	GND	–	Negative Supply Voltage
–	EP	–	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pin (VTDn, $\overline{VTDn}$) are connected to a common termination voltage or left open, and if no signal is applied on Dn/$\overline{Dn}$ input, then the device will be susceptible to self−oscillation.
2. All V_{CC} and GND pins must be externally connected to a power supply for proper operation.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200V
Moisture Sensitivity	16−QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.0	V
V_{IO}	Positive Input/Output Voltage	GND = 0 V	$-0.5 \le V_{Io} \le V_{CC} + 0.5$	4.0	V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$			2.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current (CML Output)	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range	QFN−16		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	QFN−16 QFN−16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	QFN−16	4	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, Multi−Level Inputs V_{CC} = 2.375 V to 3.63 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current (Inputs and Outputs Open)	60	80	105	mA
CML OUTPUTS (Notes 5 and 6)					
V_{OH}	Output HIGH Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 40 3260 2460	V_{CC} − 10 3290 2490	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 500 2800 2000	V_{CC} − 400 2900 2100	V_{CC} − 300 3000 2200	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (see Figures 6 and 8)					
V_{th}	Input Threshold Reference Voltage Range (Note 7)	1125		V_{CC} − 75	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} + 75		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 75	mV
V_{ISE}	Single−Ended Input Voltage Amplitude (V_{IH} − V_{IL})	150		2800	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 7 and 9) (Note 8)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{CC} − 150	mV
V_{ID}	Differential Input Voltage Swing (Dn, $\overline{Dn}$) (V_{IHD} − V_{ILD}) (**Note 15**)	150		2800	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 9)	1125		V_{CC} − 75	mV
I_{IH}	Input HIGH Current Dn/$\overline{Dn}$, (VTDn/$\overline{VTDn}$ Open)	−10		50	μA
I_{IL}	Input LOW Current Dn/$\overline{Dn}$, (VTDn/$\overline{VTDn}$ Open)	−50		10	μA
SINGLE−ENDED LVCMOS/LVTTL CONTROL INPUTS					
V_{IH}	Single−Ended Input HIGH Voltage	2000		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		800	mV
I_{IH}	Input HIGH Current	−10		10	μA
I_{IL}	Input LOW Current	−150		0	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω
R_{TOUT}	Internal Output Termination Resistor	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
5. Input and output parameters vary 1:1 with V_{CC}.
6. V_{th}, V_{IH}, $V_{IL,}$, and V_{ISE} parameters must be complied with simultaneously.
7. V_{th} is applied to the complementary input when operating in single−ended mode.
8. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{CMR} parameters must be complied with simultaneously.
9. V_{CMR} minimum varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.63 V, GND = 0 V, or V_{CC} = 0 V, GND = −2.375 V to −3.63 V, T_A = −40°C to +85°C; (Note 10)

Symbol	Characteristic		Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 15) (See Figure 4)	$f_{in} \le 3$ GHz	250	380		mV
t_{PLH}, t_{PHL}	Propagation Delay (@0.5GHz)	Dn to Qn SELn to Qn	230	360	480	ps
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew Device to Device Skew (Note 12)			 6.0	20 25 85	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \le 3.0$ GHz	40	50	60	%
t_{JITTER}	RMS Random Clock Jitter (Note 13) Peak−to−Peak Data Dependent Jitter (Note 14)	$f_{in} \le 3.0$ GHz f_{in} = 2.5 Gb/s f_{in} = 3.0 Gb/s		0.2 5.0 8.0	0.5 15 25	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15)		150		2800	mV
t_r, t_f	Output Rise/Fall Times @ 0.5 GHz, (20% − 80%),	Q, $\overline{Q}$		65	120	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing V_{INPP} (minimum) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
11. Duty cycle skew is measured between differential outputs using the deviations of the sum of $T_{pw}-$ and $T_{pw}+$ @ 0.5GHz.
12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS23.
15. Input and output voltage swing is a single−ended measurement operating in differential mode.

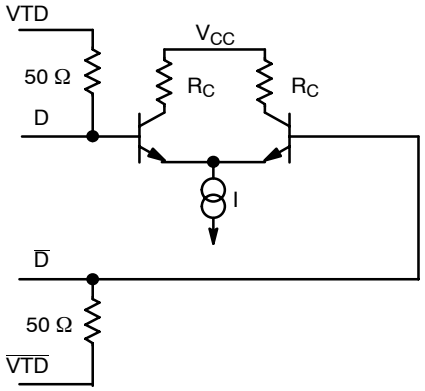


Figure 3. Input Structure

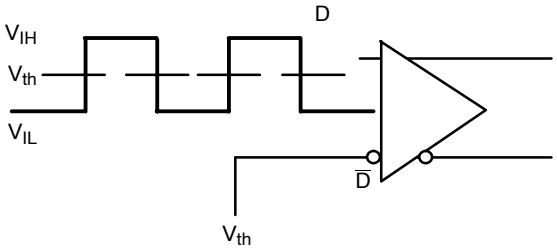


Figure 4. Differential Input Driven Single−Ended

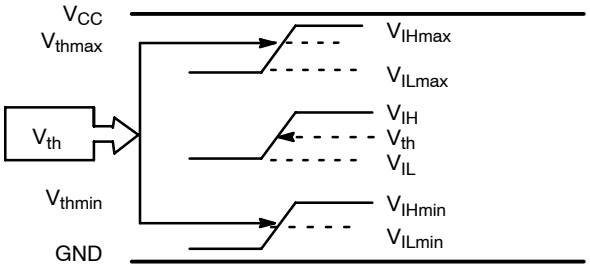


Figure 5. V_{th} Diagram

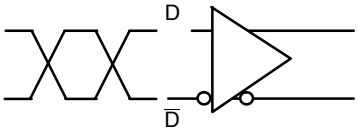


Figure 6. Differential Inputs Driven Differentially

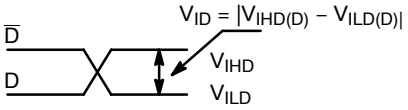


Figure 7. Differential Inputs Driven Differentially

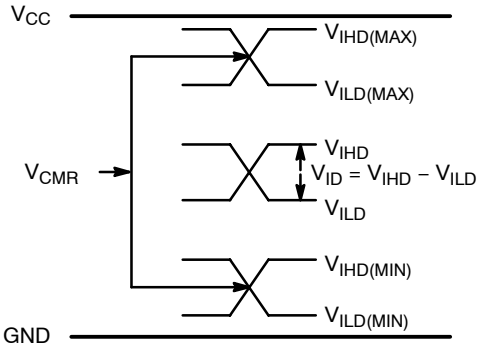


Figure 8. V_{CMR} Diagram

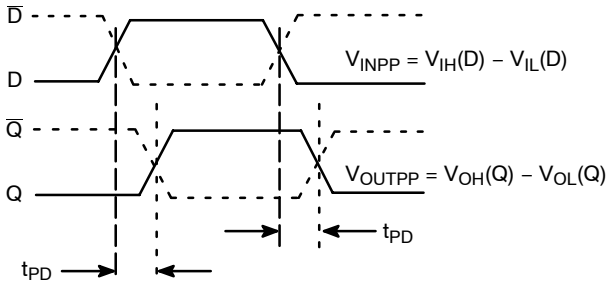


Figure 9. AC Reference Measurement

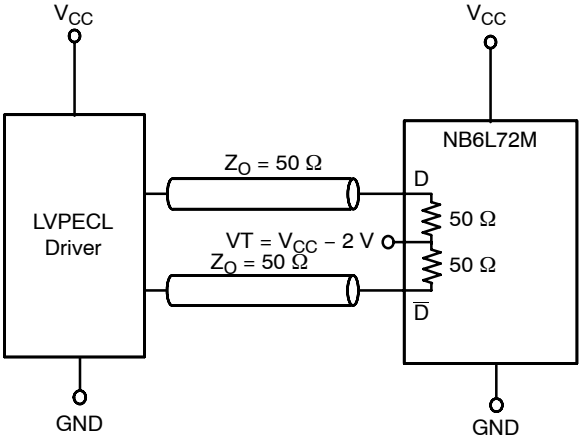


Figure 10. LVPECL Interface

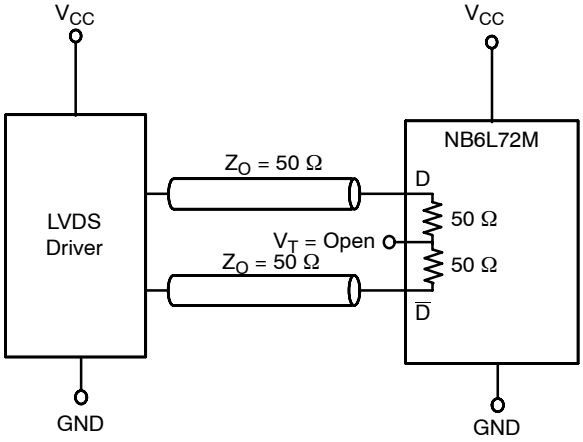


Figure 11. LVDS Interface

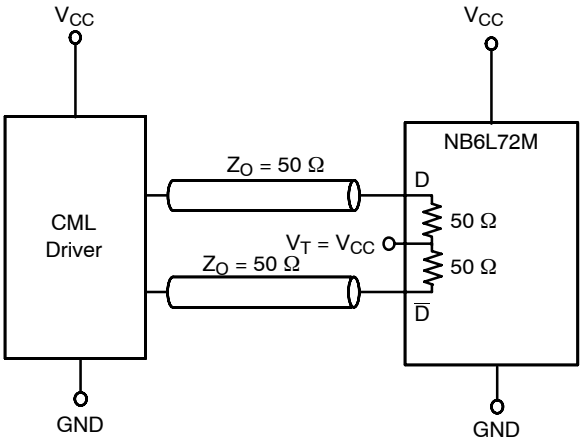


Figure 12. Standard 50 Ω Load CML Interface

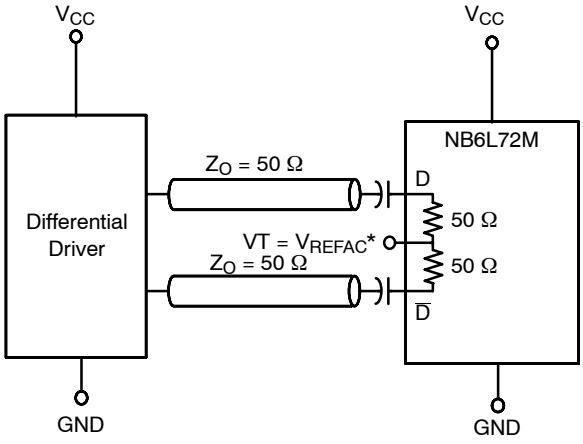


Figure 13. Capacitor−Coupled Differential Interface (VT Connected to V_{REFAC})

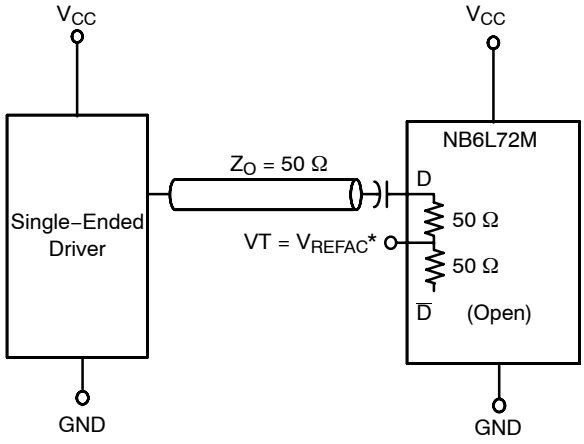


Figure 14. Capacitor−Coupled Single−Ended Interface (VT Connected to V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

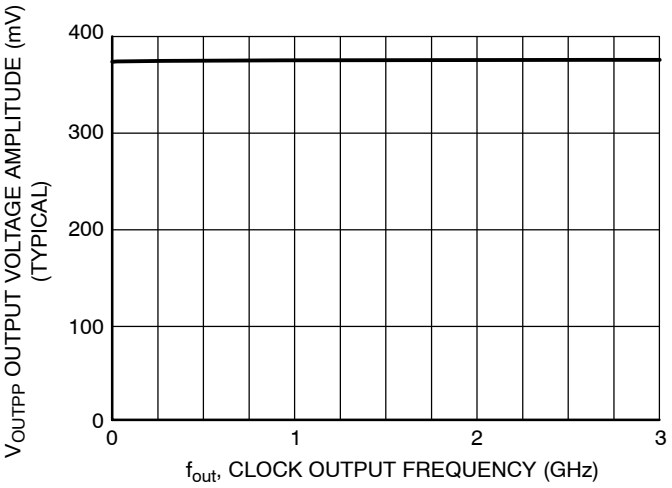


Figure 15. Output Voltage Amplitude (V_{OUTPP}) versus Output Frequency at Ambient Temperature (Typical)

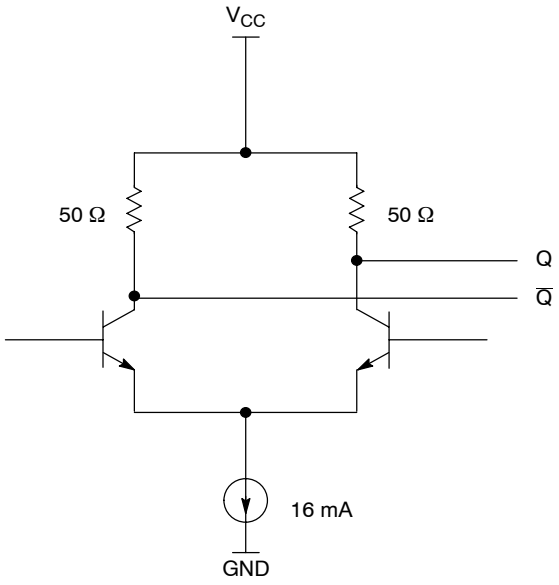


Figure 16. CML Output Structure

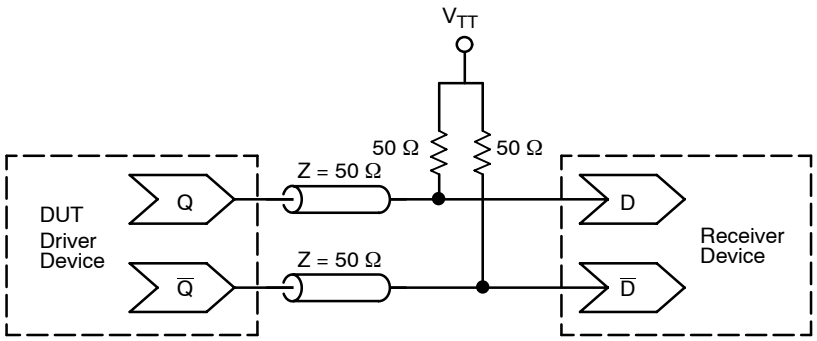


Figure 17. Typical CML Termination for Output Driver and Device Evaluation

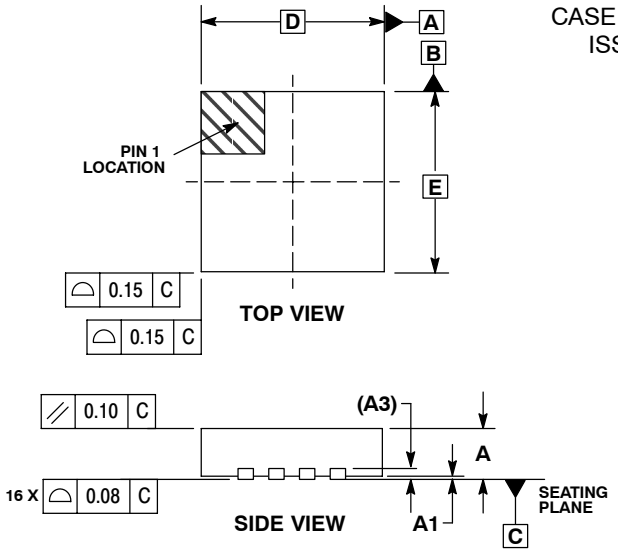
ORDERING INFORMATION

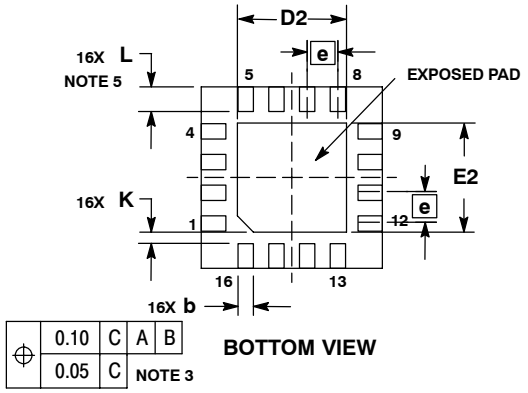
Device	Package	Shipping†
NB6L72MMNG	QFN−16 (Pb−free)	123 Units / Rail
NB6L72MMNR2G	QFN−16 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G−01
ISSUE C

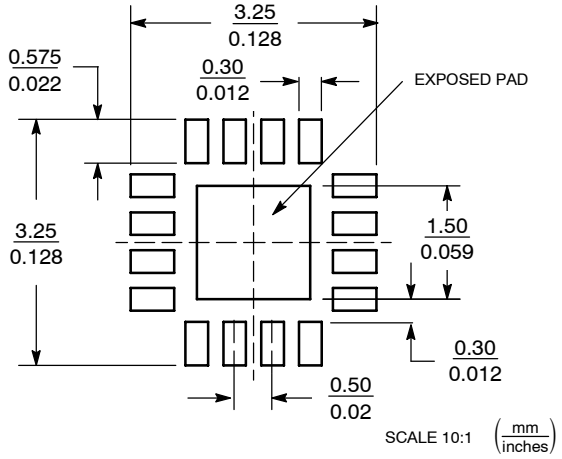




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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