Features

- **Supply Voltage Range 3 V to 4.6 V (Unregulated)**
- **Auxiliary Voltage Regulator On-chip**
- **Low Current Consumption**
- **Few Low Cost External Components**
- **No Mechanical Tuning Required**
- **Non-blindslot and Blindslot Operation**
- **Unlimited Multislot Operation with Advanced Closed-loop Modulation**
- **Supports Multiple Reference Clocks (10.368 MHz/13.824 MHz/20.736 MHz)**
- **TX Preamplifier with 0 dBm Output Power at 1.9 GHz and Ramp-signal Generator for SiGe Power Amplifier**

Electrostatic sensitive device.
Observe precautions for handling.

DECT Single-chip Transceiver

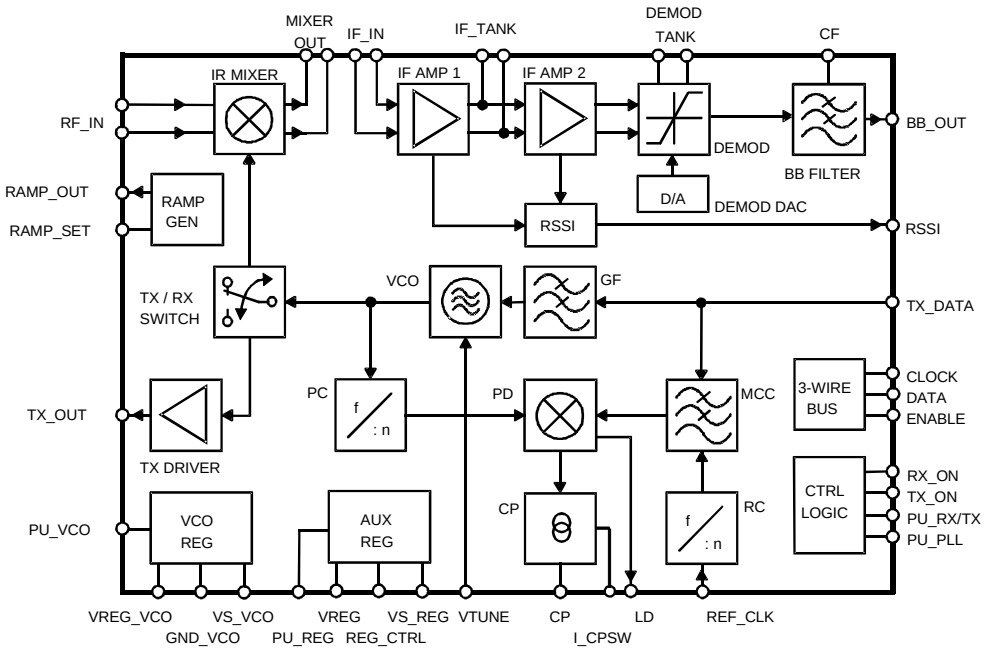
T2801

Preliminary

Description

The T2801 is an RF IC for low-power DECT applications. The HP-VFQFP-N48-packaged IC is a complete transceiver including image rejection mixer, IF amplifier, FM demodulator, baseband filter, RSSI, TX preamplifier, power-ramping generator for power amplifiers, integrated synthesizer, fully integrated VCO, TX filter and modulation compensation circuit for advanced closed-loop modulation concept. No mechanical tuning is necessary in production.

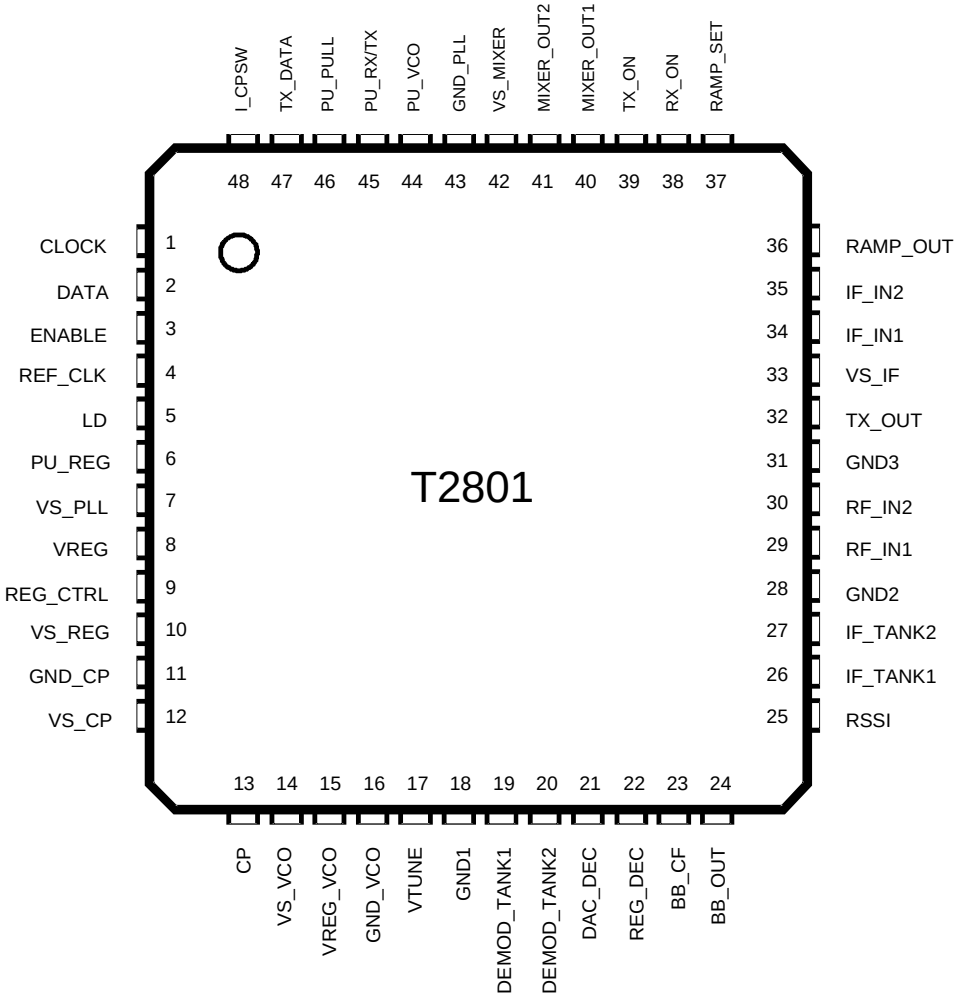
Figure 1. Block Diagram



Rev. 4567A–DECT–01/03

Pin Configuration

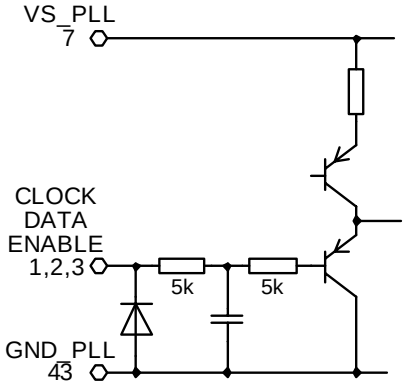
Figure 2. Pinning HP-VFQFP-N48



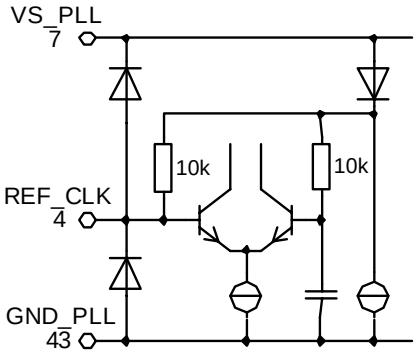
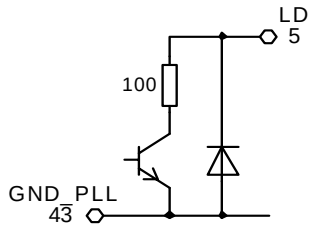
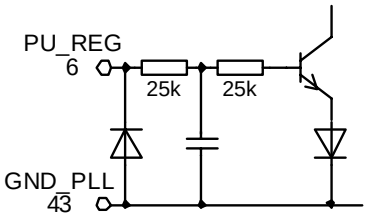
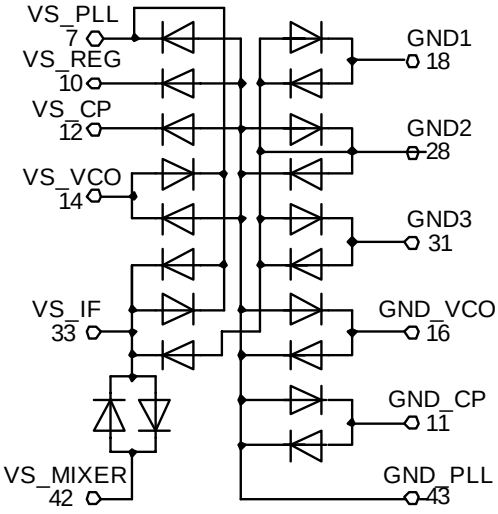
Functional Block Description

Name	Description
AUX REG	Auxiliary voltage regulator
BBF	Baseband filter
CP	Charge pump
DAC	D/A converter for demodulator tuning
DEMOD	Demodulator
GF	Gaussian filter for transmit data
IF AMP1	1st intermediate frequency amplifier
IF AMP2	2nd intermediate frequency amplifier
IR MIXER	Image rejection mixer
MCC	Modulation compensation circuit
PC	Programmable counter
PD	Phase detector
RAMP GEN	Ramp-signal generator
RC	Reference counter
RSSI	Received signal-strength indicator
TX DRIVER	Buffer amplifier for TX_OUT
TX/RX SWITCH	Switches VCO signal to IR mixer resp. TX driver
VCO	Voltage-controlled oscillator
VCO REG	Voltage regulator for VCO

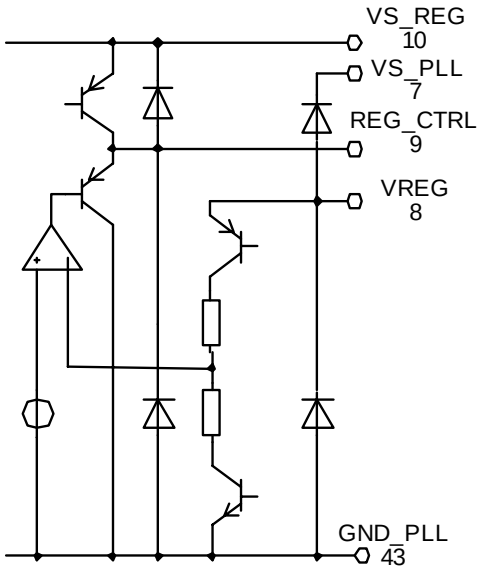
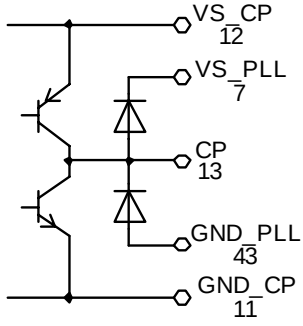
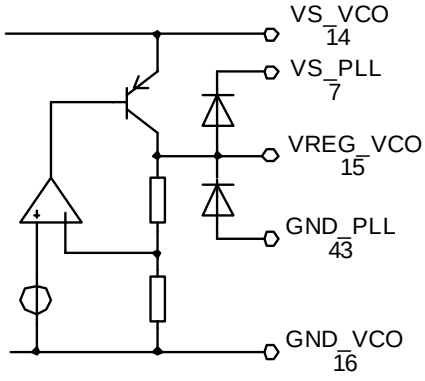
Pin Description

Pin	Symbol	Function	Configuration
1	CLOCK	3-wire-bus: Clock input	
2	DATA	3-wire-bus: Data input	
3	ENABLE	3-wire-bus: Enable input	

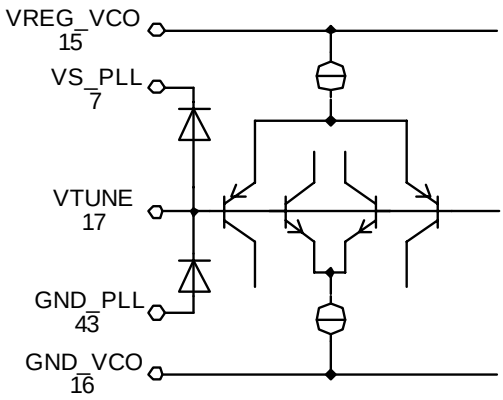
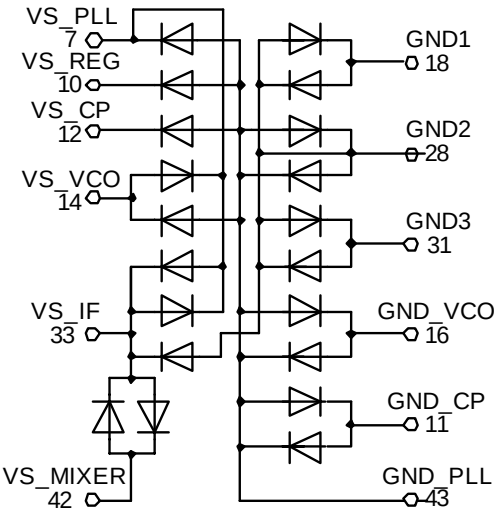
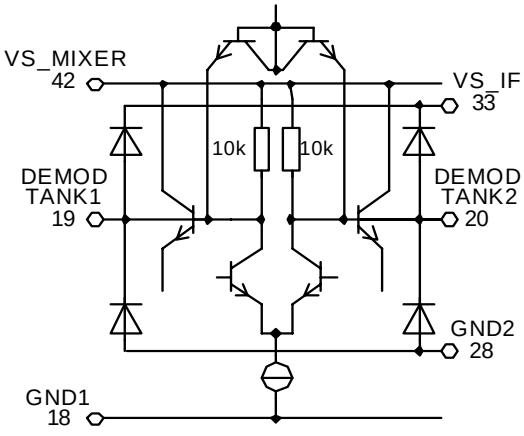
Pin Description (Continued)

Pin	Symbol	Function	Configuration
4	REF_CLK	Reference-frequency input	
5	LD	Lock-detect output	
6	PU_REG	Power-up input for auxiliary voltage regulator	
7	VS_PLL	PLL supply voltage	

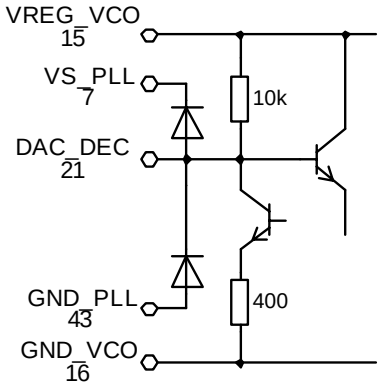
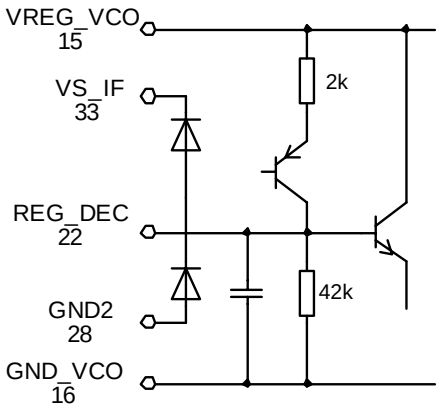
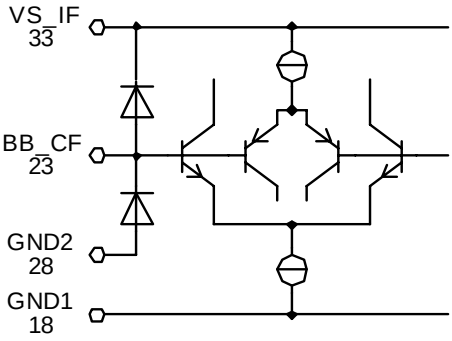
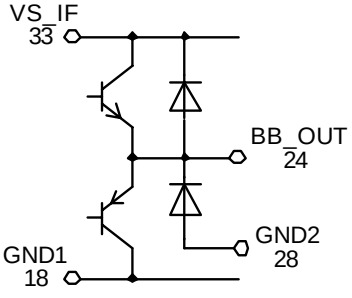
Pin Description (Continued)

Pin	Symbol	Function	Configuration
8 9 10	VREG REG_CTRL VS_REG	Auxiliary voltage-regulator output Auxiliary voltage-regulator control output Auxiliary voltage-regulator supply voltage	
11 12 13	GND_CP VS_CP CP	Charge-pump ground Charge-pump supply voltage Charge-pump output	
14 15 16	VS_VCO VREG_VCO GND_VCO	VCO voltage-regulator supply voltage VCO voltage-regulator control output VCO ground	

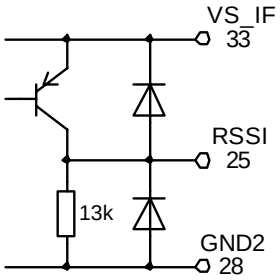
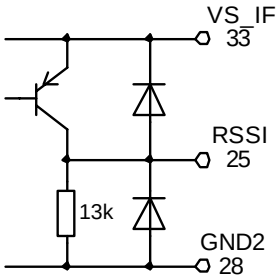
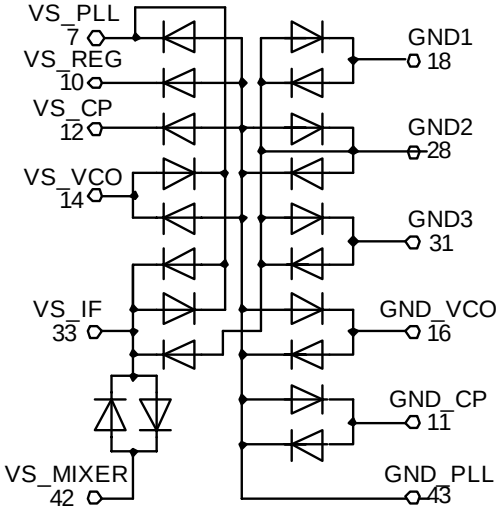
Pin Description (Continued)

Pin	Symbol	Function	Configuration
17	VTUNE	VCO tuning voltage input	
18	GND1	Ground	
19 20	DEMOD_TANK1 DEMOD_TANK2	Demodulator tank circuit Demodulator tank circuit	

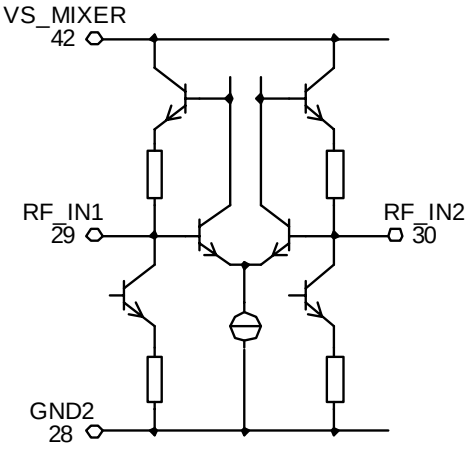
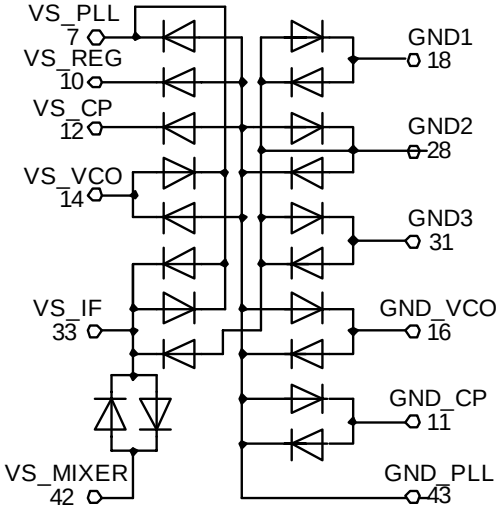
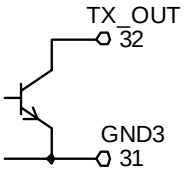
Pin Description (Continued)

Pin	Symbol	Function	Configuration
21	DAC_DEC	Decoupling pin for VCO_DAC	
22	REG_DEC	Decoupling pin for VCO_REG	
23	BB_CF	Baseband filter corner-frequency control input	
24	BB_OUT	Baseband filter output	

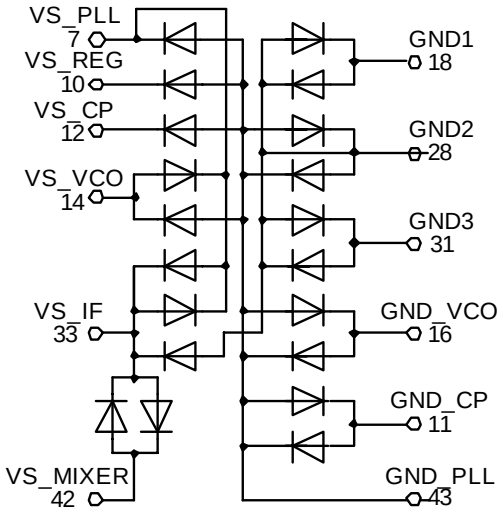
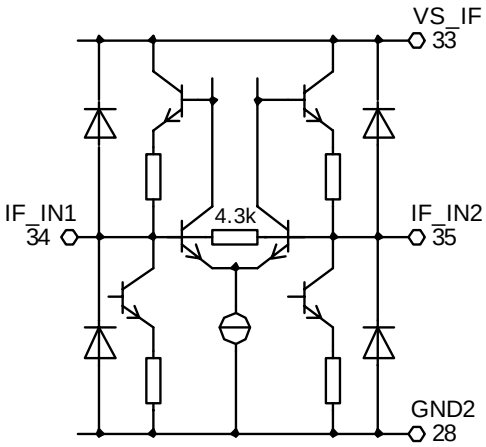
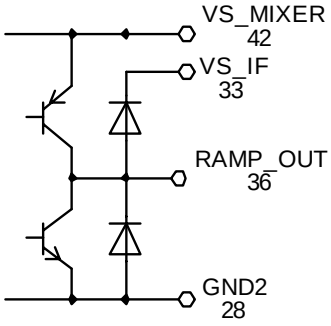
Pin Description (Continued)

Pin	Symbol	Function	Configuration
25	RSSI	Received signal-strength indicator output	
26 27	IF_TANK1 IF_TANK2	IF tank circuit IF tank circuit	
28	GND2	Ground	

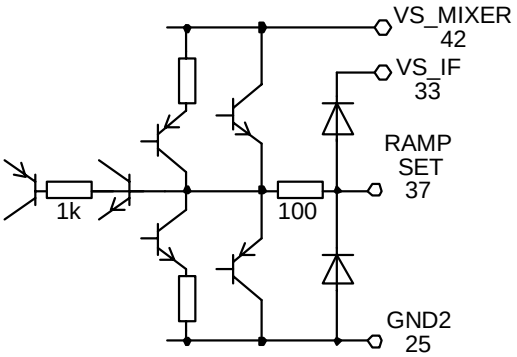
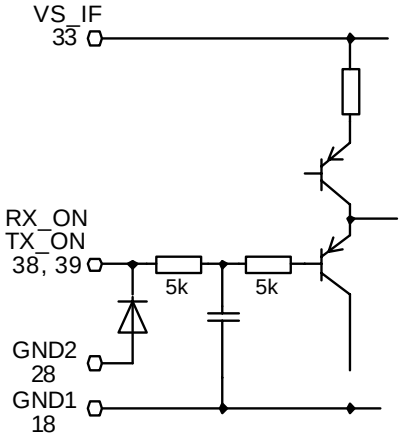
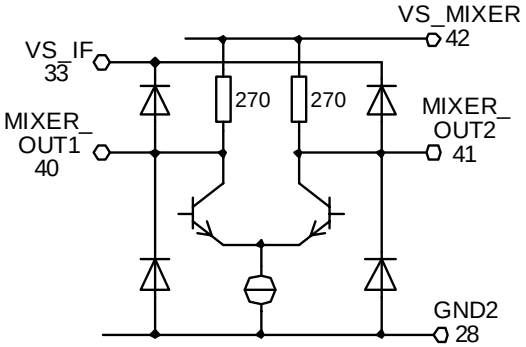
Pin Description (Continued)

Pin	Symbol	Function	Configuration
29 30	RF_IN1 RF_IN2	RF input of image reject mixer RF input of image reject mixer	
31	GND3	Ground	
32	TX_OUT	TX driver amplifier output for PA	

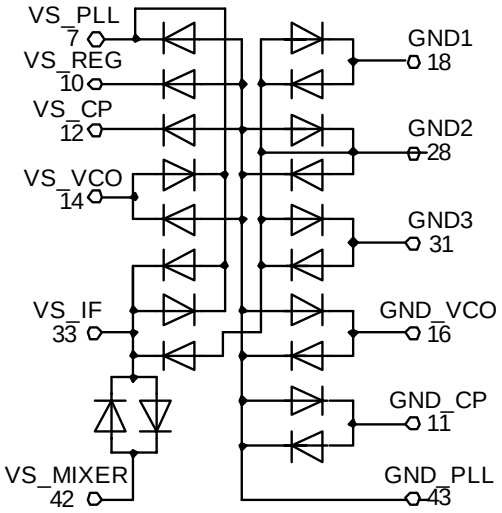
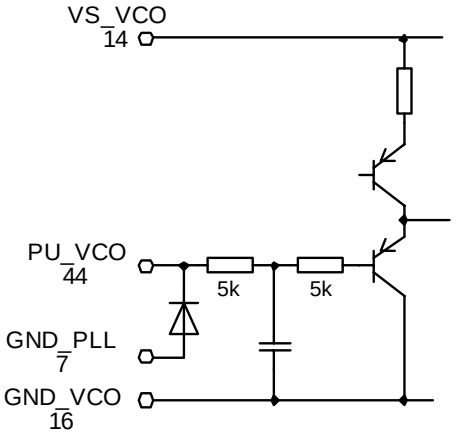
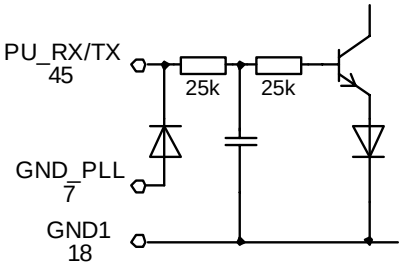
Pin Description (Continued)

Pin	Symbol	Function	Configuration
33	VS_IF	IF amplifier supply voltage	
34 35	IF_IN1 IF_IN2	IF input of IF amplifier IF input of IF amplifier	
36	RAMP_OUT	Ramp-generator output for PA power ramping	

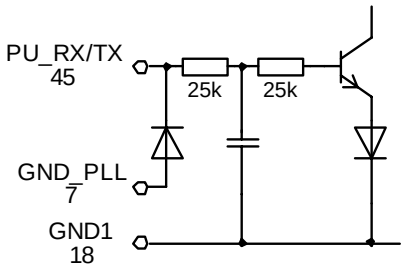
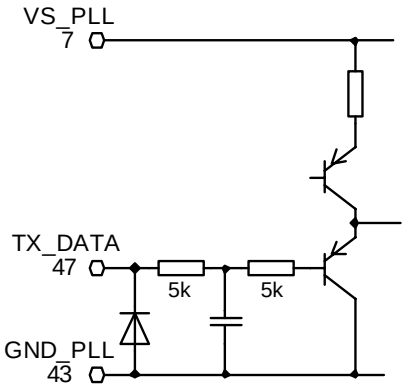
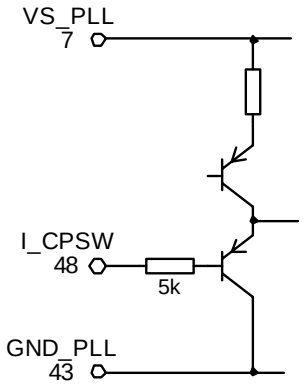
Pin Description (Continued)

Pin	Symbol	Function	Configuration
37	RAMP_SET	Slew-rate setting of ramping signal	
38 39	RX_ON TX_ON	RX control input TX control input	
40 41	MIXER_OUT1 MIXER_OUT2	Mixer output to SAW filter Mixer output to SAW filter	

Pin Description (Continued)

Pin	Symbol	Function	Configuration
42 43	VS_MIXER GND_PLL	Mixer supply voltage PLL ground	
44	PU_VCO	VCO power-up input	
45	PU_RX/TX	RX/TX power-up input	

Pin Description (Continued)

Pin	Symbol	Function	Configuration
46	PU_PLL	PLL power-up input	
47	TX_DATA	TX data input of Gaussian filter and modulation-compensation circuit	
48	I_CPSW	Charge pump switch input controls charge pump current	

Functional Description

Receiver

The RF signal at RF_IN is fed to an image rejection mixer IR_MIXER with its differential outputs MIXER_OUT1 and MIXER_OUT2 driving an IF-SAW filter at 110.592 MHz or 112.32 MHz. The IF amplifiers IF_AMP1 and IF_AMP2 with an external IF_TANK and an integrated RSSI function feed the signal to the demodulator DEMOD working at f = f_{IF}/2 ([55 MHz) and finally to an integrated baseband filter BB. For demodulator tuning in production, an integrated 5-bit Digital-to-Analog (D/A) converter is provided to control the on-chip varicap diode.

Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian Filter (GF) and fed to the fully integrated VCO operating at twice the output frequency. After modulation, the signal is frequency-divided by 2 and fed via a TX/RX SWITCH to the TX_DRIVER. This bus-controlled driver amplifier supplies typical +3 dBm output power at TX_OUT. An integrated ramp-signal generator, RAMP_GEN, provides a ramp signal at RAMP_OUT for the external power amplifier. The slope of the ramp signal is controlled by a capacitor at the RAMP_SET pin.

Synthesizer

The IR_MIXER, the TX_DRIVER and the programmable counter PC are driven by the fully integrated VCO (including on-chip inductors and varactors). An 3-bit digital-to-analog converter is used to pretune the frequency. The output signal is frequency-divided to supply the desired frequency to the TX_DRIVER, 0/90 degree phase shifter for the IR_MIXER and to be used by the PC for the phase detector PD (f_{PD} = 3.456 MHz). Unlimited multislot operation is possible by using the integrated advanced closed-loop modulation concept based on the modulation compensation circuit MCC.

Power Supply

An integrated bandgap-stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current saving modes are provided.

Figure 3. PLL Principle

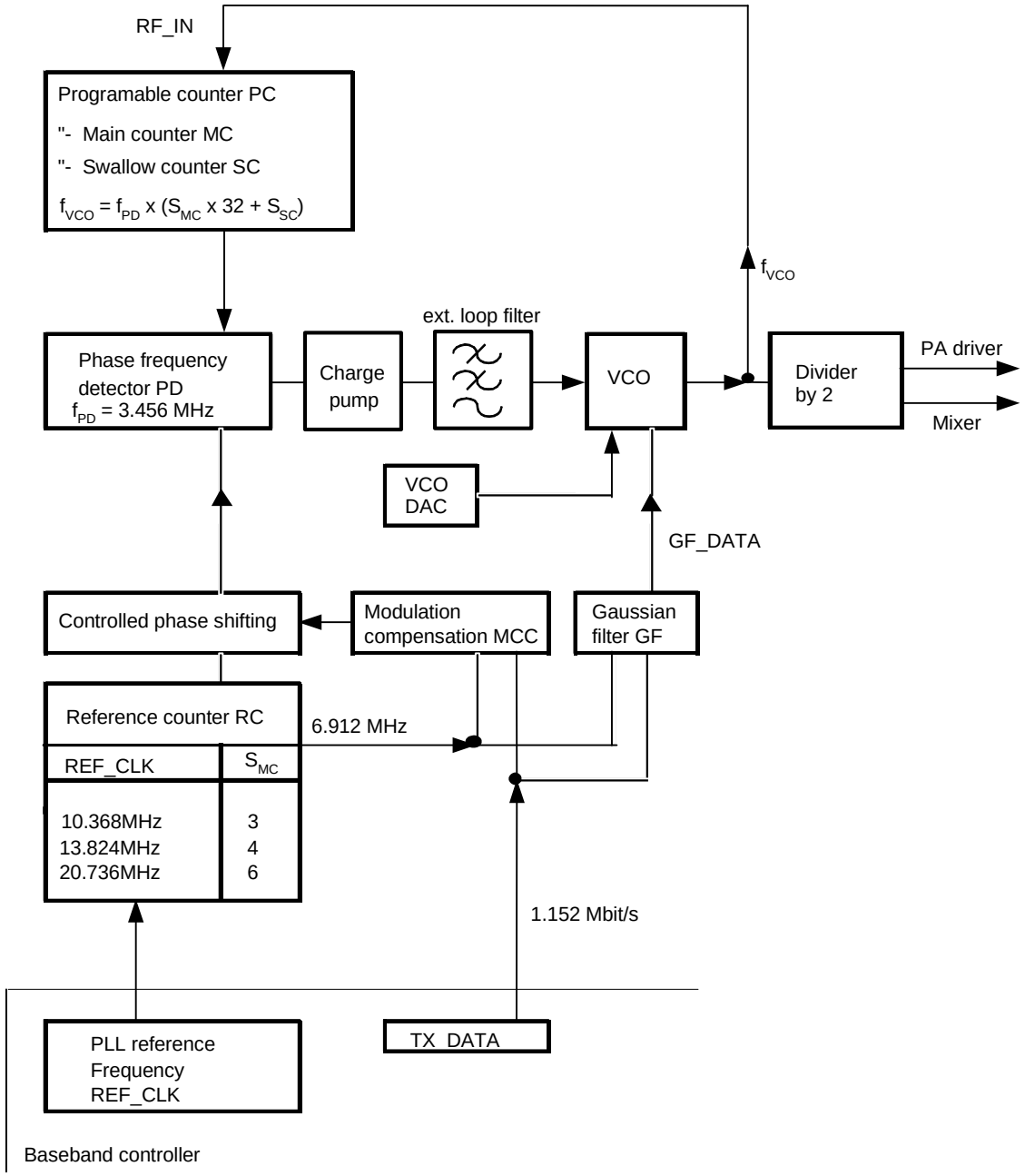


Table 1 shows the LO frequencies for RX and TX for the DECT band plus additional channels for the extended DECT band. Intermediate frequencies of 110.592 MHz and 112.32 MHz are supported.

Table 1. LO Frequencies

Mode	f_{IF}/MHz	Channel	f_{ANT}/MHz	f_{VCO}/MHz	S_{MC}	S_{SC}
TX		C9	1881.792	1881.792	34	1
TX		C8	1883.520	1883.520	34	2
TX		...	...	...	...	...
TX		C1	1895.616	1895.616	34	9
TX		C0	1897.344	1897.344	34	10
TX		C10	1899.072	1899.072	34	11
TX		C11	1900.800	1900.800	34	12
TX		...	...	...	...	...
TX		C29	1931.904	1931.904	34	30
TX		C30	1933.632	1933.632	34	31
RX	110.592	C9	1881.792	1771.200	32	1
RX	110.592	C8	1883.520	1772.928	32	2
RX	110.592	...	...	...	...	...
RX	110.592	C1	1895.616	1785.024	32	9
RX	110.592	C0	1897.344	1786.752	32	10
RX	110.592	C10	1899.072	1788.480	32	11
RX	110.592	C11	1900.800	1790.208	32	12
RX	110.592	...	...	...	...	...
RX	110.592	C29	1931.904	1821.312	32	30
RX	110.592	C30	1933.632	1823.040	32	31
RX	112.320	C9	1881.792	1769.472	32	0
RX	112.320	C8	1883.520	1771.200	32	1
RX	112.320	...	...	...	...	...
RX	112.320	C1	1895.616	1783.296	32	8
RX	112.320	C0	1897.344	1785.024	32	9
RX	112.320	C10	1899.072	1786.752	32	10
RX	112.320	C11	1900.800	1788.480	32	11
RX	112.320	...	...	...	...	...
RX	112.320	C29	1931.904	1819.584	32	29
RX	112.320	C30	1933.632	1821.312	32	30

Formula:

TX: $f_{ANT} = f_{VCO} = 1.728\ MHz \times (32 \times S_{MC} + S_{SC})$

RX: $f_{ANT} = 1.728\ MHz \times (32 \times S_{MC} + S_{SC}) + f_{IF}$

Control Signals

Table 2. Control Signals – Functions

Signal	Function
I_CPSW	Controls the charge pump current
PU_REG	Activates AUX voltage regulator supplying the complete transceiver
PU_VCO	Activates VCO voltage regulator which supplies only the VCO
PU_RX/TX	Activates RX/TX blocks
PU_PLL	Activates PLL circuits: PC, PD, CP, RC
RX_ON	Activates RX circuits: BBF, DEMOD, IF AMP, IR MIXER
TX_ON	Activates TX circuits: TX–DRIVER, RAMP GEN. Starts RAMP SIGNAL at RAMP OUT
Data Word 1, Bit D10	Activates GF in TX mode
Data Word 1, Bit D9	Activates MCC in TX mode

Table 3. Control Signals – Modes

Mode	TX Mode	RX Mode	RSSI Only
PU_REG	1	1	1
PU_VCO	1	1	1
PU_RX/TX	1	1	1
PU_PLL	1	1	1
RX_ON	0	1	1
TX_ON	1	0	1
BB filter	OFF	ON	OFF
Demodulator	OFF	ON	OFF
IF amplifiers and RSSI	OFF	ON	ON
IR mixer	OFF	ON	ON
RX switch	OFF	ON	ON
TX switch	ON	OFF	OFF
TX driver	ON	OFF	OFF
Ramp generator	ON	OFF	OFF
Programmable counter	ON	ON	ON
Voltage-controlled oscillator	ON	ON	ON
Gaussian filter	ON	OFF	OFF
Phase detector/charge pump	ON	ON	ON
Modulation compensation circuit	ON	OFF	OFF
Reference counter	ON	ON	ON
Typical current consumption/mA at V_S = 3.2 V	54	85	80

Serial Programming Bus

The transceiver is programmed by the 3-wire bus (CLOCK, DATA and ENABLE).

After setting enable signal to low condition, on the rising edge of the clock signal, the data is transferred bit by bit into the shift register, starting with the MSB-bit. After enable returning to high condition, the programmed information is loaded into the addressed latches, according to the addressbit condition (last bit). Additional leading bits are ignored and there is no check made on how many pulses arrived during enable-low condition. During enable low condition, the bus current is increased to speed up the bus logic.

The programming of the transceiver is separated into two data words. Data word 1 controls mainly the channel information together with settings, which are closely related with the channel. Data word 2 holds setup information, which is adjusted during production.

Data Word 1

MSB																						LSB
Data Bits																						Address Bit
D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A0
RC		SC					MC		VCOs	1	1	GF	MCC	GFCS			VCODAC			CPCS		GF	1

Data Word 2

E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	A0
DEMODDAC					MCCS			TEST			0

Data Word 1 Programs

PLL Settings

With the Reference Counter Bits D21-D22

RC (Referene Counter)			
D22	**D21**	**S_{RC}**	**REF_CLK (MHz)**
0	0	3	10.638
0	1	4	13.824
1	0	6	20.736

With the Main Counter Bits D14-D15

MC (Main Counter)		
D15	**D14**	**S_{RC}**
0	0	32
0	1	33
1	0	34
1	1	35

With the Swallow Counter Bits D16-D20

SC (Swallow Counter)					
D20	**D19**	**D18**	**D17**	**D16**	**S_{SC}**
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...					...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

VCO Select (RX/TX VCO)

With bit D13
Used to switch between RX/TX VCO

D13	VCOS (VCO Select)
0	RX-VCO
1	TX-VCO

Gaussian Filter On/Off

With bit D10
GF is used only in TX mode

D10	GF (Gaussian Filter)
0	OFF
1	ON

Modulation Compensation Circuit On/Off

With bit D9
MCC is used only in TX mode

D9	MCC (Modulation Compensation Circuit)
0	OFF
1	ON

GFCS Adjustment

With bit D6 - D8
Only in TXmode effective for setting the frequency deviation of the modulation

GFCS(Gaussian Filter Settings)			
D8	**D7**	**D6**	**GFCS (%)**
0	0	0	60
0	0	1	70
0	1	0	80
0	1	1	90
1	0	0	100
1	0	1	110
1	1	0	120
1	1	1	130

VCO_DAC Adjustment

With bit D3 - D5

Used to pretune the VCO frequency in case of production tolerances of the device. Tuning voltage in locked condition should be around 1.8 V at room temperature. This gives margin for ambient temperature changes.

Pretune DAYC Voltage			
D5	**D4**	**D3**	**f_{VCO}/%**
0	0	0	-5
0	0	1	...
0	1	0	...
0	1	1	...
1	0	0	...
1	0	1	...
1	1	0	...
1	1	1	5

CPCS Adjustment

With bit D0 - D2

Used to adjust the charge pump current. This can be used to compensate the change of the tuning sensitivity over frequency and device tolerances.

CPCS (Charge-pump Current Settings)			
D2	**D1**	**D0**	**CPCS**
0	0	0	-4
0	0	1	-3
0	1	0	-2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	2
1	1	1	3

Data Word 2 Programs

DEMODDAC Adjustment

With bits E6 - E10

Only in RX mode effective. Used to tune the demodulator center frequency and allows to compensate tolerances of extenal components and the T2801.

Demod DAC Voltage					
E10	**E9**	**E8**	**E7**	**E6**	**$f_{IFcenter}$ (%)**
0	0	0	0	0	-5
0	0	0	0	1	...
0	0	0	1	0	...
					...
1	1	1	0	1	...
1	1	1	1	0	...
1	1	1	1	1	5

MCCS Adjustment

With bits E3 - E5

Only in TX mode effective. Adjusts the modulation compensation circuit for closed loop modulation. This adjustment is done with a test sequence of a long stream of ‚1' - ‚0'. The correct setting is achieved, if the modulation is not affected by the PLL.

MCCS (Modulation Compensation Settings)			
E5	**E4**	**E3**	**MCCS (%)**
0	0	0	60
0	0	1	70
0	1	0	80
0	1	1	90
1	0	0	100
1	0	1	110
1	1	0	120
1	1	1	130

TEST Mode Settings

With bit E0 - E2 and D11

In normal operation Lock detect output is used. All other settings are for test only.

D11	E2	E1	E0	Signal at Lock Detect Output	CP Mode
1	0	0	0	Lock detect	Active
0	0	0	1	RC out/2	Active
1	0	1	0	PC out/2	Active
X	0	1	1	MCCTEST: RC out diviced by 512	Active
1	1	0	0	Lock detect	High imp.
0	1	0	1	RC out/2	High imp.
1	1	1	0	PC out/2	High imp.
X	1	1	1	GFTEST: RC out	High imp.

Figure 4. 3-wire Bus Protocol Timing Diagram

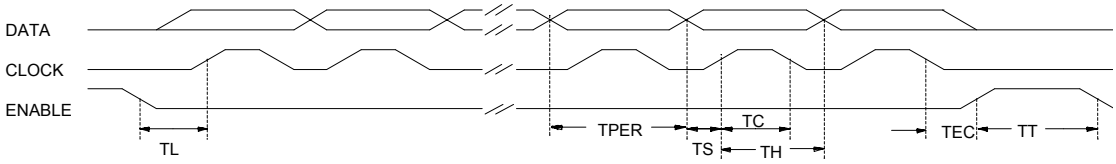


Table 4. 3-wire Bus Protocol

Description	Symbol	Minimum Value	Unit
Clock period	TPER	125	ns
Set time data to clock	TS	60	ns
Hold time data to clock	TH	60	ns
Clock pulse width	TC	60	ns
Set time enable to clock	TL	200	ns
Hold time enable to data	TEC	0	ns
Time between two protocols	TT	250	ns

Figure 5. TX DATA Timing

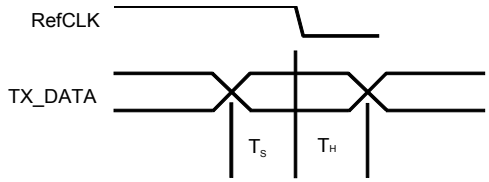


Table 5. TX DATA Timing Values

Parameters	Symbol	Value	Remarks
Set-up time TX DATA	TS	10 ns	TS and TH must be considered for both (falling and rising) edges of RefCLK when using REF_CLK = 10.368 MHz.
Hold time TX DATA	TH	10 ns	

Absolute Maximum Ratings

All voltages refer to GND

Parameters	Symbol	Min.	Max.	Unit
Supply voltage regulator, Pin 10	V_{S_REG}	3.2	4.7	V
Supply voltage, Pins 7, 12, 14, 33 and 42	V_S	3.0	4.7	V
Logic input voltage, Pins 1, 2, 3, 38, 39, 44, 45, 46, 47 and 48	V_{IN}	-0.3	V_S	V
Junction temperature	T_{jmax}		150	°C
Storage temperature	T_{Stg}	-40	+150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	TBD	K/W

Operating Range

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage regulator, Pins 10	V_{S_REG}	3.2	3.6	4.6	V
Supply voltage, Pins 7, 12, 14, 33 and 42	V_S	3.0	3.0	4.6	V
Ambient temperature	T_{amb}	-25		+85	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
IR Mixer Pins 29, 30, 40 and 41						
Input impedance	Pins 29 and 30	Z_{in}		50		Ω
Input matching	Pins 29 and 30	$VSWR_{in}$		<2:1		
Image rejection ratio	Pins 40 and 41	IRR		20		dB
DSB noise figure	Pins 40 and 41	NFDSB= NFSSB		10		dB
Conversion gain	Rload = 200 Ω	G_{conv}		11		dB
Input interception point	Pins 40 and 41	IIP3		-10		dBm
IF Amplifier Pins 26, 27, 34 and 35						
Input impedance	Pins 34 and 35	Z_{in}	200		400	Ω
Lower cut-off frequency		fl_{3dB}		90		MHz
Upper cut-off frequency		fu_{3dB}		130		MHz
Power gain		Gp		85		dB
Bandwidth of external tank circuit	Pins 26 and 27	BW3dB		10		MHz
Noise figure		NF		9		dB
RSSI Pins 25, 34 and 35						
RSSI sensitivity	At IF_IN1, IF_IN2 Pins 34 and 35	P_{min}		20		dBµV
RSSI compression	At IF_IN1, IF_IN2 Pins 34 and 35	P_{max}		100		dBµV
RSSI dynamic range		DR		80		dB
RSSI resolution	Slope of the RSSI has to be steady	Acc		±2		dB
RSSI rise time	P_{in} = 30 to 100 dBµV, Pin 25	t_r		1		µs
RSSI fall time	P_{in} = 100 to 30 dBµV, Pin 25	t_f		1		µs
Quiescent output voltage	At P_{in} < 20 dBµV at IF_IN1, IF_IN2 Pin 25	I_{out}		0.45		µA
Maximum output voltage	At P_{in} = 100 dBµV at IF_IN1, IF_IN2 Pin 25	I_{out}		2.25		µA
FM Demodulator, BB-Filter Pins 19, 20, 23 and 24						
Co-channel rejection ratio	At P_{in} = -75 dBm at IR-mixer input	CCRR		10		dB
Sensitivity	Quality factor of external tank circuit approximately 20, $f_{res} = F_{IF}/2$, Pin 24	S		0.5		V/MHz
Amplitude of recovered signal	Nominal deviation of signal ± 288 kHz, Pin 24	A		450		mVss
Corner frequency	Pin 23: C = 68 pF	f_c		680		kHz
Output voltage DC range	Pin 24	V_{outDC}	1		Vs-1	V
DAC for FM Demodulator (Internally Connected)						
DEMOD_DAC range	(see bus protocol E6 ... E10)	$\Delta f_{IFcenter}$		± 5		%

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
VCO						
RX-VCO frequency range	VCOS = '0' Bit D13	f_{vco}	1769		1824	MHz
TX-VCO frequency range	VCOS = '1' Bit D13	f_{vco}	1881		1934	MHz
Tuning gain		G_{tune}		40		MHz/V
Frequency control voltage range	Pin 17	V_{tune}	0.4		2.8	V
VCO_DAC range	(see bus protocol D3 ... D5)	$\Delta f_{vco,DAC}$		±5		%
PLL						
Scaling factor prescaler		S_{PSC}		32/33		
Scaling factor main counter		S_{MC}		32/33/34/35		
Scaling factor swallow counter		S_{SC}	0		31	
External reference input frequency	AC coupled sinewave Pin 4	f_{REF_CLK}		10.368 13.824 20.736		MHz MHz MHz
External reference input voltage	AC coupled sinewave Pin 4	V_{REF_CLK}	50		250	mV_{RMS}
Scaling factor reference counter		S_{RC}		3/4/6/8		
Charge Pump Pin 13						
Output current	$V_{CP} = V_{VS_CP}$ / 2, I_CPSW = '1' Pin 48	I_{CP_nom}		±6.5		mA
Output current	$V_{CP} = V_{VS_CP}$ / 2, I_CPSW = '0' Pin 48	I_{CP_nom}		±1.2		mA
Current scaling	$I_{CP} = I_{CP_nom} + CPCS * I_{CP_step}$ (see bus protocol D0 ... D2)	I_{CP_step}		0.2		mA
Leakage current		I_L		±100		pA
Gaussian Transmit Filter (Gaussian Shape B∗T = 0.5)						
Tx data filter clock	12 taps in filter	f_{TXFCLK}		13.824		MHz
Frequency deviation		GF_{FM_nom}		±350		kHz
Frequency deviation scaling	$GF_{FM} = GF_{FM_nom} * GFCS$ (see bus protocol D6 ... D8)	GFCS	60		130	%
Modulation Compensation Circuit						
Oversampling		OVS		6		
Digital sum variation		DSV			85	
Current scaling factor	(see bus protocol E3 ... E5)	MCCS	60		130	%
VCO Switch and TX Driver Pin 32						
Power gain	At P_{in} = -40 dBm	Gp		30		dB
Output impedance	Pin 32	Z_{out}		100		Ω
Maximum output power	Pin 32	P_{max}	0	3		dBm
Gain compression	At TX_RF_OUT, Pin 32	P_{1dB}		1		dBm
Output interception point	Pin 32	OIP3		10		dBm
Ramp Generator Pins 36 and 37						
Minimum output voltage	According to RAMP_SET input	V_{min}		0.7		V

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

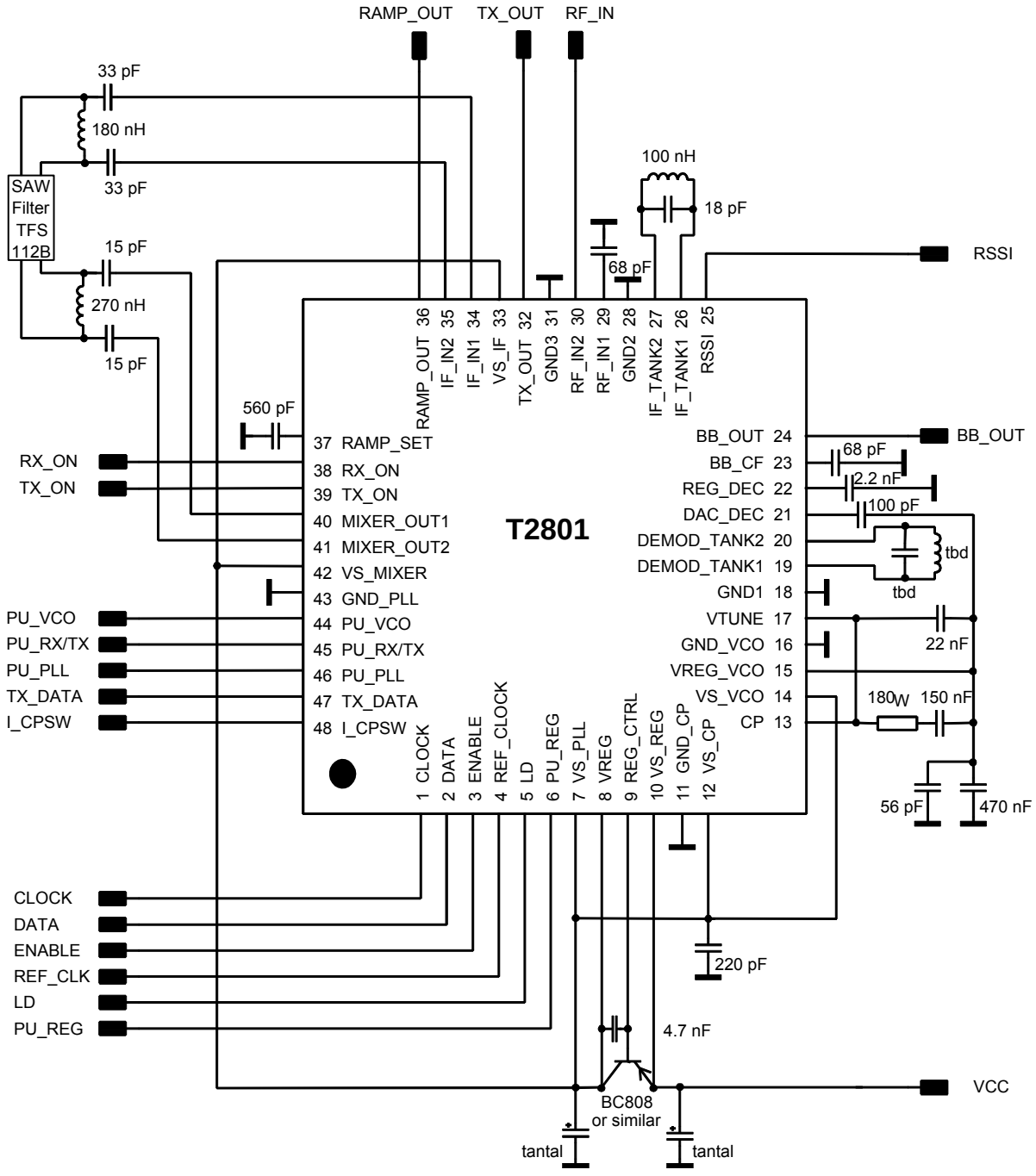
Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
Maximum output voltage	According to RAMP_SET input	V_{max}		2.2		V
Rise time	C_{ramp} = 270 pF at Pin 37	t_r		5		µs
Fall time	C_{ramp} = 270 pF at Pin 37	t_f		5		µs
Lock Detect and Test Mode Output Pin 5						
Lock detect output, test mode output	Locked = '1', unlocked = '0' Test modes (see bus protocol E0 ... E2)	LD				
Leakage current	V_{OH} = 4.6 V	I_L			5	µA
Saturation voltage	I_{OL} = 0.5 mA	V_{SL}			0.4	V
Auxiliary Regulator Pins 8, 9 and 10						
Output voltage	V_{SREG} = 3 V Pin 8	V_{REG}	2.9	3.0	3.1	V
Supply voltage rejection	$V_{Pin10} = V_{DC} + 0.1\ V_{pp}$ f_{Pin10} = 0.1 to 10 kHz C_{Pin8} = 100 nF	SVR		TBD		dB
VCO Regulator Pins 14, 15 and 12						
Output voltage	V_{SVCO} = 3 V Pin 15	V_{REG_VCO}	2.6	2.7	2.8	V
3-wire Bus						
Clock		f_{Clock}			6.912	MHz
Logic Input Levels (CLOCK, DATA, ENABLE, RX_ON, TX_ON, PU_VCO, TX_DATA, I_CPSW), Pins 1, 2, 3, 38, 39, 44, 47 and 48						
High input level	= '1'	V_{iH}	1.5			V
Low input level	= '0'	V_{iL}			0.5	V
High input current	= '1'	I_{iH}	-5		5	µA
Low input current	= '0'	I_{iL}	-5		5	µA
Standby Control Pins 6, 45 and 46						
Power up PU_REG = '1' PU_RX/TX = '1' PU_PLL = '1' High input level	Pin 6 Pin 45 Pin 46	VPU_REG VPU_RX/TX VPU_PLL	2.0			V
Standby PU_REG = '0' PU_RX/TX = '0' PU_PLL = '0' Low input level	Pin 6 Pin 45 Pin 46	VPU_REG,OFF VPU_RX/TX,OF F VPU_PLL,OFF			0.7	V
Power up PU_REG = '1' PU_RX/TX = '1' PU_PLL = '1' High input current	VPU = 3 V, Pin 6 VPU = 5.5 V, Pin 45 VPU = 3 V, Pin 46 VPU = 5.5 V	IPU_REG IPU_RX/TX IPU_PLL	20 60 100 200	30 80 125 300	40 100 150 400	µA µA µA µA
Standby PU_xxxx = '0' Low input current	VPU = 0 V, Pin 6, VPU = 0.5 V, Pins 45, 46	IPU,OFF			0.1 1	µA µA

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
Settling time V_S = 0 → active operation	Switched from V_S = 0 to V_S = 3V	t_{soa}		< 10		µs
Settling time Standby → active operation	Switched from PU = '0' to PU = '1'	t_{ssa}		< 10		µs
Settling time Aactive operation → standby	Switched from PU = '1' to standby	t_{sas}		< 2		µs
Power Supply Pins 7, 10, 12, 14, 33 and 42						
Total supply current	RX	I_S		85		mA
Total supply current	RSSI only	I_S		82		mA
Total supply current	TX	I_S		54		mA
Total supply current	TX (MCC, GF active)	I_S		58		mA
Standby current	PU_RX/TX = GND	I_S			10	µA
Supply current CP	V_{VS_CP} = 3 V, PLL in lock condition, Pin 13	I_{CP}		1		µA

Figure 6. T2801 Aplication Circuit



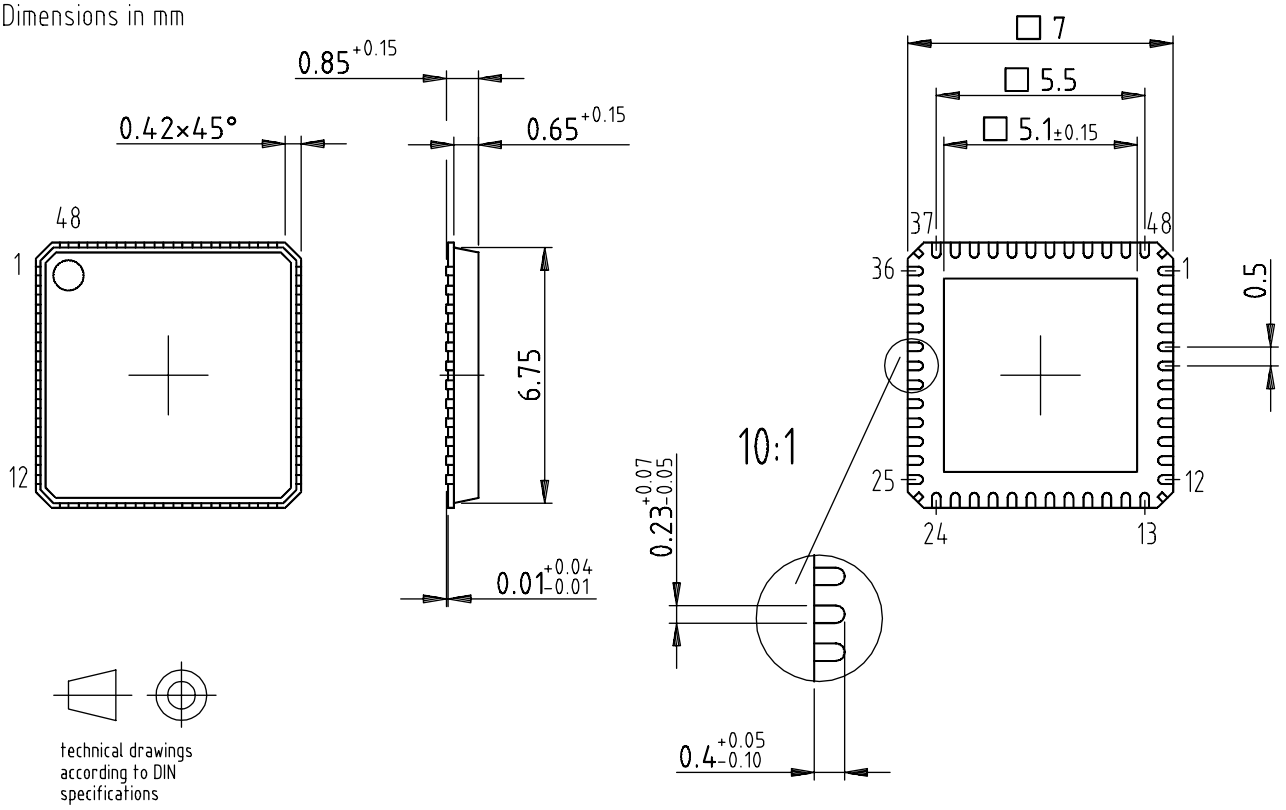
Ordering Information

Extended Type Number	Package	Remarks
T2801-PLH	HP-VFQFP-N48	Taped and reeled

Package Information

Package: HP-VFQFP-N48
Exposed pad Var. C
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Drawing-No.: 6.543-5068.01-4
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