

LDP4098T1G

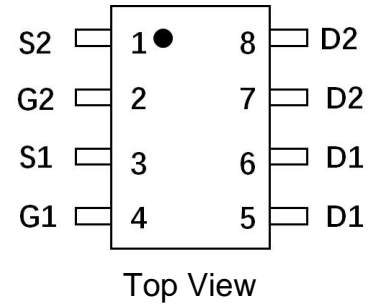
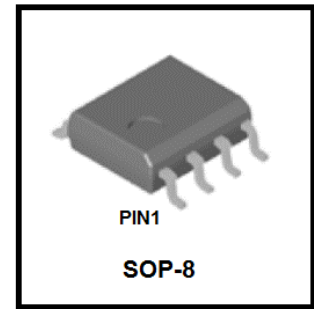
Dual P-Channel MOSFET

1. FEATURES

- Low RDS(on) trench technology.
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

2. ORDERING INFORMATION

Device	Marking	Shipping
LDP4098T1G	4098	4000/Tape&Reel



3. MAXIMUM RATINGS(Ta = 25°C unless otherwise stated)

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDSS	-30	V
Gate-to-Source Voltage		VGS	±20	V
Continuous Drain Current	TA =25°C	ID	-5.3	A
	TA =70°C		-4.2	
Pulsed Drain Current (Note 3)		IDM	-25	
Power Dissipation(Note 2)	TA =25°C	PD	2.5	W
	TA =70°C		1.9	
Operating Junction Temperature and Storage Temperature Range		TJ , TSTG	-55 ~+150	°C

- 1.Surface Mounted on 1" x 1" FR4 Board.
2. Repetitive rating, pulse width limited by junction temperature.
- 3.The RθJA is the sum of the thermal impedance from junction to lead RθJL and lead to ambient.

4. THERMAL CHARACTERISTICS

Parameter	Symbol	Typ	Limits	Unit
Maximum Junction-to-Ambient(Note 1)	RθJA		50	°C/W

5. ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit	
Static						
Drain-Source Breakdown Voltage ($I_D = -250\mu A$, $V_{GS} = 0V$)	BVDSS	-30	-	-	V	
Zero Gate Voltage Drain Current ($V_{DS} = -24V$, $V_{GS} = 0V$) ($V_{DS} = -24V$, $V_{GS} = 0V$, $T_J = 55^\circ C$)	IDSS	-	-	-1 -5	μA	
Gate-Body Leakage ($V_{DS} = 0V$, $V_{GS} = \pm 20V$)	IGSS	-	-	± 100	nA	
Gate-Source Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\mu A$)	VGS(th)	-1	-1.4	-2.5	V	
On-State Drain Current ($V_{GS} = -10V$, $V_{DS} = -5V$)	ID(on)	-25	-	-	A	
Drain-Source On-Resistance ($V_{GS} = -10V$, $I_D = -4.1A$) ($V_{GS} = -4.5V$, $I_D = -3A$)	RDS(on)	-	38 45	50 70	m Ω	
Forward Transconductance ($V_{DS} = -5V$, $I_D = -4A$)	gfs	-	10	-	S	
Diode Forward Voltage ($I_S = -1A$, $V_{GS} = 0V$)	VSD	-	-0.77	-1	V	
Maximum Body-Diode Continuous Current	IS			-2	A	
Dynamic						
Input Capacitance	(VGS = 0V, VDS = -15V, f = 1MHz)	Ciss	515	660	725	pF
Output Capacitance		Coss	70	100	130	
Reverse Transfer Capacitance		Crss	60	80	110	
Gate resistance (VGS = 0V, VDS = 0V, f = 1MHz)	Rg	3.5	7.5	11.5	Ω	
Total Gate Charge(10V)	(VGS = -10V, VDS = -15V, ID = -4A)	Qg		18.7		nC
Total Gate Charge(4.5V)		Qg		9.4		
Gate-Source Charge		Qgs		2.7		
Gate-Drain Charge		Qgd		3.3		
Turn-On Delay Time	(VGS = -10V, VDS = -15V, RL = 3.6 Ω , RGEN = 3 Ω)	td(on)	-	39	-	ns
Rise Time		tr	-	21	-	
Turn-Off Delay Time		td(off)	-	48	-	
Fall Time		tf	-	7	-	
Body Diode Reverse Recovery Time (IF = -4A, dI/dt = 100A/ μs)	trr		39		ns	
Body Diode Reverse Recovery Charge (IF = -4A, dI/dt = 100A/ μs)	Qrr		11.3		nC	

6. ELECTRICAL CHARACTERISTICS CURVES

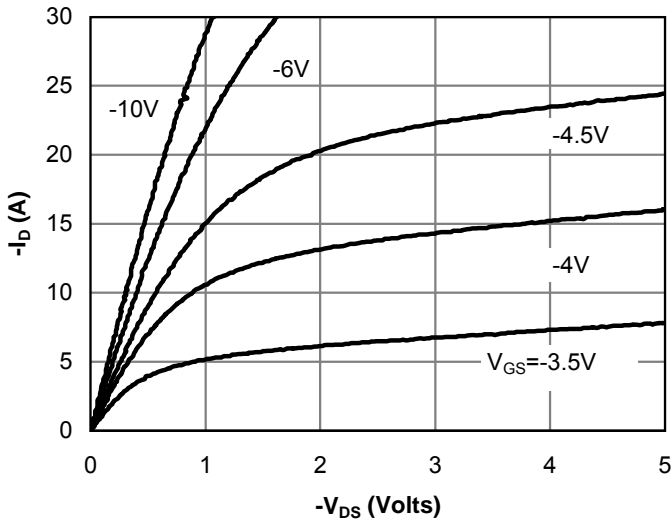


Fig 1: On-Region Characteristics (Note E)

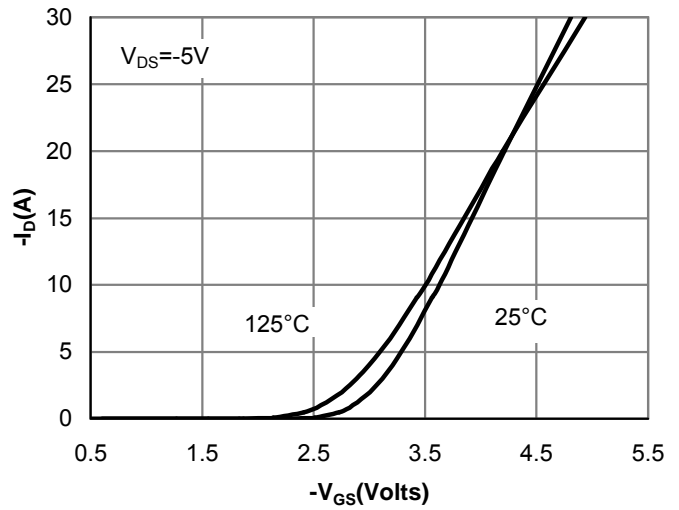


Figure 2: Transfer Characteristics (Note E)

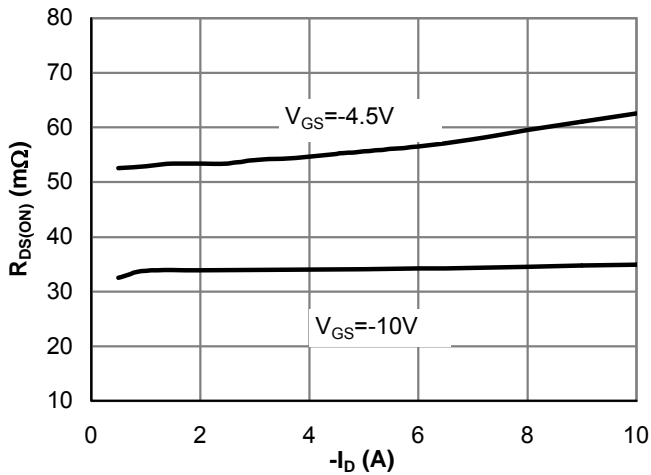


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

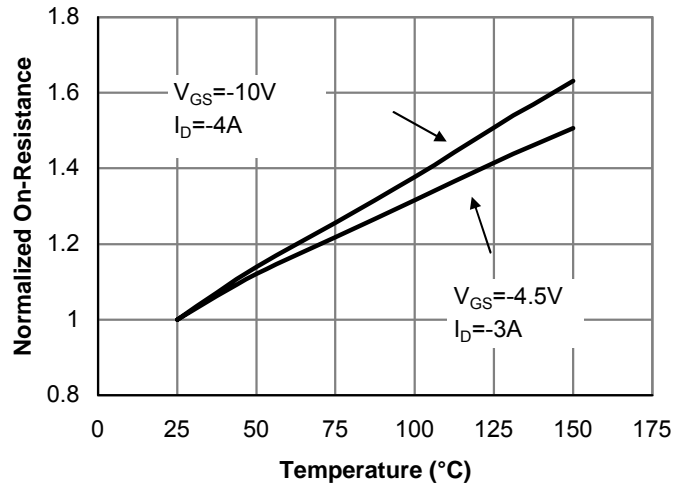


Figure 4: On-Resistance vs. Junction Temperature (Note E)

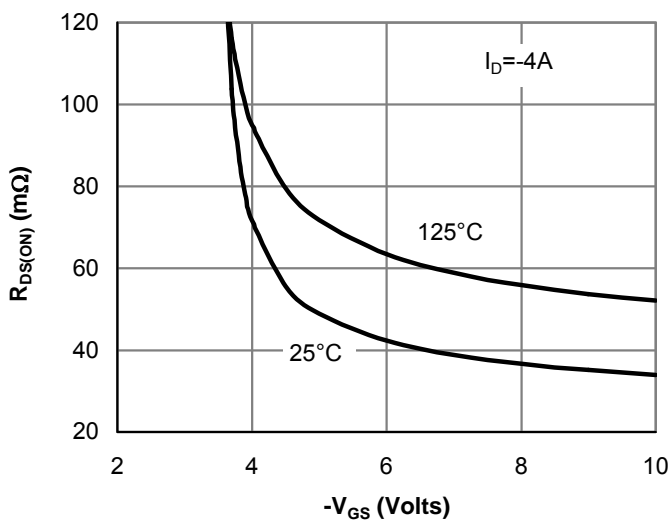


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

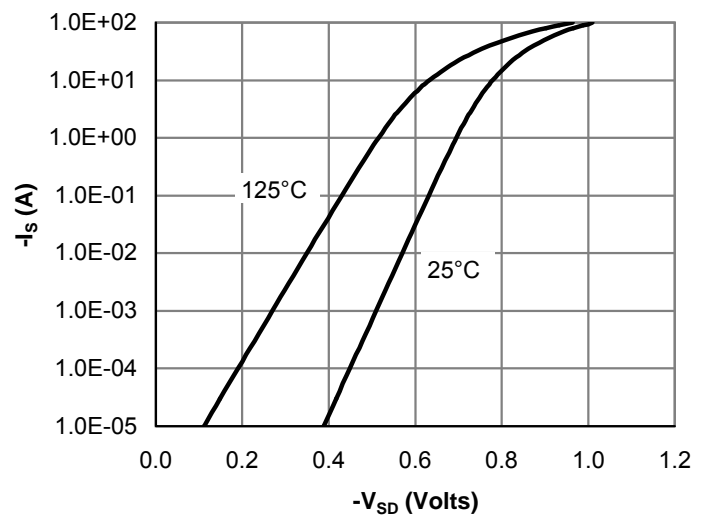


Figure 6: Body-Diode Characteristics (Note E)

6.ELECTRICAL CHARACTERISTICS CURVES(Con.)

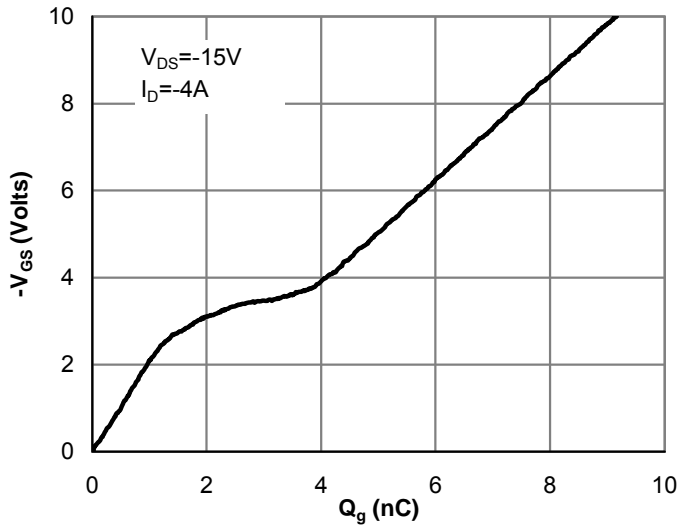


Figure 7: Gate-Charge Characteristics

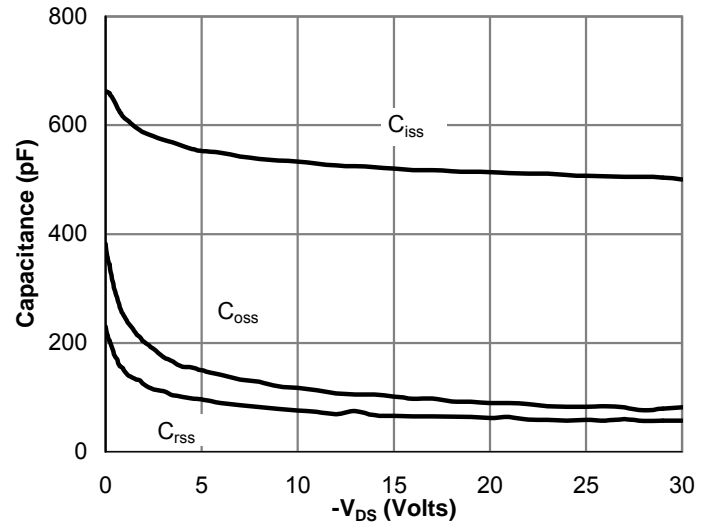


Figure 8: Capacitance Characteristics

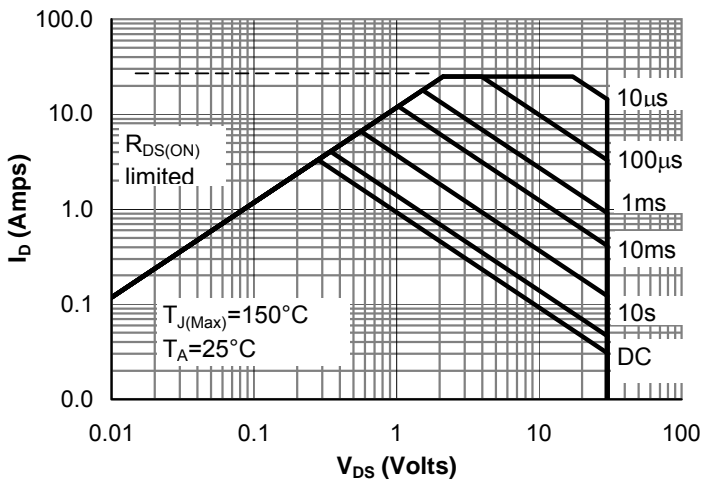


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

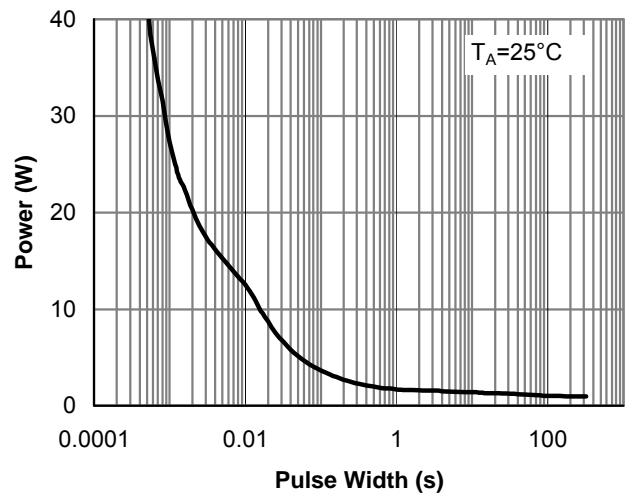


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

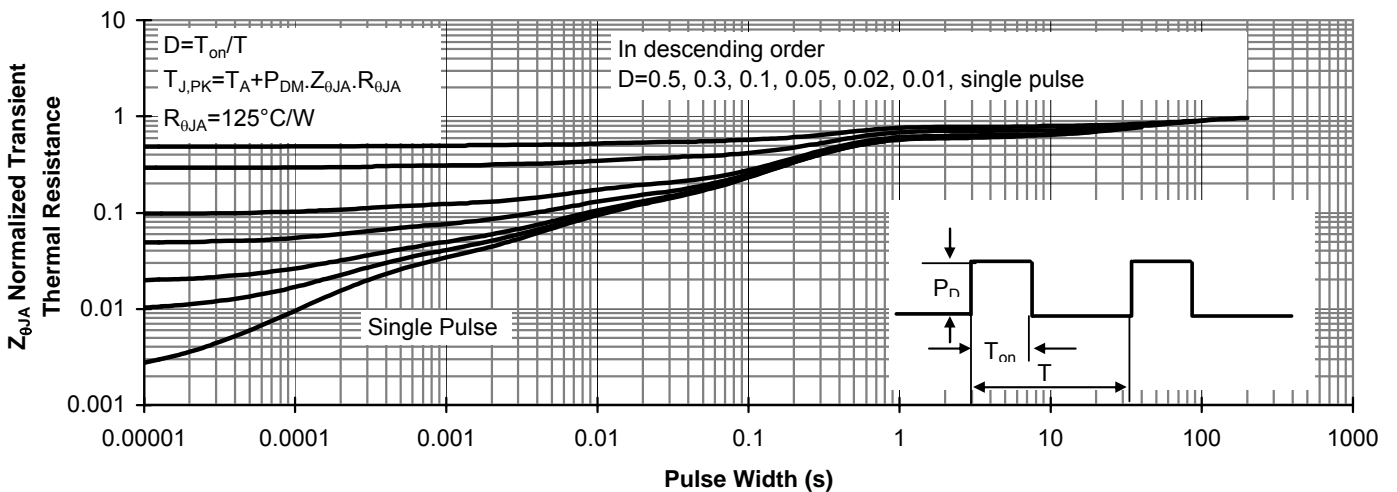
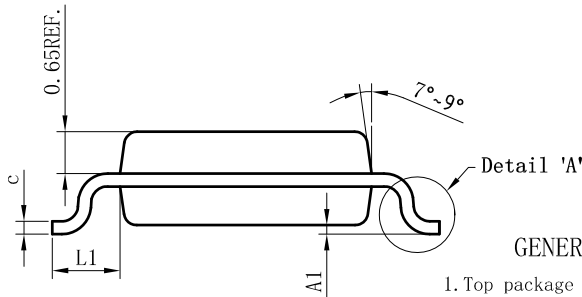
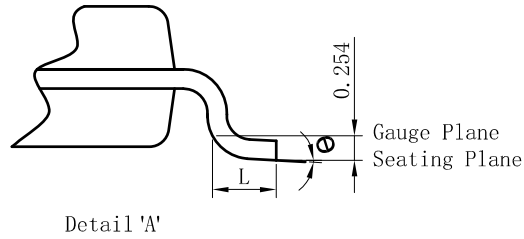
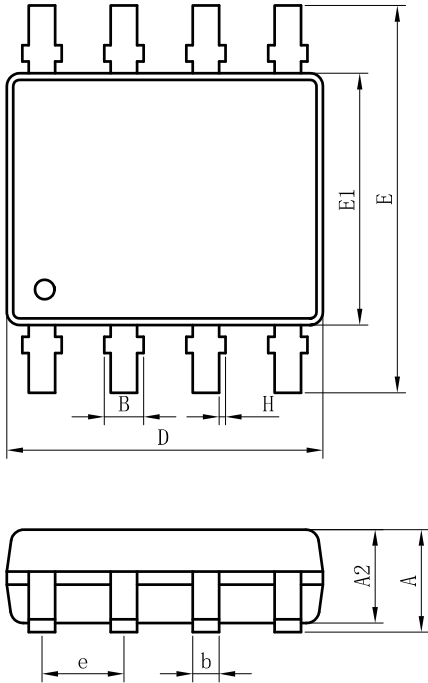


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

OUTLINE AND DIMENSIONS

SOP8

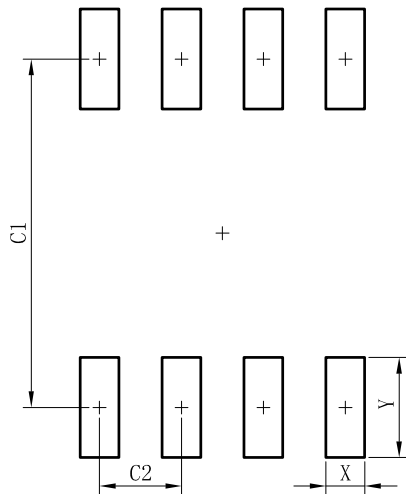


SOP8			
DIM	MIN	NOR	MAX
A	-	-	1.75
A1	0.10	0.15	0.20
A2	1.35	1.45	1.55
b	0.33	0.42	0.51
c	0.15	0.22	0.29
D	4.77	4.90	5.03
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.46	0.66	0.86
L1	0.85	1.05	1.25
θ	0°	5°	8°
B	-	-	0.55
H	0	0.05	0.10
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
5. Dimension "b" Does Not Include Dambar Protrusion.

SOLDERING FOOTPRINT



SOP8	
DIM	(mm)
X	0.60
Y	1.55
C1	5.40
C2	1.27