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L8575 Dual-Resistive, Low-Cost Subscriber Line Interface Circuit (SLIC)

Features

- Two channels in a single package
- Serial data interface
- Per-channel powerdown
- Low standby power (≤65 mW per channel)
- Integrated protection
- No external protection device required
- Battery noise cancellation
- Switchhook detector
- Ring-trip detector
- Switchhook and ring-trip detector self-test
- Fault detector
- Zero ring voltage cross detection
- Three relay drivers per channel
- 44-pin, surface-mount, plastic package (PLCC)

Description

The L8575 is a dual-resistive, low-cost subscriber line interface circuit (SLIC) that is optimized to meet both ITU-T recommendations and LSSGR requirements for 600 Ω/900 Ω resistive and complex impedance termination applications. It interfaces the low-voltage circuits on an analog line card to the Tip and Ring of two subscriber loops. The L8575 does not supply dc current to the subscriber loops—external resistors are used for this purpose. The device is built using a 90 V complementary bipolar (CBIC) process and is available in a 44-pin PLCC package.

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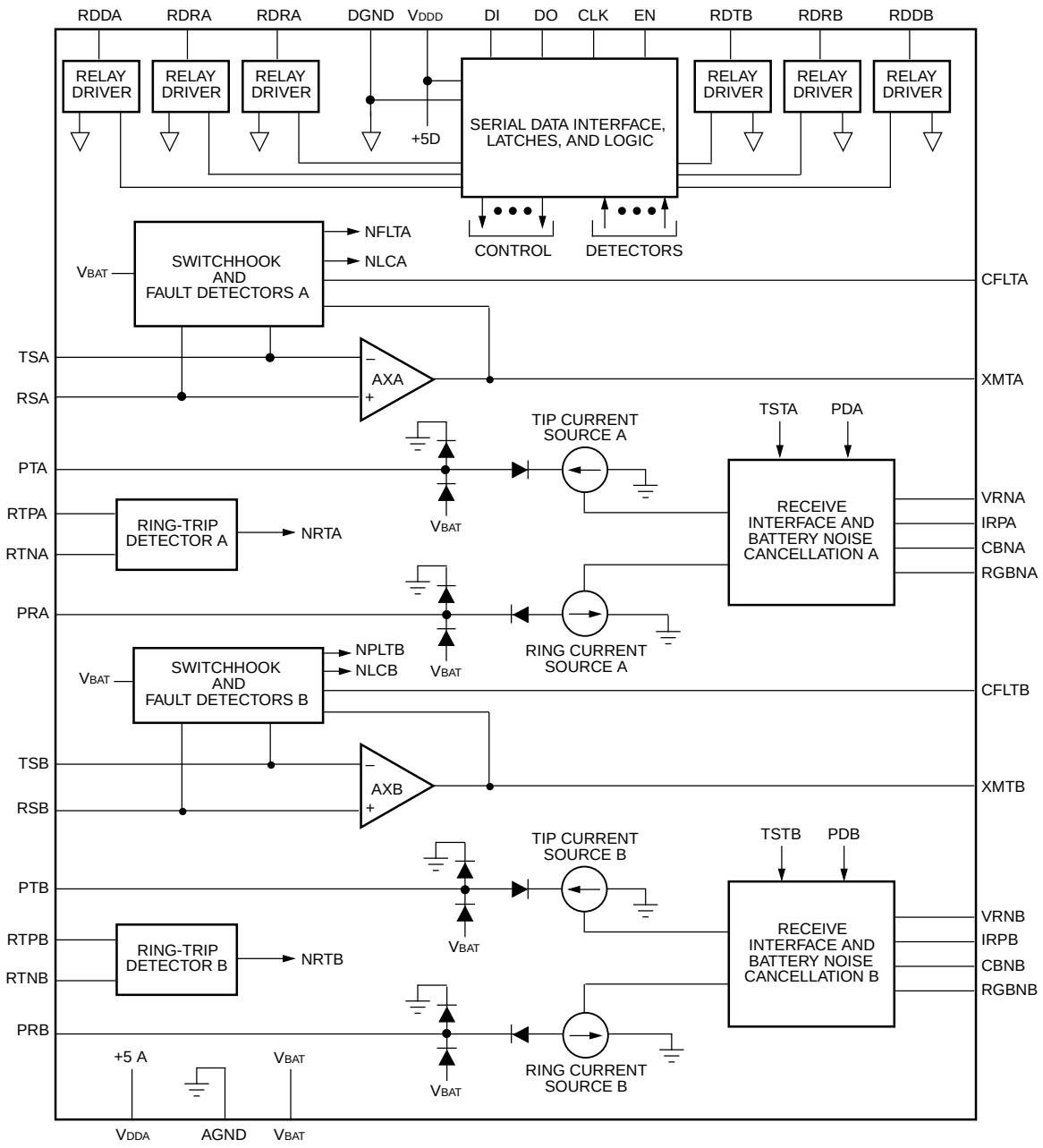
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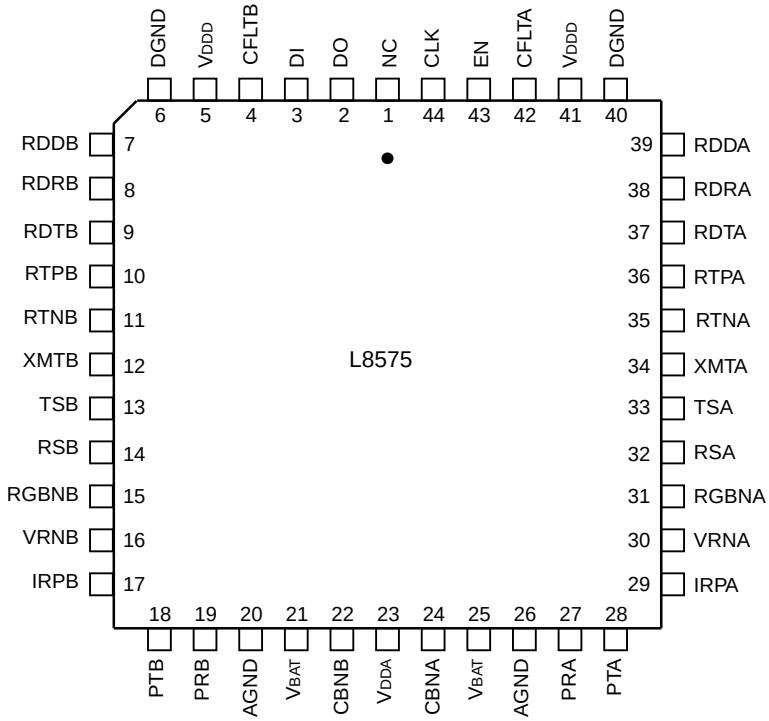
Description (continued)



12-3304(F).ar1

Figure 1. Functional Diagram

Preliminary Pin Information



12-3364(F)

Figure 2. 44-Pin PLCC Pinout

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	NC	—	**No Connect.** Unused pin (no internal connection).
2	DO	O	**Serial Data Output.** Data in the internal 8-bit serial shift register is shifted out on this logic output with the clock signal on pin CLK.
3	DI	I	**Serial Data Input.** Data on this logic input is shifted into the 8-bit serial shift register with the clock signal on pin CLK.
4	CFLTB	I/O	**Fault Filter (Channel B).** Connect a 0.1 µF capacitor from CFLTB to AGND. This capacitor filters Tip/Ring transients from the channel B fault detector.
5	V_{DDD}	—	**5 V Digital dc Supply.** 5 V supply for logic and relay driver flyback diodes.
6	DGND	—	**Digital Ground.** Ground for channel B relay drivers.
7	RDDB	O	**Disconnect Relay Driver (Channel B).** This output drives the external relay.
8	RDRB	O	**Ringing Relay Driver (Channel B).** This output drives an external ringing relay.
9	RDTB	O	**Test Relay Driver (Channel B).** This output drives an external test relay.
10	RTPB	I	**Ring-Trip Positive (Channel B).** Positive sense input for the ring-trip detector.

Preliminary Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
11	RTNB	I	**Ring-Trip Negative (Channel B).** Negative sense input for the ring-trip detector.
12	XMTB	O	**Transmit Signal Output (Channel B).** Channel B transmit amplifier output.
13	TSB	I	**Tip Sense (Channel B).** Negative input of channel B transmit op amp. Connect one high-value resistor between TSB and the Tip of loop B and another high-value resistor between TSB and XMTB.
14	RSB	I	**Ring Sense (Channel B).** Positive input of channel B transmit op amp. Connect one high-value resistor between RSB and the Ring of loop B and another high-value resistor between RSB and AGND.
15	RGBNB	I	**Battery Noise Gain Resistor (Channel B).** The current flowing out of PRB is 50 times the current flowing into RGBNB. Connect a resistor from RGBNB to AGND to set the gain of the channel B battery noise cancellation circuit.
16	VRNB	I	**Receive Voltage Negative Input (Channel B).** The differential current flowing from PTB to PRB is –200 times the voltage applied to VRNB, divided by the impedance connected between IRPB and AGND.
17	IRPB	I	**Receive Current Positive Input (Channel B).** The differential current flowing from PTB to PRB is 200 times the current flowing into IRPB.
18	PTB	O	**Protected Tip (Channel B).** Output of the Tip current drive amplifier B. Connect PTB to the Tip of loop B through an overvoltage protection resistor (1.4 kΩ minimum).
19	PRB	O	**Protected Ring (Channel B).** Output of the Ring current drive amplifier B. Connect PRB to the Ring of loop B through an overvoltage protection resistor (1.4 kΩ minimum).
20	AGND	—	**Analog Signal Ground.** Signal ground for channel B.
21	V_{BAT}	—	**Office Battery Supply.** Negative office battery supply for channel B.
22	CBNB	I	**Battery Noise Capacitor (Channel B).** The current flowing out of PRB is –50 times the voltage applied to CBNB, divided by the impedance connected between RGBNB and AGND. Couple V_{BAT} to CBNB through a high-pass filter to eliminate battery noise from the Tip/Ring of channel B.
23	V_{DDA}	—	**5 V Analog dc Supply.**
24	CBNA	I	**Battery Noise Capacitor (Channel A).** The current flowing out of PRA is –50 times the voltage applied to CBNA, divided by the impedance connected between RGBNA and AGND. Couple V_{BAT} to CBNA through a high-pass filter to eliminate battery noise from the Tip/Ring of channel A.
25	V_{BAT}	—	**Office Battery Supply.** Negative office battery supply for channel A.
26	AGND	—	**Analog Signal Ground.** Signal ground for channel A.
27	PRA	O	**Protected Ring (Channel A).** Output of the Ring current drive amplifier A. Connect PRA to the Ring of loop A through an overvoltage protection resistor (1.4 kΩ minimum).
28	PTA	O	**Protected Tip (Channel A).** Output of the Tip current drive amplifier A. Connect PTA to the Tip of loop A through an overvoltage protection resistor (1.4 kΩ minimum).
29	IRPA	I	**Receive Current Positive Input (Channel A).** The differential current flowing from PTA to PRA is 200 times the current flowing into IRPA.
30	VRNA	I	**Receive Voltage Negative Input (Channel A).** The differential current flowing from PTA to PRA is –200 times the voltage applied to VRNA, divided by the impedance connected between IRPA and AGND.

Preliminary Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
31	RGBNA	I	**Battery Noise Gain Resistor (Channel A).** The current flowing out of PRA is 50 times the current flowing into RGBNA. Connect a resistor from RGBNA to AGND to set the gain of the channel A battery noise cancellation circuit.
32	RSA	I	**Ring Sense (Channel A).** Positive input of channel A transmit op amp. Connect one high-value resistor between RSA and the Ring of loop A and another high-value resistor between RSA and AGND.
33	TSA	I	**Tip Sense (Channel A).** Negative input of channel A transmit op amp. Connect one high-value resistor between TSA and the Tip of loop A and another high-value resistor between TSA and XMTA.
34	XMTA	O	**Transmit Signal Output (Channel A).** Channel A transmit amplifier output.
35	RTNA	I	**Ring-Trip Negative (Channel A).** Negative sense input for the ring-trip detector.
36	RTPA	I	**Ring-Trip Positive (Channel A).** Positive sense input for the ring-trip detector.
37	RDTA	O	**Test Relay Driver (Channel A).** This output drives an external test relay.
38	RDRA	O	**Ringing Relay Driver (Channel A).** This output drives the external ringing relay.
39	RDDA	O	**Disconnect Relay Driver (Channel A).** This output drives an external relay.
40	DGND	—	**Digital Ground.** Ground for channel A relay drivers.
41	V_{DDD}	—	**5 V Digital dc Supply.** 5 V supply for logic and relay driver flyback diodes.
42	CFLTA	I/O	**Fault Filter (Channel A).** Connect a 0.1 µF capacitor from CFLTA to AGND. This capacitor filters Tip/Ring transients from the channel A fault detector.
43	EN	I	**Enable.** A high-to-low transition on this logic input latches the data in the 8-bit serial shift register into the output latches. The logic level of EN also controls which data is shifted into the 8-bit serial shift register (refer to CLK pin description).
44	CLK	I	**Clock.** When the enable input (EN) is high, a low-to-high transition on this logic input shifts data at the data input pin (DI) into the 8-bit serial shift register. When the enable input (EN) is low, a low-to-high transition latches the states of the internal detectors into the 8-bit serial shift register.

Absolute Maximum Ratings (@ T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Value	Max	Unit
5 V Analog dc Supply	V_{DDA}	–0.5	—	+7.0	V
5 V Digital dc Supply	V_{DDD}	–0.5	—	+7.0	V
Office Battery Supply	V_{BAT}	–65	—	+0.5	V
Logic Input Voltage	—	–0.5	—	V_{DDD} + 0.5	V
Logic Input Clamp Diode Current, per Pin	—	—	±20	—	mA
Logic Output Voltage	—	–0.5	—	V_{DDD} + 0.5	V
Logic Output Current, per Pin (excluding relay drivers)	—	—	±35	—	mA
Maximum Junction Temperature	—	—	150	—	°C
Operating Temperature Range	—	–40	—	+125	°C
Storage Temperature Range	T_{stg}	–40	—	+125	°C
Relative Humidity Range	—	5	—	95	%
Ground Potential Difference (DGND to AGND)	—	+0.5	—	–0.5	V

Notes:
Analog and battery voltages are referenced to AGND; digital (logic) voltages are referenced to DGND.

The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powering are (1) an inductor connected to Tip and Ring that can force an overvoltage on V_{BAT} through external components if the V_{BAT} connection chatters, and (2) inductance in the V_{BAT} lead that could resonate with the V_{BAT} filter capacitor to cause a destructive overvoltage.

Electrical Characteristics

Generally, minimum and maximum values are testing requirements. However, some parameters may not be tested in production because they are guaranteed by design and device characterization. Typical values reflect the design center or nominal value of the parameter; they are for information only and are not a requirement. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C) and entire battery range (–42 V to –58 V). Unless otherwise specified, typical values are defined as 25 °C, V_{DDA} = 5 V, V_{DDD} = 5 V, V_{BAT} = –48 V. Positive currents flow into the device.

Table 2. Operating Conditions and Powering

Parameter	Min	Typ	Max	Unit
Temperature Range	–40	—	85	°C
Humidity Range	5	—	95[1]	%RH
Supply Voltage: V_{DDA} V_{DDD} V_{BAT} $V_{DDA} – V_{DDD}$	 4.75 4.75 –42 —	 — — –48 —	 5.5 5.5 –58 ±0.5	 V V V V
Supply Currents (both channels active): $I_{VDDA} + I_{VDDD}$ (5 V) I_{VBAT} (–48 V)[2]	 — —	 — —	 19.0 –27.5	 mA mA
Supply Currents (both channels powerdown): $I_{VDDA} + I_{VDDD}$ (5 V) I_{VBAT} (–48 V)[2]	 — —	 — —	 18.0 –2.0	 mA mA
Total Power Dissipation (5 V; –48 V)[3]: Active (both channels) Powerdown (both channels)	 — —	 — —	 1.40 185	 W mW
Power-supply Rejection[4, 5] (50 mVrms ripple): Tip/Ring and XMT	Refer to Figure 3.			
Thermal[5]: Thermal Resistance (still air) Operating Tjc	 — —	 — —	 47 155	 °C/W °C

1. Not to exceed 26 grams of water per kilogram of dry air.
2. Includes V_{BAT} current through the external dc feed resistors, assuming the loop is open.
3. Includes power dissipation in the external dc feed resistors per application diagram, assuming the loop is open.
4. V_{BAT} power supply rejection depends on the battery noise cancellation circuit. The performance stated here applies only during the active state and assumes proper battery noise cancellation, i.e., a high-pass filter from V_{BAT} to CBN and a resistor from RGBN to AGND which is 50 times the dc feed resistor connecting V_{BAT} to Ring (refer to the application diagram).
5. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 3. Battery Feed, Switchhook Detectors (LCA and LCB), and Fault Detectors (FLTA and FLTB)

Parameter	Min	Typ	Max	Unit
Loop Resistance Range[1]: (3.17 dBm overload into 600 Ω) I_{LOOP} = 18 mA at V_{BAT} = –48 V	 1800	 —	 —	 Ω
Longitudinal Current Capability per Wire	8.5	—	—	mArms
Switchhook Detector Loop Resistance[2]: Off-hook (LC = 1) On-hook (LC = 0)	— — 4800	4000 — —	— 3200 —	Ω Ω Ω
Fault Detector[2, 3]: $\lvert V_{TIP}\rvert$ or $\lvert V_{RING} – V_{BAT}\rvert$ No Fault (FLT = 0) Fault (FLT = 1) Detection Delay t_{DET} (no fault to fault; CFLT = 0.1 µF) Release Delay (fault to no fault; CFLT = 0.1 µF)	 — 39 10 1.6 t_{DET}	 36 36 — —	 33 — 30 2.5 t_{DET}	 V V ms ms

1. Assumes 2 x 300 Ω external dc feed resistors.
2. Detector values are independent of office battery and are valid over the entire range of V_{BAT}.
3. Fault voltage is defined as the absolute value of the dc voltage across either dc feed resistor. If the voltage across either feed resistor exceeds this value, a fault is determined to be present. FLT is forced to a 0 when D2 = 1 (ringing state).

Table 4. Ring-Trip Detectors (RTA, RTB, RZA, and RZB)

Parameter	Min	Typ	Max	Unit
Ringing Source[1]: Frequency (f) dc Voltage ac Voltage	 19 –39.5 60	 20 — —	 28 –57 105	 Hz V Vrms
Ring Trip[2, 3] (RT = 1): Loop Resistance Trip Time (f = 20 Hz) RT Valid	 2000 — —	 — — —	 — 200 80	 Ω ms ms
Ringing Source Zero Crossing (referenced to V_{BAT}/2): Ringing Voltage Positive (RZ = 1) Ringing Voltage Negative (RZ = 0)	 3V_{BAT}/4 —	 — —	 — V_{BAT}/4	 V V

1. The ringing source consists of the ac and dc voltages added together (battery-backed ringing); the ringing return is ground.
2. RT must also indicate ring-trip when the ac ringing voltage is absent (<5 Vrms) from the ringing source.
3. Pretrip: Ringing must not be tripped by a 10 kΩ resistor in parallel with an 8 µF capacitor applied across Tip and Ring.

Electrical Characteristics (continued)

Relay Drivers

The relay drivers operate using the V_{DDD} supply. When V_{DDD} is first applied to the device, the relay drivers must power up and remain in the off-state until the SLIC is configured via the serial data interface. The table below summarizes their parameter requirements.

Table 5. Relay Drivers (RDRA, RDTA, RDRB, RDTB, RDDA, and RDDB)

Parameter[1]	Symbol	Min	Max	Unit
Off-state Output Current (V_{OUT} = V_{DDD})	I_{OFF}	—	±10	µA
On-state Output Voltage (I_{OUT} = 40 mA)	V_{ON}	0	0.60	V
On-state Output Voltage (I_{OUT} = 20 mA)	V_{ON}	0	0.40	V
Clamp Diode Reverse Current (V_{OUT} = 0)	I_R	—	±10	µA
Clamp Diode On Voltage (I_{OUT} = 80 mA)	V_{OC}	V_{DDD} + 0.5	V_{DDD} + 3.0	V
Turn-on Time[2]	t_{ON}	—	10	µs
Turn-off Time[2]	t_{OFF}	—	10	µs

1. Unless otherwise specified, all logic voltages are referenced to DGND.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.

Table 6. Analog Signal Pins

Parameter	Min	Typ	Max	Unit
PTA, PTB, PRA, and PRB:				
Surge Current (from external source):				
Continuous	—	—	±50	mAdc
1 ms Exponential Pulse (50 repetitions)	—	—	±750	mA
1 second, 60 Hz (60 repetitions)	—	—	±175	mArms
10 µs Rectangular Pulse (10 repetitions)	—	—	±1.25	A
Output Drive (PTA and PTB):				
Drive Current (sink only)	0.1	—	15	mA
Voltage Swing (I_{OUT} = 15 mA)	V_{BAT} + 4	—	AGND	V
dc Bias Current (active state only)	5.3	5.6	5.9	mA
Output Drive (PRA and PRB):				
Drive Current (source only)	–15	—	–0.1	mA
Voltage Swing (I_{OUT} = 15 mA)	V_{BAT}	—	AGND – 4	V
dc Bias Current (active state only)	–5.3	–5.6	–5.9	mA
Output Impedance (60 Hz—3.4 kHz)[1]	1	—	—	MΩ
Output Load Resistance (dc or ac)[1]	0	—	100	kΩ

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Relay Drivers (continued)

Table 6. Analog Signal Pins (continued)

Parameter	Min	Typ	Max	Unit
XMTA and XMTB:				
Output Drive Current	±3	—	—	mA
Output Voltage Swing (3 mA load):				
Maximum	V_{BAT}	—	V_{DDA}	V
Minimum	V_{BAT} + 10	—	+2.5	V
Output Short-circuit Current[2]	—	—	±30	mA
Output Impedance (60 Hz—3.4 kHz)	—	—	10	Ω
Output Load dc Resistance	20	—	—	kΩ
Output Load ac Impedance[1]	2	—	—	kΩ
Output Load Capacitance[1]	—	—	50	pF
VRNA and VRNB:				
Input Voltage Range	–1.75	—	3.5	V
Input Bias Current	—	—	±1	µA
Input Impedance[1]	20	—	—	MΩ
IRPA and IRPB:				
Input Offset Voltage (to respective VRN)	—	—	±10	mV
Input Impedance	—	—	5	Ω
CBNA and CBNB:				
Input Voltage Range	–1.75	—	3.5	V
Input Bias Current	—	—	±250	nA
Input Impedance	50	—	—	MΩ
RGBNA and RGBNB:				
Input Offset Voltage (to respective CBN)	—	—	±10	mV
Input Impedance	—	—	5	Ω
TSA, TSB, RSA, and RSB:				
Surge Current (from external source)	—	—	±25	mAdc
Input Voltage Range	V_{BAT} + 3	—	AGND	V
Input Bias Current	—	—	±1	µA
Differential Input Impedance[1]	50	—	—	kΩ
Common-mode Input Impedance[1]	50	—	—	MΩ
External Capacitance (67 kΩ source impedance)[1]	—	—	10	pF

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. A V_{BAT} or ground short on XMTA or XMTB will not cause a device failure.

Electrical Characteristics (continued)

Transmission

Transmit direction is Tip/Ring to XMT. Receive direction is IRP/VRN to Tip/Ring.

Table 7. Transmission Characteristics

Parameter	Min	Typ	Max	Unit
Longitudinal Balance (*IEEE*[1] Std. 455—1976)[2]:				
50 Hz—1 kHz	54	70	—	dB
1 kHz—3 kHz	50	66	—	dB
Metallic to Longitudinal Balance[2]:				
200 Hz—4 kHz	30	—	—	dB
RFI Rejection[3]:				
(0.5 Vrms, 50 Ω source, 30% AM Mod. 1 kHz)				
500 kHz—10 MHz	—	—	–65	dBV
10 MHz—100 MHz	—	—	–45	dBV
Tip/Ring Signal Level	—	—	3.17	dBm
ac Termination Impedance[4]	—	600	—	Ω
Total Harmonic Distortion (200 Hz—4 kHz)[3]	—	—	0.3	%
Transmit Gain (f = 1 kHz)[5]:				
Tip/Ring to XMT	–0.486	–0.500	–0.514	—
Receive Gain (f = 1 kHz):				
IRP Current to Differential Current Flowing from PT to PR	195	200	205	—
VRV to IRP	0.995	1	1.005	—
CBN Gain (f = 1 kHz):				
1 RGBN Current to Current Flowing	–49.5	–50	–50.5	—
CBN to RGBN	0.995	1	1.005	—
Gain vs. Frequency (transmit & receive; 1 kHz reference)[3]:				
200 Hz—3.4 kHz	–0.1	0	0.1	dB
Gain vs. Level (transmit & receive; 0 dBV reference)[3]:				
–50 dB to +3 dB	–0.05	0	0.05	dB
Interchannel Crosstalk[3]:				
200 Hz—3.4 kHz	—	—	77	dB
Idle-channel Noise (Tip/Ring; 600 Ω termination):				
Psophometric[3]	—	—	–77	dBmp
C-message	—	—	12	dBrnC
3 kHz flat[3]	—	—	20	dBrn
Idle-channel Noise (XMT; 600 Ω termination):				
Psophometric[3]	—	—	–77	dBmp0
C-message	—	—	12	dBrnC0
3 kHz flat[3]	—	—	20	dBrn0

1. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
2. Assumes ideal external components.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.
4. Transmission characteristics are specified assuming a 600 Ω resistive termination; however, feedback using external components allows the user to adjust the termination impedance from the intrinsic 600 Ω of the feed resistors to most ITU-T recommended complex termination impedances.
5. Measured with the L8575 SLIC connected per application diagram with ideal external components.

Electrical Characteristics (continued)

Serial Interface and Logic

The tables below summarize the parameter and timing requirements for logic inputs CLK, EN, DI, and DO.

Table 8. Logic Inputs (CLK, EN, and DI) and Outputs (DO)

Parameter[1]	Symbol	Min	Max	Unit
High-level Input Voltage	V_{IH}	2	V_{DDD}	V
Low-level Input Voltage	V_{IL}	0	0.8	V
Input Bias Current (high and low)	I_{IN}	—	±50	µA
High-level Output Voltage (I_{OUT} = –100 µA)	V_{OH}	V_{DDD} – 1.5	V_{DDD}	V
Low-level Output Voltage (I_{OUT} = 180 µA)	V_{OL}	0	0.4	V
Output Short-circuit Current (V_{OUT} = V_{DDD})	I_{OSS}	1	35	mA
Output Load Capacitance[2]	C_{OL}	0	50	pF

1. Unless otherwise specified, all logic voltages are referenced to DGND.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.

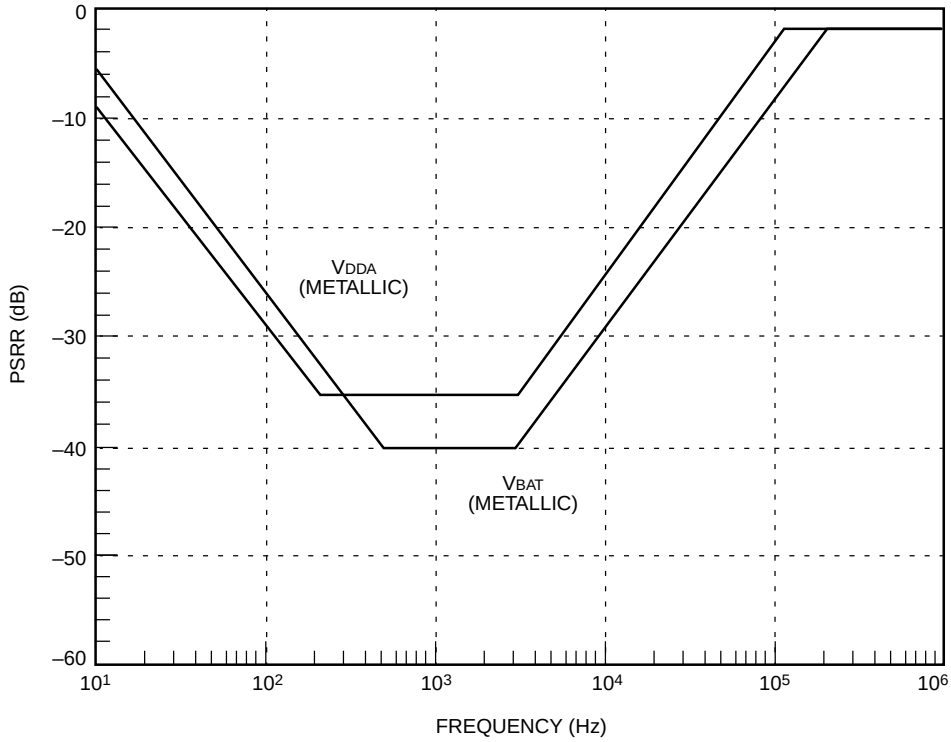
Table 9. Timing Requirements for CLK, EN, DI, and DO

Parameter[1]	Symbol	Min	Max	Unit
Input Rise and Fall Time, CLK & EN (10% to 90%)[2]	t_R, t_F	0	70	ns
Maximum Input Capacitance[2]	C_{IN}	—	5	pF
Maximum CLK Frequency (50% duty cycle)	f_{MAX}	—	1.25	MHz
Propagation Delay, CLK to DO[2]	t_{PCO}	0	350	ns
Propagation Delay, EN to RD Outputs[2]	t_{PCR}	0	10	µs
Minimum Setup Time from DI to CLK[2]	t_{SDC}	150	—	ns
Minimum Setup Time from DI to EN[2]	t_{SDE}	150	—	ns
Minimum Setup Time from EN to CLK[2]	t_{SEC}	150	—	ns
Minimum Hold Time from CLK to DI[2]	t_{HDC}	50	—	ns
Minimum Hold Time from EN to CLK[2]	t_{HEC}	50	—	ns
Minimum Pulse Width of CLK	t_{WCK}	400	—	ns
Minimum Pulse Width of EN	t_{WEN}	800	—	ns

1. Unless otherwise specified, all times are measured from the 50% point of logic transitions.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Serial Interface and Logic (continued)



12-3307(F)

Figure 3. Power Supply Rejection vs. Frequency Diagram

Applications

General

The L8575 is a dual (channels A and B) subscriber line interface circuit (SLIC). Each channel operates independently such that no interaction occurs between the channels. The following description applies to both channels though the description may refer to only a single channel. Some circuits, such as reference circuits which do not impact interchannel crosstalk, are common to both channels.

The L8575 device supplies a precise differential current to the Tip/Ring pair (via PT and PR) as a function of analog signal voltages on IRP and VRN. However, the current drivers connected to PT and PR are not designed to supply dc feed current to the loop. Two external resistors (typically 300 Ω), connected to office battery and ground, must be used in conjunction with the L8575 SLIC to provide dc loop current. These resistors will primarily determine the longitudinal balance of the line feed; thus, they must be matched appropriately to meet the longitudinal balance requirements (0.4% for 50 dB balance).

These resistors also have a significant impact on the termination impedance of the SLIC. Feedback, using external components, allows the user to adjust the termination impedance from the intrinsic 600 Ω of the feed resistors to most ITU-T recommended complex termination impedances. Since the L8575 does not supply dc to the loop, outputs PT and PR can be coupled to the Tip and Ring through a resistance high enough to allow for simple lightning protection of the drivers. However, the resistance must be low enough to achieve the coupling of sufficient ac signals to the Tip and Ring from the available power supply. Since the Tip and Ring drivers are current sources, the value of the resistance is arbitrary and does not affect the performance of the SLIC. A minimum value of 1400 Ω (1.4 kΩ) is required for protection purposes.

The L8575 also senses the Tip voltage, Ring voltage, and differential Tip/Ring voltage via the TS and RS sense inputs. The differential dc voltage is used internally for switchhook detection. The Tip and Ring voltages are also used internally to detect faults on Tip and Ring. Both detector thresholds are preset internally. The status of each detector is monitored at pin DO by reading the 8-bit serial shift register. The differential Tip/Ring ac signal appears on analog output XMT.

The L8575 also includes:

- Per-channel ring-trip detectors, loop closure detectors.
- Six relay drivers (three per channel).
- 8-bit serial-to-parallel and parallel-to-serial logic interface.
- Per-channel circuits which eliminate the battery noise that is coupled to the Tip and Ring through the dc feed resistors.
- Fault detection.
- Zero ring voltage detection.

Resistor Module

The L8575 requires certain external resistors at the Tip and Ring interface. Because of matching and protection requirements, one of the most economical options recommended to implement these registers is in a thick film resistor module. A schematic and a brief description of the function of each of these resistors is given in Figure 4. Note that Microelectronic Modules Corporation* *MMC* A31A8575AA Thick Film resistor module is an application-specific resistor module designed for use with the L8575 SLIC. The values, tolerance, matching, and power rating of the *MMC* A31A8575AA module are given in Table 10.

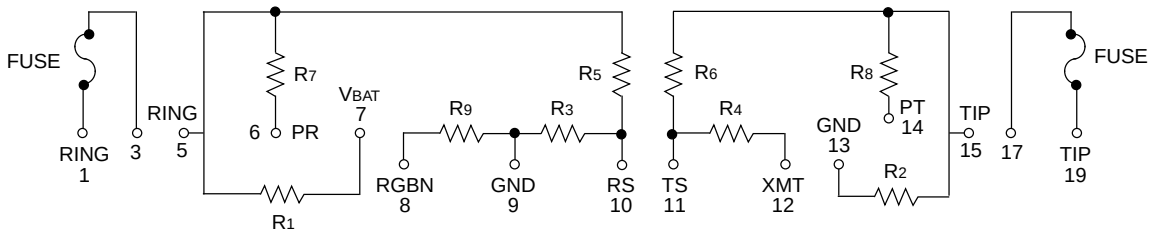
Resistors R_1 and R_2 are the dc feed resistors. R_1 is connected from battery to Ring, and R_2 is connected from Tip to ground. The dc loop current is fed to the subscriber loop via these resistors. These resistors will set the dc I/V template of the line circuit with the I/V template being linear with a –1/600 Ω slope. No constant current region at short dc loops is provided by resistors R_1 and R_2, or the L8575 SLIC.

* For additional information, contact Microelectronic Modules Corporation (*MMC*), 2601 S. Moorland Rd., New Berlin, WI 53151:

U.S.A: (414) 785-6506
FAX Number: (414) 785-6516

Applications (continued)

Resistor Module (continued)



5-3428(F)

Note: Pin numbers are *MMC* A31A8575AA pin numbers. Resistors are labeled per *MMC* A31A8575AA description. Nodes are L8575 SLIC package nodes.

Figure 4. L8575 SLIC Resistor Module

Table 10. *MMC* A31A8575AA Thick Film Resistor Module

Resistor	Value	Tolerance	Power	Surge Rating
R_1	300 Ω	1.0%	2.0 W	Lightning: Power Cross
R_2	300 Ω	1.0%	2.0 W	Lightning: Power Cross
R_3	100 kΩ	1.0%	250 mW	None
R_4	100 kΩ	1.0%	250 mW	None
R_5	200 kΩ	1.0%	250 mW	Lightning: Power Cross
R_6	200 kΩ	1.0%	250 mW	Lightning: Power Cross
R_7	1.4 kΩ	2.0%	0.5 W	Lightning: Power Cross
R_8	1.4 kΩ	2.0%	0.5 W	Lightning: Power Cross
R_9	15 kΩ	—	10 mW	None
R_9/R_1	50	1.0%	—	—
R_1/R_2	1	0.35%	—	—
$(R_3 + R_6)/(R_4 + R_5)$	1	0.35%	—	—

Note: For 50 dB longitudinal balance, 0.2% for 58 dB balances. Continuous power (rms).

Resistors R_1 and R_2 also provide a common-mode impedance of (300 || 300) 150 Ω. These resistors will primarily determine the longitudinal balance of the line circuit; thus they must be matched appropriately to meet longitudinal balance requirements (0.35% for 50 dB and 0.2% for 58 dB). Also, they have a significant impact on the termination impedance of the SLIC. Feedback using external components (external components when a first- or second-generation codec is used) allows the user to set the termination impedance at 600 Ω, or most ITU-T recommended complex termination impedances.

Resistors R_1 and R_2, along with R_3 and R_7, are used in conjunction with the self-test feature of the L8575 SLIC. In this mode, the Ring current drive amplifier is saturated to ground, and the Tip amplifier is saturated to battery, which causes both the ring-trip and loop closure detectors to trip. Ring-trip and loop closure detector output are bits RT and LC, respectively, in the serial output stream.

Under normal operating conditions, resistors R_1 and R_2 will see the battery voltage less the Tip/Ring voltage. Assuming a Tip/Ring voltage of 6 V (representative of a short into a handset), the nominal continuous operating power of R_1 and R_2 is given by:

$(48\text{ V} - 6\text{ V})^2/600\ \Omega = 2.94\text{ W}$
per R_1 and R_2 resistor pair

2.94 W/2 = 1.47 W per resistor

The operating power rating of R_1 and R_2 is 2 W. This is the steady-state power rating of R_1 and R_2, and it is adequate for normal operating conditions. The ability of these resistors to withstand fault conditions depends on the power ratings of the individual resistors and on the power rating of the thick film resistor module itself. Obviously, the higher the power capabilities of the resistor module, the less susceptible the resistors are to damage during faults. The various fault conditions are discussed further in the Protection section of this data sheet.

Applications (continued)

Resistor Module (continued)

Resistors R3 through R6 set the gain of the SLIC in the transmit (2-wire to 4-wire) direction. This is shown in Figure 5.

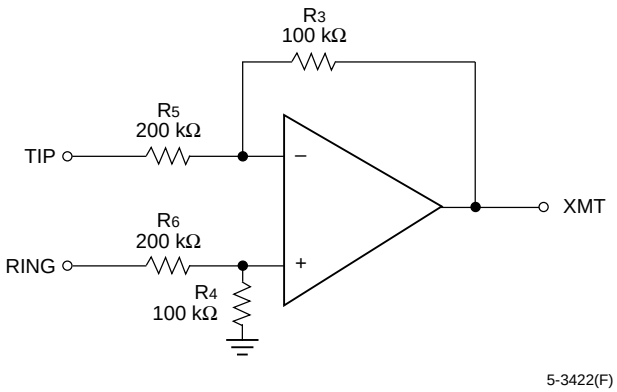


Figure 5. L8575 SLIC Dual-Resistive Matching Requirements

The matching of resistors R3 through R6 will determine the gain accuracy of the SLIC; therefore, these resistors must also be matched accordingly. The matching requirements are given in Table 10.

Because of the high resistance values, the normal operating power of resistors R3 through R6 will be relatively low. Given design margin and thick film technology capabilities, a power rating of 250 mW for these resistors is not unreasonable.

Resistors R7 and R8 are used to couple the PT and PR current drive amplifiers to Tip and Ring. Since the PT and PR drive amplifiers are current sources, the value of the series resistance does not affect the loop length or other performance of the SLIC, and may be arbitrarily high for protection purposes. A value of 1.4 kΩ is adequate for protection purposes.

Under normal operating conditions, these resistors will see the battery voltage less the Tip/Ring voltage. Assuming a Tip/Ring voltage of 6 V (representative of a short into a handset), the nominal continuous operating power of R7 and R8 is given by:

$(48\ V - 6\ V)^2/2.8\ k\Omega = 0.630\ W$
per R7 and R8 resistor pair

630 mW/2 = 315 mW
per resistor (R7 and R8)

Hence, the operating power rating of 500 mW for R7 and R8. This is the nominal rating for R7 and R8 under normal operating conditions. Again, the ability of these resistors to withstand fault conditions depends on the power rating.

Resistor R9 is also included on the thick film resistor module. This resistor is used to set the gain of the battery noise cancellation circuit. See the Battery Noise Cancellation section of this data sheet for design equations to set the value of R9.

Protection

Because of the resistive feed architecture, a simple inexpensive protection scheme that does not require a separate external protection device may be used. The *MMC* A31A8575AA resistor module has specifications which are qualified to Bellcore GR-CORE-1089, *UL**1459, *UL* 497A, FCC part 68.302 (d) & (e) and REA form 397G, ITU-T K20, and ITU-T K21.

Lightning and power cross protection are provided by the two dc feed resistors, R1 and R2, in the external resistor module. Under fault conditions, these resistors serve as fault current-limiting resistors. Fault current is steered to ground and to battery via resistors R2 and R1, respectively. Thus, the battery design must be such that the various specified faults can be applied to the battery through 300 Ω, without damaging the battery or the line circuit.

Resistors R1 and R2 need to be designed to survive lightning surges and to dissipate power associated with a Ring ground dc fault and specified ac power cross faults—both a sneak under and full surge type fault. Under certain sustained fault conditions, R1 and R2 could fail when they are required to survive. For this reason, a per-channel fault detector is included on the L8575 SLIC.

When the voltage across either R1 and/or R2 is greater than a nominal 36 V, the fault detect bit (FLT) in the serial data output will go high. The control logic on the line card detects FLT is high, and opens an external electromechanical relay (EMR) to isolate the resistors from the loop, enabling the resistors to service extended power cross. (Note the EMR is the test in or test out EMR, and this relay is driven by one of the internal relay drivers on the L8575 SLIC.)

A delay of 10 ms to 30 ms is provided (using an external capacitor on pin CFLT) in the fault detector. This prevents transients on the Tip and Ring from tripping the fault detector when a fault is not present.

* *UL* is a registered trademark of Underwriters Laboratories, Inc.

Applications (continued)

Protection (continued)

The Tip/Ring drive amplifiers, which feed the ac signal to nodes PR and PT, are high-impedance current drivers. Since these nodes are current sources, the value of protection current-limiting series resistance does not affect the loop length or other SLIC performance, and may be arbitrarily high for protection purposes.

Resistors R_7 and R_8 in the resistor module are used for this purpose. These resistors have a value of 1.4 kΩ with a power rating 0.5 W. Internal diodes clamp nodes PR and PT to ground and battery.

The voltage sense leads, RS and TS, are also exposed to the outside plant. Current to these nodes is limited by resistors R_3 and R_4 in the resistor module. Resistors R_3 and R_4 are 100 kΩ, 250 mW resistors. Internal diodes also clamp nodes RS and TS to ground and battery.

The ability of the resistors to survive faults is a function of the power dissipated in the individual resistors and the total power dissipated on the entire thick film module. Fault conditions include:

- A continuous worst-case (fault detector) sneak under condition of 39 Vdc applied metallically to Ring in the case of a Ring ground fault, and
- A sneak under condition of 39 Vp (voltage peak) applied to Tip and Ring, as described in Bellcore 1089, ITU-T K20, etc., in the case of power cross.

Additionally, there is a transient fault condition, assuming full specified power cross fault voltages (Bellcore 1089, ITU-T K20, etc.,) for a time duration equal to the maximum response time that it will take to isolate the line circuit from the fault via the fault detector and EMR described above.

For example, a Ring ground fault assuming fault detector sneak under will result in a worst-case potential across the R_1 of 39 V. The power dissipated in R_1 under this condition is calculated as follows:

(39 V * 39 V)/300 Ω = 5 W

Since this is a sneak under condition, the fault detector will not trigger and the time duration of the fault can be infinite. In the case of a longitudinally applied sneak under power cross, the maximum voltage seen, this time by both R_1 (Ring) and R_2 (Tip), is 39 Vp (voltage peak). The power dissipation is given by:

Maximum Voltage = 39 Vp = 27.6 Vrms
Maximum Power = (27.6 Vrms * 27.6 Vrms)/(300 Ω)
= 2.54 W per resistor.

Thus, 2.54 W will be dissipated per resistor or a total of 5.1 W in a longitudinal sneak under condition.

If R_1 and R_2 are rated for 2 W, they can fail under these fault conditions. Also, the *MMC* A31A8575AA resistor module includes a fail-safe thermal fuse located at the Tip and Ring nodes (pin 1 and pin 19) of the module for this reason. A fail-safe fuse is recommended for any resistor module used with the L8575 SLIC.

With thick film technology, not only is the power capabilities of the individual resistors important, but also the power handling capabilities of the entire module. The total module power dissipation is calculated by summing the power dissipation for each of the resistors under a given condition.

For example, the module power dissipation for the above sneak under fault conditions is calculated in Table 11. Thus, the HIC will require a minimum power rating of 6 W continuous to survive these sneak under conditions.

Table 11. Total Module Power Dissipation

Resistor (R)	Value (Ω)	Ring Ground Maximum dc Fault Voltage (V)	Ring Ground Maximum dc Fault Power (W)	Longitudinal Fault Maximum Peak Voltage (Vp)	Longitudinal Fault Maximum rms Voltage (Vrms)	Longitudinal Fault Maximum rms Power (W)
1	300	39	5.07	39	27.577	2.535
2	300	0	0	39	27.577	2.535
3	100 k	29	0.015	39	27.577	0.0076
4	100 k	0	0	39	27.577	0.0076
5	200 k	39	0.0076	39	27.577	0.0038
6	200 k	0	0	39	27.577	0.0038
7	1.4 k	39	1.086	39	27.577	0.543
8	1.4 k	0	0	39	27.577	0.543
Total HIC Power:			6.18	—	—	6.18

Applications (continued)

Protection (continued)

Similar consideration to the individual resistor and total module power capability should be given to full voltage power faults, but taking into account the fault detector will isolate the SLIC and resistor module after some finite period of time. The fault detector indicates a fault in the serial data output stream in 10 ns to 30 ms. Recognition and relay activation time need to be considered.

Tip/Ring Drivers

Each channel of the L8575 utilizes a current source for the Tip/Ring driver. The driver is capable of sinking (but not sourcing) up to 15 mA from the Tip (PT) while swinging to within 4 V of office battery (V_{BAT}), and sourcing (but not sinking) up to 15 mA to the Ring (PR) while swinging to within 4 V of ground (AGND). Since the current driver is not bidirectional, during transmission (powerup) each lead is biased at 5.6 mAdc.

Receive Interface

The receive interface circuitry couples the differential signal on receive inputs IRP and VRN to the Tip/Ring drivers. Input IRP is a low-impedance (<5 Ω) current input while VRN is a high-impedance voltage input. Internal feedback forces the voltage at IRP to be equal to VRN such that a voltage applied to VRN causes a current flow out of IRP, which equals that voltage divided by the impedance connected from IRP to AGND (assuming the input voltage is referenced to AGND).

The receive interface and Tip/Ring drivers provide a current gain of 200, i.e., a differential output current flows from PT to PR which is 200 times the current flowing into IRP. The receive interface also provides a level shift since the inputs, IRP and VRN, are referenced to analog ground, while the outputs, PT and PR, swing between AGND and V_{BAT}. The receive interface ensures that the input current is not converted to a common-mode current at PT and PR.

Transmit Interface

The transmit interface circuitry interfaces the differential voltage on Tip and Ring to transmit output XMT. The Tip/Ring differential voltage (both ac and dc) appears on output XMT with a gain of 0.5.

The transmit interface uses an operational amplifier with four external resistors to perform a differential to single-ended conversion. Output XMT is referenced to ground (AGND). The longitudinal balance and gain accuracy at XMT depends on the matching of the external resistors.

Because a large dc potential exists at XMT, a capacitor must be used to couple the ac signal to the low-voltage codec circuitry. The operational amplifier inputs are TS and RS. These inputs are also used by the fault-detection circuitry to detect fault voltages on Tip or Ring. A fault is detected when the magnitude of the voltage across either dc feed resistor exceeds a nominal 36 V (equivalent to approximately 4 W dissipation in either resistor). A delay is provided (using an external capacitor on pin CFLT) in the fault detector. This prevents transients on Tip and Ring from tripping the fault detector when a fault is not actually present.

Battery Noise Cancellation

The battery noise cancellation circuit senses the ac noise on the battery via the capacitor connected from input CBN to V_{BAT}. It then couples this noise, 180 degrees out of phase, to the Ring current driver amplifier. This cancels the battery noise that is coupled to the Ring through the feed resistor connected to V_{BAT}.

Additionally, it ensures longitudinal balance which depends only on the matching of the battery feed resistors by creating an ac ground at V_{BAT} with respect to signals on the Ring lead.

For the cancellation to operate properly, both the phase and gain must be accurate. The battery noise cancellation gain is a transconductance that is equal to 50 divided by resistor R9 on the thick film resistor module connected from RGBN to ground (AGND). This value must be equal to the reciprocal of the dc feed resistor (1/300 Ω), that is,

$$\frac{50}{R_9} = \frac{1}{300\ \Omega}$$
$$R_9 = 15\ k\Omega$$

It is advantageous if the two resistors are matched and tracked thermally, i.e., located on the same film integrated circuit (FIC).

Applications (continued)

On-Hook Transmission

In powerup mode, the L8575 SLIC provides a dc bias of 5.6 mA. The 5.6 mA bias is also present under on-hook conditions. The L8575 SLIC is able to support on-hook transmission because of this bias. It is sufficiently high to drive a 3.17 dBm signal into a 600 Ω or 900 Ω loop under open-circuit conditions. An internal current source provides a dc bias of 112 µA. There is an internal current gain of 50; thus (50 * 112 µA) 5.6 mA flows from battery through R_1 to PR, and 5.6 mA flows from PT through R_2 to ground under on-hook conditions.

Self-Test

The L8575 SLIC offers a self-test capability. This is set via logic inputs D1 and D0 in the serial input data stream. In this mode, shown in Figure 6, the Ring current drive amplifier is saturated to ground, and the Tip amplifier is saturated to battery, which causes both the ring-trip and loop closure detectors to indicate an off-hook condition. In this operation mode, the ring relay must not be active. The ring relay driver output in the L8575 is at package nodes RDR (A&B). These relay drivers are controlled by logic inputs D2 (A&B) in the serial input data stream. See Table 14 for details.

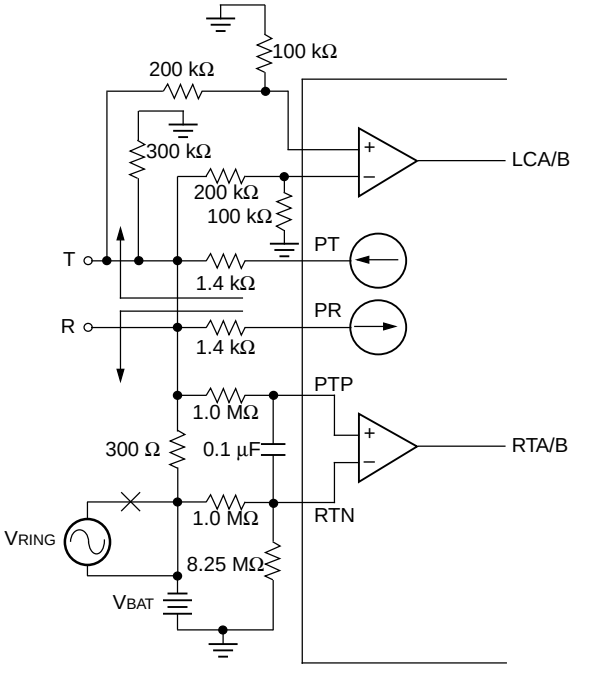


Figure 6. Self-Test Mode Circuit

Serial Data Interface

A 4-wire serial interface (DI, DO, CLK, and EN) is used to pass data from the control logic on the line card to the L8575 SLIC, and to pass detector information from L8575 SLIC to the control logic on the line card. When enable input EN is high, data on input DI is clocked into an 8-bit shift register on a high-to-low transition of the clock input CLK.

Eight latches (four per channel) are provided to store the data. Data is loaded into the eight latches from input DI and the first 7 bits of the shift register on the high-to-low transition of EN. When EN is low, a high-to-low transition on CLK loads all of the detector information (loop closure, fault zero voltage, and ring-trip from the internal detector circuitry) into the 8-bit shift register. When EN is high, data in the 8-bit shift register is clocked out on output DO on the high-to-low transition of CLK.

Two latch outputs per channel drive relay drivers. The drivers are included on the L8575 SLIC. These are the relay drivers whose outputs are at external package nodes RDR (A&B) and RDT (A&B). The remaining two latch output power channels are internal control signals. These are logic data bits D0 (A&B) and D1 (A&B). These bits input to a combinational logic circuit that controls the operational state of each channel and also controls the state of the third relay driver. The third relay driver's output is at external package node RDD (A&B). Refer to the Truth Table (see Table 15) for more details.

Note that up to 16 channels may be daisy-chained together. The DO lead of package 1 (channels 1 and 2) may be tied to the DI lead of package 2 (channels 3 and 4), etc. All EN and CLK should also be tied together in this mode.

The L8575 SLIC device has an internal reset which guarantees that all relay drivers power up in the off-state when 5 V (V_{CCD} and V_{CCA}) is applied to the device. This reset operates properly only if input EN is held high (within 0.5 V of V_{CCD}) when the 5 V is applied. An external pull-up resistor from the EN bus to V_{CCD} satisfies this requirement, provided that the logic-driving EN does not pull the EN bus low during powerup.

Applications (continued)

Serial Data Interface (continued)

Figure 7 shows the timing characteristics and requirement definitions.

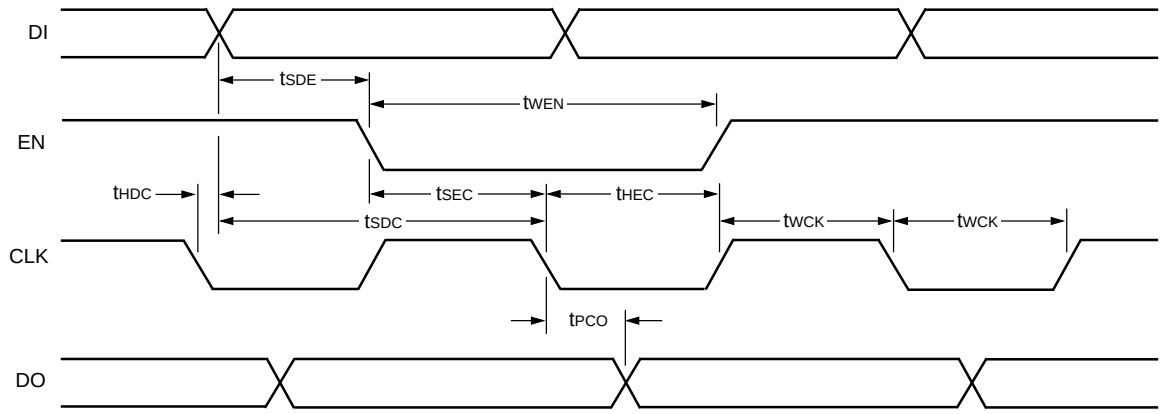


Figure 7. Timing Requirements for CLK, EN, DI, and DO

Table 12. Truth Table for EN and CLK

EN	CLK	Function
1	↓	Shift register clocked, QN = QN – 1; latches unaffected.
0	↓	Channel data latched into shift register; latches unaffected.
↓	X	Contents of shift register transferred to output latches.

Table 13. Output DATA Bit Definition

DATA Bit	Output	Output Bit Definition
D0A	D0A	Latch output state D0A (refer to Operating States section).
D1A	D1A	Latch output state D1A (refer to Operating States section).
D2A	RDRA	Ringing relay driver A is on (RDRA low = relay energized) when D2A = 1.
D3A	RDTA	Test relay driver A is on (RDTA low = relay energized) when D3A = 1.
D0B	D0B	Latch output state D0B (refer to Operating States section).
D1B	D1B	Latch output state D1B (refer to Operating States section).
D2B	RDRB	Ringing relay driver B is on (RDRB low = relay energized) when D2B = 1.
D3B	RDTB	Test relay driver B is on (RDTB low = relay energized) when D3B = 1.

Electrical Characteristics (continued)

Serial Data Interface (continued)

Table 14. Input DATA Bit Definition

Input	DATA Bit	Input Bit Definition
RZA	D0A	Channel A ringing voltage zero crossing detector output (positive = 1).
FLTA	D1A	Channel A fault detector output (loop fault = 1).
RTA	D2A	Channel A ring-trip detector output (ring-trip = 1).
LCA	D3A	Channel A switchhook detector output (off-hook = 1).
RZB	D0B	Channel B ringing voltage zero crossing detector output (positive = 1).
FLTB	D1B	Channel B fault detector output (loop fault = 1).
RTB	D2B	Channel B ring-trip detector output (ring-trip = 1).
LCB	D3B	Channel B switchhook detector output (off-hook = 1).

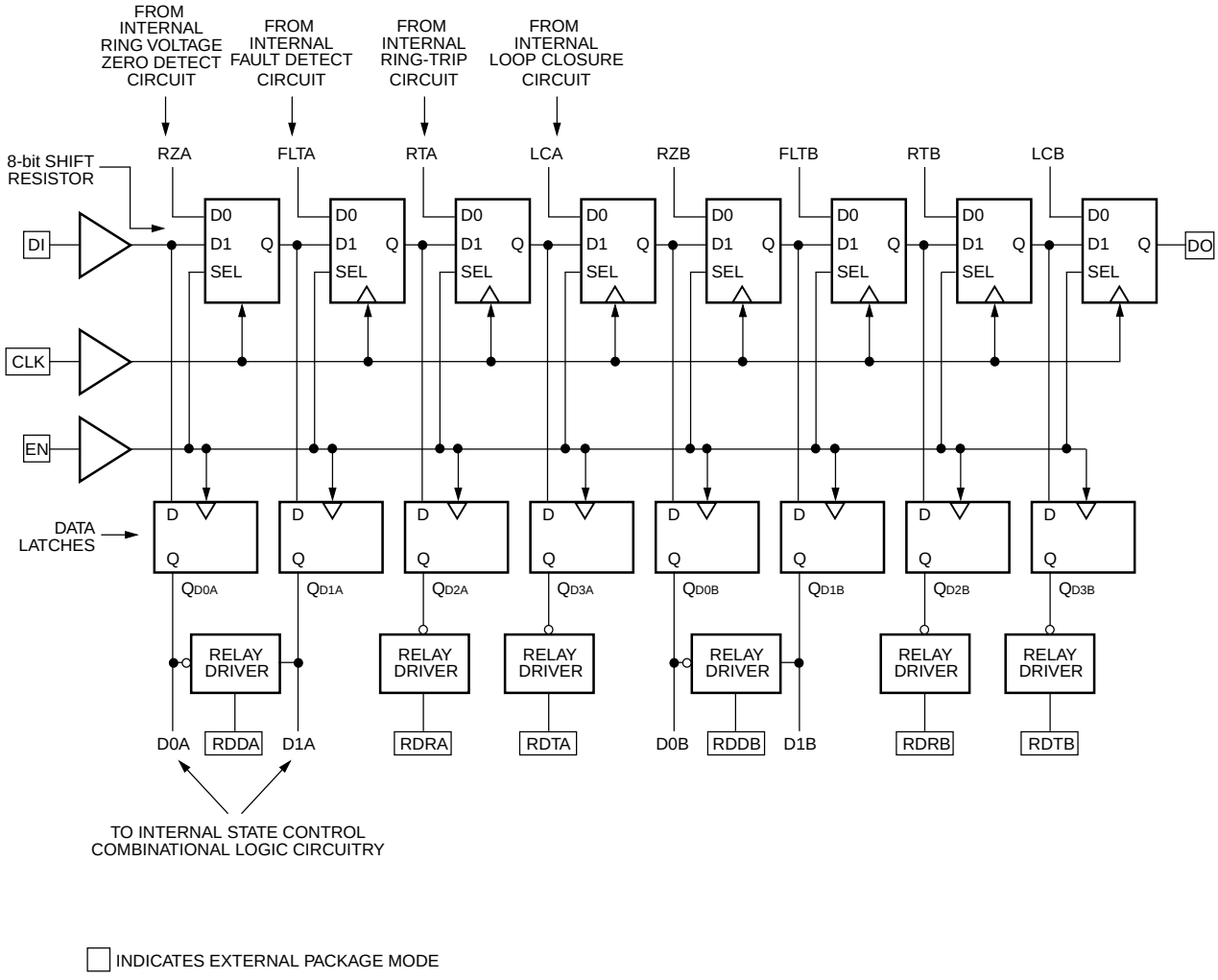


Figure 8. Logic Diagram (Positive Logic; Flip-Flops Clocked on High-to-Low Transition)

Operating States

Each channel of the L8575 has four operating states: active, test, powerdown with relay driver RDD ON, and powerdown with relay driver RDD OFF. These states are selected using 2 bits, D0 and D1, via the serial interface according to the truth table shown below.

Table 15. Truth Table for D1 and D0

D1	D0	State
1	1	Channel Active.
1	0	Channel Test.
0	1	Channel Powerdown and Relay RDD driver ON (RDD low).
0	0	Channel Powerdown. Relay RDD driver OFF/RDD high.

Logic input D2 operates the ringing relay driver, RDR, independent of the state of bits D0 and D1; however, the ring-trip detector is enabled only when D2 operates the ringing relay driver. Hence, the ringing relay driver is not interchangeable with any of the other relay drivers. Logic input D3 operates the test relay driver, RDT, independent of the state of bits D0 and D2.

Active State

This is the normal operating state (talk state) of the channel. All circuits are operational. The Tip drive current source sinks 5.6 mAdc from PT; the Ring drive current source sinks 5.6 mAdc into PR.

Test State

This is the test state of the channel. It is the same as the active state except that the Ring drive current source is saturated to ground and the Tip driver current source is saturated to V_{BAT}. This forces the loop-closure and ring-trip detectors to indicate an off-hook. This state is valid only when the ringing relay is not operated (D2 = 0).

Powerdown State with Relay Driver RDD Operated

This is the disconnect state of the channel. It is the same as the powerdown state except that relay driver RDD is also operated. When required, this relay may be used to disconnect the external dc feed resistors in order to provide a high-impedance termination to the subscriber loop.

Powerdown State

This is the normal idle state (scan state) of the channel. The loop-closure, ring-trip, and common-mode fault detectors are active, but all other circuits are shut down to conserve power. All circuits common to both channels remain active. The powerdown of channel A does not affect an active channel B and vice-versa.

Ringing State (D2 = 1)

When D2 = 1, the ringing relay driver is activated. The operational state of the SLIC is unaffected except for the ring-trip and fault detectors. The digital portion of the ring-trip detector is enabled when D2 = 1 (relay drive activated) and disabled when D2 = 0 (relay drive deactivated). The ring-trip detector functions properly only when D2 = 1 so that a valid ringing signal (ac and dc) is present. When D2 = 0, the digital portion of the ring-trip detector is bypassed so that most of the ring-trip circuit can be tested in the test state. When D2 = 1, the fault detector is also disabled (FLT forced to 0).

Supervision

Off-Hook Detection

The off-hook detection threshold is a function of the dc feed resistors R_1 and R_2, and of a ratio of resistors that are fixed on the L8575 silicon die.

Thus, when $R_1 = R_2 = 300\ \Omega$, the off-hook threshold is set at 4 kΩ. This relationship is shown in the equation below:

$$R_T = \frac{R_1 + R_2}{\frac{1}{2\ k\Omega} - 1}$$

Where,

R_T is the loop closure threshold
$R_1 = R_2$ = dc feed resistors = 300 Ω

$$K = \frac{R_{T1}}{R_{T1} + R_{T2}} = 0.4333\ \Omega$$

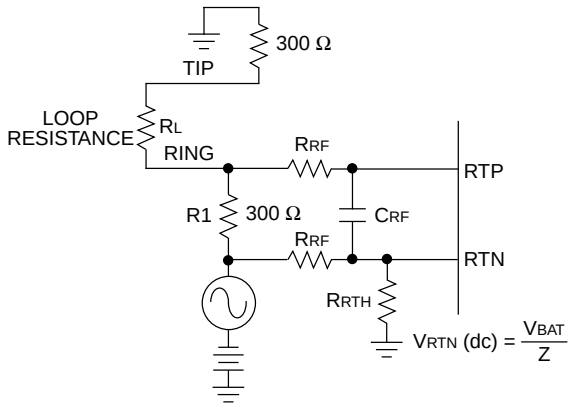
Where,

R_{T1} and R_{T2} are internal resistors
R_{T1} = 170 kΩ
R_{T2} = 130 kΩ

Thus,

$$R_T = \frac{300\ \Omega + 300\ \Omega}{\frac{1}{2\left(\frac{130\ k\Omega}{130\ k\Omega + 170\ k\Omega}\right)} - 1} = 3900\ \Omega \approx 4\ k\Omega$$

Ring-Trip Threshold



12-3424(F)

Figure 9. Ring-Trip Threshold

Ring-trip threshold (Figure 9) is calculated as follows:

At ring-trip: $\left(\frac{V_{BAT}}{2}\right)\left(\frac{R_{RF}}{R_{RTH}}\right) = \left(\frac{300\ \Omega}{R_L + 600\ \Omega}\right)V_{20\ Hz\ (dc)}$

If,

$$V_{BAT} = V_{20\ Hz\ (dc)}$$

Then,

$$\frac{R_{RF}}{2R_{RTH}} = \frac{300\ \Omega}{R_L + 600\ \Omega}$$

$$R_{RTH} = R_{RF}\left(1 + \frac{R_L}{600\ \Omega}\right)$$

R_{RF} = 1 MΩ; R_L (ring-trip) = 6 kΩ [Avg: 2 kΩ & 10 kΩ]

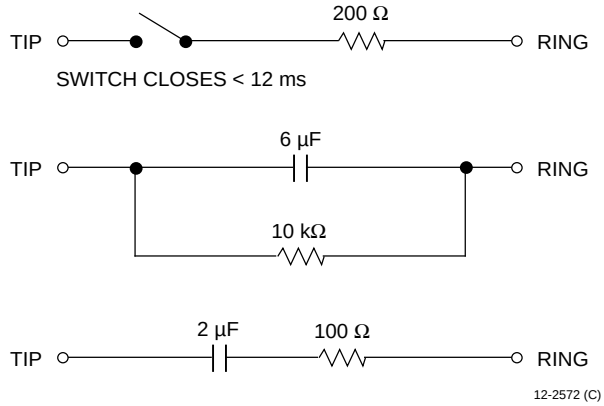
$$\therefore R_{RTH} = 11\ M\Omega$$

$$2R_{RF}C_{RF} \approx 100\ ms$$

$$\therefore C_{RF} = 0.047\ \mu F$$

Ring-Trip Requirements

- Ringing signal:
  - — Voltage: minimum 35 Vrms, maximum 100 Vrms.
  - — Frequency: 17 Hz to 23 Hz.
  - — Crest factor: 1.4 to 2.
- Ringing trip:
  - — ≤100 ms (typical), ≤250 ms (V_{BAT} = –33 V, loop length = 530 Ω).
- Pretrip:
  - — The circuits in Figure 10 will not cause ringing trip.



12-2572 (C)

Figure 10. Ring-Trip Circuits

Supervision (continued)

Fault Detection

The dc feed resistors R_1 and R_2 need to be designed to survive lightning surges and to dissipate power associated with a Ring ground dc fault and specified ac power cross faults—both in a sneak under and full surge type fault.

Under certain sustained fault conditions, R_1 and R_2 could fail when they are required to survive. For this reason, a per-channel fault detector is included on the L8575. When the voltage across either R_1 and R_2 is a nominal 36 V (maximum 39 V), the fault detect bit, FLT in the serial data output, will go high, as calculated below:

FLT = 1, if
$|V_{TIP}| > 36$ V nominal

or

$|V_{RING} – V_{BAT}| > 36$ V nominal, which corresponds to dc power in R_1 or $R_2 > 4$ W

The control logic on the line card detects FLT is high and opens an external electromechanical relay to isolate the resistors from the loop, enabling the resistors to survive extended power cross. (Note the EMR is the test in or test out EMR, and this relay is driven by one of the internal relay drivers on the L8575 SLIC.)

With an external 0.1 µF capacitor on pin CFLT, a no-fault to fault delay of 10 ns to 30 ms is provided in the fault detector. This prevents transients on Tip and Ring from tripping the fault detector when a fault is not present. There is a release delay (fault to no-fault) of 1.6 T to 2.5 T, where T is the no-fault to fault delay time.

Zero Voltage Current Cross

The L8575 provides a bit, RZA (and RZB for channel B), in the serial data stream which gives an indication when the ringing voltage is crossing zero. This signal bit may be used in timing the application and removal of the ringing signal.

Relay Drivers

Six relay drivers, three relay drivers per channel, are included on the L8575 SLIC. The output of these drivers are package nodes RDD (A&B), RDR (A&B), and RDT (A&B). Drivers RDR (A&B) are controlled by input bits D2 (A&B) on the serial input stream. Drivers RDT(A&B) are controlled by input bits D3 (A&B) on the serial input stream. In these cases, a logic 1 on D2 or D3 activates the respective relay driver.

Relay drivers RDD (A&B) are controlled per the truth table (see Table 2) via bits D0 (A&B) and D1 (A&B). In order to activate driver DDR, D0 = logic 1 and D1 = logic 0. Note that with D0 = logic 1 and D1 = logic 0, the SLIC is set to the channel powerdown state.

Relay drivers RDR (A&B) must be used for the Ring relay function because the ring-trip detector is enabled only when D2 is high; that is, when D2 operates the ringing relay driver (RDR). Hence, the test and ringing relay drivers are not interchangeable.

When relay driver RDD is active, the L8575 is forced into a powerdown state. Thus, using RDD with the test-in relay is not appropriate. This relay may be used for test out or as a channel isolation relay.

Relay driver RDT is controlled by D3 in the serial bit stream. Logic input D3 operates driver RDT independent of the state of bits D0, D1, and D2. RDT may be used with a test-in, test-out, or channel isolation relay.

dc Characteristics

I/V Characteristics

Resistors R_1 and R_2 are the dc feed resistors. R1 is connected from battery to Ring, and R2 is connected from Tip to ground. The dc loop current is fed to the subscriber loop via these resistors. These resistors will set the dc I/V template for the line circuit, with the I/V template being linear with a –1/600 Ω slope. No constant current region at short dc loops is provided by resistors R_1 and R_2 or the L8575 SLIC.

The dc Tip/Ring voltage under open loop conditions is 3.36 V less than battery. In order to drive an on-hook ac signal, the Tip and Ring voltage must be set to a value less than the battery voltage. The amount that the open loop voltage (V_{OC}) is decreased relative to the battery (V_{BAT}) is referred to as the overhead voltage (V_{OH}). This overhead voltage is due to 5.6 mA of bias current flow from both the Tip and Ring current drive amplifier's flow through resistors R2 and R1, respectively. Thus, the overhead is given by:

$V_{OH} = (R_1 \times 5.6\ mA) + (R_2 \times 5.6\ mA)$

$V_{OH} = (300 \times 5.6\ mA) + (300 \times 5.6\ mA) = 3.36\ V$

The nominal dc I/V template for the L8575 SLIC is shown in Figure 11.

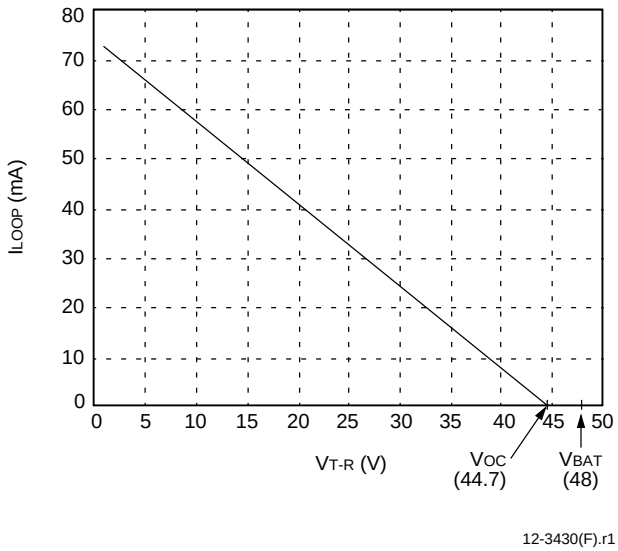


Figure 11. L8575 SLIC I/V Template

Loop Length

The loop range equation is given by:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_L} - R_1 - R_2$$

Where,

R_L is the dc resistance of the subscriber loop.

I_L is the dc loop current.

$|V_{BAT}|$ is the magnitude of the battery voltage.

V_{OH} is the overhead voltage—nominal 3.36 V.

$R_1 = R_2$ = dc feed resistors = 300 Ω.

Thus, for a nominal –48 V battery with a minimum 18 mA loop requirement, the loop range will be:

$$R_L = \frac{|48\ V| - 3.36\ V}{0.018\ A} - 300\ \Omega - 300\ \Omega$$

$R_L = 1880\ \Omega$

ac Design

Codec Features and Selection Summary

There are four key ac design parameters:

- *Termination impedance* is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set.
- *Transmit gain* is measured from the 2-wire port to the PCM highway.
- *Receive gain* is done from the PCM highway to the transmit port.
- *Hybrid balance network* cancels the unwanted amount of the receive signal that appears at the transmit port.

At this point in the design, the codec needs to be selected. The discrete network between the SLIC and the codec can then be designed. Below is a brief codec feature and selection summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, and μ-law/A-law selectability. This generation of codec has the lowest cost. It is most suitable for applications with fixed gains, termination impedance, and hybrid balance.

Second-Generation Codecs

This class of devices includes a microprocessor interface for software control of the gains and hybrid balance. The hybrid balance is included in the device. ac programmability adds application flexibility and saves several passive components. It also adds several I/O latches that are needed in the application. It does not have the transmit op amp, since the transmit gain and hybrid balance are set internally.

Third-Generation Codecs

This class of devices includes the gains, termination impedance, and hybrid balance—all under microprocessor control. Depending on the device, it may or may not include latches.

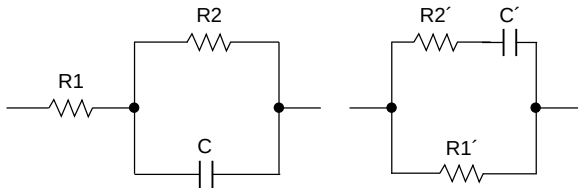
In the codec selection, increasing software control and flexibility are traded for device cost. To help decide, it may be useful to consider the following:

- Will the application require only one value for each gain and impedance?
- Will the board be used in different countries with different requirements?
- Will several versions of the board be built? If so, will one version of the board be most of the production volume?
- Does the application need only real termination impedance?
- Does the hybrid balance need to be adjusted in the field?

ac Design (continued)

Design Equations

The following section gives the relevant design equations to choose component values for any desired gain, termination and balance network, assuming a complex termination is desired. Complex termination will be specified in one of the two forms shown below:



12-3425(F)

Figure 12. Equivalent Complex Terminations

Both forms are equivalent to each other, and it does not matter which form is specified. The component values in the interface circuit of Figure 12 are calculated assuming the parallel form is specified. If the termination impedance to be synthesized is specified in the series form, convert it to the parallel form using the equations below:

$$R_1' = R_1 + R_2$$

$$R_2' = \frac{R_1^2 + R_2 R_1}{R_2}$$

$$C' = \frac{C}{1 + 2\frac{R_1}{R_2} + \left(\frac{R_1}{R_2}\right)^2}$$

Note that if the termination impedance is specified as pure resistive:

$$R_2 = R_2' = 0 \text{ and } C = C' = \infty$$

Define the gain constant, K, as follows:

$$K_{RCV} = K_0 10^{Rx/20} \text{ for receive gain}$$

$$K_{TX} = \frac{1}{K_0} 10^{Tx/20} \text{ for transmit gain}$$

Where,

R_X = desired receive (or PCM to Tip/Ring) gain in dB

T_X = desired transmit (or Tip/Ring to PCM) gain in dB

$$K_0 = \sqrt{\frac{|Z_T|\ 1\ kHz}{600}} = \text{ power transfer ratio}$$

$|Z_T|$ 1 kHz is the magnitude of the complex termination impedance Z_T being synthesized, calculated at 1000 Hz. This equation assumes that the TLP of the codec is 0 dBm referenced to 600 Ω.

The following equation applies when referring to Figure 13:

$$Z_T = \frac{\omega^2 C^2 R_1 R_2^2 + R_1 + R_2 - j\omega R_2^2 C}{1 + \omega^2 R_2^2 C^2}$$

Where,

$\omega = 2\pi f$

f = 1000 Hz

CR_1R_2 is defined per Figure 12 (series form), and

$$|Z_T| = \sqrt{\left(\frac{\omega^2 C^2 R_1 R_2^2 + R_1 + R_2}{1 + \omega^2 R_2^2 C^2}\right)^2 + \left(\frac{\omega R_2^2 C}{1 + \omega^2 R_2^2 C^2}\right)^2}$$

ac Design (continued)

Design Equations (continued)

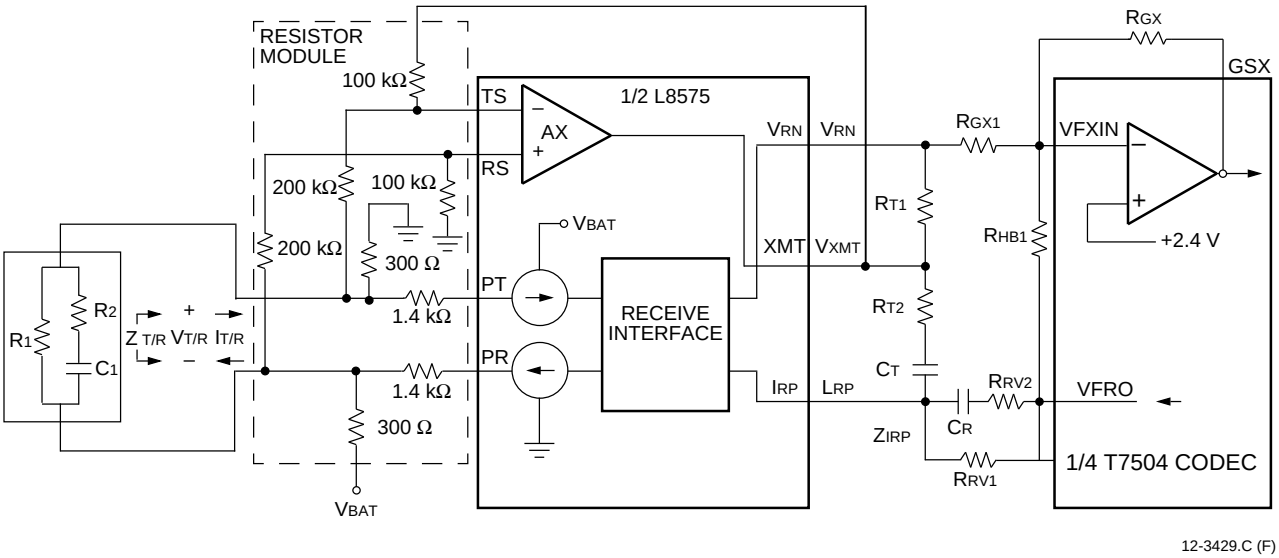


Figure 13. Initial ac Interface for Complex Termination Between L8575 SLIC and T7504 Codec
Note: dc Blocking Capacitors (C_B) Not Shown, C_T and C_R Separate

ac Design (continued)

Design Equations (continued)

The Tip/Ring differential current is given by:

$$I_{T/R} = 200\left(I_{RP} - \frac{V_{RN}}{Z_{IRP}}\right)$$

The voltage at pin XMT is given by:

$$V_{XMT} = \frac{-V_{T/R}}{2}$$

The component values in the ac interface of Figure 13 are calculated (for the transmit and receive gains defined by the respective gain constants K_{RX} and K_{RCV}, and for the termination impedance seen in Figure 12) using the following equations:

$$R_{RV1} = \frac{100R_1'}{K_{RCV}}$$

$$R_{RV2} = \frac{100R_2'}{K_{RCV}}$$

$$C_R = \frac{K_{RCV}C'}{100}$$

$$\frac{R_{GX1}}{R_{GX1} + R_{T1}} = \frac{R_{RV1}}{100}\left(\frac{1}{600} - \frac{1}{R_1'}\right)$$

$600\ \Omega = 2 \times 300\ \Omega$ feed resistors

$$R_{GX} = 2 \times K_{TX}(R_{GX1} + R_{T1})$$

$$C_T = \frac{C'}{100}\left[1 + \frac{R_{GX1}}{R_{T1}}\left(1 + \frac{100R_1'}{R_{RV1}}\right)\right]$$

$$R_{T2} = \frac{R_2'C'}{C_T}$$

The 300 Ω feed resistors contribute 600 Ω to the termination impedance. The termination impedance associated with the circuit in Figure 13 consists of this inherent 600 Ω feeding impedance in parallel with:

- A negative impedance, where,

$$\frac{2}{100} \times \frac{R_{GX1}}{R_{GX1} + R_{T1}}$$

- A positive impedance, where,

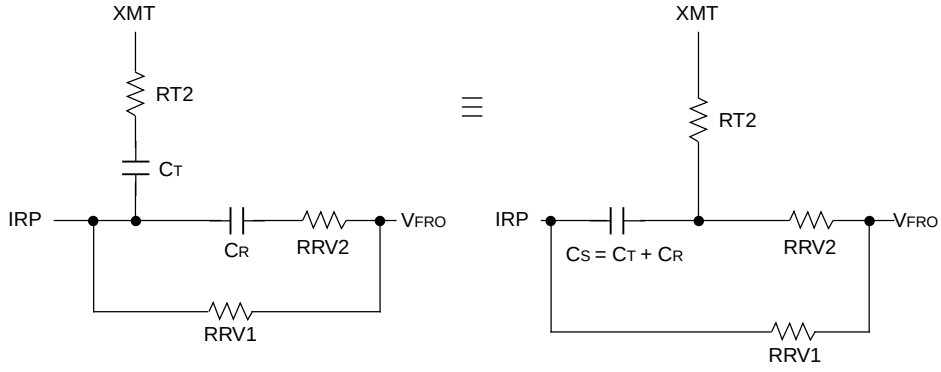
$$\left(R_{T2} + \frac{1}{j\omega C_T}\right) \times \left(\frac{R_{GX1} + R_{T1}}{R_{T1}}\right)$$

The negative and positive impedance terms are used to adjust the termination impedance from the inherent 600 Ω to any complex termination.

Note in the case of a pure 600 Ω dc termination, the two 300 Ω feed resistors provide this termination, and components R_{T1}, R_{T2}, and C_T are not used in the ac interface circuit.

Using the circuit of Figure 13, the ratio of capacitors C_T and C_R will affect the (transmit and receive) gain flatness, and to a lesser degree the return loss of the line circuit. Thus, depending on the requirements, C_T and C_R may need to be tight tolerance capacitors.

If this is the case, capacitors C_T and C_R may be combined into a single capacitor with a looser tolerance. This is illustrated in Figure 14.



12-3426a(F)

Figure 14. Revised ac Interface C_T and C_R Combined into a Single Capacitor C_S

ac Design (continued)

Design Equations (continued)

To scale C_S (higher), increase C_T (and decrease R_{T2}) by increasing the $R_{GX1}/ (R_{GX1} + R_{T1})$ ratio by rearranging the circuit in Figure 13 and by adding resistor R_{SC} from XMT to IRP as shown in the figure below:

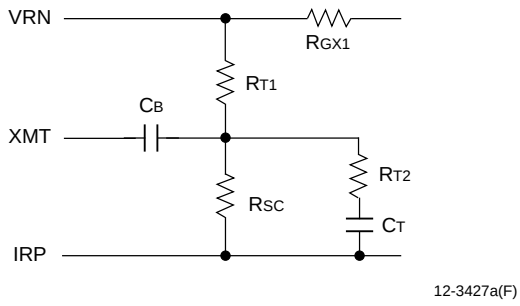


Figure 15. Addition of Resistor R_{SC} from XMT to IRP

Then,

$$\frac{R_{GX1}}{R_{GX1} + R_{T1}} = \frac{(R_{RV1} \| R_{SC})}{100}\left(\frac{1}{600} - \frac{1}{R_1'}\right) + \frac{R_{RV1}}{R_{RV1} + R_{SC}}$$

Once the gains and complex termination are set, if the hybrid balance network is identical to the termination impedance, then the hybrid balance is set by a single resistor (shown in Figure 15) and is computed as follows:

$$R_{HB} = \frac{R_{GX}}{K_{RCV} \times K_{TX}}$$

The L8575 SLIC is ground referenced. However, a +5 V only codec, such as T7504, is referenced to +2.5 V. The L8575 SLIC has sufficient dynamic range to accommodate an ac signal from the codec that is referenced to +2.5 V without clipping distortion.

With a –48 V battery, the dc voltage at node XMT will be a nominal –22 V or $\frac{(V_{TIP} - V_{RING})}{2} - 4$ V. This is the common-mode dc voltage. This will cause a dc current flow from the codec to the SLIC. This current will not affect ac performance, but it will effectively waste power. To avoid this wasted power consumption, blocking capacitors can be added. The blocking capacitors block the dc path from any low impedance node at the codec to SLIC node XMT. Blocking capacitors are added to the application diagram in Figure 16.

After the blocking capacitor C_B is added, the above component values may have to be adjusted slightly to optimize performance.

The effects of the blocking capacitor are best evaluated and optimized by circuit simulation. Contact your Lucent Technologies Microelectronics Group Account Representative for information on availability of a *PSPICE** model.

Figure 16 shows a complete reference design using the L8575 SLIC and T8502/3 codec. This line circuit is designed to meet the requirements of the People's Republic of China. The basic ac design parameters are listed below:

Termination impedance: 200 Ω + 680 Ω || 0.1 μF
Hybrid balance network: 200 Ω + 680 Ω || 0.1 μF
Transmit gain: 0 dB
Receive gain: –3.5 dB or –7.0 dB

Notice that the interface circuit between the L8575 and T8502/3 is designed for a receive gain of –3.5 dB. The T8502 codec offers a pin selectable receive gain of 0 dB or –3.5 dB. Thus, via logic control, a receive gain of either –3.5 dB or 7.0 dB is achieved.

The T8502/3 codec is a dual +5 V only codec. When used with the dual L8575 SLIC, a complete low-cost, dual-line circuit is achieved.

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Application Diagram

The following diagram and table show the basic components required with the L8575 SLIC. Specific component values are given in cases where the value is fixed. In cases where the value may change (i.e., components that determine the ac interface), the value is not listed but equations to determine these values are given later in this document.

Table 16. External Components Required

Comp.	Function	Implementation	Value	Attribute*
R_1	dc Feed Protection	Resistor Module	300 Ω	1.0%, 2 W†
R_2	dc Feed Protection	Resistor Module	300 Ω	1.0%, 2 W†
R_3	Transmit Gain	Resistor Module	100 kΩ	1.0%, 25 mW‡
R_4	Transmit Gain	Resistor Module	100 kΩ	1.0%, 25 mW‡
R_5	Transmit Gain	Resistor Module	200 kΩ	1.0%, 25 mW‡
R_6	Transmit Gain	Resistor Module	200 kΩ	1.0%, 25 mW‡
R_7	Protection	Resistor Module	1.4 kΩ	2.0%, 0.1 W
R_8	Protection	Resistor Module	1.4 kΩ	2.0%, 0.1 W
R_9	Battery Noise Cancellation	Resistor Module	15 kΩ	10 mW§
C_{VCC}	V_{CC} Filter	External	0.1 µF	20%, 10 V
C_{VDD}	V_{DD} Filter	External	0.1 µF	20%, 10 V
C_{BAT}	V_{BAT} Filter	External	0.1 µF	20%, 100 V
R_{CBN}	Battery Noise Cancellation	External	301 kΩ	1%, 1/16 W
C_{CBN}	Battery Noise Cancellation	External	0.1 µF	20%, 100 V
C_{RF}	Ring Trip	External	0.1 µF	20%, 100 V
R_{RF1}	Ring Trip	External	1 MΩ	20%, 100 V
R_{RF2}	Ring Trip	External	1 MΩ	1%, 1/16 W
R_{RTH}	Ring Trip Threshold	External	11 MΩ	1%, 1/16 W
C_{FLTA}	Fault Filter	External	0.1 µF	20%, 100 V
C_{B1}	dc Blocking	External	0.1 µF	20%, 50 V
C_{B2}	dc Blocking	External	0.1 µF	20%, 50 V
R_{T1}	ac Interface	External	34 kΩ	1%, 1/32 W
R_{T2}	ac Interface	External	7.32 kΩ	1%, 1/32 W
R_{GX}	ac Interface	External	150 kΩ	1%, 1/32 W
R_{GX1}	ac Interface	External	52.3 kΩ	1%, 1/32 W
R_{RV1}	ac Interface	External	113 kΩ	1%, 1/32 W
R_{RV2}	ac Interface	External	35.7 kΩ	1%, 1/32 W
C2 or C_S	ac Interface	External	2.7 nF	5%, 10 V
R_{HB1}	ac Interface	External	221 kΩ	1%, 1/32 W

* Power is continuous RMS power.

† $R_1/R_2 = 1$, with a tolerance of 0.35% for 50 dB longitudinal balance, 0.2% for 58 dB longitudinal balance. Fuses on F1 and F2 provide fail-safe operation if excessive overvoltage conditions exist on Tip and Ring. They will not operate if the total power dissipation of the entire resistor network is >5.0 W at 85 °C.

‡ $(R_3 \times R_6)/(R_4 \times R_5) = 1$ with a tolerance of 0. 35% for 50 dB longitudinal balance, 0.2% for 58 dB longitudinal balance.

§ $R_9/R_1 = 100$ with a tolerance of 0.5%.

Application Diagram (continued)

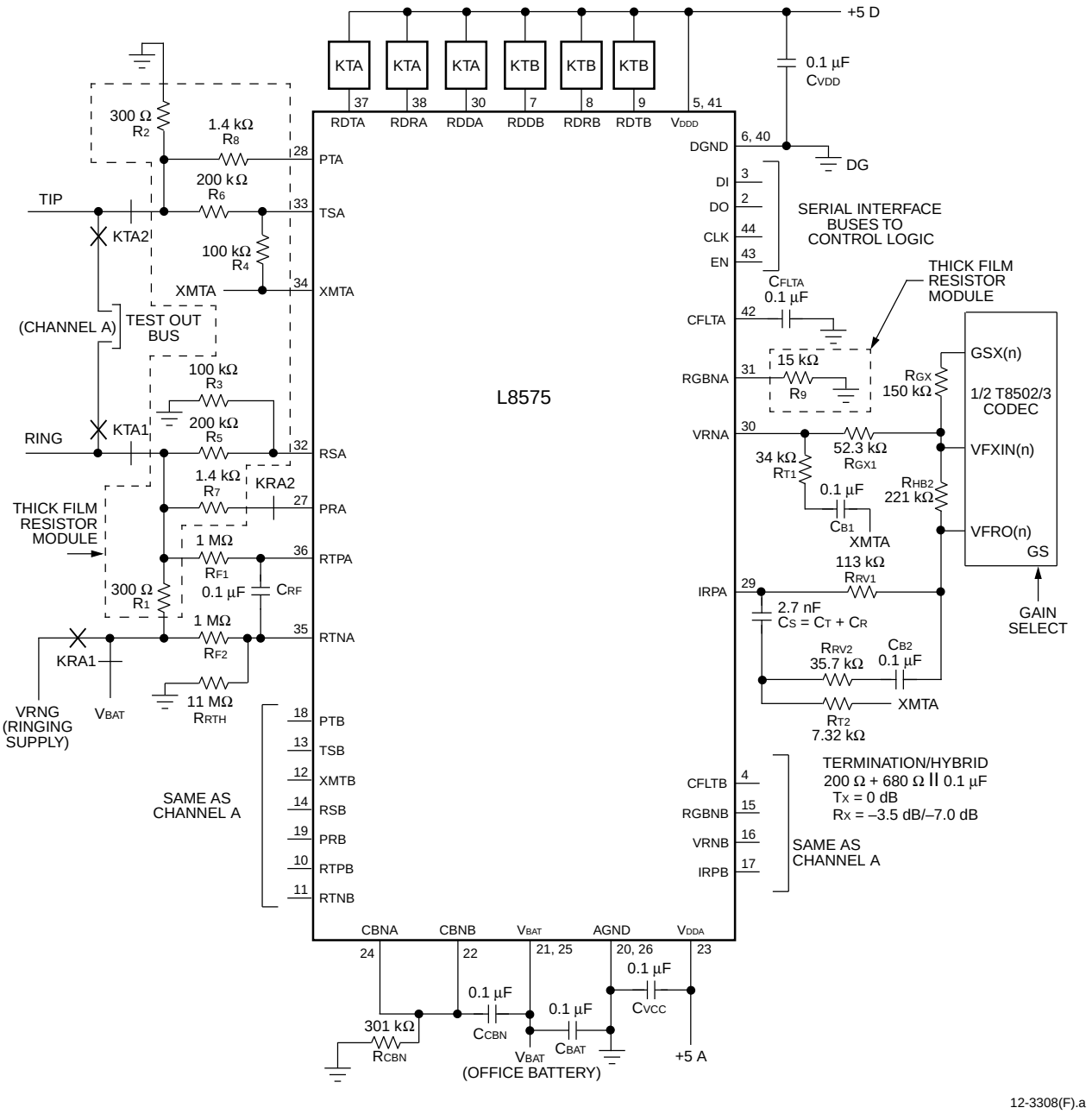
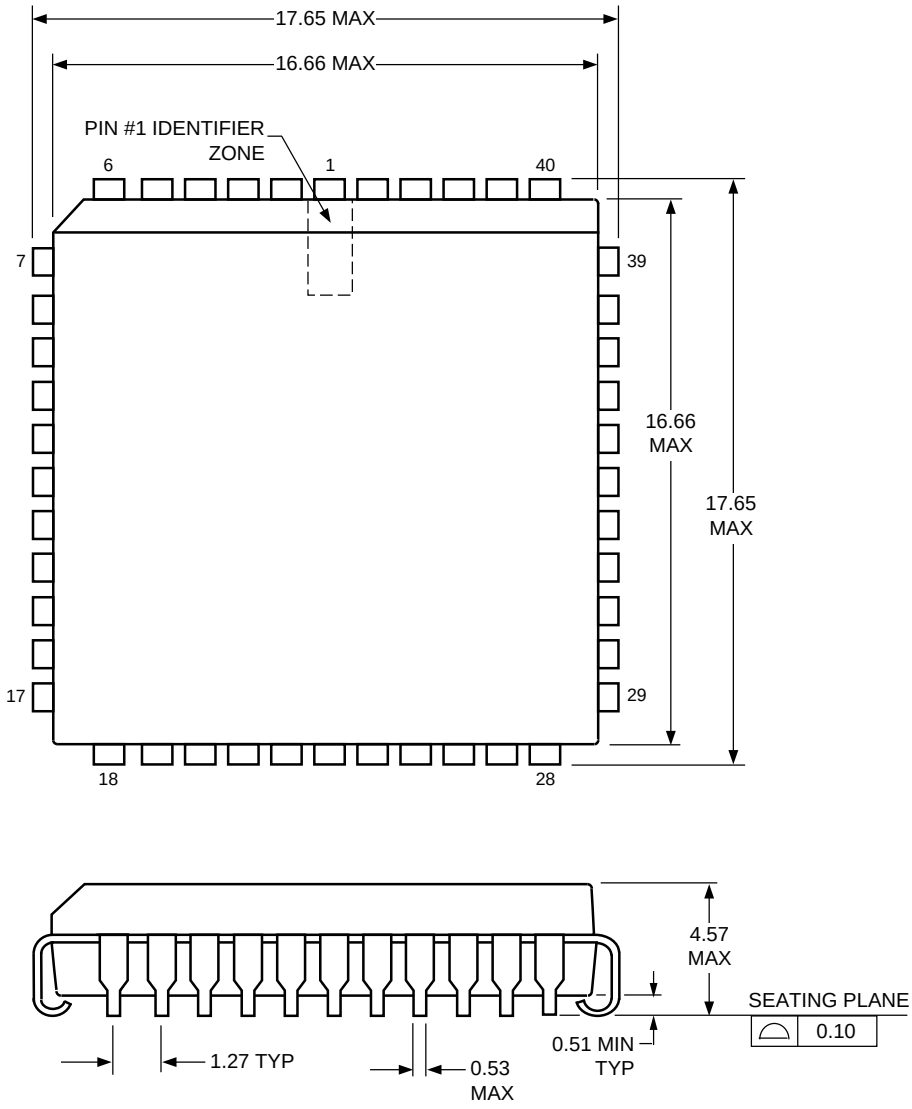


Figure 16. Typical Application Diagram with Blocking Capacitors (C_B) Included

Outline Diagram

44-Pin PLCC

Dimensions are in millimeters.



5-2506r7

Ordering Information

Device Part No.	Description	Package	Comcode
LUCL8575 BP	Dual-Resistive SLIC	44-pin PLCC	107890386
LUCL8575 BP-TR	Dual-Resistive SLIC	44-pin PLCC (Tape & Reel)	107890394

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