MPM3606A

21V/0.6A DC/DC Module Synchronous Step-Down Converter with Integrated Inductor

The Future of Analog IC Technology®

DESCRIPTION

The MPM3606A is a synchronous rectified, step-down module converter with built-in power MOSFETs, inductor, and two capacitors. It offers a compact solution that requires only 5 external components to achieve a 0.6A continuous output current with excellent load and line regulation over a wide input-supply range. Also, it provides fast load transient response.

Full protection features include over-current protection (OCP) and thermal shutdown (TSD).

MPM3606A eliminates design and manufacturing risks while dramatically improving time-to-market.

The MPM3606A is available in a space-saving QFN20 (3mmx5mmx1.6mm) package.

FEATURES

- 4.5V-to-21V Operating Input Range
- 0.6A Continuous Load Current
- 100mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Integrated Inductor
- Integrated VCC and Bootstrap Capacitors
- Power-Save Mode at Light Load
- Power Good Indicator
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in QFN20 (3x5x1.6mm) Package
- Total solution size 6.7mm x7.3mm

APPLICATIONS

- Industrial Controls
- Medical and Imaging Equipment
- Telecom and Networking Applications
- LDO Replacement
- Space and Resource-limited Applications

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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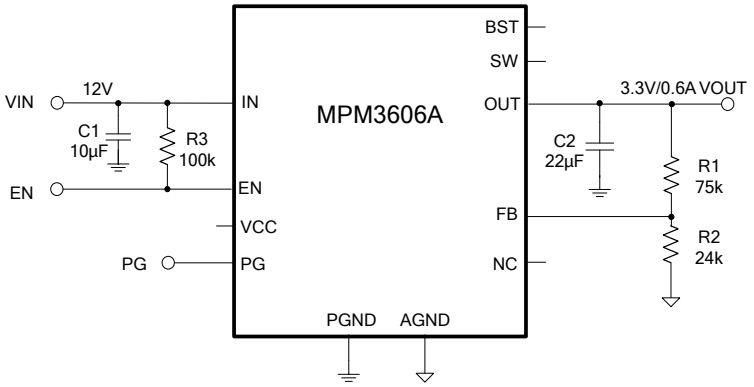
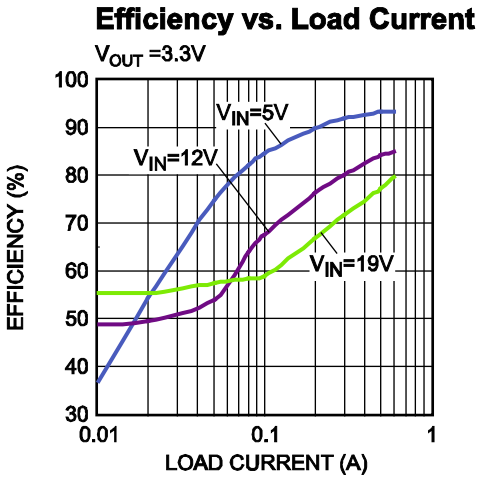
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3606AGQV	QFN-20 (3mmx5mmx1.6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPM3606AGQV–Z);

TOP MARKING

MPYW
3606
ALLL
M

MP: MPS prefix:
Y: year code;
W: week code:
3606A: first five digits of the part number;
LLL: lot number;
M: module;

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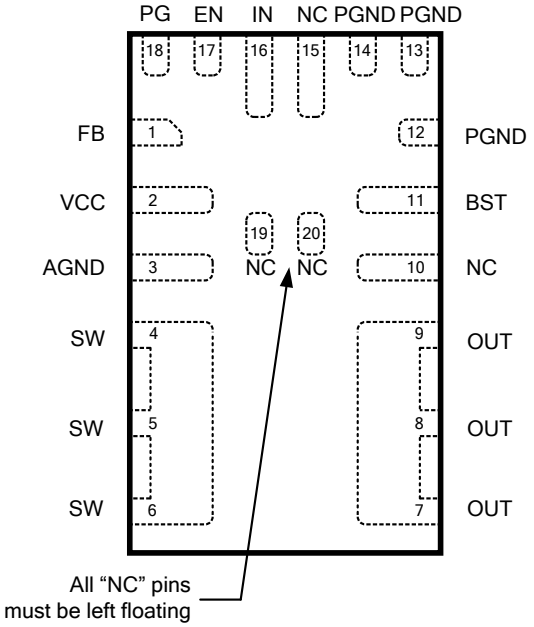
PACKAGE REFERENCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 28V
V_{SW} .....
-0.3V (-5V for <10ns) to 28V (30V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins..... -0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
.....2.7W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 21V
Output Voltage V_{OUT}.....0.8V to V_{IN}*D_{MAX}(5)
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-20 (3mmx5mmx1.6mm). 46..... 10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to page 14, Enable control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) In practical design, the minimum V_{OUT} is limited by minimum on time, 50ns on time is commonly recommended for calculating to give some margin. For output voltage setting above 5.5V, please refer to the application information on page 17.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C to +125°C[7], typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_s	V_{EN} = 0V, T_J =+25°C		6.5	8	μA
		V_{EN} = 0V, T_J =-40°C to +125°C		6.5	9	μA
Supply Current (Quiescent)	I_q	V_{FB} = 1V, T_J =+25°C		0.3	0.39	mA
		V_{FB} = 1V, T_J =-40°C to +125°C		0.3	0.44	mA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		100		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V		50		mΩ
Integrated Inductor Inductance[8]	L			1		μH
Inductor DC Resistance	L_{DCR}			60		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit	I_{LIMIT}	Under 40% Duty Cycle	1.7	2.4		A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V, T_J =+25°C	1600	2000	2400	kHz
		V_{FB}=0.75V, T_J =-40°C to +125°C	1500	2000	2500	kHz
Fold-Back Frequency	f_{FB}	V_{FB}=200mV		0.3		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV, T_J =+25°C	78	83	88	%
		V_{FB}=700mV, T_J =-40°C to +125°C	77	83	89	%
Minimum On Time[8]	τ_{ON_MIN}			30		ns
Feedback Voltage	V_{FB}	T_J =25°C	786	798	810	mV
		T_J =-40°C to +125°C	782	798	814	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
EN Rising Threshold	V_{EN_RISING}	T_J =+25°C	1.2	1.4	1.6	V
		T_J =-40°C to +125°C	1.15	1.4	1.65	V
EN Falling Threshold	$V_{EN_FALLING}$	T_J =+25°C	1.05	1.25	1.4	V
		T_J =-40°C to +125°C	1	1.25	1.45	V
EN Input Current	I_{EN}	V_{EN}=2V, T_J =+25°C	2	2.3	2.6	μA
		V_{EN}=2V, T_J =-40°C to +125°C	1.8	2.3	2.8	μA
Power Good Rising Threshold	PG_{VTH-Hi}	T_J =+25°C	0.86	0.9	0.95	V_{FB}
Power Good Falling Threshold	PG_{VTH-LO}	T_J =+25°C	0.78	0.83	0.88	V_{FB}
Power Good Rising Delay	PG_{TD_RSING}	T_J =+25°C	15	35	55	μs
		T_J =-40°C to +125°C	10	35	60	μs
Power Good Falling Delay	$PG_{TD_FALLING}$	T_J =+25°C	40	80	125	μs
		T_J =-40°C to +125°C	30	80	135	μs
Power Good Sink Current Capability	V_{PG}	Sink 1mA			0.4	V
Power Good Leakage Current	$I_{PG-LEAK}$	V_{PG}=6V			1	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN}=12V, T_J=-40°C to +125°C, typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN Under-Voltage Lockout Threshold—Rising	$INUV_{Vth}$	T_J =+25°C	3.7	3.9	4.1	V
		T_J =-40°C to +125°C	3.65	3.9	4.15	V
VIN Under-Voltage Lockout Threshold—Hysteresis	$INUV_{HYS}$		600	675	750	mV
VCC Regulator	V_{CC}	T_J =+25°C	4.75	4.9	5.05	V
		T_J =-40°C to +125°C	4.7	4.9	5.1	V
VCC Load Regulation		I_{CC}=5mA		1.5	3	%
Soft-Start Time	t_{SS}	V_{OUT} from 10% to 90%, T_J =+25°C	0.8	1.6	2.4	ms
		V_{OUT} from 10% to 90%, T_J =-40°C to +125°C	0.6	1.6	2.6	ms
Thermal Shutdown (8)	T_{SD}			150		°C
Thermal Hysteresis (8)	T_{SD_HYS}			20		°C

Notes:
7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by characterization test.

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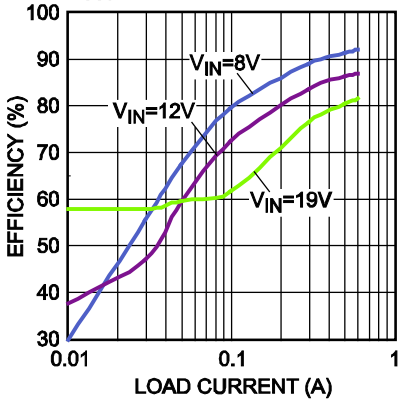
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

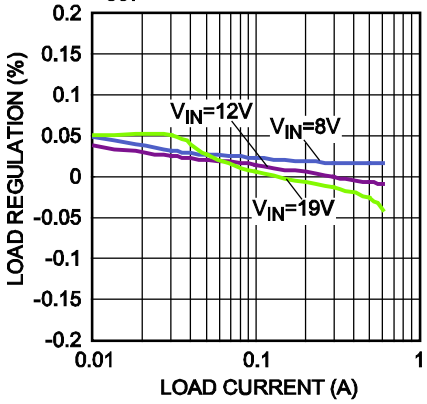
Efficiency vs. Load Current

V_{OUT} =5V



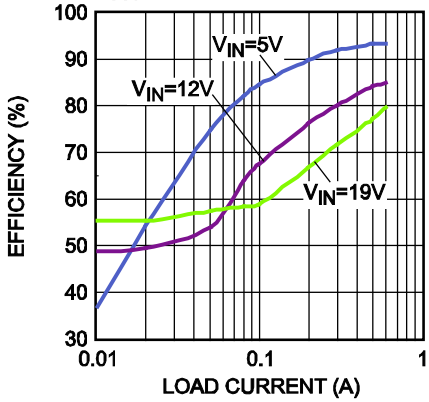
Load Regulation

V_{OUT} =5V



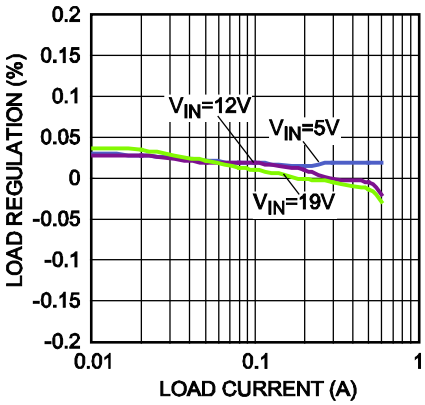
Efficiency vs. Load Current

V_{OUT} =3.3V



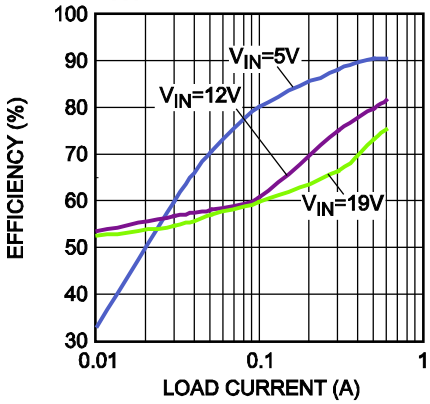
Load Regulation

V_{OUT} =3.3V



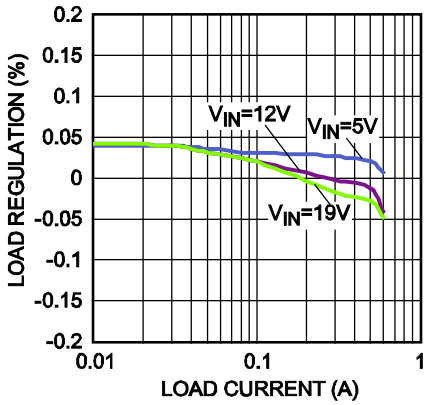
Efficiency vs. Load Current

V_{OUT} =2.5V



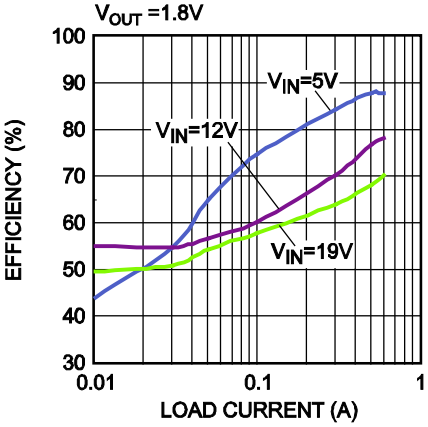
Load Regulation

V_{OUT} =2.5V



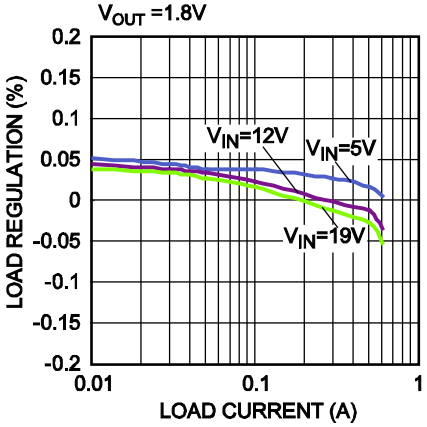
Efficiency vs. Load Current

V_{OUT} =1.8V



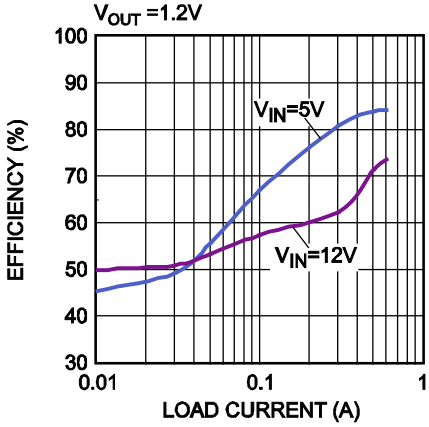
Load Regulation

V_{OUT} =1.8V



Efficiency vs. Load Current

V_{OUT} =1.2V



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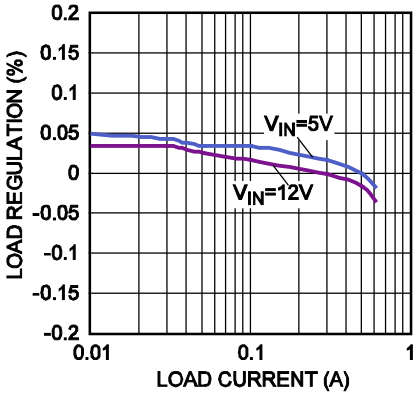
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

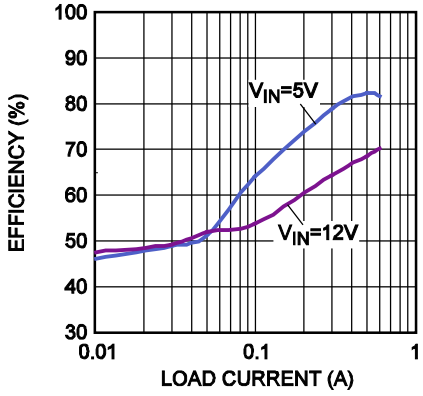
Load Regulation

V_{OUT} =1.2V



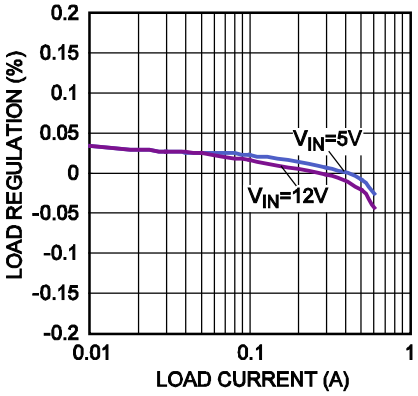
Efficiency vs. Load Current

V_{OUT} =1V



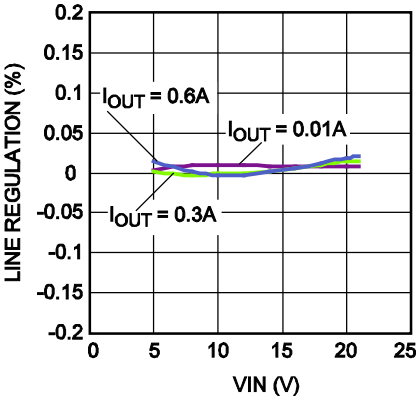
Load Regulation

V_{OUT} =1V

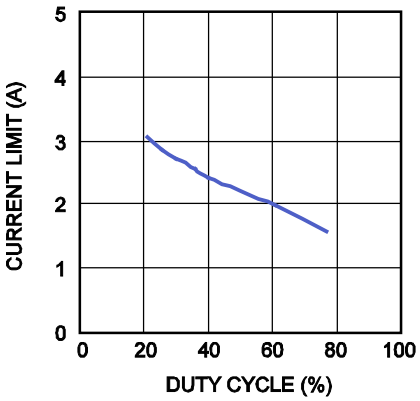


Line Regulation

V_{IN}=5V-21V, V_{OUT} =3.3V

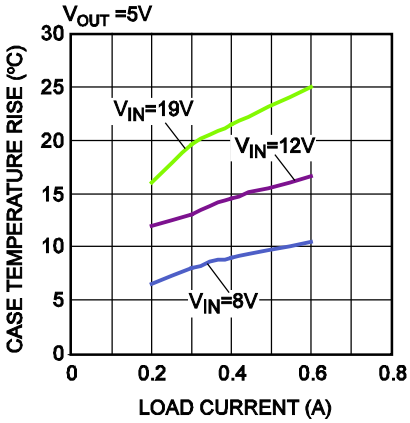


Inductor Peak-Current Limit vs. Duty Cycle



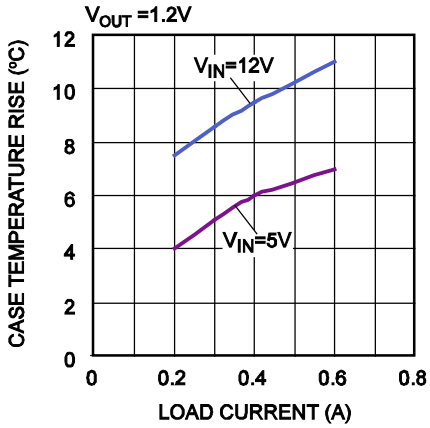
Case Temperature Rise vs. Output Current

V_{OUT} =5V



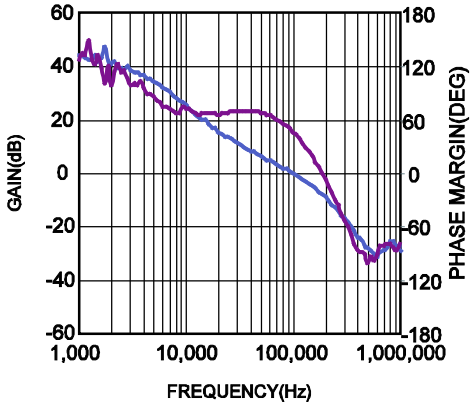
Case Temperature Rise vs. Output Current

V_{OUT} =1.2V



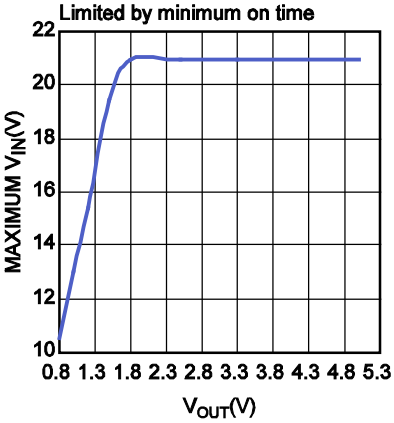
Bode Plot

I_{OUT} =0.6A



Maximum Input Voltage for a Certain Output Voltage

Limited by minimum on time



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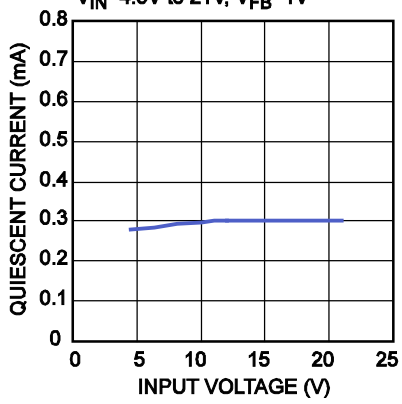
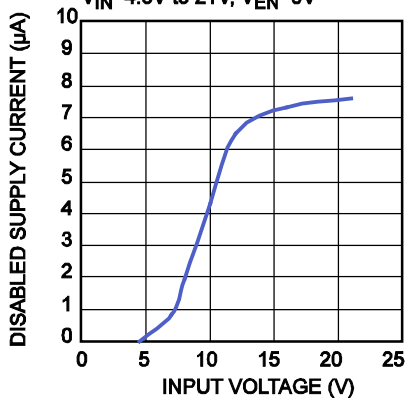
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

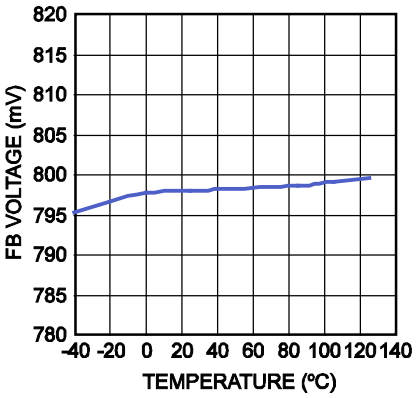
Quiescent Current vs. Input Voltage
V_{IN}=4.5V to 21V, V_{FB}=1V



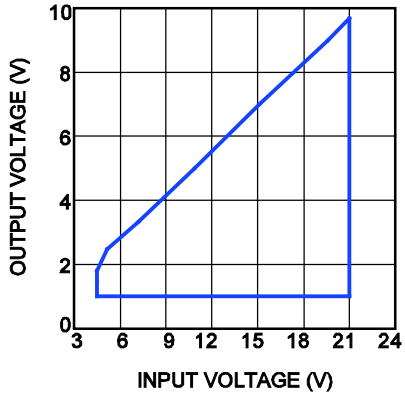
Disabled Supply Current vs. Input Voltage
V_{IN}=4.5V to 21V, V_{EN}=0V



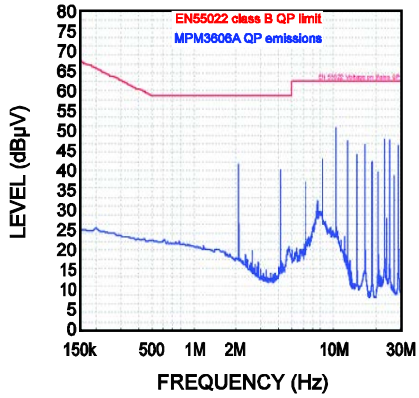
FB Voltage vs. Temperature



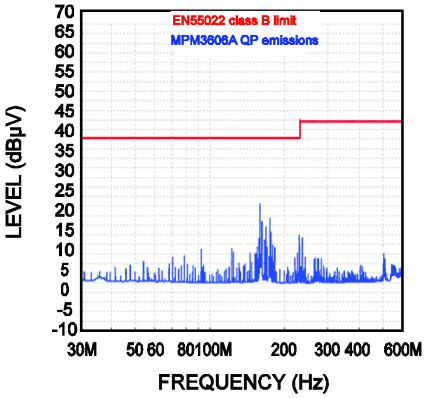
Power-Save Mode Range
Recommend operating the device within this range for optimal power save



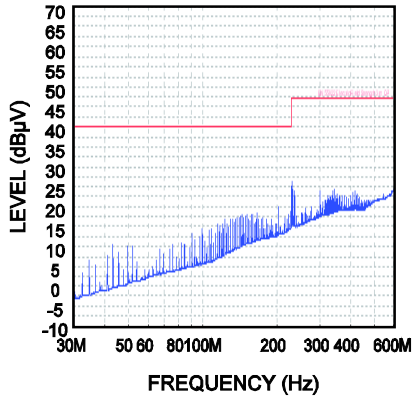
Conduction-EMI
I_{OUT}=0.6A
C_{IN}=64µF+10nF/0402



Radiated-EMI
I_{OUT}=0.6A
C_{IN}=64µF+10nF/0402



Radiated-EMI with RC Snubber
R_S=5.6Ω, C_S=330pF, I_{OUT}=0.6A



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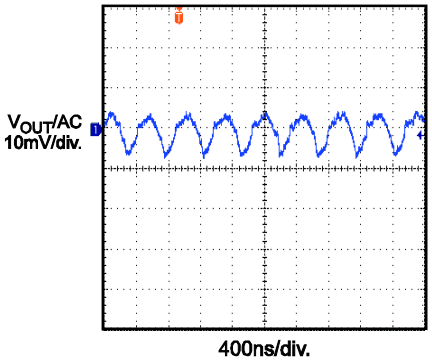
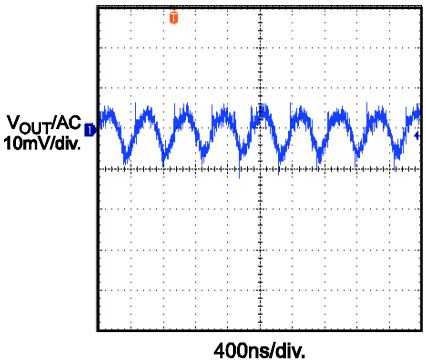
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

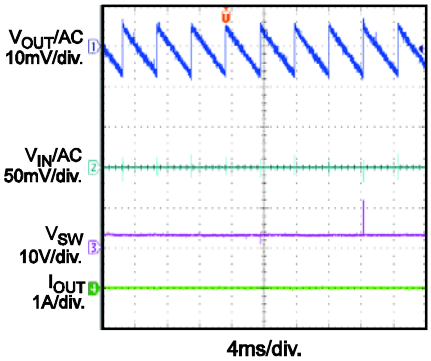
Output Ripple
Bandwidth=20MHz,
I_{OUT} = 0.6A



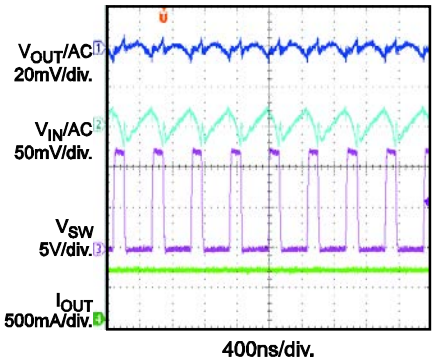
Output Ripple
Bandwidth=150MHz,
I_{OUT} = 0.6A



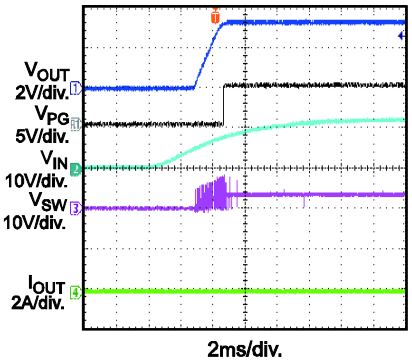
Input/Output Ripple
I_{OUT} = 0A



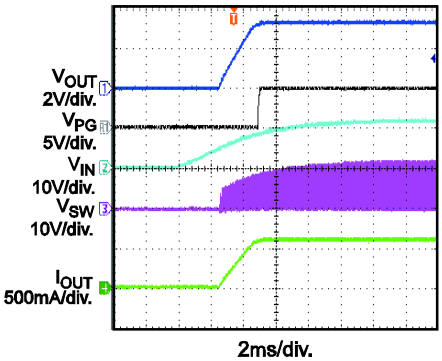
Input/Output Ripple
I_{OUT} = 0.6A



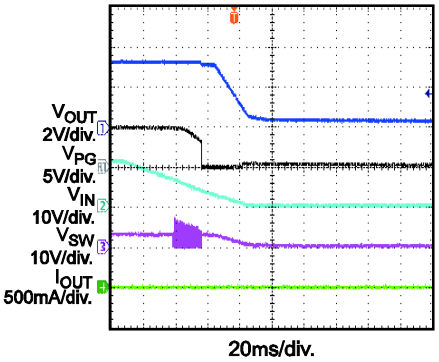
Start-Up through Input Voltage
I_{OUT} = 0A



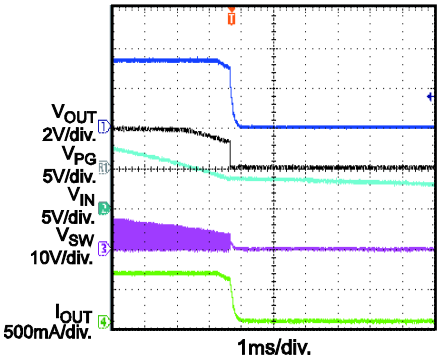
Start-Up through Input Voltage
I_{OUT} = 0.6A



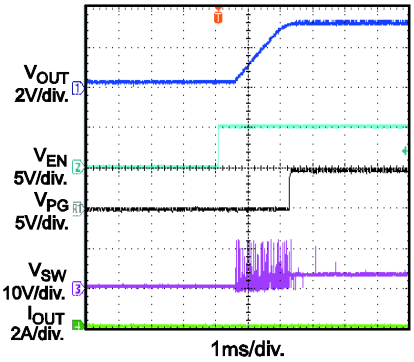
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 0.6A



Start-Up through Enable
I_{OUT} = 0A



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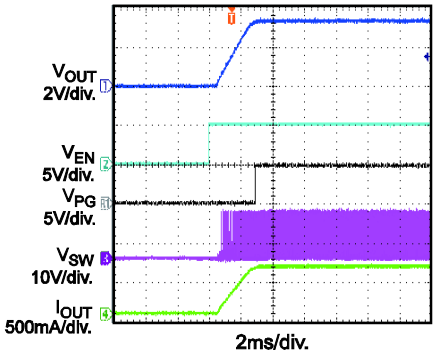
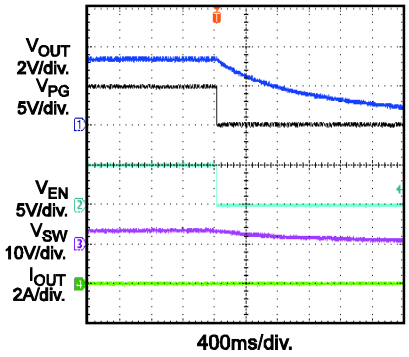
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

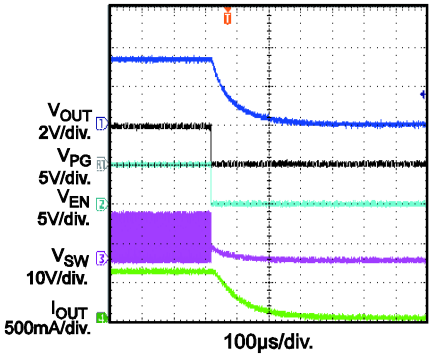
Start-Up through Enable
I_{OUT} = 0.6A



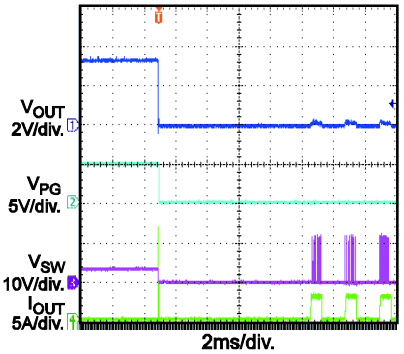
Shutdown through Enable
I_{OUT} = 0A



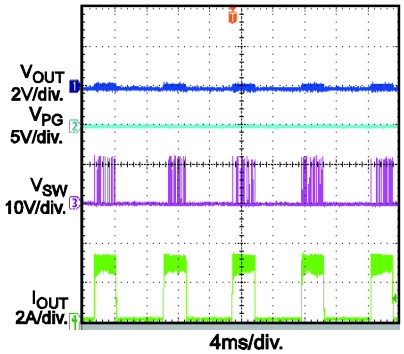
Shutdown through Enable
I_{OUT} = 0.6A



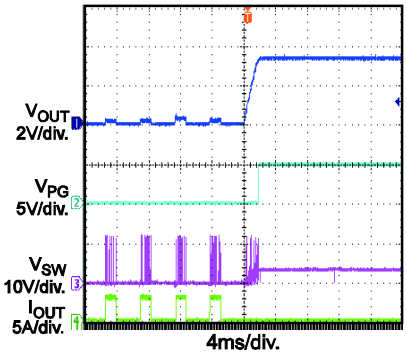
Short-Circuit Entry



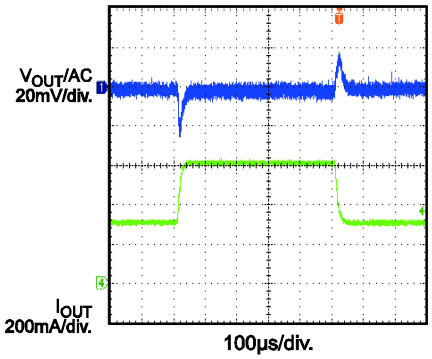
Short-Circuit Steady State



Short-Circuit Recovery



Load Transient Response
I_{OUT} = 0.3A to 0.6A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	Feedback. Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. To prevent current-limit runaway during a short-circuit fault, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
2	VCC	Internal 4.9V LDO output. The module integrates a LDO output capacitor, so there is no need to add an external capacitor.
3	AGND	Analog Ground. Reference ground of logic circuit. AGND is connected internally to PGND, so there is no need to add any external connections to PGND.
4, 5, 6	SW	Switch Output. Large copper plane is recommended on pins 4, 5 and 6 to improve thermal performance.
7, 8, 9	OUT	Power Output. Connect the load to OUT; an output capacitor is needed.
10, 15, 19, 20	NC	DO NOT CONNECT. NC must be left floating.
11	BST	Bootstrap. A bootstrap capacitor is integrated internally, so an external connection is not needed.
12, 13, 14	PGND	Power Ground. Reference ground of the power device. PCB layout requires extra care, please refer to PCB guideline recommendations. For best results, connect to PGND with copper and vias.
16	IN	Supply Voltage. IN supplies power to the internal MOSFET and regulator. The MPM3606A operates from a +4.5V to +21V input rail. It requires a low-ESR, and low-inductance capacitor to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
17	EN	Enable. Pull EN high to enable the module. Leave EN floating or connect it to GND to disable the module.
18	PG	Power Good Indicator. PG is an open-drain output. Connect PG to VCC (or another voltage source) through a pull-up resistor (e.g. 100kΩ). Additional details on PG behavior can be found in the OPERATION section under “Power Good Indicator.”

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FUNCTIONAL BLOCK DIAGRAM

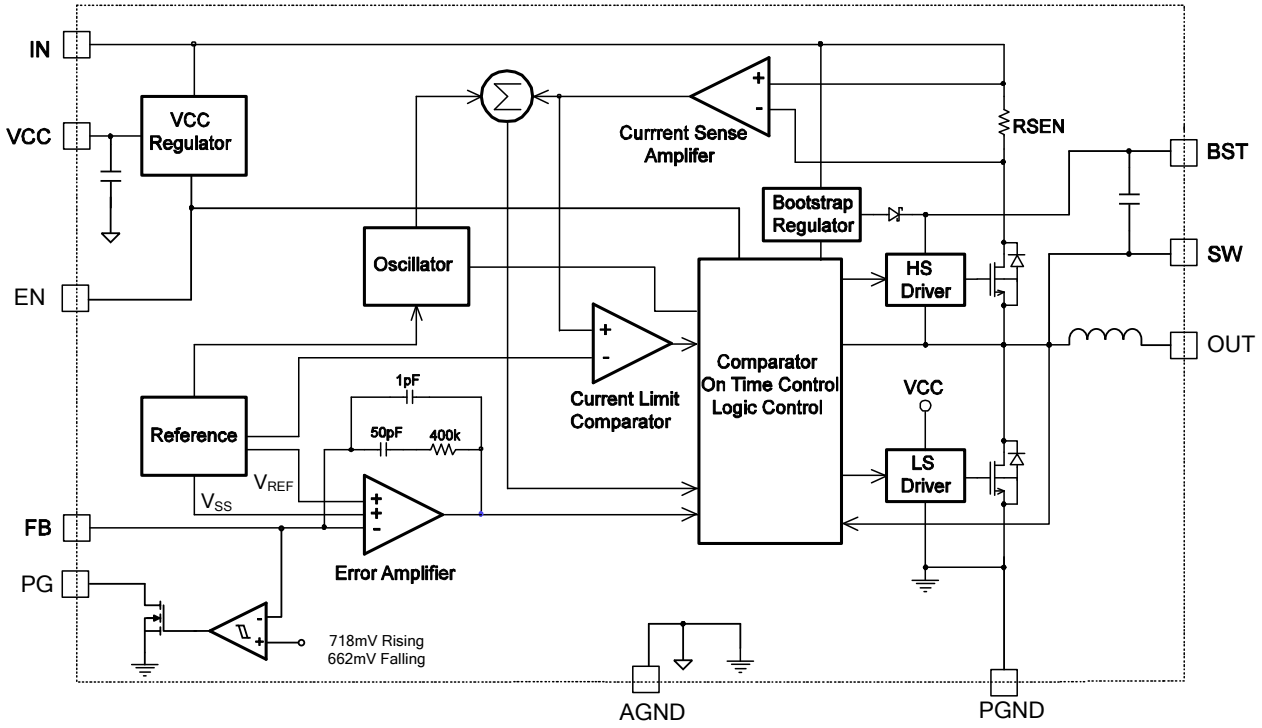

Figure 1. Functional Block Diagram

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OPERATION

The MPM3606A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs, integrated inductor, and two capacitors. It offers a compact solution that achieves a 0.6A continuous output current with excellent load and line regulation over a 4.5V to 21V input-supply range.

The MPM3606A has three working modes: advanced asynchronous modulation (AAM), similar to PFM mode, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The load current increases as the device transitions from AAM mode to DCM to CCM. In particular conditions, the device will not enter AAM mode during a light-load condition (See Power-Save Mode Range graph on page 8).

AAM Control Operation

In a light-load condition, MPM3606A operates in AAM mode (see Figure 2). The V_{AAM} is an internally fixed voltage when input and output voltages are fixed. V_{COMP} is the error amplifier output, which represents the peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked. This will make the MPM3606A skips pulses, achieving the light-load power save. Refer to AN032 for additional detail.

The internal clock re-sets every time V_{COMP} exceeds V_{AAM}. Simultaneously, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12V input applications.

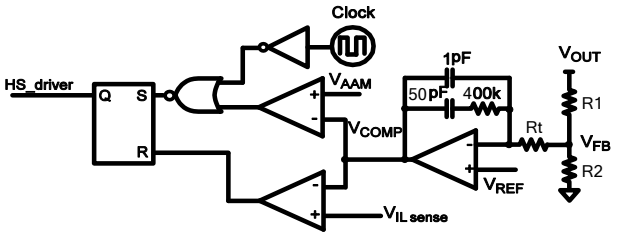

Figure 2. Simplified AAM Control Logic

DCM Control Operation

The V_{COMP} ramps up as the output current increases. When its minimum value exceeds V_{AAM}, the device enters DCM. In this mode, the internal 2MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and then the low-side MOSFET (LS-FET) turns on and remains on until the inductor-current value decreases to zero. The device repeats the same operation in every clock cycle to regulate the output voltage (see Figure 3).

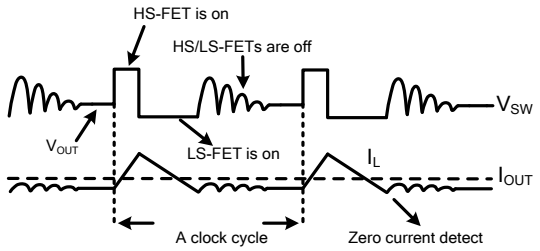

Figure 3. DCM Control Operation

CCM Control Operation

The device enters CCM from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM, the internal 2MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and then the LS-FET turns on and remains on until the next clock cycle starts. The device repeats the same operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 83% of one PWM period, the HS power MOSFET will be forced off.

Internal V_{CC} Regulator

A 4.9V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the output of the regulator is in full regulation. If V_{IN} is less than 4.9V, the output decreases. The device integrates an internal decoupling capacitor, so adding an external VCC output capacitor is unnecessary.

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Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.798V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage; the COMP voltage controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient input-supply voltage. The MPM3606A UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.9V while its falling threshold is 3.225V.

Enable Control (EN)

EN turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 870kΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 6.5V series-Zener-diode (see Figure 4). Connecting EN to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

Connecting the EN input through a pull-up resistor to the voltage on V_{IN} limits the EN input current to less than 100µA.

For example, with 12V connected to V_{IN}, R_{PULLUP} ≥ (12V – 6.5V) ÷ 100µA = 55kΩ.

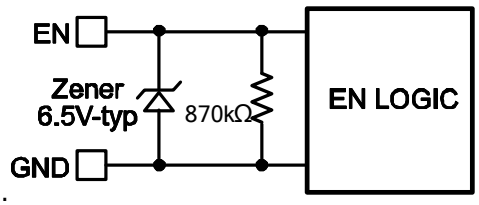

Figure 4. 6.5V Zener Diode Connection

Internal Soft-Start (SS)

Soft-start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 4.9V. When SS is lower than V_{REF}, the error amplifier uses SS as the reference. When SS is higher than V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set internally to 1.6ms (V_{OUT} from 10% to 90%).

Pre-Bias Start-Up

The MPM3606A is designed for a monotonic start-up into a pre-biased output voltage. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft-start capacitor is charged. When the soft-start capacitor's voltage exceeds the sensed output voltage at FB, the device turns on the HS-FET and the LS-FET sequentially. Output voltage ramps up following the soft-start slew rate.

Power Good Indicator (PG)

The MPM3606A has power good (PG) output to indicate whether the output voltage of the module is ready. PG is an open-drain output. Connect PG to VCC (or another voltage source) through a pull-up resistor (e.g. 100kΩ). When the input voltage is applied, PG is pulled down to GND before internal V_{SS}>1V. After V_{SS}>1V, when V_{FB} is above 90% of V_{REF}, PG is pulled high (after a 35µs delay time). During normal operation, PG is pulled low when the V_{FB} drops below 83% of V_{REF} (after a 80µs delay).

When UVLO or OTP occurs, PG is pulled low immediately; when OC (over-current) occurs, PG is pulled low when V_{FB} drops below 83% of V_{REF} (after a 80µs delay).

Since MPM3606A doesn't implement dedicated output over-voltage protection, the PG won't response to an output over-voltage condition.

Over-Current-Protection and Hiccup

The MPM3606A has a cycle-by-cycle over-current limiting control. When the inductor current-peak value exceeds internal peak current-limit threshold, the HS-FET turns off and the LS-FET turns on, remaining on until the inductor current falls below the internal valley current-limit threshold. The valley current-limit circuit is employed to decrease the

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operation frequency (after the peak current-limit threshold is triggered). Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (50% below the reference, typically). Once UV is triggered, the MPM3606A enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead-shorted to ground and greatly reduces the average short-circuit current to alleviate thermal issues and protect the converter. The MPM3606A exits hiccup mode once the over-current condition is removed.

Thermal Shutdown (TSD)

To prevent thermal damage, MPM3606A stops switching when the die temperature exceeds 150°C. As soon as the temperature drops below its lower threshold (130°C, typically), the power supply resumes operation.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1 and C2 (see Figure 5). If (V_{BST}-V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V voltage across C4.

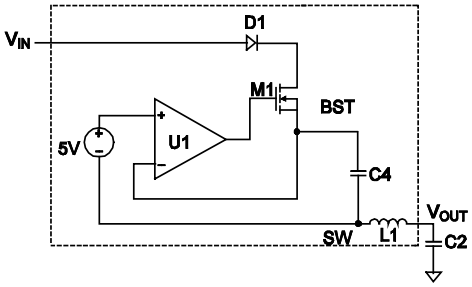

Figure 5. Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events shut down the chip: V_{IN} low, V_{EN} low and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Additional RC Snubber Circuit

An additional RC snubber circuit can be chosen to clamp the voltage spike and damp the ringing voltage for better EMI performance.

The power dissipation of the RC snubber circuit is estimated by the formula below:

$$P_{Loss} = f_S \times C_S \times V_{IN}^2$$

Where f_S is the switching frequency, C_s is the snubber capacitor, and V_{IN} is the input voltage.

For improved efficiency, the value of C_S should not be set too high. Generally, a 5.6Ω R_S and a 330pF C_S are recommended to generate the RC snubber circuit (see Figure 6).

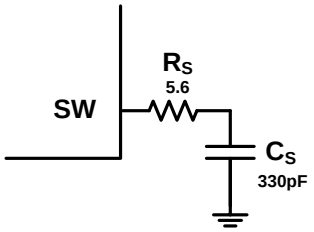

Figure 6. Additional RC Snubber Circuit

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). Choose R1 (see Table 1); R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.798V} - 1}$$

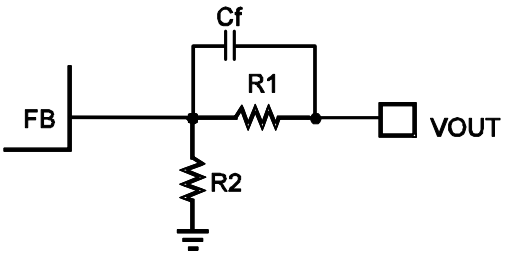

Figure 7. Feedback Network

See Table 1 and Figure 7 for the feedback network and a list of recommended feedback network parameters for common output voltages.

Table 1. Recommended Parameters for Common Output Voltages

		Small Solution Size(C_{IN}=10µF/0805/25V, C_{OUT}=22µF/0805/16V)				Low V_{OUT} Ripple(C_{IN}=10µF/0805/25V, C_{OUT}=2X22µF/0805/16V)			
V_{IN} (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV)(9)	R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV)(9)
21	5	115	22	NS	17.6	40.2	7.68	NS	9.4
	3.3	102	32.4	NS	12.4	62	19.6	NS	7
	2.5	102	47.5	5.6	10	62	29.4	5.6	5.2
19	5	115	22	NS	16.4	40.2	7.68	NS	8.8
	3.3	102	32.4	NS	11.4	62	19.6	NS	6.6
	2.5	102	47.5	5.6	9.8	62	29.4	5.6	5
16	5	115	22	NS	15.6	40.2	7.68	NS	7.8
	3.3	102	32.4	NS	10.6	62	19.6	NS	6
	2.5	102	47.5	5.6	9.6	62	29.4	5.6	4.8
	1.8	102	82	5.6	8.6	62	49.9	5.6	4
14	5	115	22	NS	14.8	40.2	7.68	NS	7.4
	3.3	102	32.4	NS	10.2	40.2	12.7	NS	5.6
	2.5	75	34.8	5.6	9.4	40.2	18.7	5.6	4.6
	1.8	102	82	5.6	8.4	62	49.9	5.6	4.2
	1.5(10)	158	180	5.6	7.2	62	69.8	5.6	3.6
12	5	100	19.1	NS	13.8	34	6.49	NS	6.4
	3.3	75	24	NS	9.4	40.2	12.7	NS	5.2
	2.5	75	34.8	5.6	9	40.2	18.7	5.6	4.4
	1.8	102	82	5.6	7.8	47	37.4	5.6	4
	1.5(10)	158	180	5.6	6.6	47	53.6	5.6	3.4
	1.2(10)	158	316	5.6	6.2	75	147	5.6	3

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Table 1: Recommended Parameters For Common Output Voltages *(continued)*

		Small Solution Size(C_{IN}=10µF/0805/25V, C_{OUT}=22µF/0805/16V)				Low V_{OUT} Ripple(C_{IN}=10µF/0805/25V, C_{OUT}=2X22µF/0805/16V)			
V_{IN} (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV) (9)	R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV) (9)
10	5	100	19.1	NS	13.2	34	6.49	NS	6.2
	3.3	75	24	NS	8.4	40.2	12.7	NS	4.8
	2.5	75	34.8	5.6	8.2	40.2	18.7	5.6	4
	1.8	75	59	5.6	7.2	47	37.4	5.6	3.6
	1.5	102	115	5.6	6	47	53.6	5.6	3.2
	1.2(10)	102	205	5.6	5.4	62	124	5.6	2.8
	1(10)	102	402	5.6	4.8	82	324	5.6	2.6
8	5	100	19.1	NS	9.2	34	6.49	NS	5
	3.3	75	24	NS	7.6	40.2	12.7	NS	3.8
	2.5	75	34.8	5.6	7	40.2	18.7	5.6	3.4
	1.8	75	59	5.6	6.4	47	37.4	5.6	3
	1.5	75	84.5	5.6	5.4	47	53.6	5.6	2.8
	1.2(10)	75	147	5.6	5	47	93.1	5.6	2.6
	1(10)	75	294	5.6	4.6	56	221	5.6	2.2
5	3.3	75	24	NS	6	40.2	12.7	NS	3.4
	2.5	75	34.8	5.6	5.8	40.2	18.7	5.6	3.2
	1.8	75	59	5.6	5.2	47	37.4	5.6	2.8
	1.5	62	69.8	5.6	5	47	53.6	5.6	2.4
	1.2(10)	62	124	5.6	4.6	47	93.1	5.6	2.2
	1(10)	62	243	5.6	4.4	47	187	5.6	2

Notes:

9) The output voltage ripple is tested at 0.6A output current.
10) In these specs, BST operation current will charge the output voltage higher than the setting value when completely no load due to large divider resistor value. 10µA load current is able to pull the output voltage to normal regulation level.

Normally, it is recommended to set output voltage from 0.8V to 5.5V. However, it can be set higher than 5.5V. In this case, the output-voltage ripple is larger due to a larger inductor ripple current. An additional output capacitor is needed to reduce the output-ripple voltage.

If output voltage is high, heat dissipation becomes more important. Refer to PC board layout guidelines on page 18 to achieve better thermal performance.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for improved performance. Use ceramic capacitors with X5R or X7R dielectrics for optimum results because of their low ESR and small temperature coefficients. For most applications, use a 10µF capacitor.

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Since C1 absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor is estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, make sure they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input-voltage ripple caused by capacitance can be estimated as:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output-voltage ripple low. The output-voltage ripple is estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor, and L_1=1μH.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency; the capacitance causes the majority of the output-voltage ripple. For simplification, the output-voltage ripple is estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple is approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor affect the stability of the regulation system. The MPM3606A internal compensation is optimized for a wide range of capacitance and ESR values.

PC Board Layout [11]

Efficient PCB layout is critical to achieve stable operation, particularly for input capacitor placement. For best results, refer to figure 8, and follow the guidelines below:

1. Use large ground plane to connect directly to PGND. Add vias near the PGND if the bottom layer is ground plane.
2. The high-current paths (PGND, IN and OUT) should have short, direct and wide traces. Place the ceramic input capacitor close to IN and PGND. Keep the input capacitor and IN connection as short and wide as possible.
3. Place the external feedback resistors next to FB.
4. Keep the feedback network away from the switching node.

Notes:

11) The recommended layout is based on Typical Application Circuits section on page 20.

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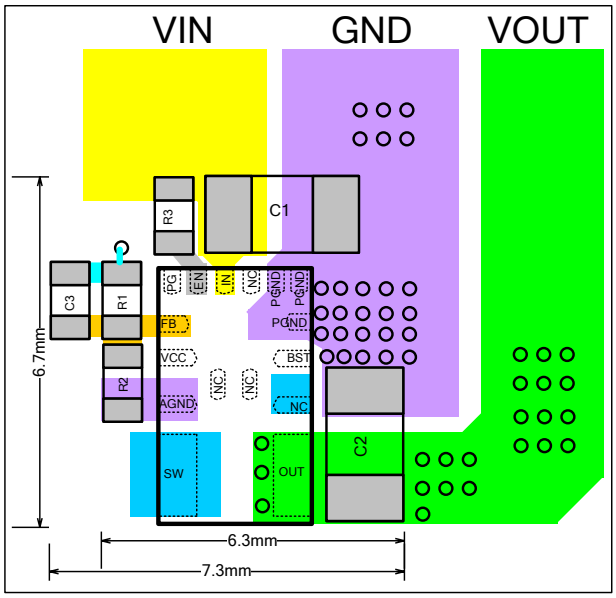
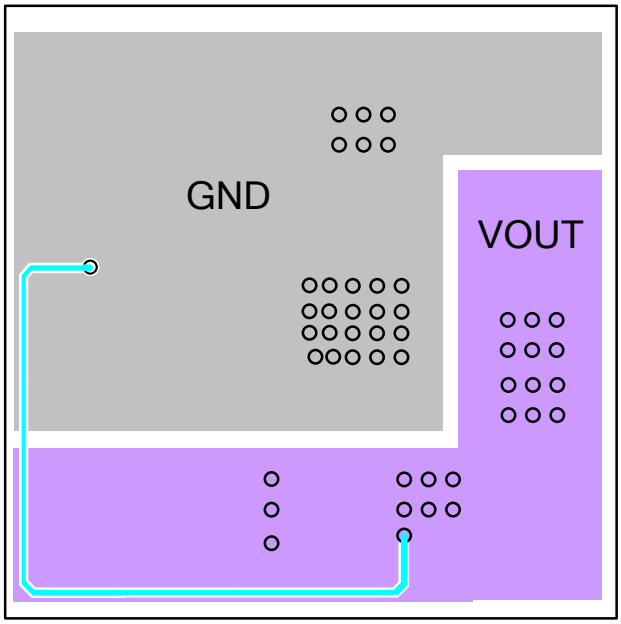


Top Layer



Bottom Layer

Figure 8. Recommended PC Board Layout

Design Example

Table 2 shows a design example following the application guidelines for the specifications:

Table 2. Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	0.6A

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms are shown in the Typical Characteristics section (For additional device applications, please refer to the related evaluation board datasheets).

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TYPICAL APPLICATION CIRCUITS(12)(13)

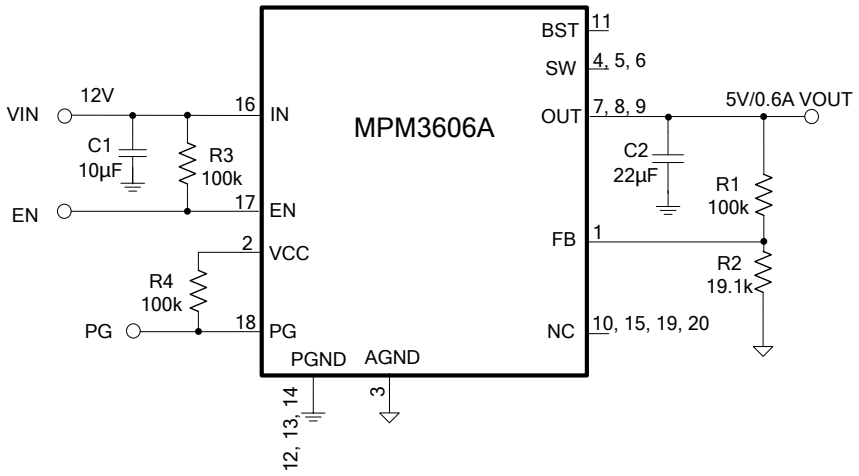

Figure 9. Vo=5V, Io=0.6A

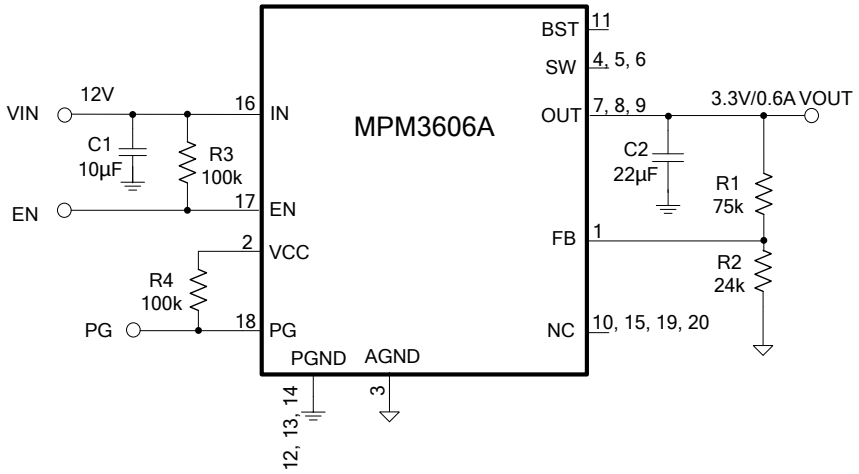

Figure 10. Vo=3.3V, Io=0.6A

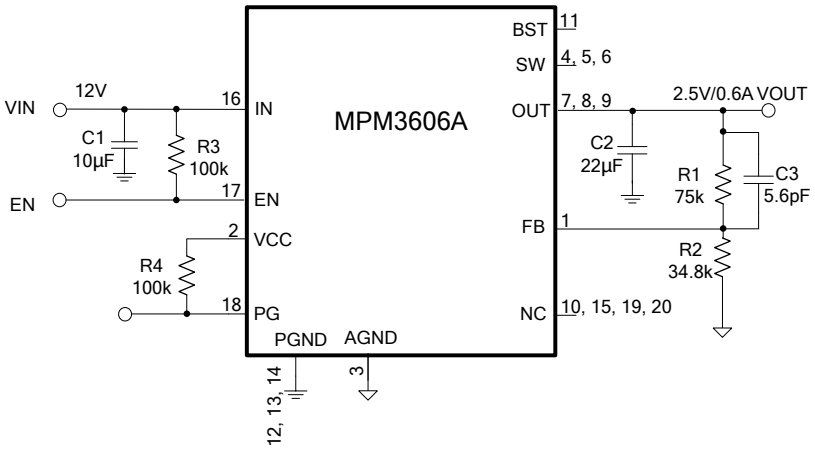

Figure 11. Vo=2.5V, Io=0.6A

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TYPICAL APPLICATION CIRCUITS(*continued*)

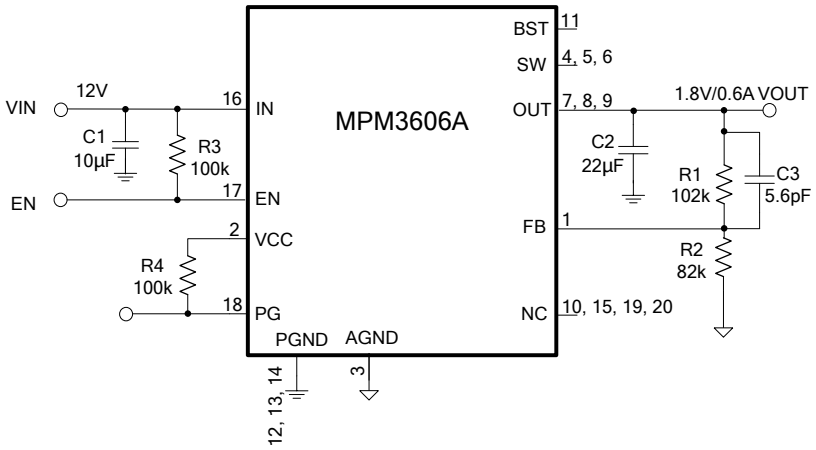

Figure 12. Vo=1.8V, Io=0.6A

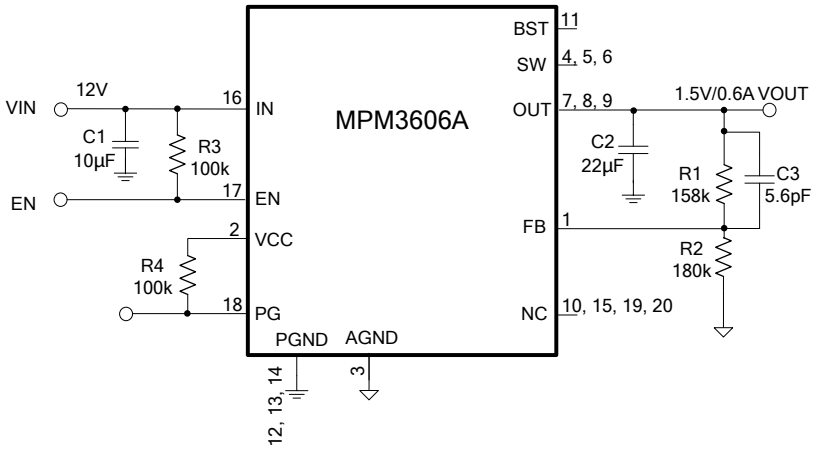

Figure 13. Vo=1.5V, Io=0.6A

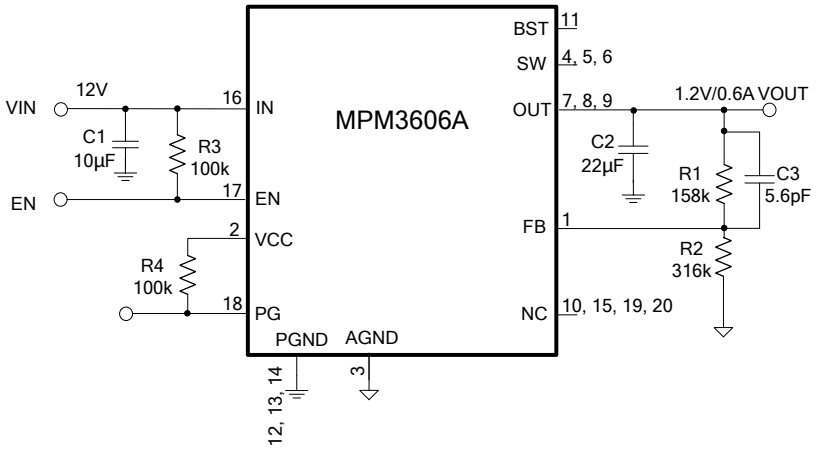

Figure 14. Vo=1.2V, Io=0.6A

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TYPICAL APPLICATION CIRCUITS (*continued*)

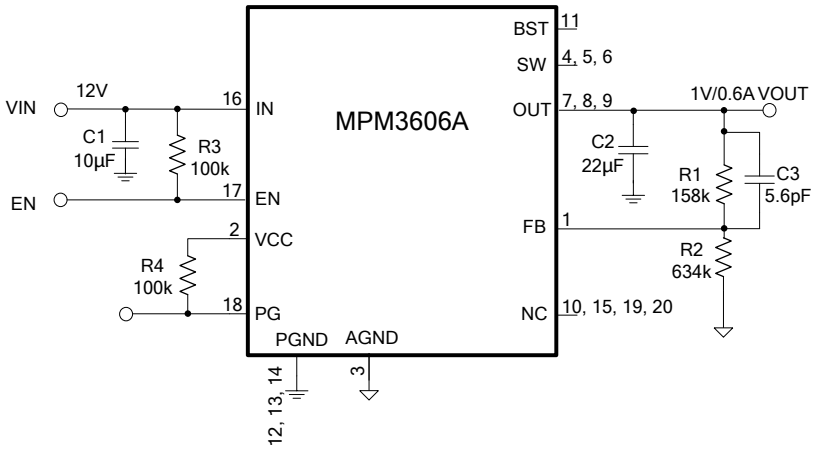

Figure 15: Vo=1V, Io=0.6A

Notes:

12) In $12V_{IN}$ to $1V_{OUT}$ application condition, the HS-FET's on time is close to minimum on time, the SW may have a little jitter, even so the output voltage ripple is smaller than 15mV in PWM mode.

13) In $12V_{IN}$ to 1.5/1.2/1 V_{OUT} application condition, BST operation current will charge the output voltage higher than the setting value when completely no load due to large divider resistor value. 10µA load current is able to pull the output voltage to normal regulation level.

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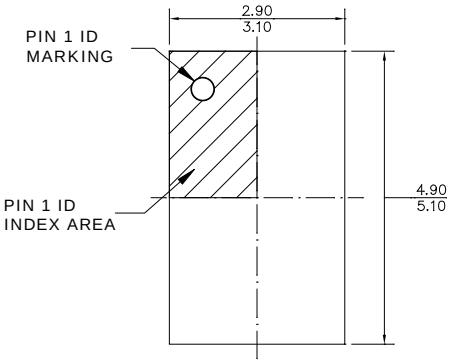
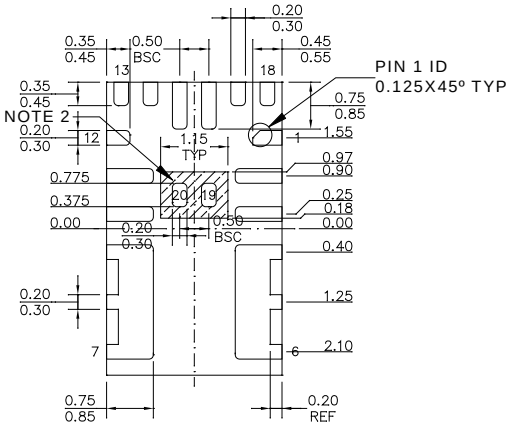
PACKAGE INFORMATION

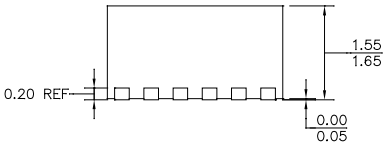
QFN-20 (3mmx5mmx1.6mm)



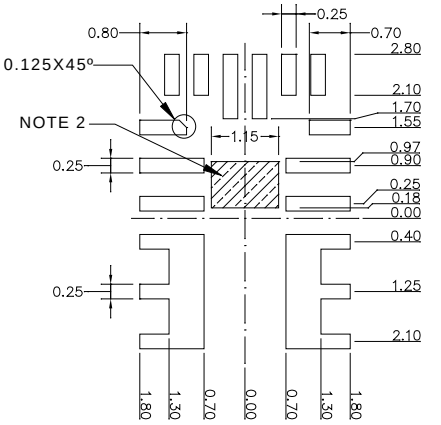
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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