

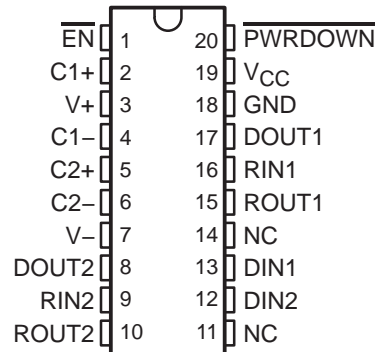
SN65C3222, SN75C3222

3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS534B – MAY 2002 – REVISED OCTOBER 2004

- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up To 1 Mbit/s
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The SN65C3222 and SN75C3222 consist of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ μ s to 150 V/ μ s.

The SN65C3222 and SN75C3222 can be placed in the power-down mode by setting $\overline{\text{PWRDOWN}}$ low, which draws only 1 μ A from the power supply. When the devices are powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled, $V+$ is lowered to V_{CC} , and $V-$ is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting $\overline{\text{EN}}$ high.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------|--------------|-----------------------|------------------|
| –0°C to 70°C | SOIC (DW) | Tube of 25 | SN75C3222DW | 75C3222 |
| | | Reel of 2000 | SN75C3222DWR | |
| | SSOP (DB) | Reel of 2000 | SN75C3222DBR | CA3222 |
| | TSSOP (PW) | Tube of 70 | SN75C3222PW | CA3222 |
| Reel of 2000 | | SN75C3222PWR | | |
| –40°C to 85°C | SOIC (DW) | Tube of 25 | SN65C3222DW | 65C3222 |
| | | Reel of 2000 | SN65C3222DWR | |
| | SSOP (DB) | Reel of 2000 | SN65C3222DBR | CB3222 |
| | TSSOP (PW) | Tube of 70 | SN65C3222PW | CB3222 |
| Reel of 2000 | | SN65C3222PWR | | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN65C3222, SN75C3222

3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

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Function Tables

EACH DRIVER

| INPUTS | | OUTPUT DOUT |
|--------|---------|----------------|
| DIN | PWRDOWN | |
| X | L | Z |
| L | H | H |
| H | H | L |

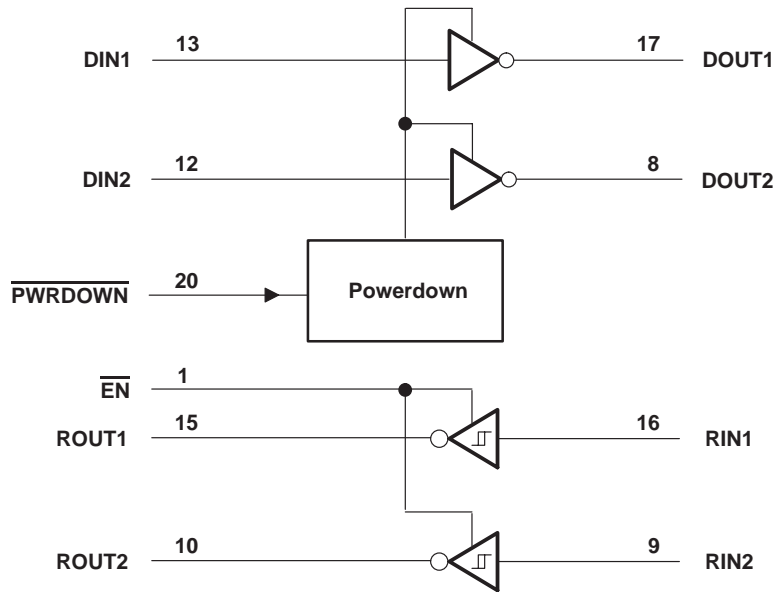
H = high level, L = low level, X = irrelevant,
Z = high impedance

EACH RECEIVER

| INPUTS | | OUTPUT ROUT |
|--------|------------------------|----------------|
| RIN | $\overline{\text{EN}}$ | |
| L | L | H |
| H | L | L |
| X | H | Z |
| Open | L | H |

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), Open = input
disconnected or connected driver off

logic diagram (positive logic)



SN65C3222, SN75C3222

3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} (see Note 1) | –0.3 V to 6 V |
| Positive output supply voltage range, $V+$ (see Note 1) | –0.3 V to 7 V |
| Negative output supply voltage range, $V-$ (see Note 1) | 0.3 V to –7 V |
| Supply voltage difference, $V+ - V-$ (see Note 1) | 13 V |
| Input voltage range, V_I : Drivers, \overline{EN} , $\overline{PWRDOWN}$ | –0.3 V to 6 V |
| Receivers | –25 V to 25 V |
| Output voltage range, V_O : Drivers | –13.2 V to 13.2 V |
| Receivers | –0.3 V to $V_{CC} + 0.3$ V |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package | 70°C/W |
| DW package | 58°C/W |
| PW package | 83°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to network GND.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 5)

| | | MIN | NOM | MAX | UNIT | |
|----------------|---|---|-----|--|------|---|
| Supply voltage | $V_{CC} = 3.3$ V | 3 | 3.3 | 3.6 | V | |
| | $V_{CC} = 5$ V | 4.5 | 5 | 5.5 | | |
| V_{IH} | Driver and control high-level input voltage | DIN, \overline{EN} , $\overline{PWRDOWN}$ | | $V_{CC} = 3.3$ V 2 $V_{CC} = 5$ V 2.4 | V | |
| V_{IL} | Driver and control low-level input voltage | DIN, \overline{EN} , $\overline{PWRDOWN}$ | | 0.8 | V | |
| V_I | Driver and control input voltage | DIN, \overline{EN} , $\overline{PWRDOWN}$ | | 0 | 5.5 | V |
| V_I | Receiver input voltage | –25 | | 25 | V | |
| T_A | Operating free-air temperature | SN65C3222 | –40 | 85 | °C | |
| | | SN75C3222 | 0 | 70 | | |

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|-----------|--|---|--|-----|------------|---------|---------|
| I_I | Input leakage current (\overline{EN} , $\overline{PWRDOWN}$) | | | | \pm 0.01 | \pm 1 | μ A |
| I_{CC} | Supply current | No load, $\overline{PWRDOWN}$ at V_{CC} | | | 0.3 | 1 | mA |
| | Supply current (powered off) | No load, $\overline{PWRDOWN}$ at GND | | | 1 | 10 | μ A |

‡ All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ$ C.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.



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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|--|-----|-------|-----|------|
| V _{OH} High-level output voltage | DOUT at R _L = 3 kΩ to GND, DIN = GND | | 5 | 5.4 | | V |
| V _{OL} Low-level output voltage | DOUT at R _L = 3 kΩ to GND, DIN = V _{CC} | | -5 | -5.4 | | V |
| I _{IH} High-level input current | V _I = V _{CC} | | | ±0.01 | ±1 | μA |
| I _{IL} Low-level input current | V _I at GND | | | ±0.01 | ±1 | μA |
| I _{OS} Short-circuit output current‡ | V _{CC} = 3.6 V, | V _O = 0 V | | ±35 | ±60 | mA |
| | V _{CC} = 5.5 V, | V _O = 0 V | | ±35 | ±90 | |
| r _o Output resistance | V _{CC} , V+, and V- = 0 V, V _O = ±2 V | | 300 | 10M | | Ω |
| I _{off} Output leakage current | PWRDOWN = GND | V _O = ±12 V, V _{CC} = 3 V to 3.6 V | | | ±25 | μA |
| | | V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V | | | ±25 | |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--|---|--|-----|------|-----|--------|
| Maximum data rate (see Figure 1) | R _L = 3 kΩ, One DOOUT switching | C _L = 1000 pF | | 250 | | kbit/s |
| | | C _L = 250 pF, V _{CC} = 3 V to 4.5 V | | 1000 | | |
| | | C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V | | 1000 | | |
| t _{sk(p)} Pulse skew§ | C _L = 150 pF to 2500 pF | R _L = 3 kΩ to 7 kΩ, See Figure 2 | | 300 | | ns |
| SR(tr) Slew rate, transition region (see Figure 1) | R _L = 3 kΩ to 7 kΩ, V _{CC} = 3.3 V | C _L = 150 pF to 1000 pF | | 18 | 150 | V/μs |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

§ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|---|--|-------------------------|-------------------------|-----|------|
| V _{OH} | High-level output voltage | I _{OH} = -1 mA | V _{CC} - 0.6 V | V _{CC} - 0.1 V | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{IT+} | Positive-going input threshold voltage | V _{CC} = 3.3 V | | 1.5 | 2.4 | V |
| | | V _{CC} = 5 V | | 1.8 | 2.4 | |
| V _{IT-} | Negative-going input threshold voltage | V _{CC} = 3.3 V | 0.6 | 1.2 | | V |
| | | V _{CC} = 5 V | 0.8 | 1.5 | | |
| V _{hys} | Input hysteresis (V _{IT+} - V _{IT-}) | | | 0.3 | | V |
| I _{off} | Output leakage current | $\overline{\text{EN}} = V_{\text{CC}}$ | | ±0.05 | ±10 | μA |
| r _i | Input resistance | V _I = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--------------------|---|---|-----|------|-----|------|
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 150 pF, See Figure 3 | | 300 | | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | C _L = 150 pF, See Figure 3 | | 300 | | ns |
| t _{en} | Output enable time | C _L = 150 pF, R _L = 3 kΩ, See Figure 4 | | 200 | | ns |
| t _{dis} | Output disable time | C _L = 150 pF, R _L = 3 kΩ, See Figure 4 | | 200 | | ns |
| t _{sk(p)} | Pulse skew‡ | See Figure 3 | | 300 | | ns |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

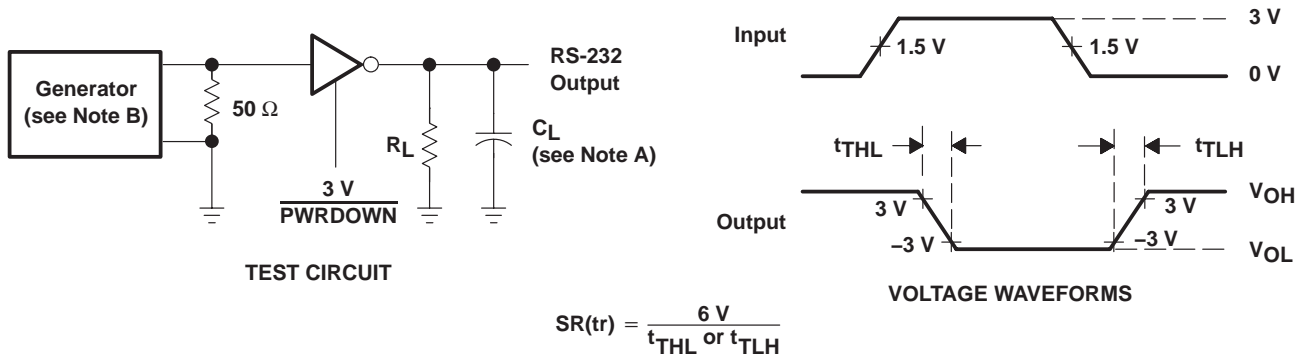


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3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

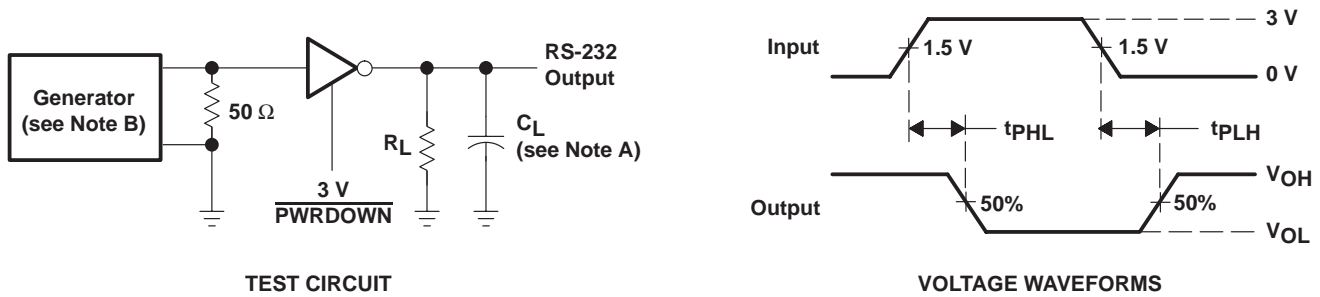
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PARAMETER MEASUREMENT INFORMATION



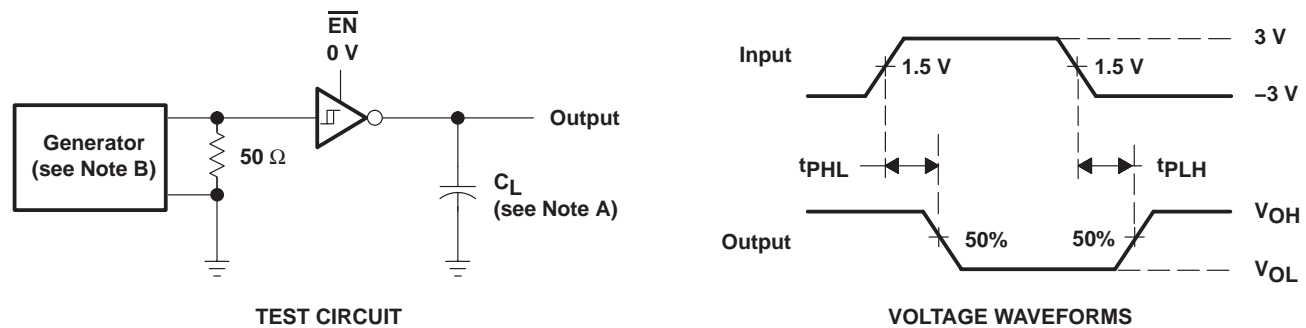
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

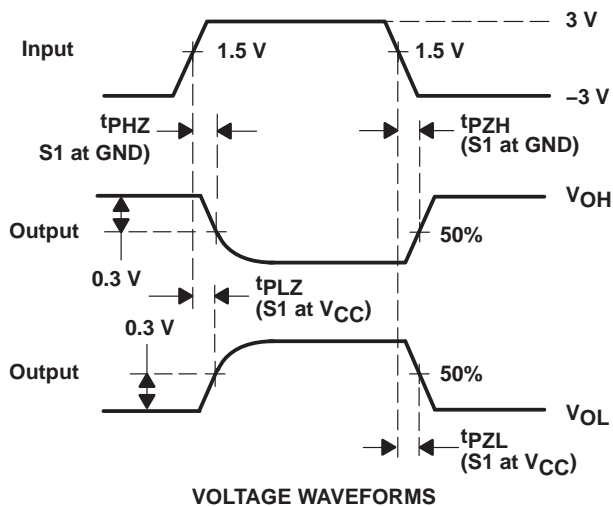
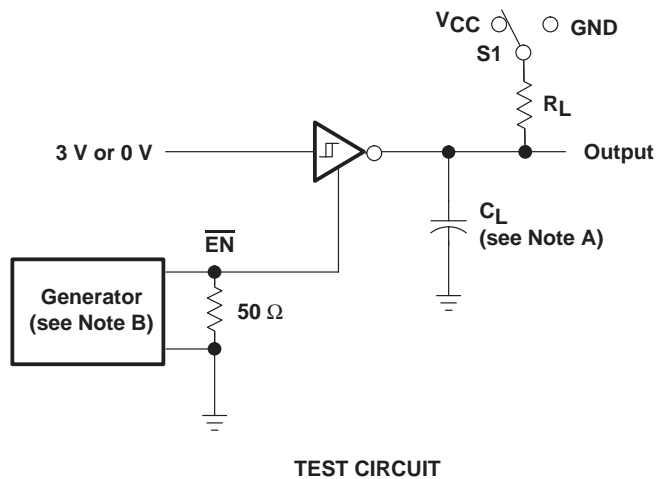
Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation-Delay Times

PARAMETER MEASUREMENT INFORMATION



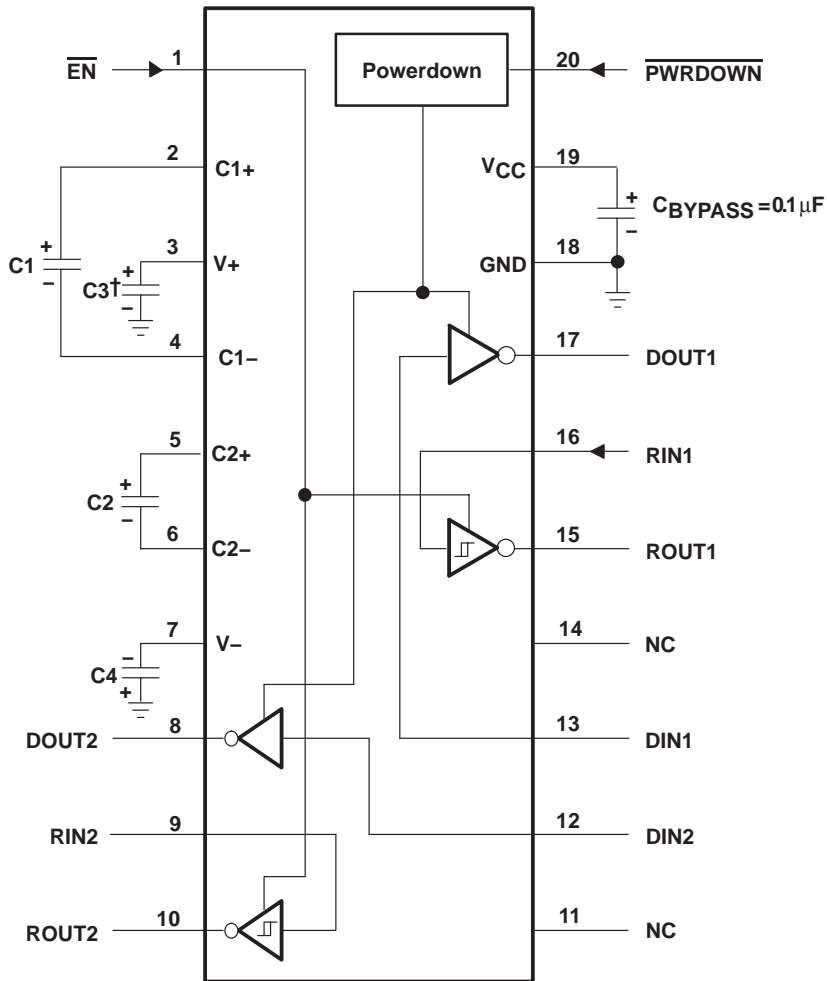
- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 4. Receiver Enable and Disable Times

SN65C3222, SN75C3222 3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

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APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.
 NOTES: A. Resistor values shown are nominal.
 B. NC – No internal connection

V_{CC} vs CAPACITOR VALUES

| V _{CC} | C1 | C2, C3, and C4 |
|-----------------|----------|----------------|
| 3.3 V ± 0.3 V | 0.1 μF | 0.1 μF |
| 5 V ± 0.5 V | 0.047 μF | 0.33 μF |
| 3 V to 5.5 V | 0.1 μF | 0.47 μF |

Figure 5. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65C3222DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3222 | Samples |
| SN65C3222DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C3222 | Samples |
| SN65C3222PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3222 | Samples |
| SN65C3222PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3222 | Samples |
| SN75C3222DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75C3222 | Samples |
| SN75C3222DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75C3222 | Samples |
| SN75C3222DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75C3222 | Samples |
| SN75C3222PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3222 | Samples |
| SN75C3222PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3222 | Samples |
| SN75C3222PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3222 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65C3222DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C3222DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN65C3222PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN75C3222DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN75C3222PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65C3222DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN65C3222DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN65C3222PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN75C3222DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN75C3222PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

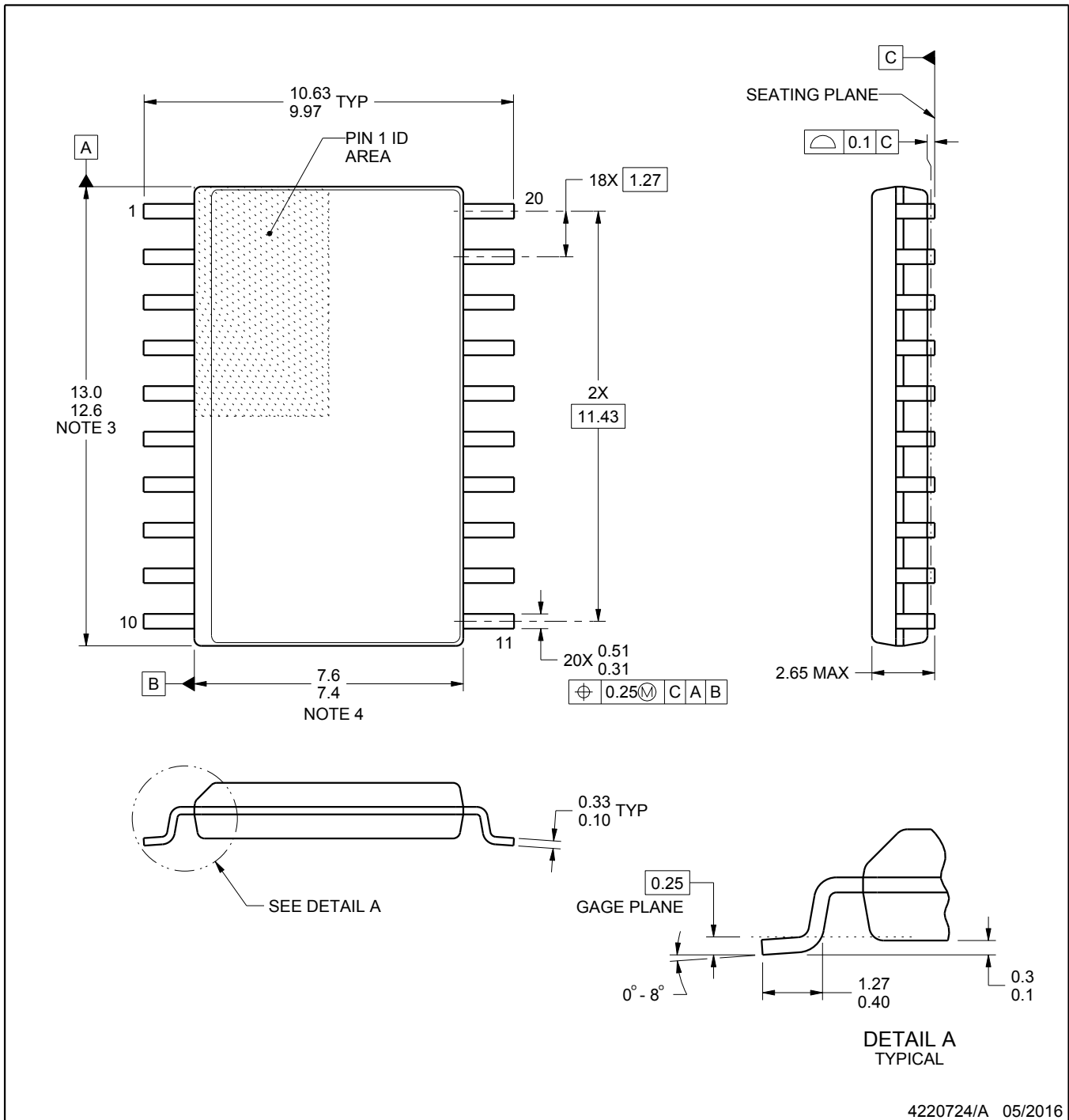
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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