Integrated
Circuit
Systems, Inc.

ICS9147-14

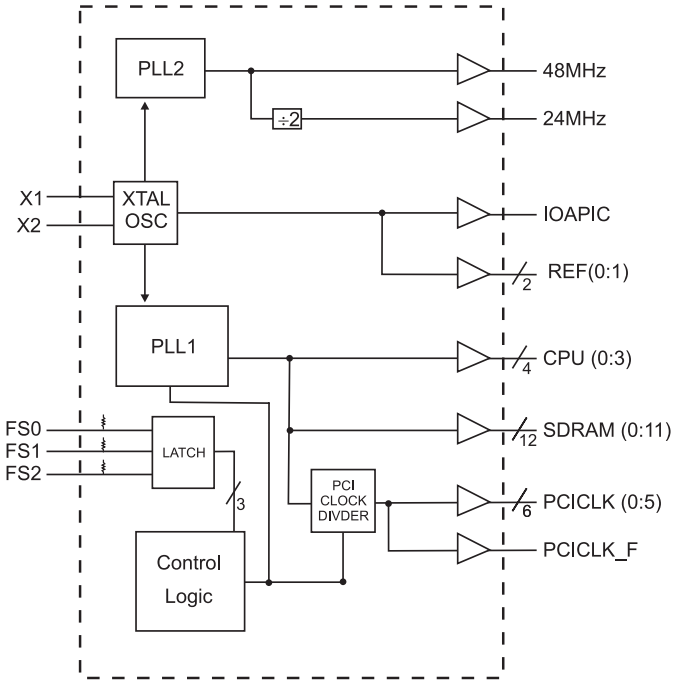
Frequency Generator & Integrated Buffers for PENTIUM/Pro™

General Description

The **ICS9147-14** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. Two bidirectional I/O pins (FS1,FS2) are latched at power-on to the functionality table, with FS0 selectable in real-time to toggle between conditions.

High drive PCICLK and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. CPU outputs typically provide better than 1V/ns slew rate into 20 pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates. Seperate buffers supply pins VDDL1 allow for 3.3V or reduced voltage swing (from 2.9 to 2.5V) for CPU (0:3) and IOAPIC outputs.

Block Diagram



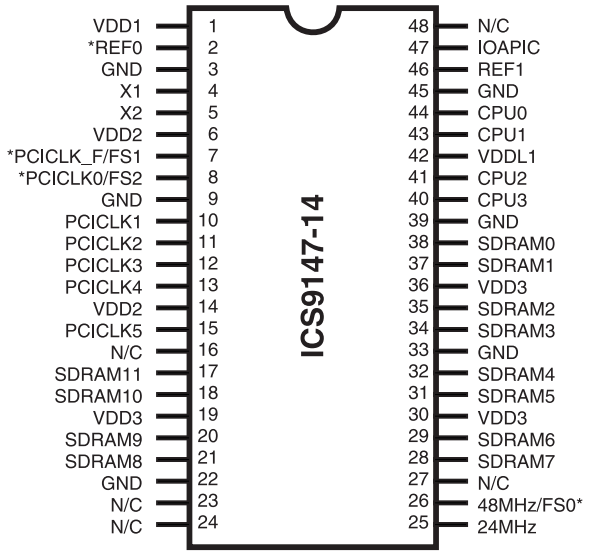
Power Groups

VDD1 = REF (0:1), X1, X2, 24MHz, 48MHz
VDD2 = PCICLKF, PCICLK(0:5)
VDD3 = SDRAM (0;11)
VDDL1 = CPUCLK (0:3)

Features

- Four copies of CPU clock
- Twelve SDRAM (3.3V TTL), usable as AGP clocks
- Seven copies of PCICLK clock (synchronous with CPU clock/2 or CPU/2.5 for 75 and 83.3 MHz CPU)
- CPU clocks to PCICLK clocks skew 1-4ns, center 2.6ns.
- One IOAPIC clock @14.31818MHz
- Two copies of Ref. clock @14.31818MHz
- Ref. 14.31818MHz Xtal oscillator input
- Separate V_{DDL1} for four CPU and single IOAPIC output buffers to allow 2.5V output (or Std. Vdd)
- One each 48/24MHz (3.3V TTL)
- 3.3V outputs: SDRAM, PCI, REF, 48/24MHz.
- 2.5V or 3.3V outputs: CPU, IOAPIC.
- 20 ohm CPU clock output impedance
- 20 ohm PCI clock output impedance
- 1.5ns rise time (30 pF loading)
- ±250 ps CPU, PCI clock skew
- 350ps (cycle by cycle) CPU jitter
- 2ms Power up clock stable time
- 45-55% Clock duty cycle
- 48 pin 300 mil SSOP package
- 3.0V – 3.7V supply range w/2.5V compatible outputs

Pin Configuration



48-Pin SSOP

* Internal Pull-up Resistor of
300K to 3.3V on indicated inputs

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD1	PWR	Ref (0:2), XTAL, 24MHz, 48MHz power supply
2	REF0	OUT	14.318 Mhz reference clock.
3,9,22,33,39,45	GND	PWR	Ground
4	X1	IN	Crystal input has internal load cap and feedback resistor from X2
5	X2	OUT	Crystal output nominally 14.318MHz. Has internal load cap
16,23,24, 27,48	N/C	-	Pins are not internally connected
6,14	VDD2	PWR	Supply for PCICLK_F and PCICLK (0:5)
7	PCICLK_F	OUT	Free running PCI clock
	FS1*	IN	Frequency select pin. *
8	PCICLK0	OUT	PCI clock output.
	FS2*	IN	Frequency select pin. *
10, 11, 12, 13	PCICLK(1:4)	OUT	PCI clock outputs
15	PCICLK5	OUT	PCI clock output.
17, 18, 20, 21, 28, 29, 31, 32, 34, 35,37,38	SDRAM (0:11)	OUT	SDRAM clock outputs.
19,30,36	VDD3	PWR	Supply for SDRAM (0:11)
25	24MHz	OUT	24MHz output clock
26	48MHz	OUT	48MHz output clock
	FS0*	IN	Frequency select pin
40, 41, 43, 44	CPUCLK(0:3)	OUT	CPU clock outputs, powered by VDD1
42	VDDL1	PWR	Supply for CPU (0:3) and IOAPIC clock, can be 2.5 or 3.3V
46	REF1	OUT	14.318 Mhz reference clock.
47	IOAPIC	OUT	IOAPIC clock output. Powered by VDDL1.

*** Internal Pull-up Resistor of 120K to 3.3V on indicated inputs**

Functionality

3.3v±10% 0-70°c
Crystal (X1, X2 = 14.3181MHz

FS2	FS1	FS0	CPU, SDRAM(MHz)	PCICLK (MHz)	REF, IOAPIC (MHz)
0	0	0	50.0	25.0	14.318
0	0	1	75.0	32.0	14.318
0	1	0	33.3	16.65	14.318
0	1	1	68.5	34.25	14.318
1	0	0	55.0	27.5	14.318
1	0	1	75.0	37.5	14.318
1	1	0	60.0	30.0	14.318
1	1	1	66.8	33.4	14.318

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	Latched inputs	-	-	0.8	V
Input High Voltage	V_{IH}	Latched inputs	2.0	-	-	V
Output Low Current[1]	I_{OL1}	VOL=0.8V; for SDRAM, PCICLK	19.0	30.0	-	mA
Output High Current[1]	I_{OH1}	VOH=2.0V; for SDRAM PCICLK	-	-26.0	-16.0	mA
Output Low Current[1]	I_{OL2}	VOL=0.8V; 24, 48 CLKs, CPU, REF & IOAPIC	16.0	25.0	-	mA
Output High Current[1]	I_{OH2}	VOH=2.0V; 24, 48 CLKs, CPU, REF & IOAPIC	-	-22.0	-14.0	mA
Output Low Current[1]	I_{OL3}	VOL=0.8V; for CPU at VDDL = 2.5V	10.0	18.0	-	mA
Output High Current[1]	I_{OH3}	VOH = 1.7V; for CPU at VDDL = 2.5V	-	-14.0	-8.0	mA
Output Low Voltage[1]	V_{OL1}	IOL = 10mA; for PCICLK, SDRAM	-	0.3	0.4	V
Output High Voltage[1]	V_{OH1}	IOH = -10mA; for SDRAM, PCICLK	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL2}	IOL = 8mA; for fixed CLKs, CPU, REF & IOAPIC	-	0.3	0.4	V
Output High Voltage[1]	V_{OH2}	IOH = -8mA; for fixed CLKs, CPU, REF & IOAPIC	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL3}	IOL = 5mA; for CPU at VDDL = 2.5V	-	0.25	0.4	mA
Output High Voltage[1]	V_{OH3}	IOH = -5mA; for CPU at VDDL = 2.5V	2.1	2.25	-	mA
Supply Current	I_{DD}	@66.6 MHz; all outputs unloaded	-	70	120	mA
Pullup Resistor[1]	R_{PU1}	FS0, FS1 FS2 inputs	150	300	450	K ohm

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V CPU, IOAPIC, Fixed & REF	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V CPU, IOAPIC, Fixed & REF	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% CPU, IOAPIC, Fixed & REF	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% CPU, IOAPIC, Fixed& REF	-	1.4	2.4	ns
Rise Time[1]	T_{r3}	20pF load, 0.8 to 2.0V PCI, SDRAM	-	0.9	1.5	ns
Fall Time[1]	T_{f3}	20pF load, 2.0 to 0.8V PCI, SDRAM	-	0.8	1.4	ns
Rise Time[1]	T_{r4}	20pF load, 0.4 to 2.0V , CPU and IOAPIC with VDDL = 2.5V	-	-	3.0	ns
Fall Time[1]	T_{f4}	20pF load, 2.0 to 0.4V, CPU and IOAPIC with VDDL = 2.5V	-	-	2.0	ns
Duty Cycle[1]	D_t	20pF load @ VOUT=1.4V All clocks except REF	45	50	55	%
Duty Cycle[1]	D_{T2}	20pF load @ VOUT=1.4V REF outputs	40	50	60	%
Jitter, One Sigma[1]	T_{jis1}	CPU & PCICLK Clocks; Load=20pF, SDRAM; Load = 30pF	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	CPU & PCICLK Clocks; Load=20pF, SDRAM; Load = 30pF	-250	-	250	ps
Jitter, Cycle to Cycle	T_{jc-c}	CPU	-	200	350	ps
Jitter, One Sigma[1]	T_{jis2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From VDD=1.6V to 1st crossing of 66.6 MHz VDD supply ramp < 40ms	-	2.5	4.5	ms
Clock Skew[1]	T_{sk1}	CPU to CPU or PCI to PCI; Load=20pF; @1.4V (Same VDD)	-	150	250	ps
Clock Skew[1]	T_{sk2}	SDRAM to SDRAM; Load=20pF; @1.4V	-	300	500	ps
Clock Skew[1]	T_{sk3}	CPU to PCICLK; Load=20pF; @1.4V (CPU is early)	1	2.1	4	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Shared Pin Operation - Input/Output Pins

Pins 7, 8 and 26 on the **ICS9147-14** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

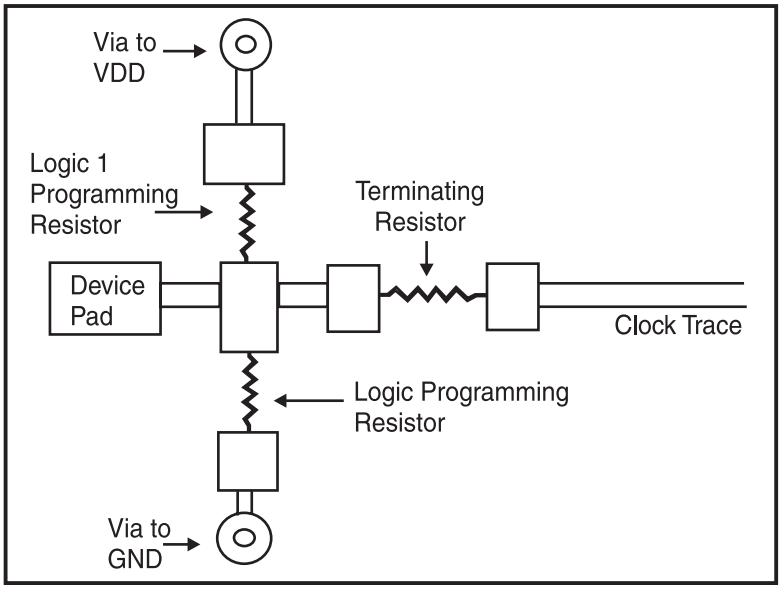


Fig. 1

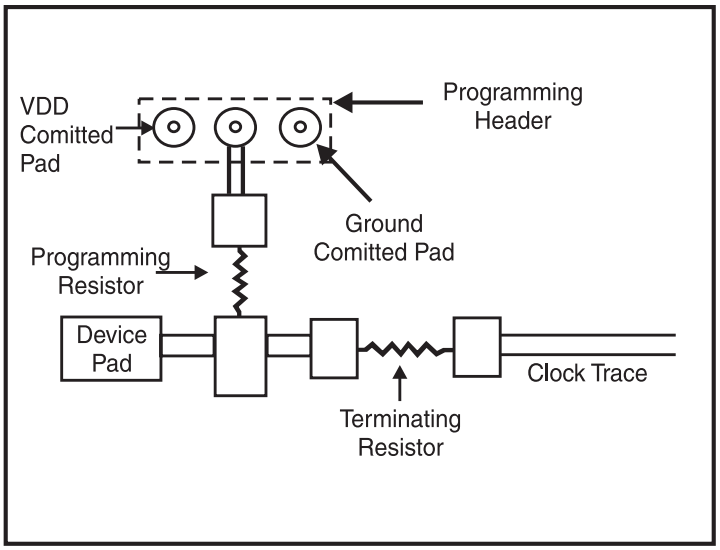

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

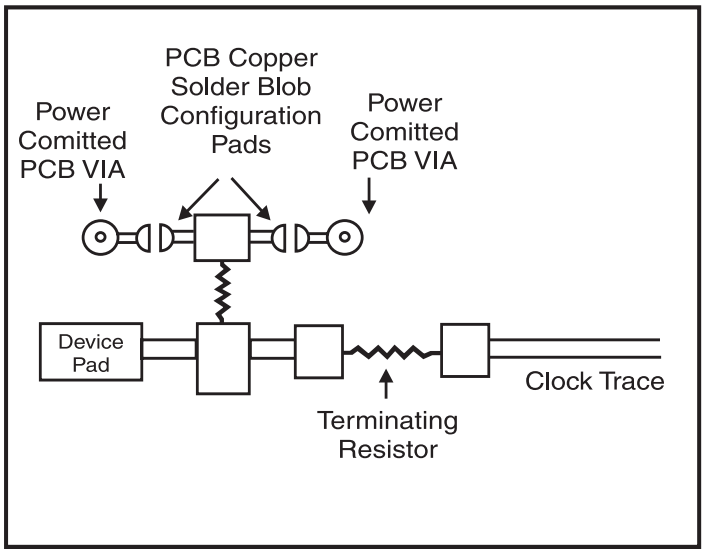
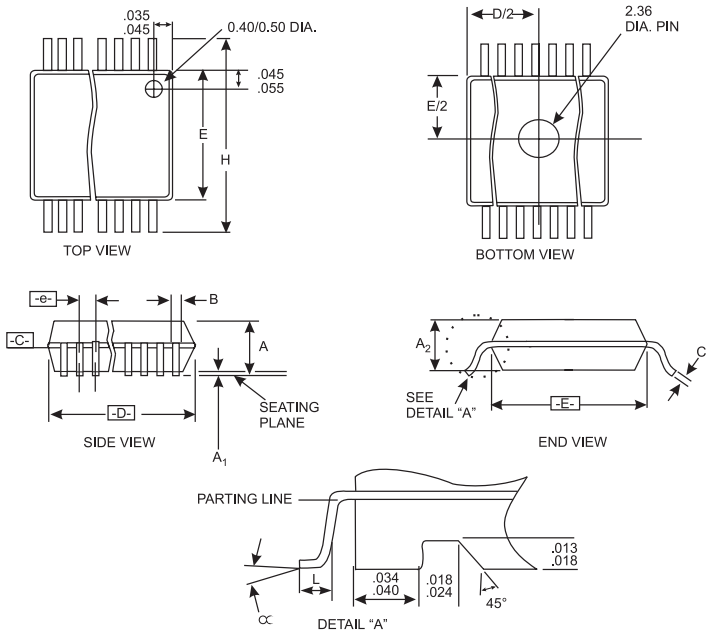

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Power
Comitted
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

Ordering Information

ICS9147F-14

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device