SONY

CXA2025AS

Y/C/RGB/Sync/Deflection for Color TV

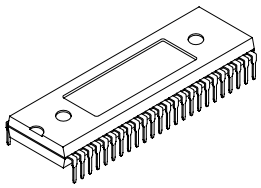
Description

The CXA2025AS is a bipolar IC which integrates the luminance signal processing, chroma signal processing, RGB signal processing, and sync and deflection signal processing functions for NTSC system color TVs onto a single chip.

The following functions have been added to the same function IC, CXA2025S.

1) Vertical sync pull-in speed switching function
2) YUV SW Y signal switching function

48 pin SDIP (Plastic)



Features

- I^2C bus compatible
- Sync signal processing uses a countdown system with non-adjusting H/V oscillator frequencies
- Built-in deflection compensation circuit capable of supporting various wide modes
- Non-adjusting Y/C block filter
- Built-in AKB
- Video signal I/Os: Y/C separation input, Y/color difference input, analog RGB input and RGB output
- YUV SW Y signal switching function allows picture quality adjustment for the Y signal in the same manner as for the normal Y signal even when Y/color difference input is selected

Absolute Maximum Ratings

(Ta = 25°C, SGND, JGND = 0V)

• Supply voltage	SV_{CC}, JV_{CC}	–0.3 to +12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.5	W
• Voltages at each pin		–0.3 to SV_{CC}, JV_{CC} + 0.3	V

Operating Conditions

Supply voltage	SV_{CC}	9.0 ± 0.5	V
	JV_{CC}	9.0 ± 0.5	V

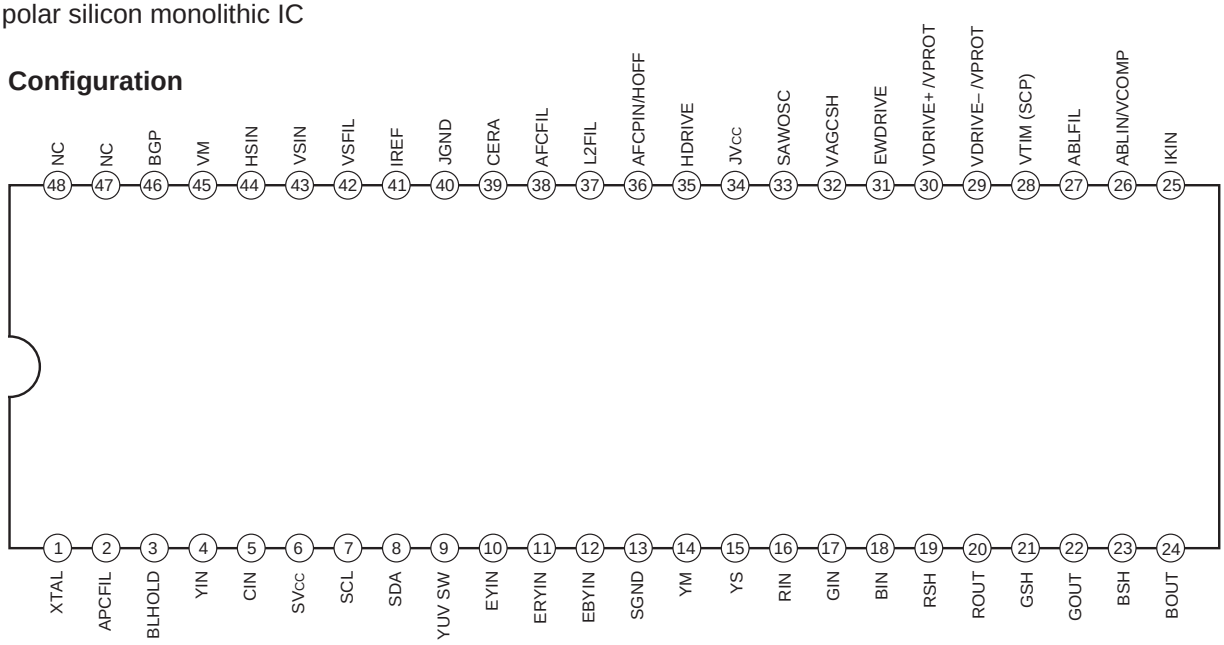
Applications

Color TVs (4:3, 16:9)

Structure

Bipolar silicon monolithic IC

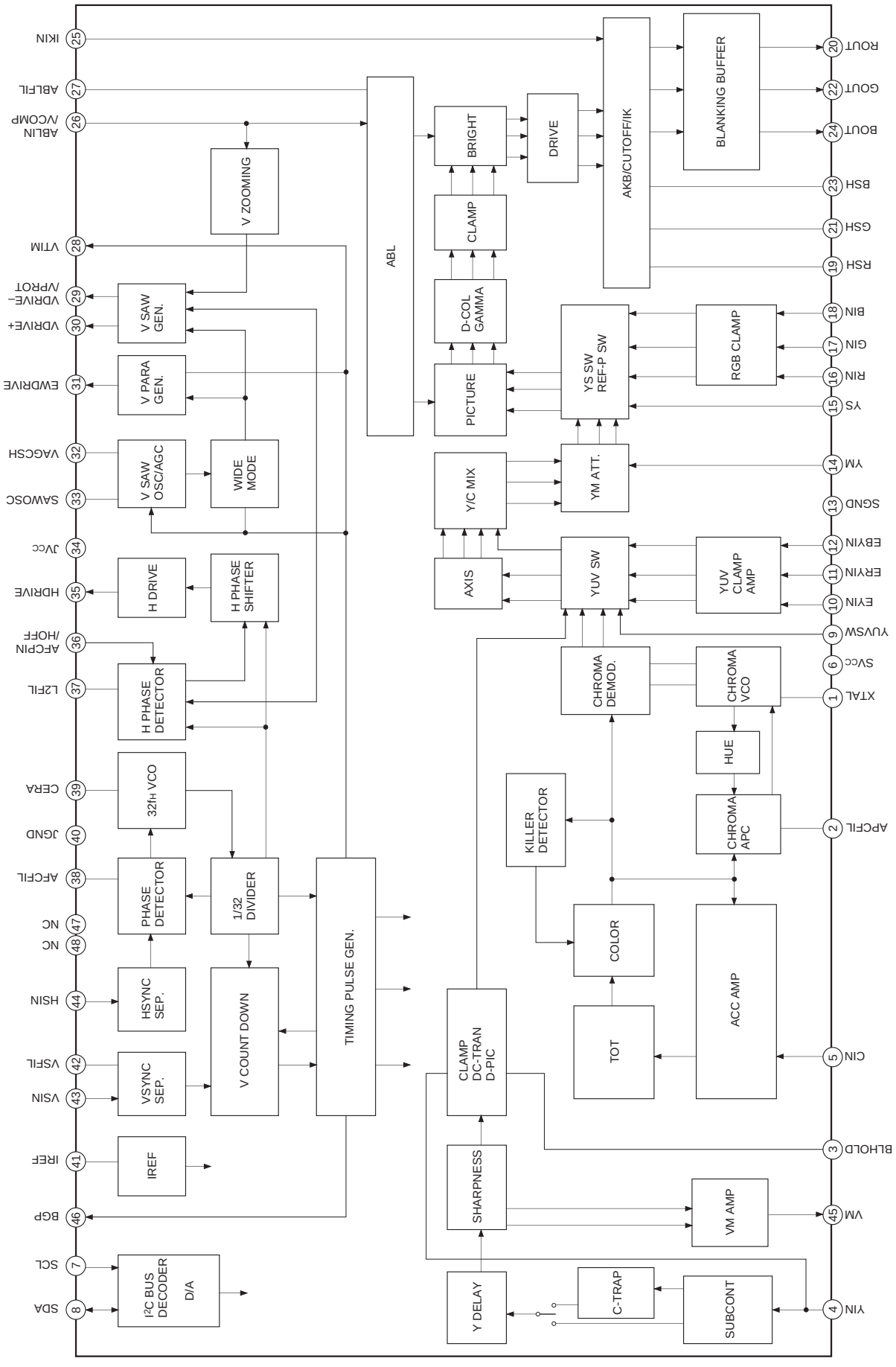
Pin Configuration



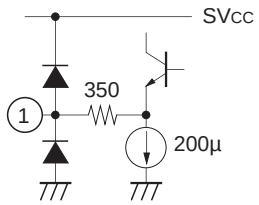
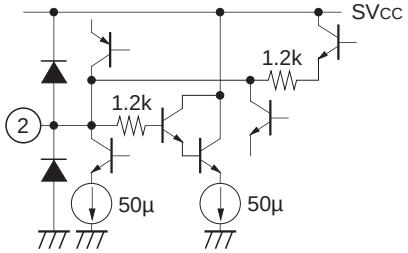
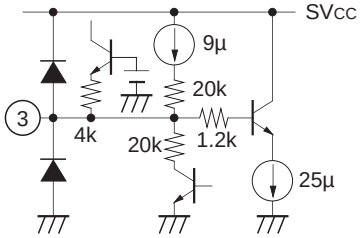
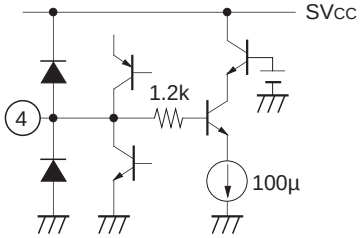
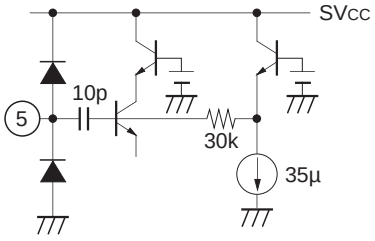
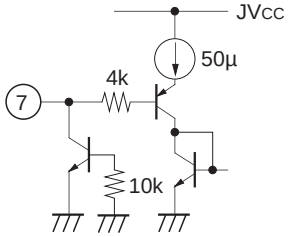
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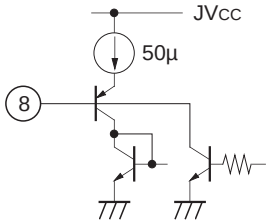
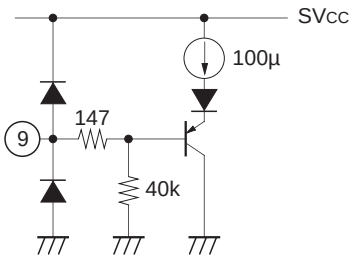
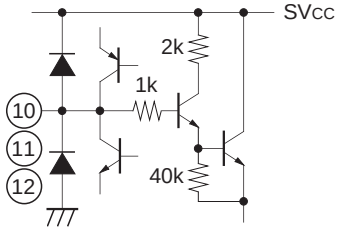
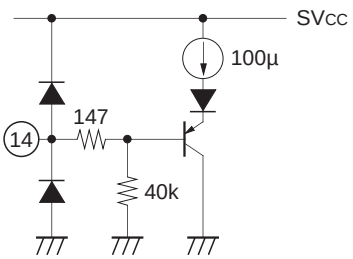
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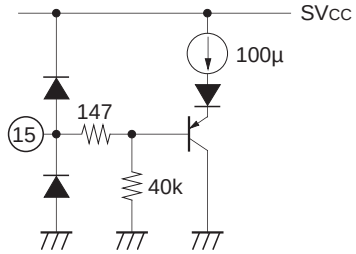
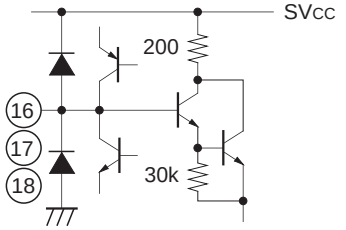
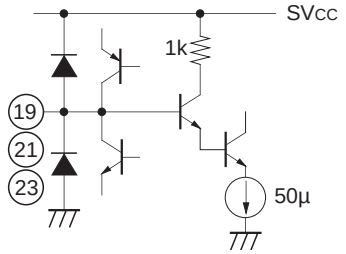
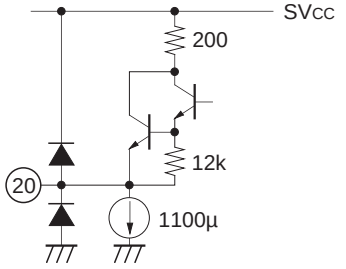
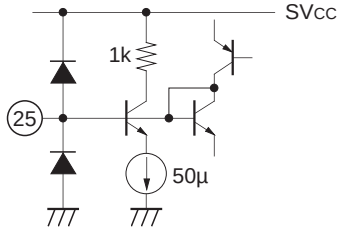
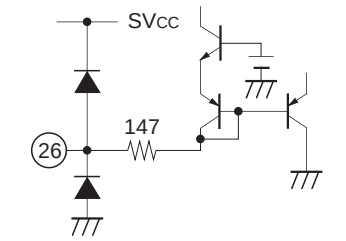
Block Diagram

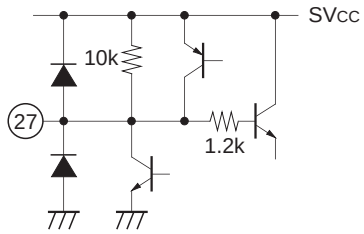
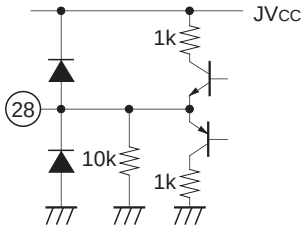
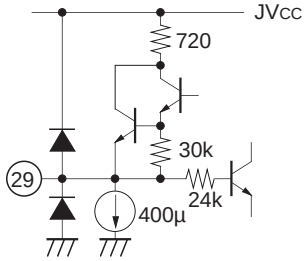
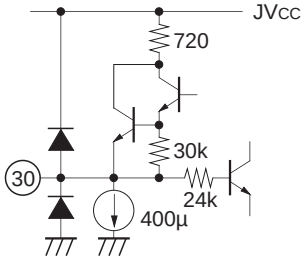
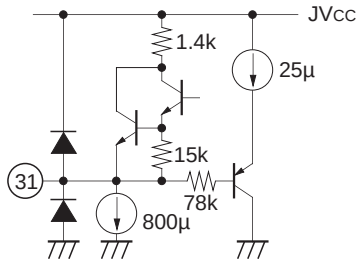
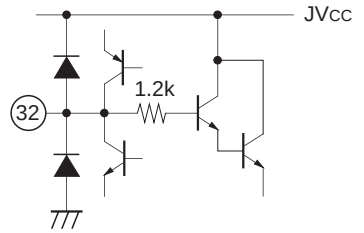


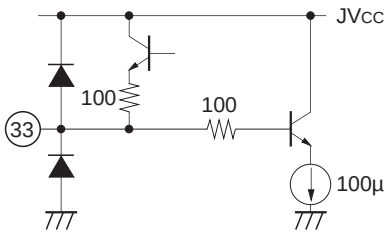
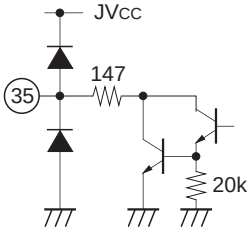
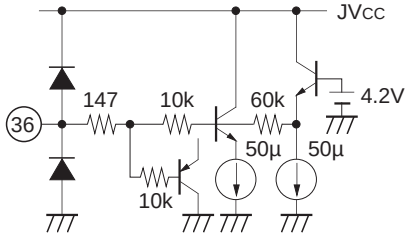
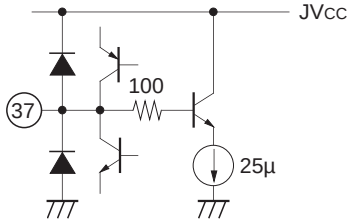
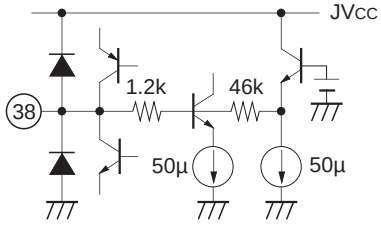
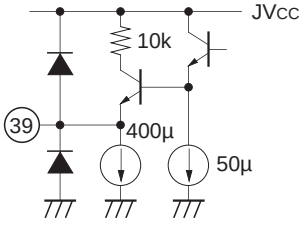
Pin Description

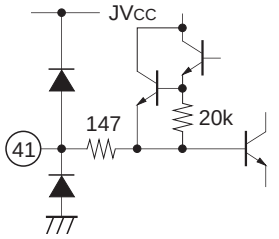
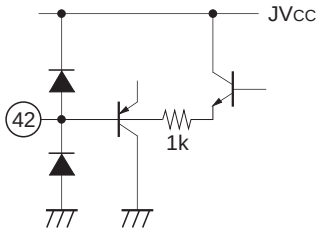
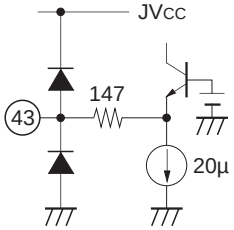
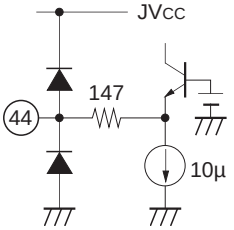
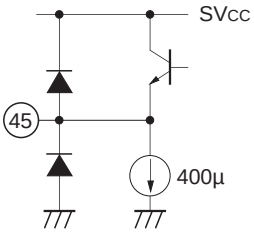
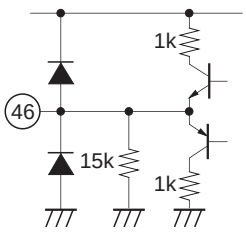
Pin No.	Symbol	Equivalent circuit	Description
1	XTAL		Connect a 3.579545MHz crystal oscillator.
2	APCFIL		CR connection for the chroma APC lag-lead filter.
3	BLHOLD		Capacitor connection for black peak hold of the dynamic picture (black expansion).
4	YIN		Y signal input. Input a 2Vp-p (including sync, 100% white) Y signal via a capacitor. The pedestal level of the input signal is clamped to 4.2V.
5	CIN		Chroma signal input. Provide a bias of about Vcc/2 and input a C signal (including sync, 100% white, 2Vp-p CV signal) with a 570mVp-p burst level.
6	SVcc		Power supply for the video block.
7	SCL		I^2C bus protocol SCL (Serial Clock) input. VILMAX = 1.5V VIHMIN = 3.5V

Pin No.	Symbol	Equivalent circuit	Description
8	SDA		I²C bus protocol SDA (Serial Data) I/O. VILMAX = 1.5V VIHMIN = 3.5V VOLMAX = 0.4V
9	YUV SW		Switch control for the external YUV signal input. When YUV SW is high, the external YUV signal is selected; when YUV SW is low, the Y/C block signal is selected. However, when the EY-SW register is 1, the YIN (Pin 4) input is selected for the Y signal even if YUV SW is high. VILMAX = 0.4V VIHMIN = 1.0V VIHMAX = 3.0V
10	EYIN		External Y signal input. Input a 0.7Vp-p (100 IRE) Y signal via a capacitor. The signal is clamped to 6.5V at the burst timing of the signal input to the sync input pin (Pin 44).
11	ERYIN		External R-Y signal input. Input a 0.78Vp-p (color difference signal obtained by detecting a 100 IRE, 0.7Vp-p, 100% color bar chroma signal at the orthogonal axis) + (R-Y) signal via a capacitor. The signal is clamped to 6.2V at the burst timing of the signal input to the sync input pin (Pin 44).
12	EBYIN		External B-Y signal input. Input a 1.0Vp-p (color difference signal obtained by detecting a 100 IRE, 0.7Vp-p, 100% color bar chroma signal at the orthogonal axis) + (B-Y) signal via a capacitor. The signal is clamped to 6.2V at the burst timing of the signal input to the sync input pin (Pin 44).
13	SGND		GND for the video block.
14	YM		YM switch control input. When YM is high, the Y/C block signal is attennated by 6dB. VILMAX = 0.4V VIHMIN = 1.0V VIHMAX = 3.0V

Pin No.	Symbol	Equivalent circuit	Description
15	YS		YS switch control input. When YS is high, the RGB block signal is selected; when YS is low, the Y/C block is selected. VILMAX = 0.4V VIHMIN = 1.0V VIHMAX = 3.0V
16 17 18	RIN GIN BIN		Analog R, G and B signal input. Input a 0.7Vp-p (no sync, 100 IRE) signal via a capacitor. The signal is clamped to 5.1V at the burst timing of the signal input to the sync input pin (Pin 44).
19 21 23	RSH GSH BSH		Sample-and-hold for R, G and B AKB. Connect to GND via a capacitor. When not using AKB (manual cut-off mode), R, G and B cut-off voltage can be controlled by applying a control voltage to each pin. The control voltage is 4.2 ± 2V.
20 22 24	ROUT GOUT BOUT		R, G and B signal output. 2.4Vp-p is output during 100% white input.
25	IKIN		Input the signal converted from the CRT beam current (cathode current IK) to a voltage via a capacitor. The V blanking part is clamped to 2.7V at the V retrace timing. The input for this pin is the reference pulse return, and the loop operates so that the Rch is 1Vp-p and the G and Bch are 0.83Vp-p. The G and Bch can be varied by ±0.5V by the bus CUTOFF control. When not using AKB, this pin should not be connected.
26	ABLIN /VCOMP		ABL control signal input and VSAW high voltage fluctuation compensation signal input. High voltage compensation has linear control characteristics for the pin voltage range of about 3V to 1V. ABL does not operate when the pin voltage is 9 [V], and operates with increasing strength as the voltage becomes lower than 9 [V].

Pin No.	Symbol	Equivalent circuit	Description
27	ABLFIL		Connect a capacitor to form the LPF of the ABL control signal.
28	VTIM (SCP)		V timing pulse output. Outputs the timing pulse from V sync identification to the end of V blanking. Pulses are positive polarity from 0 to 6 [V]. During zoom mode, the V blanking pulse which has been expanded before and after the V sync is superimposed and output as the 0 to 3 [V] pulse.
29	VDRIVE– /VPROT		V sawtooth wave output and Vprotect signal input. When a large current (3mA) is led from this pin, the RGB outputs are all blanked and the status is returned to the I^2C bus.
30	VDRIVE+ /VPROT		Outputs a V sawtooth wave of the opposite polarity as VDRIVE–. The Vprotect function can also be operated by this pin.
31	EWDRIVE		V parabola wave output.
32	VAGCSH		Sample-and-hold for AGC which maintains the V sawtooth wave at a constant amplitude. Connect to GND via a capacitor.

Pin No.	Symbol	Equivalent circuit	Description
33	SAWOSC		Connect a capacitor to generate the V sawtooth wave.
34	JVCC		Power supply for the deflection block.
35	HDRIVE		H drive signal output. This signal is output with the open collector. This pin goes high (OFF) during hold-down. * For the CXA2025S, this pin is low (ON) during hold-down.
36	AFCPIN /HOFF		H deflection pulse input for H AFC. Input an about 5Vp-p pulse via a capacitor. Set the pulse width to 10 to 12µs. This pin is also used as the hold-down signal input for the HD output, and if this pin is 1 [V] or less for a 7V cycle or longer, the hold-down function operates and the HD output goes to high (OFF). In addition, the RGB outputs are all blanked and the status is returned to the I^2C bus.
37	L2FIL		Filter for H AFC. Connect to GND via a capacitor. The H phase can also be controlled from this pin by leading current in and out of this capacitor. As the pin voltage rises, the picture shifts to the left; as the pin voltage drops, the picture shifts to the right.
38	AFCFIL		CR connection for the AFC lag-lead filter.
39	CERA		Connect the $32f_H$ VCO ceramic oscillator.
40	JGND		GND for the deflection block.

Pin No.	Symbol	Equivalent circuit	Description
41	IREF		Internal reference current setting. Connect to GND via a 15kΩ resistor.
42	VSFIL		Filter for V sync separation. Connect to GND via a capacitor.
43	VSIN		Sync signal input for V sync separation. Input a 2Vp-p Y signal.
44	HSIN		Sync signal input for H sync separation. Input a 2Vp-p Y signal.
45	VM		Outputs the differential waveform of the VM (Velocity Modulation) Y signal. (7.1VDC, 2.0Vp-p) The signal delayed for 250ns from YIN is output. The delay time from YIN and the differential coefficient of the output signal vary according to sharpness f_0 control.
46	BGP		Burst gate pulse output. This pulse is a 0 to 3V positive polarity pulse. While this pulse is gated near V-Sync for the CXA2025S, it is constantly output for the CXA2025AS.
47 48	GND GND		Not connected. Normally connected to GND to prevent interference with other pins.

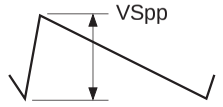
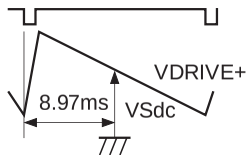
Electrical Characteristics

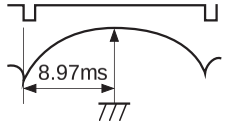
Setting conditions

- Ta = 25°C, SV_{CC} = JV_{CC} = 9V, SGND = JGND = 0V
- Measures the following after setting the I^2C bus register as shown in "I^2C bus register initial settings".

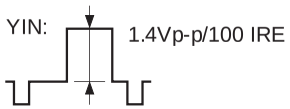
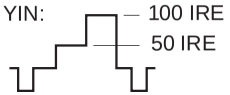
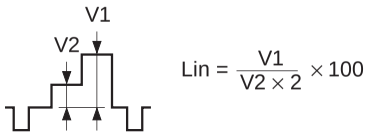
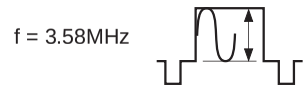
No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
1	Signal block current consumption	SI_{CC}	SV_{CC} = 9.0V, Bus data = center	6	Measure the pin inflow current.	40	65	90	mA
2	Sync block current consumption	JI_{CC}	JV_{CC} = 9.0V, Bus data = center	34	Measure the pin inflow current.	25	45	60	mA

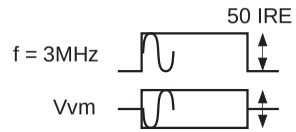
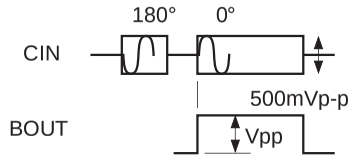
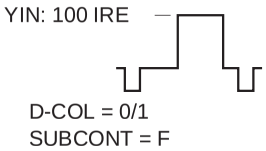
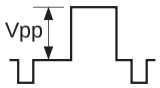
Sync deflection block items

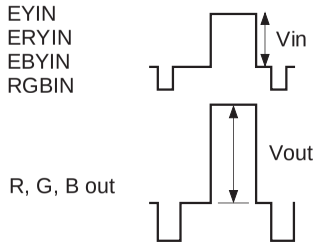
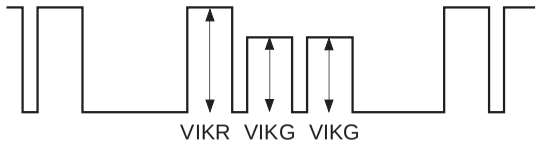
No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
3	Horizontal free-running frequency	f_{HFR}	AFC MODE = 0H	35	HDRIVE output frequency	15.55	15.734	15.9	kHz
4	Horizontal sync pull-in range	Δf_{HR}	SYNC IN: composite sync	—	Confirm that I^2C status register HLOCK is 1 (the pull-in range when f_H is shifted from 15.734kHz).	–400	—	400	Hz
5	HD output pulse width	HDw	SYNC IN: composite sync	35	Measure the pulse width for the section where the HDRIVE output is high.	24.5	25.5	26.5	µs
6	BGP output pulse width	VBGPh		46	Measure the pulse width for the section where the BGP output is high.	3.1	4.0	4.9	µs
7	VDRIVE output amplitude	VSpp	SYNC IN: composite sync	29, 30	Measure the VDRIVE output Vp-p. 	0.8	0.95	1.1	V
8	VDRIVE output center potential	VSdc		29, 30	43: VSIN in 	2.9	3.0	3.15	V

No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
9	EWDRIVE output amplitude	VEWpp	SYNC IN: composite sync	31	Measure the EWDRIVE output Vp-p. 	0.5	0.65	0.8	V
10	EWDRIVE output center potential	VEWdc		31	43: VSIN in 	3.7	4.0	4.2	V

Signal block items

No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
11	R, G and B output amplitude	VRout1		20, 22, 24	Output amplitude when a video signal with an amplitude of 1.4Vp-p/100 IRE is input	2.1	2.4	2.7	V
12	R, G and B output linearity	Lin		20, 22, 24		95	100	105	%
13	C-TRAP attenuation	C-Trap	 C-TRAP = 0/1 CTRAP-ADJ = 7H	20	Input fsc to YIN. Ratio of the fsc component of the Rout amplitude when CTRAP=1 against the Rout amplitude when CTRAP=0. 	—	–37.5	—	dB

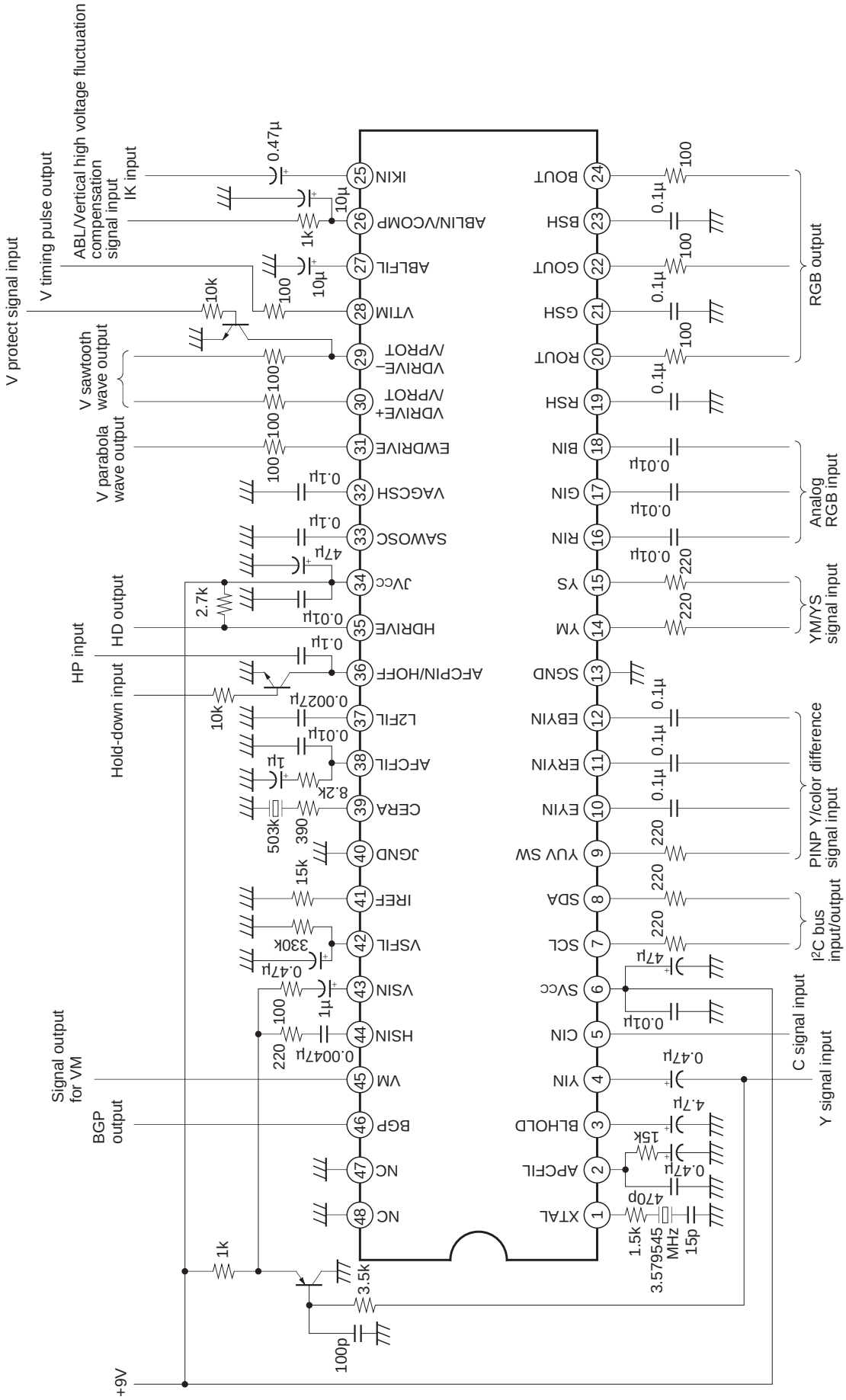
No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
14	VM output	Vvm	YIN: 3MHz, 50 IRE VM = 1	45		1.5	2.2	2.4	V
15	Color gain	Vcol	YIN: GND CIN: burst +180°, 500mVp-p COLOR = 1F	24		0.75	0.98	1.2	V
16	Hue center offset	ϕoffset	HUE = 1F, SUB-HUE = 7	—		–8.5	0	8.5	deg
17	Killer point	KP	YIN = GND CIN: Burst only	—	Confirm that status register KILLER is 1 when the burst level is –31dB assuming burst 570mVp-p to be 0dB.	—	–31	—	dB
18	APC pull-in range	Δf_{APC}		—	Confirm that the burst frequency is pulled in at 3.58MHz ±400Hz.	–400	—	400	Hz
19	Dynamic color operation R output	ΔGdcolR		20	ROUT, BOUT 	94	96	98	%
20	Dynamic color operation B output	ΔGdcolB		24	$\Delta GdcolR = \frac{Vpp\ (DCOL = 1)}{Vpp\ (DCOL = 0)} \times 100$ $\Delta GdcolB = \frac{Vpp\ (DCOL = 1)}{Vpp\ (DCOL = 0)} \times 100$	104	106	108	%
21	YM gain	ΔGYM		20, 22, 24	Output amplitude ratio when the R, G and BOUT YM = 1	–7.1	–6.1	–5.1	dB

No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents		Min.	Typ.	Max.	Unit
22	R output amplitude during external EY input	VRout2	YUVSW: 2V EYIN: 0.7V	20		VRout2 = Vout	2.05	2.4	2.75	V
23	R output amplitude during external R-Y input	VRout3	YUVSW: 2V ERYIN: 0.4V	20		VRout3 = Vout	1.75	2.2	2.65	V
24	B output amplitude during external B-Y input	VBout1	YUVSW: 2V EBYIN: 0.4V	24		VBout1 = Vout	1.34	1.64	1.94	V
25	R output amplitude during external R input	VLRout	YS: 1V RGBIN: 0.7V	20		VRout = Vout	1.9	2.23	2.55	V
26	G output amplitude during external G input	VLGout	YS: 1V RGBIN: 0.7V	22		VGout = Vout	1.9	2.23	2.55	V
27	B output amplitude during external B input	VLBout	YS: 1V RGBIN: 0.7V	24		VBout = Vout	1.9	2.23	2.55	V
28	IK level R	VIKR	SYNC IN: composite sync	25			0.8	0.98	1.16	V
29	IK level G	VIKG	GCUTOFF = 0 BCUTOFF = 0	25			0.24	0.42	0.6	V
30	IK level B	VIKB		25			0.24	0.42	0.6	V

Electrical Characteristics Measurement Conditions "I²C bus register initial settings"

PICTURE	= 3F Hex	C-TRAP	= 0
VM	= 0	HUE	= 1F Hex
DC-TRAN	= 0	D-PIC	= 0
COLOR	= 1F Hex	TOT	= 0
AXIS	= 0	BRIGHT	= 1F Hex
D-COL	= 0	ABL	= 0
SHARPNESS	= 7 Hex	PRE-OVER	= 3
SHP-F0	= 2	SUB-CONT	= 7 Hex
CTRAP-ADJ	= 7 Hex	SUB-COLOR	= 7 Hex
SUB-HUE	= 7 Hex	SUB-BRIGHT	= 1F Hex
GAMMA	= 0	G-DRIVE	= 2A Hex
AGING1	= 0	AGING2	= 0
B-DRIVE	= 2A Hex	G-CUTOFF	= 0
B-CUTOFF	= 0	EY-SW	= 0
CD-MODE2	= 0	RON	= 1
GON	= 1	BON	= 1
PICON	= 1	VOFF	= 0
FHHI	= 0	CD-MODE	= 0
AKBOFF	= 0	V-SIZE	= 1F Hex
V-COMP	= 0	V-POSITION	= 1F Hex
AFC-MODE	= 1	S-CORR	= 0
V-LIN	= 7 Hex	H-SIZE	= 1F Hex
REF-POSI	= 3	PIN-COMP	= 1F Hex
VBLKW	= 0	H-POSITION	= 7 Hex
PIN-PHASE	= 7 Hex	UP-CPIN	= 0
LO-CPIN	= 0	AFC-BOW	= 7 Hex
AFC-ANGLE	= 7 Hex	V-ASPECT	= 0 Hex
ZOOMSW	= 0	HBLKSW	= 0
V-SCROLL	= 1F Hex	JMPSW	= 0
UP-VLIN	= 0 Hex	LO-VLIN	= 0 Hex
LEFT-BLK	= 7 Hex	RIGHT-BLK	= 7 Hex

Application Circuit

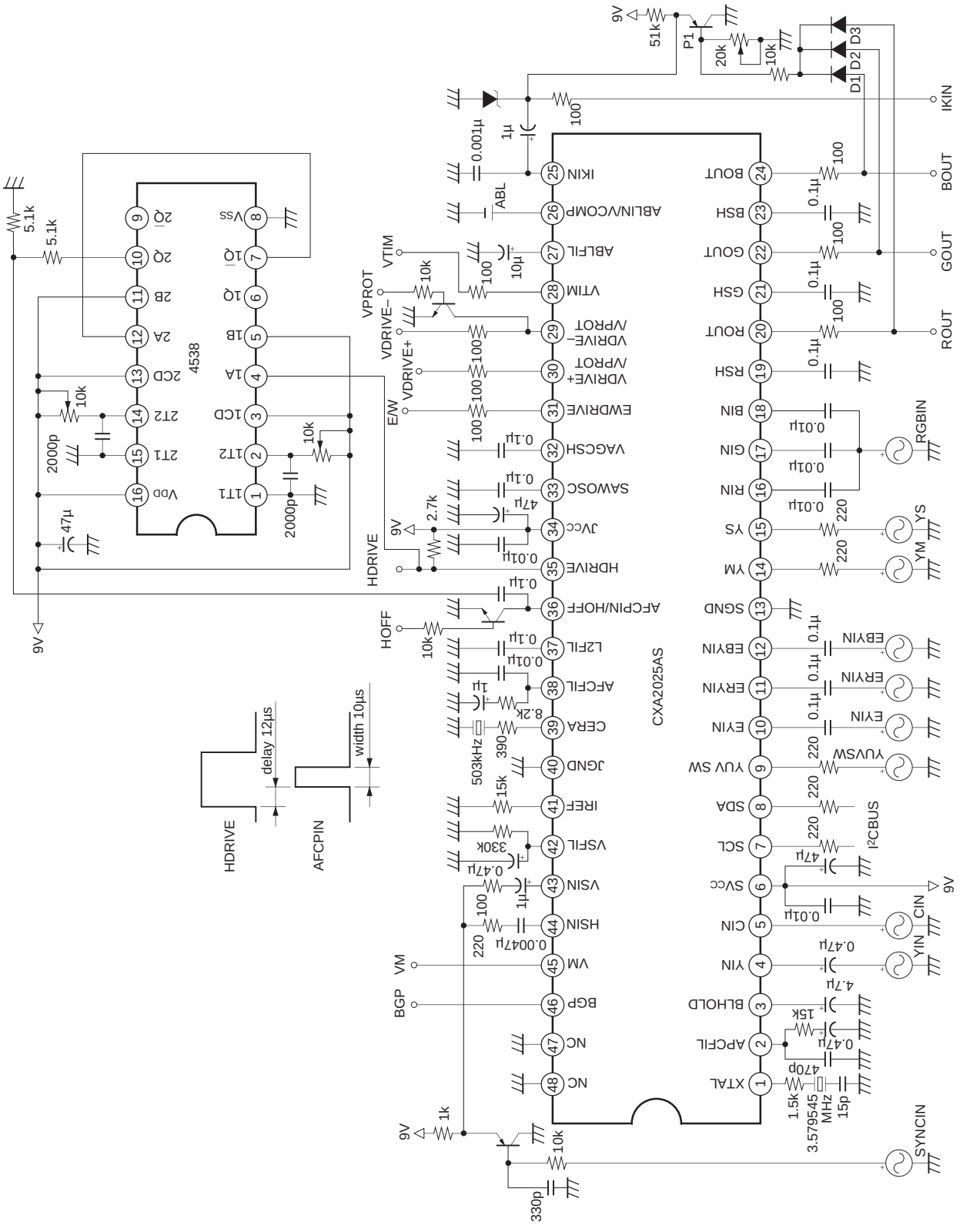


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Electrical Characteristics Measurement Circuit

Signal sources ⏦ are all GND unless otherwise specified in the Measurement conditions column of Electrical Characteristics.

ABL ⏚ is 9V unless otherwise specified.



Definition of I²C Bus Registers

Slave Addresses

88H: Slave receiver

89H: Slave transmitter

Control Register

Sub Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
＊＊＊0 0000 00 H	PICTURE						C-TRAP	VM
＊＊＊0 0001 01 H	HUE						DC-TRAN	D-PIC
＊＊＊0 0010 02 H	COLOR						TOT	AXIS
＊＊＊0 0011 03 H	BRIGHT						D-COL	ABL
＊＊＊0 0100 04 H	SHARPNESS				PRE-OVER		SHP-F0	
＊＊＊0 0101 05 H	SUB-CONT				CTRAP-ADJ			
＊＊＊0 0110 06 H	SUB-COLOR				SUB-HUE			
＊＊＊0 0111 07 H	SUB-BRIGHT						GAMMA	
＊＊＊0 1000 08 H	G-DRIVE						AGING1	AGING2
＊＊＊0 1001 09 H	B-DRIVE						EY-SW	CD-MODE2
＊＊＊0 1010 0A H	G-CUTOFF				B-CUTOFF			
＊＊＊0 1011 0B H	RON	GON	BON	PICON	VOFF	FHHI	CD-MODE	AKBOFF
＊＊＊0 1100 0C H	V-SIZE						V-COMP	
＊＊＊0 1101 0D H	V-POSITION						AFC-MODE	
＊＊＊0 1110 0E H	S-CORR				V-LIN			
＊＊＊0 1111 0F H	H-SIZE						REF-POSI	
＊＊＊1 0000 10 H	PIN-COMP						VBLKW	
＊＊＊1 0001 11 H	H-POSITION				PIN-PHASE			
＊＊＊1 0010 12 H	UP-CPIN				LO-CPIN			
＊＊＊1 0011 13 H	AFC-BOW				AFC-ANGLE			
＊＊＊1 0100 14 H	V-ASPECT						ZOOMSW	HBLKSW
＊＊＊1 0101 15 H	V-SCROLL						JMPSW	0
＊＊＊1 0110 16 H	UP-VLIN				LO-VLIN			
＊＊＊1 0111 17 H	LEFT-BLK				RIGHT-BLK			

Status Register

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
HLOCK	IKR	VNG	HNG	KILLER	0	1	0

Note) EY-SW and CD-MODE2 have been added to the CXA2025S.

Description of Registers

Register name	No. of bits	Function
PICTURE	(6)	: Picture gain control (RGB gain control) 0H = –15dB 3FH = 0dB RGB output: 2.4Vp-p (I/O gain: +4.7dB, 1.4Vp-p input)
C-TRAP	(1)	: Y block chroma trap ON/OFF switch 0 = Trap OFF 1 = Trap ON (Y signal delay time adjusted when C-TRAP turned ON or OFF.)
VM	(1)	: Y signal differential output ON/OFF switch for VM 0: Output OFF 1: Output ON (2.0Vp-p)
HUE	(6)	: Hue control (Chroma demodulation axis control when SUB-HUE is 8H) 0H = +35° Flesh color appears red. 1FH = 0° 3FH = –35° Flesh color appears green
DC-TRAN	(1)	: Y DC transmission ratio selector switch 0 = 100% 1 = 82%
DPIC	(1)	: Y black expansion ON/OFF switch 0 = OFF 1 = ON Point of inflection: 30 IRE
COLOR	(6)	: (Color gain control) 0H = Color OFF (–40dB or less) 1FH = 0dB B output: 1.1Vp-p (I/O gain: +5.7dB, 0.57Vp-p input) 3FH = +5.4dB
TOT	(1)	: Chroma TOT filter band selector switch 0 = TOT-TRAP OFF 1 = TOT-TRAP ON (TRAP f0 2.0MHz)
AXIS	(1)	: R-Y, G-Y axis selector switch 0 = Japan axis R-Y: 95° × 0.78, G-Y: 240° × 0.3 1 = US axis R-Y: 112° × 0.83, G-Y: 252° × 0.3 (B-Y: 0° × 1)

BRIGHT (6) : Bright level control (RGB DC bias control)
0H = –300mV
1FH = 0mV –300mV from REF-P level
3FH = +300mV

D-COL (1) : Dynamic color ON/OFF switch
0 = Dynamic color OFF
1 = Dynamic color ON (R, Bch level control)

ABL (1) : ABL mode selector switch
0 = Picture ABL mode
1 = Picture/bright ABL mode

SHARPNESS (4) : Sharpness gain control (Y aperture correction gain control)
0H = –8dB
7H = 1dB
FH = +5.1dB

PRE-OVER (2) : Sharpness preshoot/overshoot ratio control
0H = 1:1 (PRE:OVER)
3H = 5:1

SHP-F0 (2) : Sharpness f0 control (Delay line current control for aperture correction)
0H = 2.5MHz
3H = 4.0MHz

SUB-CONT (4) : Contrast gain control (Y gain control)
0H = –3.0dB
7H = 0dB
FH = +2.5dB

CTRAP-ADJ (4) : Chroma trap f0 adjustment (Y block chroma trap current control)
0H = +300kHz
7H = 0kHz
FH = –300kHz
fsc adjustable to –30dB or less (SHP-F0 min.); adjustment value: 3 to 4

SUB-COLOR (4) : Color gain control (ACC reference level control)
0H = –4.0dB
7H = 0dB
FH = +2.1dB

SUB-HUE (4) : Hue control (Phase control for chroma demodulation axis when HUE is 1FH)
0H = +10°
7H = 0
FH = –10°
B-Y axis adjustable to 0°

SUB-BRIGHT (6) : Bright level control (RGB DC bias control)
0H = –300mV
1FH = 0mV –300mV from REF-P level
3FH = +300mV

GAMMA (2) : Gamma control (RGB gamma correction amount control)
0H = Gamma OFF
3H = Gamma peak (40 IRE) +400mV

G-DRIVE (6) : Gch drive gain adjustment (Gch gain control)
0H = G/R –3.8dB
2AH = G/R 0dB
3FH = G/R +2.5dB

AGING1 (1) : White output aging mode ON/OFF switch
(Has priority over RGBON and PICON control, set to OFF mode at power-on.)
0 = Aging mode OFF
1 = Aging mode ON 60 IRE flat signal output from Y block when input signal present.

AGING2 (1) : Black output aging mode ON/OFF switch
(Has priority over AGING1, set to OFF mode at power-on.)
0 = Aging mode OFF
1 = Aging mode ON Black level output.

B-DRIVE (6) : Bch drive gain adjustment (Bch gain control)
0H = B/R –3.8dB
2AH = B/R 0dB
3FH = B/R +2.5dB

EY-SW (1) : Internal Y signal fixed mode ON/OFF switch
0 = YUV SW (Pin 9) standard operation. (EYIN, ERYIN and EBYIN input selected when Pin 9 = high.)
1 = EYIN (Pin 10) input only invalid. (Internal Y, ERYIN and EBYIN input selected when Pin 9 = high.)

CD-MODE2 (1) : Vertical sync pull-in speed switch
0 = Standard (equivalent to CXA2025S)
1 = High speed

G-CUTOFF (4) : Gch cut-off adjustment (Gch reference pulse value control of IKIN pin input)
0H = –45%
7H = 83% (G/R)
FH = +133%

B-CUTOFF (4) : Bch cut-off adjustment (Bch reference pulse value control of IKIN pin input)
0H = –45%
7H = 83% (B/R)
FH = +133%

RON (1) : ON/OFF switch for Rch video output without a reference pulse
(Operates when PICON = 1, set to OFF mode at power-on.)
0 = Rch video output OFF (Blanked status, reference pulse only output)
1 = Rch video output ON

GON (1) : ON/OFF switch for Gch video output without a reference pulse
(Operates when PICON = 1, set to OFF mode at power-on.)
0 = Gch video output OFF (Blanked status, reference pulse only output)
1 = Gch video output ON

BON (1) : ON/OFF switch for Bch video output without a reference pulse
(Operates when PICON = 1, set to OFF mode at power-on.)
0 = Bch video output OFF (Blanked status, reference pulse only output)
1 = Bch video output ON

PICON (1) : ON/OFF switch for RGB output with a reference pulse (Set to OFF mode at power-on.)
0 = RGB output OFF (All blanked status)
1 = RGB output ON

VOFF (1) : V sawtooth wave oscillation stop ON/OFF switch (Set to ON mode at power-on.)
0 = Oscillation stop OFF (VDRIVE– and VDRIVE+: normal output)
1 = Oscillation stop ON (VDRIVE– and VDRIVE+: DC output and DC value vary according to V-POSITION.)

FHHI (1) : H oscillator frequency fixation ON/OFF switch (Set to ON mode at power-on.)
0 = H oscillator frequency fixation OFF AFC normal mode
1 = H oscillator frequency fixation ON Oscillator frequency fixed to maximum value (16.252kHz).

CD-MODE (1) : V countdown system mode selector switch
(Set to automatic selection mode during power-on.)
0 = Non-standard signal mode, standard signal mode and no signal mode automatically selected
1 = Fixed to non-standard signal mode
(V oscillator frequency is 55Hz during no signal mode (free run).)

AKBOFF (1) : AKB ON/OFF switch (Set to ON mode at power-on.)
0 = AKB ON
1 = AKB OFF IK clamp, IK S/H and reference pulse fixed to OFF.
R, G and B cut-off adjustment at AKB OFF performed by voltage applied to Pins 19 (RSH), 21 (GSH) and 23 (BSH), respectively.

V-SIZE (6) : Vertical amplitude adjustment (V sawtooth wave gain control: Func.)
0H = –14% Vertical picture size decreases.
1FH = 0% Amplitude: 1.15Vp-p, center potential: DC 3V when V-ASPECT is 1FH
3FH = +14% Vertical picture size increases.

V-COMP (2) : Compensation amount setting for vertical high voltage fluctuation (V sawtooth wave gain control: Func.)
0H = 0% V sawtooth wave amplitude compensation amount when VCOMP (Pin 26) is 1V
3H = –5% V sawtooth wave amplitude compensation amount when VCOMP (Pin 26) is 1V

V-POSITION (6) : Vertical position adjustment (V sawtooth wave DC bias control: Func.)
0H = –0.09V Picture position drops, VDRIVE+ output DC Down.
1FH = 0V Center DC: 3V
2FH = +0.09V Picture position rises, VDRIVE+ output DC Up.

AFC MODE (2) : AFC loop gain control (PLL between Hsync and Hvco)
0H = H free run mode
1H = Small gain
2H = Medium gain
3H = Large gain

S-CORR (4) : Vertical S correction amount adjustment (V sawtooth wave secondary component gain control: Func.)
0H = Secondary component amplitude by adding sawtooth and other signals = 0
FH = Secondary component amplitude by adding sawtooth and other signals = Maximum

V-LIN (4) : Vertical linearity adjustment (Gain control for V sawtooth wave secondary component: Func.)
0H = 85% (Bottom/top of picture) Top of picture expanded; bottom of picture compressed.
7H = 100% (Bottom/top of picture)
FH = 115% (Bottom/top of picture) Top of picture compressed; bottom of picture expanded.

H-SIZE (6) : Horizontal amplitude adjustment (V parabola wave DC bias control: Func.)
0H = –0.5V Horizontal picture size decreases, EWDRIVE output DC Down.
1FH = 0V Amplitude: 0.58Vp-p, center: DC 4V when V-ASPECT is 2FH
3FH = +0.5V Horizontal picture size increases, EWDRIVE output DC Up.

REF-POSI (2) : Reference pulse timing setting
0H = (From VTIM rise) Rch: 22H, Gch: 23H, Bch: 24H
1H = (From VTIM rise) Rch: 20H, Gch: 21H, Bch: 22H
2H = (From VTIM rise) Rch: 18H, Gch: 19H, Bch: 20H
3H = (From VTIM rise) Rch: 16H, Gch: 17H, Bch: 18H

PIN-COMP (6) : Horizontal pin distortion compensation amount adjustment (V parabola wave gain control: Func.)
0H = 0.11Vp-p Compensation amount minimum
1FH = 0.47Vp-p Center potential: DC 4V when V-ASPECT is 2FH
3FH = 0.84Vp-p Compensation amount maximum

VBLKW (2) : VBLK width control (Blanked pulses after reference pulse. Operates when JMPSW = 1; blanked pulses after reference pulse fixed to 1H when JMPSW = 0.)
0H = 12H from Bch REF-P
1H = 11H from Bch REF-P
2H = 10H from Bch REF-P
3H = 9H from Bch REF-P

H-POSITION (4) : Horizontal position adjustment (HAFC phase control)
0H = 1µs delay Picture position shifts to right. Video delayed with respect to HD.
7H = 0µs
FH = 1µs advance Picture position shifts to left. Video advanced with respect to HD.

PIN-PHASE (4) : Horizontal trapezoidal distortion compensation adjustment (V parabola wave center timing control: Func.)
0H = 1.5ms advance Horizontal size for top of picture increases; horizontal size for bottom of picture decreases.
7H = 0ms 8.9ms from 4VDC VTIM
FH = 1.5ms delay Horizontal size for top of picture decreases; horizontal size for bottom of picture increases.

UP-CPIN (4) : Horizontal pin distortion compensation amount adjustment for top of picture (V parabola wave gain control: Func.)
0H = +0.2V Horizontal size for top of picture increases (Compensation amount minimum).
7H = 0V (0.7Vp-p, 4:3 mode)
FH = –0.2V Horizontal size for top of picture decreases (Compensation amount maximum).

LO-CPIN (4) : Horizontal pin distortion compensation amount adjustment for bottom of picture (V parabola wave gain control: Func.)
0H = +0.2V Horizontal size for bottom of picture increases (Compensation amount minimum).
7H = 0V (0.7Vp-p, 4:3 mode)
FH = –0.2V Horizontal size for bottom of picture decreases (Compensation amount maximum).

AFC-BOW (4) : Vertical bow line compensation amount adjustment (Phase control according to HAFC parabola wave)
0H = Top and bottom of picture delayed 500ns with respect to picture center.
7H = 0ns
FH = Top and bottom of picture advanced 500ns with respect to picture center.

AFC-ANGLE (4) : Vertical line slope compensation amount adjustment (Phase control according to HAFC sawtooth wave)
0H = Top of picture delayed 500ns, bottom of picture advanced 500ns with respect to picture center.
7H = 0ns
FH = Top of picture advanced 500ns, bottom of picture delayed 500ns with respect to picture center.

V-ASPECT (6) : Aspect ratio control
(Gain control for sawtooth wave input to Func.: Mode)
0H = 75% 16:9 CRT full
2FH = 100% 4:3 CRT full, amplitude: 1.23Vp-p
3FH = 112%

ZOOMSW (1) : Zoom mode ON/OFF switch for 16:9 CRT
(Top and bottom of sawtooth wave input to Func. squeezed and 25% of video cut: Mode)
0 = Zoom OFF Sawtooth wave amplitude: 1.23Vp-p
1 = Zoom ON Sawtooth wave amplitude: 70%

HBLKSW (1) : HBLK width control ON/OFF switch during 4:3 software full display mode on a 16:9 CRT
0 = Control OFF HBLK pulse generated from HPIN.
1 = Control ON HBLK pulse generated as pulse generated from HPIN or as pulse generated from HVCO and width adjusted.
Width adjustment is performed by the LEFT-BLK and RIGHT-BLK registers.

V-SCROLL (6) : Vertical picture scroll control during zoom mode on a 16:9 CRT
(DC component added to sawtooth wave AGC output to control ZOOMSW cut timing.: Mode)
0H = –0.25V Scrolled toward top of screen by 32H and top of picture zoomed.
1FH = 0V
3FH = +0.25V Scrolled toward bottom of screen by 32H and bottom of picture zoomed.

JUMPSW (1) : Reference pulse jump mode ON/OFF switch
(In addition to V-ASPECT control, sawtooth wave gain control performed for 100% of VBLK interval and 67% of picture interval: Mode)
0 = Jump mode OFF
1 = Jump mode ON
On a 4:3 CRT, jump mode expands the sawtooth wave amplitude to 112% with V-ASPECT; on a 16:9 CRT, jump mode compresses the sawtooth wave amplitude to 75% with V-ASPECT. The V blanking width is expanded at both the top and bottom of the picture. Blanking for the bottom of the picture starts 251H after VTIM, and blanking for the top of the picture can be varied as the blanking width after the reference pulse from the VBLKW register.

UP-VLIN (4) : Vertical linearity adjustment for top of picture
(Secondary component gain control for sawtooth wave added to sawtooth wave AGC output: Mode)
0H = 100% (Bottom/top of picture)
FH = 115% (Bottom/top of picture) Top of picture compressed.

LO-VLIN (4) : Vertical linearity adjustment for bottom of picture
(Tertiary component gain control for sawtooth wave added to sawtooth wave AGC output: Mode)
0H = 100% (Bottom/top of picture)
FH = 85% (Bottom/top of picture) Bottom of picture compressed.

LEFT-BLK (4) : HBLK width control for left side of picture when HBLKSW = 1
(Phase control for timing pulse generated from HVCO)
0H = +1.3µs HBLK width maximum
7H = 0µs Center HBLK: 13µs
FH = –1.3µs HBLK width minimum

RIGHT-BLK (4) : HBLK width control for the right side of picture when HBLKSW = 1
(Phase control for timing pulse generated from HVCO)
0H = +1.3µs HBLK width maximum
7H = 0µs Center HBLK: 13µs
FH = –1.3µs HBLK width minimum

HLOCK (1) : Lock status between Hsync and HVCO
0 = HVCO free run status
1 = Locked to Hsync

IKR (1) : AKB operation status
0 = REF-P return small and AKB loop unstable.
1 = REF-P return sufficient and AKB loop stable.

VNG (1) : Signal input status to VPROT pin
0 = No VPROT input
1 = VPROT input

HNG (1) : Signal input status to HOFF pin
0 = No HOFF input
1 = HOFF input

KILLER (1) : Color killer status
0 = Killer OFF status
1 = Killer ON status

Note) The following have been added to the CXA2025S.
EY-SW: Sub Add 09H, Bit 1
CD-MODE2: Sub Add 09H, Bit 0

Description of Operation

1. Power-on sequence

The CXA2025AS does not have an internal power-on sequence. Therefore, all IC operations are controlled by the set microcomputer (I^2C bus controller).

1) Power-on

The IC is reset and the RGB outputs are all blanked. Hdrive starts to oscillate, but oscillation is at the maximum frequency (16kHz or more) and is not synchronized to the input signal. Output of vertical signal VTIM starts, but Vdrive is DC output. Bus registers which are set by power-on reset are as follows.

AGING1 = 0: All white output aging mode OFF
AGING2 = 0: All black output aging mode OFF
RON = 0: Rch video blanking ON
GON = 0: Gch video blanking ON
BON = 0: Bch video blanking ON
PICON = 0: RGB all blanking ON
VOFF = 1: VDRIVE output stopped mode
FHHI = 1: H oscillator maximum frequency mode
CD-MODE = 0: Automatic selector mode of the countdown mode
AKBOFF = 0: AKB mode

2) Bus register data transfer

The register setting sequence differs according to the set sequence. Register settings for the following sequence are shown as an example.

Set sequence	CXA2025AS register settings
Power-on	Reset status in 1) above.
↓	↓
Degauss	Reset status in 1) above. The CRT is degaussed in the completely darkened condition.
↓	↓
VDRIVE oscillation	The IC is set to the power-on initial settings. (See the following page.) A sawtooth wave is output to VDRIVE and the IC waits for the vertical deflection to stabilize. The HDRIVE oscillator frequency goes to the standard frequency (around 15.734kHz).
↓	↓
AKB operation start	PICON is set to 1 and a reference pulse is output from Rout,Gout and Bout. Then, the IC waits for the cathode to warm up and the beam current to start flowing.
↓	↓
AKB loop stable	Status register IKR is monitored. IKR = 0: No cathode current IKR = 1: Cathode current Note that the time until IKR returns to 1 differs according to the initial status of the cathode.
↓	↓
Video output	RON, GON and BON are set to 1 and the video signal is output from Rout,Gout and Bout.

3) Power-on initial settings

The initial settings listed here are reference values, and initial settings may be determined freely according to the set usage conditions.

PICTURE	= 3F Hex	Max (User Cont.)
C-TRAP	= 0	Chroma Trap OFF
VM	= 1	VM out ON
HUE	= 1F Hex	Center (User Cont.)
DC-TRAN	= 0	Y DC transmission ratio 100%
D-PIC	= 1	Y black expansion ON
COLOR	= 1F Hex	Center (User Cont.)
TOT	= 0	Chroma low frequency increased
AXIS	= 0	R-Y, G-Y Japan axis
BRIGHT	= 1F Hex	Center (User Cont.)
D-COL	= 1	Dynamic Color ON
ABL	= 1	Picture/bright ABL mode
SHARPNESS	= 7 Hex	Center (User Cont.)
PRE-OVER	= 0	Sharpness pre/over ratio 2:1
SHP-F0	= 1	Sharpness f0 3MHz
SUB-CONT	= 7 Hex	Center (Adjust)
CTRAP-ADJ	= 7 Hex	Center (Adjust)
SUB-COLOR	= 7 Hex	Center (Adjust)
SUB-HUE	= 7 Hex	Center (Adjust)
SUB-BRIGHT	= 1F Hex	Center (Adjust)
GAMMA	= 0	Gamma OFF
G-DRIVE	= 1F Hex	Center (Adjust)
AGING1	= 0	Aging Mode OFF
AGING2	= 0	Aging Mode OFF
B-DRIVE	= 1F Hex	Center (Adjust)
G-CUTOFF	= 7 Hex	Center (Adjust)
B-CUTOFF	= 7 Hex	Center (Adjust)
EY-SW	= 0	Standard
CD-MODE2	= 0	Standard
RON	= 0	Rch video output OFF
GON	= 0	Gch video output OFF
BON	= 0	Bch video output OFF
PICON	= 0	RGB all blanked
VOFF	= 0	Vdrive oscillation stopped
FHHI	= 0	Horizontal oscillator frequency standard
CD-MODE	= 0	V countdown auto mode
AKBOFF	= 0	AKB ON
V-SIZE	= 1F Hex	Center (Adjust)
V-COMP	= 3	Vertical high voltage fluctuation compensation amount max.
V-POSITION	= 1F Hex	Center (Adjust)
AFC-MODE	= 2	Center
S-CORR	= 7 Hex	Center (Adjust)
V-LIN	= 7 Hex	Center (Adjust)
H-SIZE	= 1F Hex	Center (Adjust)
REF-POSI	= 0	
PIN-COMP	= 1F Hex	Center (Adjust)
VBLKW	= 0	

(Power-on initial settings cont.)

H-POSITION	= 7 Hex	Center (Adjust)
PIN-PHASE	= 7 Hex	Center (Adjust)
UP-CPIN	= 7 Hex	Center (Adjust)
LO-CPIN	= 7 Hex	Center (Adjust)
AFC-BOW	= 7 Hex	Center (Adjust)
AFC-ANGLE	= 7 Hex	Center (Adjust)
V-ASPECT	= 0 Hex	16:9 CRT Full Mode
ZOOMSW	= 1	16:9 CRT
HBLKSW	= 1	Hblk width adjust ON
V-SCROLL	= 1F Hex	Center (User)
JMPSW	= 0	16:9 CRT Full Mode
UP-VLIN	= 7 Hex	16:9 CRT Full Mode
LO-VLIN	= 7 Hex	16:9 CRT Full Mode
LEFT-BLK	= F Hex	Hblk width min.
RIGHT-BLK	= F Hex	Hblk width min.

2. Various mode settings

The CXA2025AS contains bus registers for deflection compensation which can be set for various wide modes. Wide mode setting registers can be used separately from registers for normal picture distortion adjustment, and once deflection adjustment has been performed in full mode, wide mode settings can be made simply by changing the corresponding register data.

- VDRIVE signal picture distortion adjustment registers
  V-SIZE, V-POSITION, S-CORR, V-LIN
- E/WDRIVE signal picture distortion adjustment registers
  H-SIZE, PIN-COMP, PIN-PHASE, UP-CPIN, LO-CPIN
- Wide mode setting registers
  V-ASPECT, ZOOMSW, HBLKSW, V-SCROLL, JMPSW, UP-VLIN, LO-VLIN, LEFT-BLK, RIGHT-BLK

Examples of various modes are listed below. These modes are described using 480 lines as the essential number of display scanning lines. Wide mode setting register data is also listed, but settings may differ slightly due to IC variation. The standard setting data differs for 16:9 CRTs and 4:3 CRTs.

Register	16:9 CRT	4:3 CRT
V-ASPECT	0 H	2F H
V-SCROLL	1F H	1F H
ZOOMSW	1	0
UP-VLIN	0 H	0 H
LO-VLIN	0 H	0 H
JMPSW	0	0
HBLKSW	0	0
LEFT-BLK	7 H	7 H
RIGHT-BLK	7 H	7 H

1) 16:9 CRT full mode

This mode reproduces the full 480 lines on a 16:9 CRT. 4:3 images are reproduced by stretching the picture to the left and right. Normal images are compressed vertically, but 16:9 images can be reproduced in their original 16:9 aspect ratio with a video source which compresses (squeezes) 16:9 images to 4:3 images.
The register settings are the 16:9 CRT standard values.

2) 16:9 CRT normal mode

In this mode, 4:3 images are reproduced without modification. A black border appears at the left and right of the picture. In this mode, the H deflection size must be compressed by 25% compared to full mode. The CXA2025AS also has a register (H-SIZE) which controls the H size, but the control width is not sufficient for 25% compression. Therefore, external measures must be taken such as switching the H deflection coil, etc. Full mode should be used when performing memory processing and attaching a black border to the video signal.
H blanking of the image normally uses the flyback pulse input to AFCPIN (Pin 36). However, the blanking width can be varied according to the control register setting when blanking is insufficient for the right and left black borders.
The following three settings are added to the 16:9 CRT standard values for the register settings.

HBLKSW = 1
LEFT-BLK = Adjustment value
RIGHT-BLK = Adjustment value

The H angle of deflection also decreases, causing it to differ from the PIN compensation amount during H size full status. Therefore, in addition to the wide mode registers, PIN-COMP must also be readjusted only for this mode.

3) 16:9 CRT zoom mode

In this mode, 4:3 images are reproduced by enlarging the picture without other modification. The top and bottom of normal 4:3 images are lost, but almost the entire picture can be reproduced for vista size video software, etc. which already has black borders at the top and bottom. The enlargement ratio can be controlled by the V-ASPECT register, and enlarging the picture by 33% compared to full mode allows zooming to be performed for 4:3 images without distortion. In this case, the number of scanning lines is reduced to 360 lines compared to 480 lines for full mode. The zooming position can be shifted vertically by the V-SCROLL register.
V blanking of the image normally begins from V sync and continues for 2H after the AKB reference pulse, and the top and bottom parts are also blanked during this mode.
Adjust the following two registers with respect to the 16:9 CRT standard values for the register settings.

V-ASPECT = 2FH
V-SCROLL = 1FH or user control

4) 16:9 CRT subtitle-in mode

When Cinema Scope size images which have black borders at the top and bottom of the picture are merely enlarged with the zoom mode in 3) above, subtitles present in the black borders may be lost. Therefore, this mode is used to super-compress only the subtitle part and reproduce it on the display.
Add the LO-VLIN adjustment to the zoom mode settings for the register settings.

V-ASPECT = 2FH
V-SCROLL = 1FH or user control
LO-VLIN = Adjustment value

The LO-VLIN register causes only the linearity at the bottom of the picture to deteriorate. Therefore, UP-VLIN should also be adjusted if the top and bottom of the picture are to be made symmetrical. Since the picture is compressed vertically, the number of scanning lines exceeds 360 lines.

5) 16:9 CRT V compression mode

This mode is used to reproduce two 4:3 video displays such as for PandP. The V size must be compressed to 67% in order to reproduce two displays on a 16:9 CRT without distortion using 480 scanning lines, and this can be set by JMPSW. Compression is performed after the AKB reference pulse, so the reference pulse remains in the overscan position. The V blanking width after the reference pulse becomes larger than normal and can be varied by the VBLKW register. During this mode, the bottom V blanking width is also expanded to 10H wider than normal so that the bottom of the picture is not overscanned.

16:9 CRT standard values are used with only the JMPSW setting changed for the register settings.

JMPSW = 1

6) 16:9 CRT Sony type wide zoom mode

This mode reproduces 4:3 video software naturally on wide displays by enlarging 4:3 images without other modification and compressing the parts of the image which protrude from the picture into the top and bottom parts of the picture. The display enlargement ratio is controlled by V-ASPECT, and the compression ratios at the top and bottom of the picture are controlled by UP-VLIN and LO-VLIN.

Adjust the following three registers with respect to the 16:9 CRT standard values for the register settings.

V-ASPECT = Adjustment value
UP-VLIN = Adjustment value
LO-VLIN = Adjustment value

7) 4:3 CRT normal mode

This is the standard mode for 4:3 CRTs.

The register settings are the 4:3 CRT standard values.

8) 4:3 CRT V compression mode

This mode is used to reproduce M-N converter output consisting of 16:9 images expanded to a 4:3 aspect ratio and other squeezed signals without distortion on a 4:3 CRT. The V size must be compressed to 75% in order to reproduce 4:3 images in a 16:9 aspect ratio. Compressing the V size with the JMPSW register used in mode 5) above, compresses the V size to 67%. Therefore, V-ASPECT is set to enlarge the V size by 8%. AKB reference pulse handling and V blanking are the same as for mode 5) above.

4:3 CRT standard values are used with the V-ASPECT and JMPSW settings changed for the register settings.

V-ASPECT = 3FH
JMPSW = 1

3. Signal processing

The CXA2025AS is comprised of sync signal processing, H deflection signal processing, V deflection signal processing, and Y/C/RGB signal processing blocks, all of which are controlled by the I^2C bus.

1) Sync signal processing

The Y signals input to Pins 43 and 44 are sync separated by the horizontal and vertical sync separation circuits. The resulting horizontal sync signal and the signal obtained by frequency dividing the 32 FH-VCO output using the ceramic oscillator (frequency 503.5kHz) by 32 are phase-compared, the AFC loop is constructed, and an H pulse synchronized with the H sync is generated inside the IC. Adjustment of the H oscillator frequency is unnecessary. When the AFC is locked to the H sync, 1 is output to the status register (HLOCK) and that can be used to detect the presence of the video signal.

The vertical sync signal is sent to the V countdown block where the most appropriate window processing is performed to obtain V sync timing information which resets the counter. AKB and other V cycle timing are then generated from this reset timing.

2) H deflection signal processing

The H pulse obtained through sync processing is phase-compared with the H deflection pulse input from Pin 36 to control the phase of the HDRIVE output and the horizontal position of the image projected on the CRT. In addition, the compensation signal generated from the V sawtooth wave changes the phase of HDRIVE.As a result,the vertical picture distortion is compensated.

The H deflection pulse is used to H blank the video signal. When the pulse input from Pin 36 has a narrow width, the pulse generated by the IC can be added to the H deflection pulse and used as the H blanking pulse. (HBLKSW)

Pin 36 is normally pulse input, but if the pin voltage drops to the GND level, HDRIVE output goes to high level (DC) and 1 is output to the status register (HNG). To release this status, turn the power off and then on again.

3) V deflection signal processing

The V sawtooth wave is generated at the cycle of the reset pulse output from the countdown system. After performing wide deflection processing for this sawtooth wave, picture distortion adjustment is performed by the VDRIVE and E/WDRIVE function circuits and the signal is output as the VDRIVE and E/WDRIVE signals.

4) Y signal processing

The Y signal input to Pin 4 (specified input level: level at which a 100% white (including sync, 140 IRE) signal with a gain of 6dB with respect to the video signal standard becomes a 2Vp-p signal) passes through the subcontrast control, trap for eliminating the chroma signal, sharpness control, clamp and black expansion circuits, and is then input to the switching circuit (YUV SW) for the external Y/color difference signal. The differential waveform of the Y signal delayed for approximately 200ns from the Y input is output from Pin 45 as the signal for VM.

The VM signal is not output in the following cases.

When EY-SW = 0 and YUV SW (Pin 9) or YS (Pin 15) = high

When EY-SW = 1 and YS (Pin 15) = high

The f0 of the built-in filter is automatically adjusted inside the IC, but the trap f0 may require fine adjustment by the I^2C bus (CTRAP-ADJ) if it is affected by variation. When inputting a signal which has been Y/C separated by a comb filter, etc., the trap should be turned OFF.

5) C signal processing

The chroma signal input to Pin 5 (specified input level: level at which a 40 IRE burst level signal with a gain of 6dB with respect to the video signal standard becomes a 570mVp-p signal) passes through the ACC, TOT (secondary HPF), color control and demodulation circuits. The signal then becomes the R-Y and B-Y color difference signal and is input to the YUV SW circuit. When the burst level goes to –31dB or less with respect to the specified input level, the color killer operates and the color difference signal is not output.

The external Y, color difference signals input to Pins 10, 11 and 12 passes through the clamp and amplifier circuits and are input to the YUV SW circuit. The YUV SW circuit is controlled by the YUV SW (Pin 9). However, its operation differs depending on the data in the I^2C bus register (EY-SW). In other words, the YUV SW circuit output is as follows.

When EY-SW = 0: Internal Y/color difference signal when YUV SW = low,
external Y/color difference signal (Pins 9, 10 and 11) when YUV SW = high

When EY-SW = 1: Internal Y/color difference signal when YUV SW = low,
internal Y/external color difference signal when YUV SW = high

When external Y/color difference signal is selected , the picture quality can be adjusted in the same manner as with the normal internal Y signal by setting EY-SW to 1 and then inputting the external Y signal to YIN (Pin 4). However, in this case the relative time difference between the Y and color difference signals must be realigned.

The specified input level for the external Y signal is the level at which a normal video signal standard, 100 IRE, 100% white signal becomes a 0.7Vp-p signal. The specified input level for the external color difference signal is the level at which a normal video signal standard, 40 IRE burst level demodulates a 258mVp-p chroma signal at orthogonal coordinates to become a 0.8 times signal (R-Y is demodulated by the 90° axis to become a 1.14 times signal, B-Y is demodulated by the 0° axis to become a 2.03 times signal).

The G-Y signal is generated as the base of Y, color difference signals at the axis adjustment circuit.The Y signal is added to R-Y, G-Y, and B-Y respectively and these signals become R, G, and B signals.And they are input to the RGB block.

6) RGB signal processing

The RGB signals obtained from the Y/C block pass through the half-tone switch circuit (YM SW), the switch circuit for the external RGB signal (YS SW), the picture control, dynamic color, gamma compensation, clamp, brightness control, drive adjustment, cut-off adjustment and auto cut-off circuits, and are output to Pins 20, 22 and 24.

The RGB signals input to Pins 16, 17 and 18 are the level at which a normal video standard, 100 IRE, 100% white signal becomes a 0.7Vp-p signal.

The voltage applied to Pin 26 (ABLIN) is compared with the internal reference voltage, integrated by the capacitor which is connected to Pin 27, and performs picture control and brightness control. In order to adjust the white balance (black balance), this IC has a drive control function which adjusts the gain between the RGB outputs and a cut-off control function which adjusts the DC level between the RGB outputs. Both drive control and cut-off control are adjusted by the I^2C bus, with the Rch fixed and the G and Bch variable. An auto cut-off function (AKB) which forms a loop between the IC and CRT and performs adjustment automatically has also been added. This function can compensate for changes in the CRT with time. Auto cut-off operation is as follows.

- R, G and B reference pulses for auto cut-off, shifted 1H each in the order mentioned, appear at the top of the picture (actually, in the overscan portion). The reference pulse uses 1H in the V blanking interval, and is output from each R, G and B output pin.
- The cathode current (IK) of each R, G and B output is converted to a voltage and input to Pin 25.
- The voltage input to Pin 25 is compared with the reference voltage in the IC, and the current generated by the resulting error voltage charges the capacitors connected to Pins 19, 21 and 23 for the reference pulse interval and is held during all other interval.
- The loop functions to change the DC level of the R, G and B outputs in accordance with the capacitor pin voltage so that the Pin 25 voltage matches the reference voltage in the IC.

The Rch for the reference voltage in the IC is fixed and the G and Bch are cut-off controlled by the I^2C bus. During G/B-CUTOFF center status, the loop functions so that the Rch for the reference pulse input to Pin 25 is 1Vp-p and the G and Bch are 0.83Vp-p.

The reference pulse timing can be varied by the I^2C bus.

When AKB is not used, the IC can be set to manual cut-off adjustment mode with I^2C bus settings. In this case, the DC level of the R, G and B outputs can be varied by applying voltages independently to Pins 19, 21 and 23.

4. Notes on operation

When designing the board pattern for the CXA2025AS, interference from around the power supply and GND should be considered as the RGB and deflection signals output from the CXA2025AS are DC direct connected. Do not separate the GND patterns for each pin; a solid earth is ideal. Locate the power supply side of the by-pass capacitor which is inserted between the power supply and GND as near to the pin as possible. Also, locate the XTAL oscillator, ceramic oscillator and IREF resistor as near to the pin as possible, and do not wire signal lines near this pin.

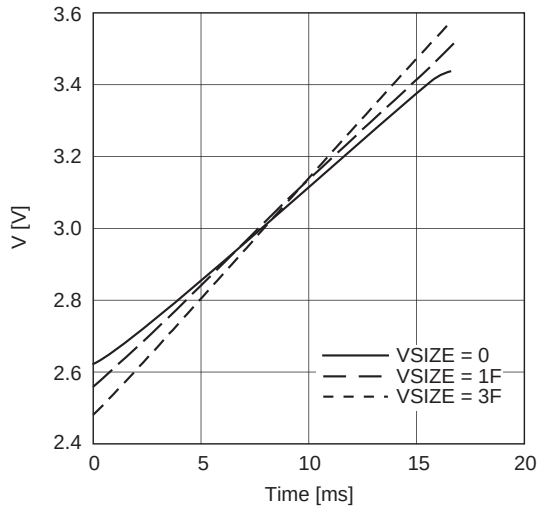
Drive the Y, external Y/color difference and external RGB signals at a sufficiently low impedance, as these signals are clamped when they are input using the capacitor connected to the input pin.

The built-in capacitor receives the chroma signal, so apply a DC bias of about $V_{CC}/2$ externally and input the chroma signal at a sufficiently low impedance.

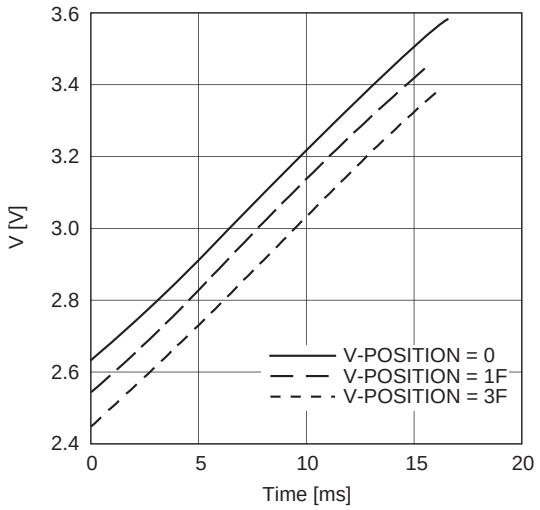
Curve Data

I²C bus data conforms to the "I²C bus register initial settings" of the Electrical Characteristics Measurement Conditions (P. 13).

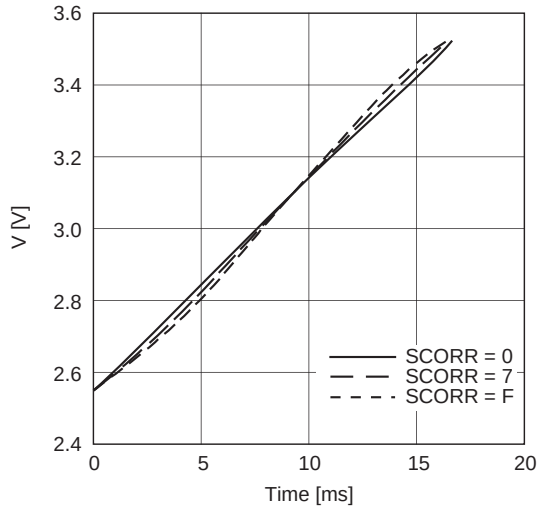
V-SIZE



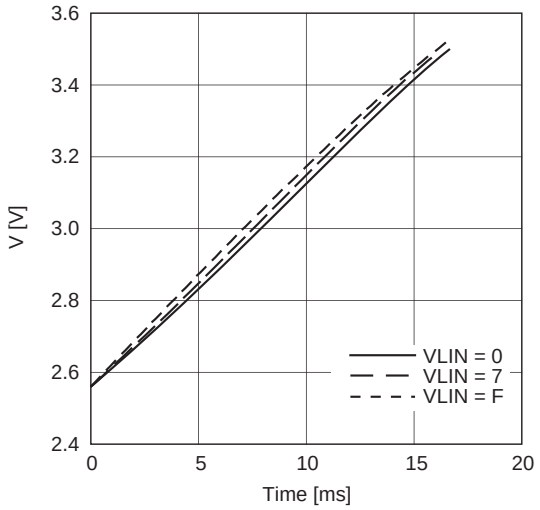
V-POSITION



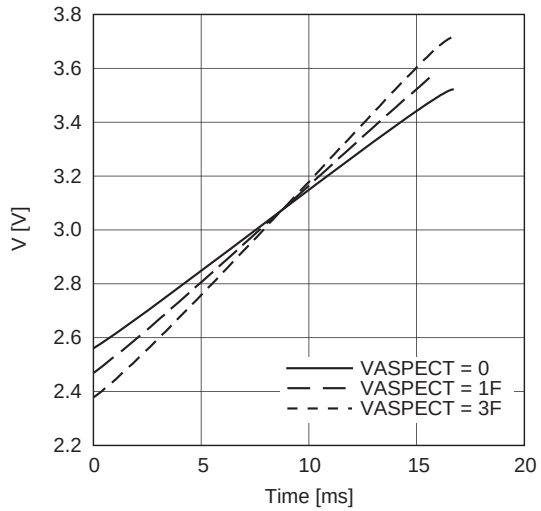
S-CORR



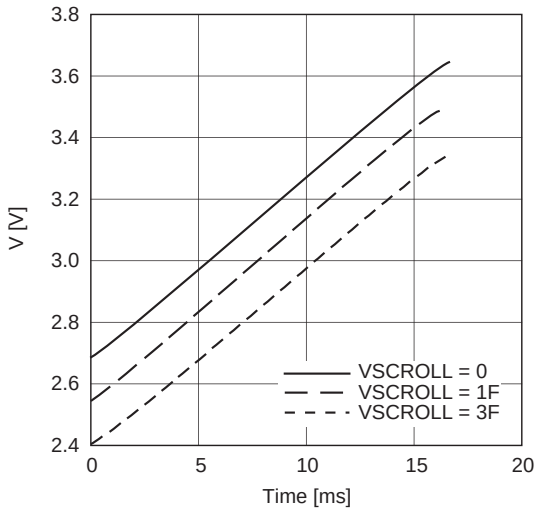
V-LIN



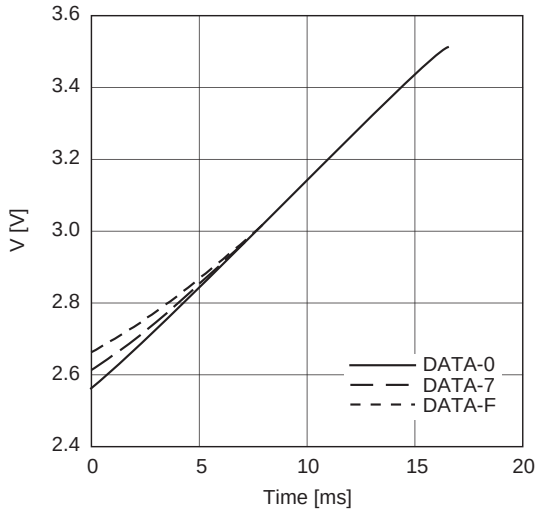
V-ASPECT



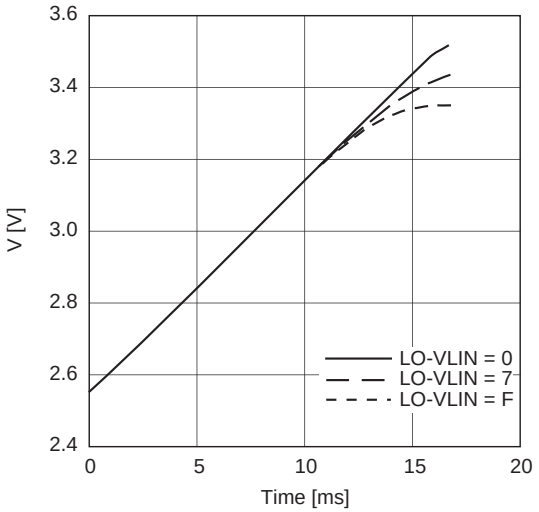
V-SCROLL



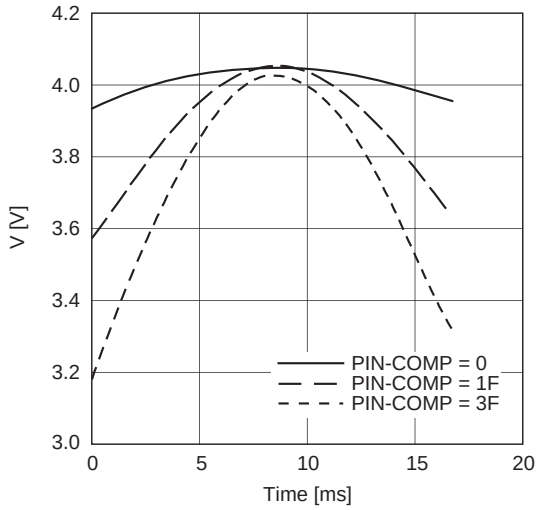
UP-VLIN



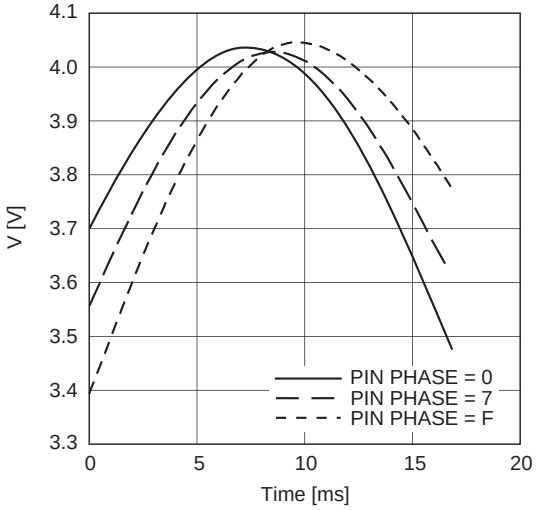
LO-VLIN



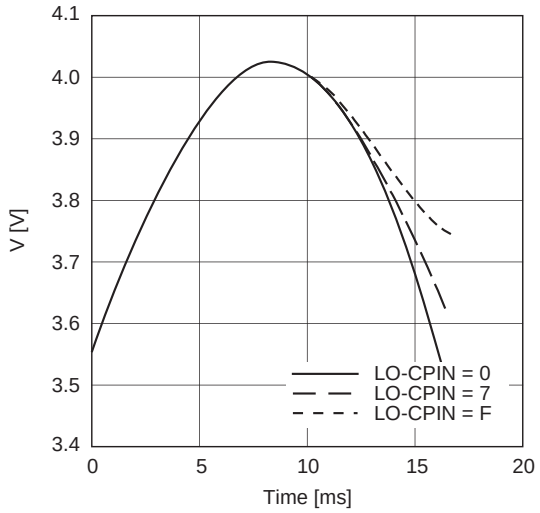
PIN-COMP



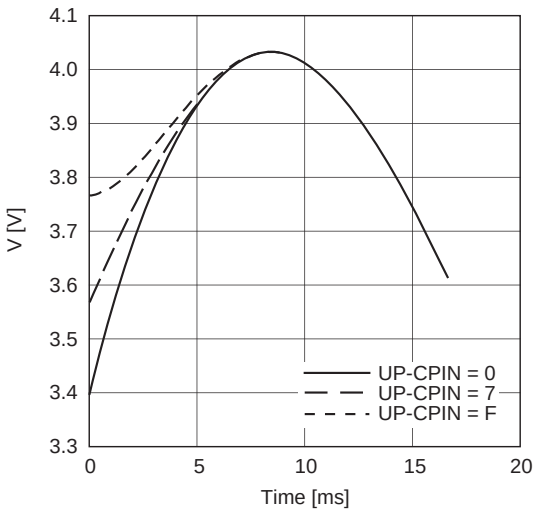
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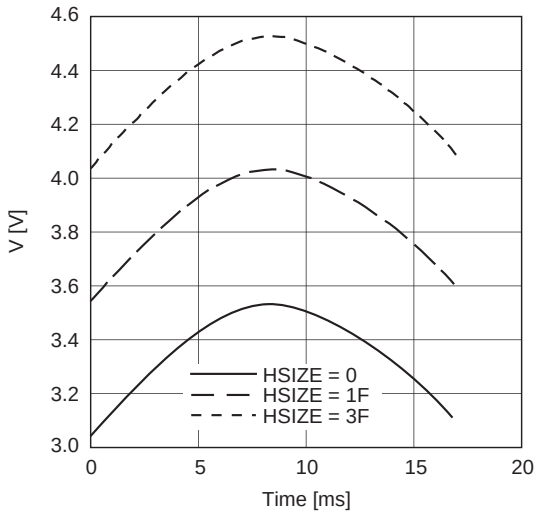
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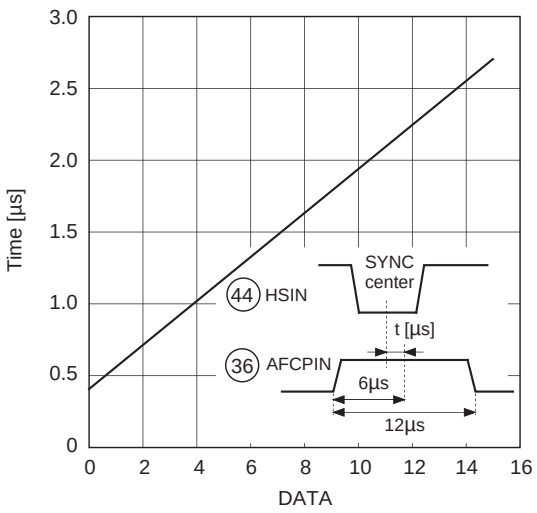
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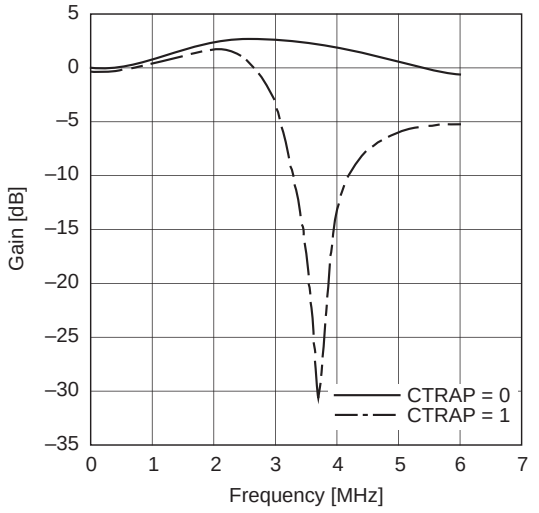
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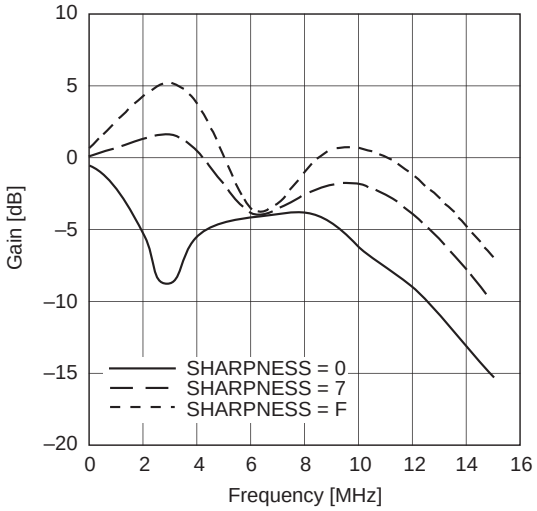
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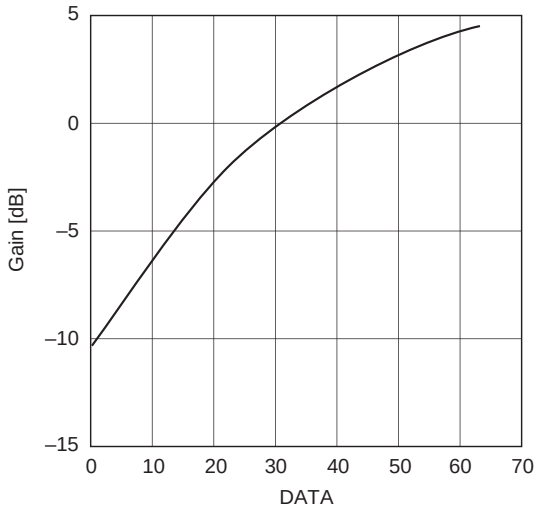
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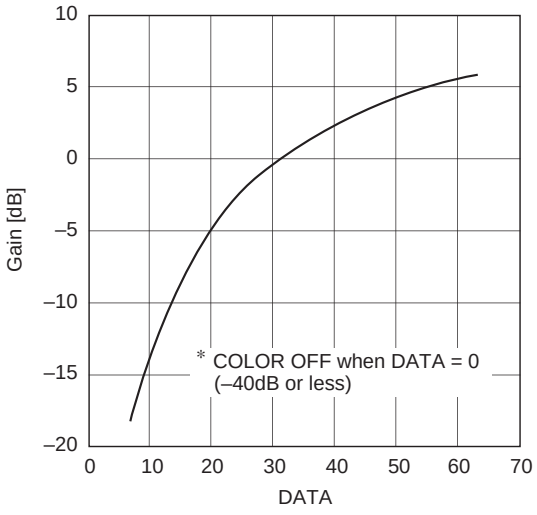
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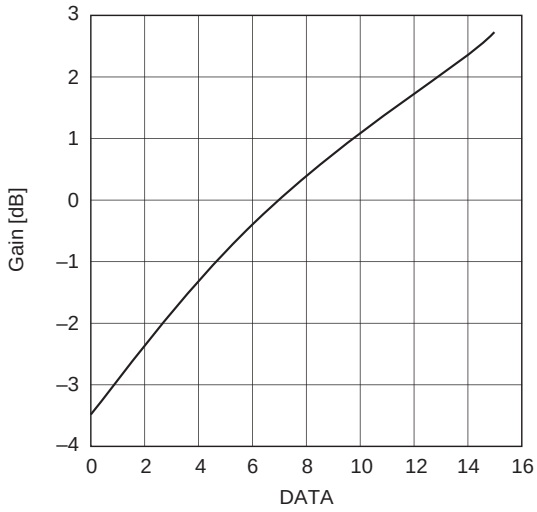
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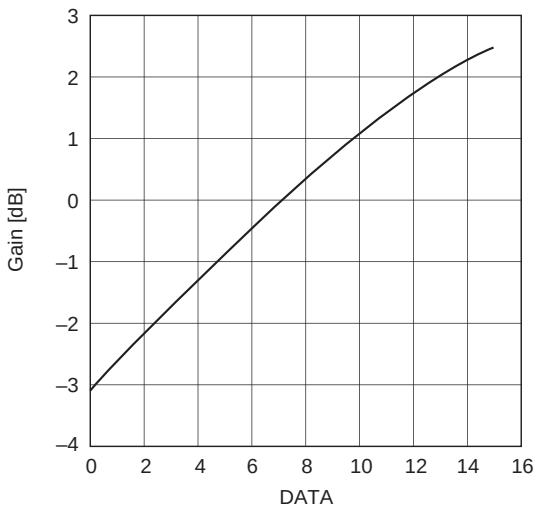
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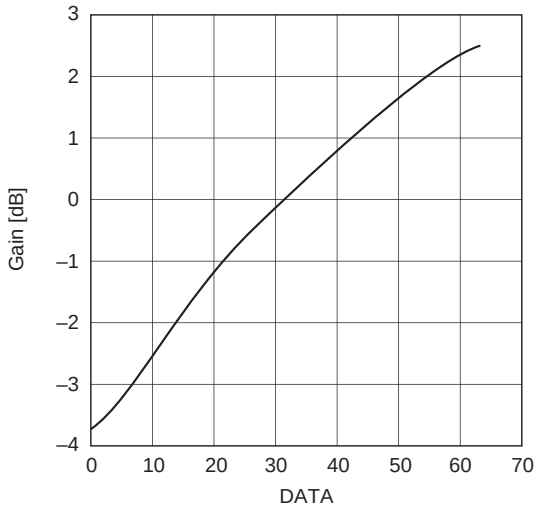
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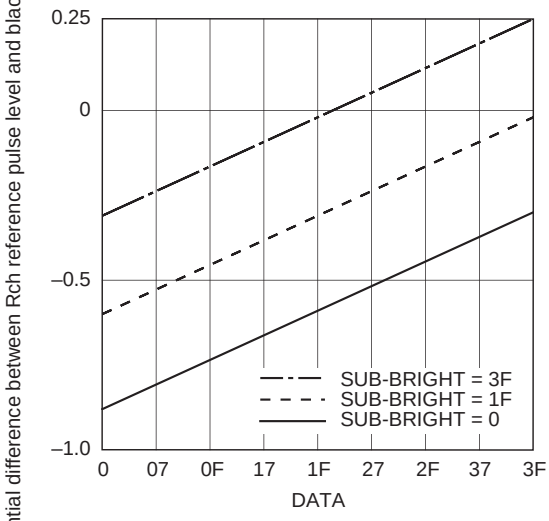
SUB CONT



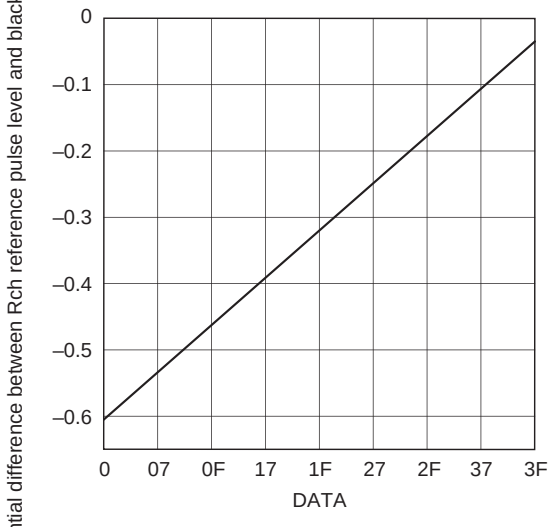
B-DRIVE, G-DRIVE



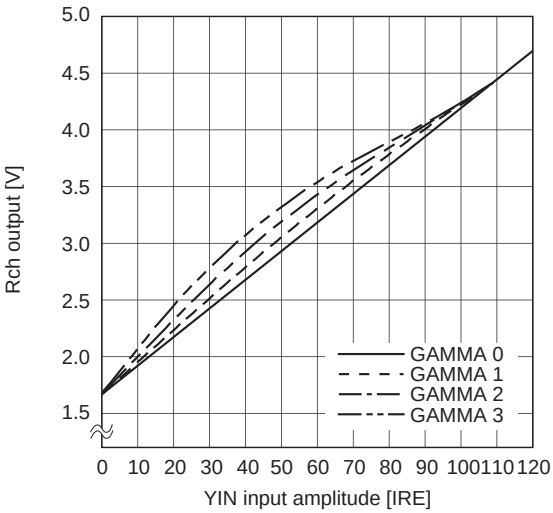
BRIGHT control characteristics



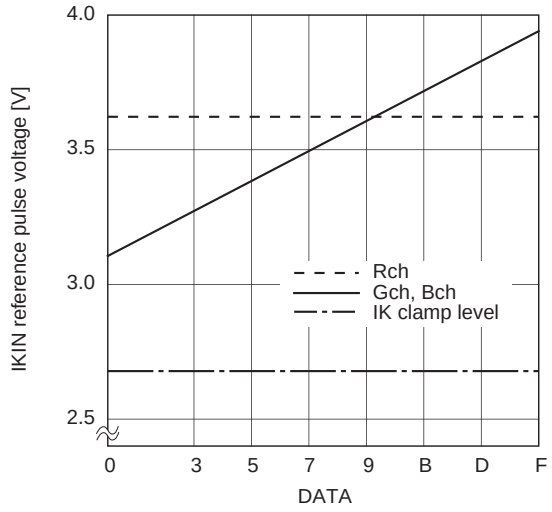
SUB-BRIGHT control characteristics



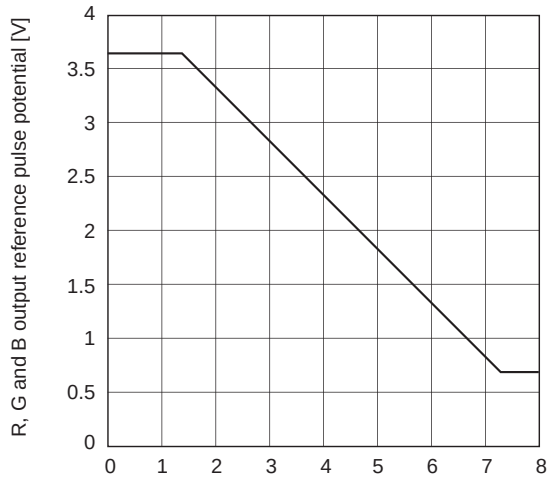
GAMMA control characteristics



Cut-off control characteristics

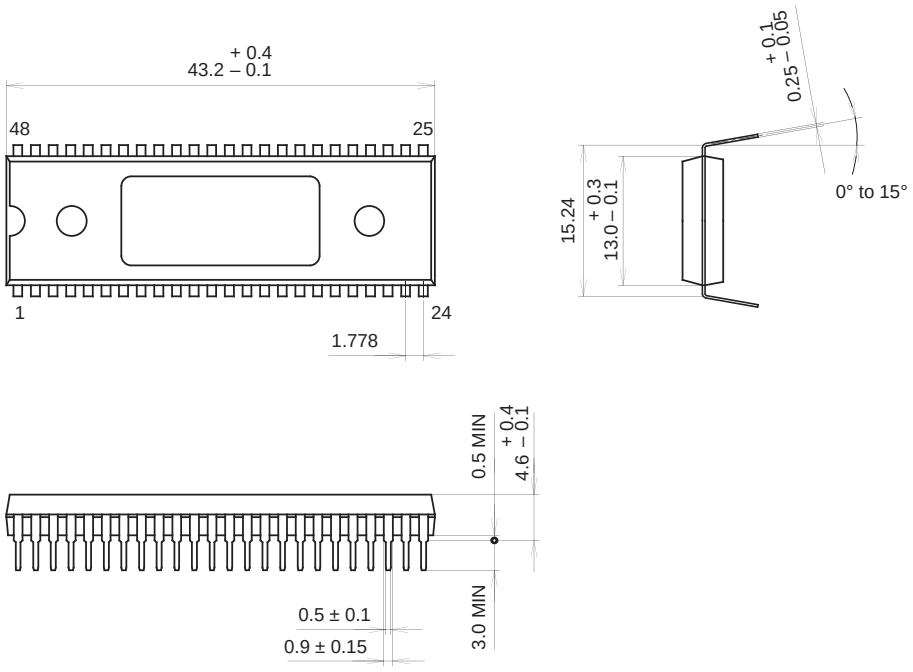


AKB open loop characteristics



Package Outline Unit: mm

48PIN SDIP (PLASTIC) 600mil



SONY CODE	SDIP-48P-02
EIAJ CODE	SDIP048-P-0600-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	5.1g