6-CHANNEL POWER MGMT IC WITH TWO STEP-DOWN CONVERTERS AND 4 LOW-INPUT VOLTAGE LDOs

FEATURES

- **Up To 95% Efficiency**
- **Output Current for DC/DC Converters:**
  - **TPS65050: 2 x 0.6 A**
  - **TPS65051: DCDC1 = 1 A; DCDC2 = 0.6 A**
  - **TPS65052: DCDC1 = 1 A; DCDC2 = 0.6 A**
  - **TPS65054: 2 x 0.6 A**
  - **TPS65056: DCDC1 = 1 A; DCDC2 = 0.6 A**
- **Output Voltages for DC/DC Converters**
  - **TPS65050: Externally Adjustable**
  - **TPS65051: Externally Adjustable**
  - **TPS65052: DCDC1 = Fixed at 3.3 V; DCDC2 = 1 V / 1.3 V for Samsung Application Processors**
  - **TPS65054: DCDC1 = Externally Adjustable; DCDC2 = 1.3 V / 1.05 V for OMAP™1710 Processor**
  - **TPS65056: DCDC1 = Fixed at 3.3 V; DCDC2 = 1 V / 1.3 V for Samsung Application Processors**
- **V_I Range for DC/DC Converters From 2.5 V to 6 V**
- **2.25-MHz Fixed Frequency Operation**
- **Power Save Mode at Light Load Current**
- **180° Out-of-Phase Operation**
- **Output Voltage Accuracy in PWM mode ±1%**
- **Low Ripple PFM Mode**
- **Total Typical 32-μA Quiescent Current for Both DC/DC Converters**
- **100% Duty Cycle for Lowest Dropout**
- **Two General-Purpose 400-mA, High PSRR LDOs**
- **Two General-Purpose 200-mA, High PSRR LDOs**
- **V_I range for LDOs from 1.5 V to 6.5 V**
- **Digital Voltage Selection for the LDOs**
- **Available in a 4 mm x 4 mm 32-Pin QFN Package**

APPLICATIONS

- **Cell Phones, Smart-Phones**
- **WLAN**
- **PDAs, Pocket PCs**
- **OMAP™ and Low-Power TMS320™ DSP Supply**
- **Samsung S3C24xx application processor Supply**
- **Portable Media Players**

DESCRIPTION

The TPS6505x are integrated Power Management ICs for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS6505x provides two efficient, 2.25-MHz step-down converters targeted at providing the core voltage and I/O voltage in a processor based system. Both step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents.

For low noise applications, the devices can be forced into fixed frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 μA. The devices allow the use of small inductors and capacitors to achieve a small solution size. TPS6505x provides an output current of up to 1 A on each DC/DC converter. The TPS6505x also integrate two 400-mA LDO and two 200-mA LDO voltage regulators, which can be turned on/off using separate enable pins on each LDO. Each LDO operates with an input voltage range between 1.5 V and 6.5 V allowing them to be supplied from one of the step-down converters or directly from the main battery.

Four digital input pins are used to set the output voltage of the LDOs from a set of 16 different combinations for LDO1 to LDO4 on TPS65050 and TPS65052. In TPS65051, TPS65054 and TPS65056, the LDO voltages are adjustable using external resistor dividers.

The TPS6505x come in a small 32-pin leadless package (4 mm x 4 mm QFN) with a 0.4 mm pitch.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER	OPTION	OUTPUT CURRENT for DC/DC CONVERTERS	QFN(1) PACKAGE(2)	PACKAGE MARKING
-40°C to 85°C	TPS65050	LDO voltages according to Table 1 DC/DC converters externally adjustable	2 x 600 mA	RSM	65050
	TPS65051	LDO voltages externally adjustable DC/DC converters externally adjustable	DCDC1 = 1 A DCDC2 = 600 mA		65051
	TPS65052	LDO voltages according to Table 1 DCDC1 = 3.3 V; DCDC2 = 1 V / 1.3 V	DCDC1 = 1 A DCDC2 = 600 mA		65052
	TPS65054	LDO voltages externally adjustable DCDC1 = externally adjustable DCDC2 = 1.3 V / 1.05 V	2 x 600 mA		65054
	TPS65056	LDO voltages externally adjustable DCDC1 = 3.3 V DCDC2 = 1.0 V / 1.3 V	DCDC1 = 1A DCDC2 = 600 mA		65056

(1) The RSM package is available in tape and reel. Add the R suffix (TPS65050RSMR) to order quantities per reel. Add the T suffix (TPS65050RSMT) to order quantities of 250 parts per reel.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNITS
V_I	Input voltage range on all pins except AGND, PGND, and EN_LDO1 pins with respect to AGND	-0.3 V to 7 V
	Input voltage range on EN_LDO1 pins with respect to AGND	-0.3 V to V_{CC} + 0.5 V
I_I	Current at VINDCDC1/2, L1, PGND1, L2, PGND2	1800 mA
	Current at all other pins	1000 mA
	Continuous total power dissipation	See the dissipation rating table
T_A	Operating free-air temperature	–40°C to 85°C
T_J	Maximum junction temperature	125°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$(1)	POWER RATING $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$	POWER RATING $T_A = 70°C$	POWER RATING $T_A = 85°C$
RSM	58 K/W	1.7 W	17 mW/K	0.95 W	0.68 W

(1) The thermal resistance junction to case of the RSM package is 4 K/W measured on a high K board

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range for step-down converters, VINDCDC1/2	2.5		6	V
V_O	Output voltage range for step-down converter, VDCDC1	0.6		VINDCDC1/2	V
	Output voltage range for step-down converter, VDCDC2	0.6		VINDCDC1/2	V
V_I	Input voltage range for LDOs, VINLDO1, VINLDO2, VINLDO3/4	1.5		6.5	V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_O	Output voltage range for LDO1 and LDO2	1		VINLDO1, VINLDO2	V
	Output voltage range for LDO3 and LDO4	1		VINLDO3/4	V
I_O	Output current at L1 (DCDC1) for TPS65051, TPS65052			1000	mA
	Output current at L1 (DCDC1) for TPS65050, TPS65054			600	mA
	Output current at L1 (DCDC2)			600	mA
	Output current at VLDO1, VLDO2			400	mA
	Output current at VLDO3, VLDO4			200	mA
	Inductor at L1, L2 (1)	1.5	2.2		µH
C_O	Output capacitor at VDCDC1, VDCDC2 (2)	10	22		µF
	Output capacitor at VLDO1, VLDO2, VLDO3, VLDO4 (2)	2.2			µF
C_I	Input capacitor at VCC (2)	1			µF
	Input capacitor at VINLDO1/2 (2)	2.2			µF
	Input capacitor at VINLDO3/4 (2)	2.2			µF
T_A	Operating ambient temperature range	-40		85	°C
T_J	Operating junction temperature range	-40		125	°C
	Resistor from battery voltage to V_{CC} used for filtering (3)		1	10	Ω

(1) See the *Application Information* section of this data sheet for more details.
(2) See the *Application Information* section of this data sheet for more details.
(3) Up to 2 mA can flow into V_{CC} when both converters are running in PWM, this resistor causes the UVLO threshold to be shifted accordingly.

ELECTRICAL CHARACTERISTICS

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF. T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range at VINDCDC1/2		2.5		6	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2, VINLDO3/4	One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1= EN_LDO2 = EN_LDO3/4 = GND		20	30	µA
		Two converters, I_O = 0 mA PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		32	40	µA
		One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = V_I		180	250	µA
I_Q	Operating quiescent current into V_{CC}	One converter, I_O = 0 mA. Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		0.85		mA
		Two converters, I_O = 0 mA Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		1.25		mA
$I_{(SD)}$	Shutdown current	EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = GND		9	12	µA
$V_{(UVLO)}$	Undervoltage lockout threshold for DCDC converters and LDOs	Voltage at V_{CC}		1.8	2	V

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF. T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4								
V_{IH}	High-level input voltage		MODE/DATA, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4		1.2		V_{CC}	V
V_{IL}	Low-level input voltage		MODE/DATA, EN_DCDC1, EN_DCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4, DEFDCDC2		0		0.4	V
I_{IB}	Input bias current		MODE/DATA = GND or V_I MODE/DATA, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4			0.01	1	µA
			TPS65051 and TPS65052 only V_FB_LDOx = 1 V FB_LDO1, FB_LDO2, FB_LDO3, FB_LDO4				100	nA
POWER SWITCH								
$r_{DS(on)}$	P-channel MOSFET on resistance		DCDC1	VINDCDC1/2 = 3.6 V		280	630	mΩ
				VINDCDC1/2 = 2.5 V		400		
			DCDC2	VINDCDC1/2 = 3.6 V		280	630	
				VINDCDC1/2 = 2.5 V		400		
I_{lkg}	P-channel leakage current		VDCDCx = $V_{(DS)}$ = 6 V				1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance		DCDC1	VINDCDC1/2 = 3.6 V		220	450	mΩ
				VINDCDC1/2 = 2.5 V		320		
			DCDC2	VINDCDC1/2 = 3.6 V		220	450	
				VINDCDC1/2 = 2.5 V		320		
I_{lkg}	N-channel leakage current		VDCDCx = $V_{(DS)}$ = 6 V			7	10	µA
$I_{(LIMF)}$	Forward Current Limit PMOS (High-Side) and NMOS (Low side)	DCDC1:	TPS65050 TPS65054	2.5 V ≤ VINDCDC1/2 ≤ 6 V	0.85	1	1.15	A
			TPS65051, TPS65052, TPS65056		1.19	1.4	1.65	
		DCDC2:	TPS65050 - TPS65056	2.5 V ≤ VINDCDC1/2 ≤ 6 V	0.85	1	1.15	A
	Thermal shutdown		Increasing junction temperature			150		°C
	Thermal shutdown hysteresis		Decreasing junction temperature			20		°C
OSCILLATOR								
f_{SW}	Oscillator frequency				2.025	2.25	2.475	MHz

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF. T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Output voltage range for DCDC1, DCDC2		externally adjustable versions	0.6		VINDCDC 1/2	V
V_{ref}	Reference voltage		externally adjustable versions		600		mV
V_O	DC output voltage accuracy	DCDC1, DCDC2(1)	VINDCDC1/2 = 2.5 V to 6 V 0 mA < I_O = < I_O(max) Mode = GND, PFM operation	-2%	0	2%	
			VINDCDC1/2 = 2.5 V to 6 V 0 mA < I_O = < I_O(max) Mode = V_I, PWM operation	-1%	0	1%	
ΔV_O	Power save mode ripple voltage(2)		I_O = 1 mA, Mode = GND, V_O = 1.3 V, Bandwith = 20 MHz		25		mV_{PP}
t_{Start}	Start-up time		time from active EN to Start switching		170		µs
t_{Ramp}	VOUT Ramp up Time		time to ramp from 5% to 95% of V_O		750		µs
	$\overline{\text{RESET}}$ delay time		Input voltage at threshold pin rising	80	100	120	ms
	PB-ONOFF debounce time			26	32	38	ms
V_{OL}	$\overline{\text{RESET}}$, PB_OUT output low voltage		I_{OL} = 1 mA, Vhysteresis < 1 V, Vthreshold < 1 V			0.2	V
I_{OL}	$\overline{\text{RESET}}$, PB_OUT sink current				1		mA
	$\overline{\text{RESET}}$, PB_OUT output leakage current		After PB_IN has been pulled high once; Vthreshold > 1 V and Vhysteresis > 1 V, V_{OH} = 6 V		10		nA
V_{th}	Vthreshold, Vhysteresis threshold			0.98	1	1.02	V
VLDO1, VLDO2, VLDO3 and VLDO4 Low Dropout Regulators							
V_I	Input voltage range for LDO1, LDO2, LDO3, LDO4			1.5		6.5	V
V_O	LDO1 output voltage range		TPS65050, TPS65052 only	1.2		3.3	V
	LDO2 output voltage range		TPS65050, TPS65052 only	1.8		3.3	V
	LDO3 output voltage range		TPS65050, TPS65052 only	1.1		3.3	V
	LDO4 output voltage range		TPS65050, TPS65052 only	1.2		2.85	V
$V_{(FB)}$	Feedback voltage for FB_LDO1, FB_LDO2, FB_LDO3, and FB_LDO4		TPS65051, TPS65054 and TPS65056 only		1		V
I_O	Maximum output current for LDO1, LDO2			400			mA
	Maximum output current for LDO3, LDO4			200			mA
$I_{(SC)}$	LDO1 short-circuit current limit		VLDO1 = GND			750	mA
	LDO2 short-circuit current limit		VLDO2 = GND			850	mA
	LDO3 and LDO4 short-circuit current limit		VLDO3 = GND, VLDO4 = GND			420	mA
	Dropout voltage at LDO1		I_O = 400 mA, VINLDO = 3.4 V			400	mV
	Dropout voltage at LDO2		I_O = 400 mA, VINLDO = 1.8 V			280	mV
	Dropout voltage at LDO3, LDO4		I_O = 200 mA, VINLDO = 1.8 V			280	mV
I_{lkg}	Leakage current from VinLDOx to VLDOx		LDO enabled, VINLDO = 6.5 V, V_O = 1 V, at T_A = 140°C		3		µA
V_O	Output voltage accuracy for LDO1, LDO2, LDO3, LDO4		I_O = 10 mA	-2%		1%	
	Line regulation for LDO1, LDO2, LDO3, LDO4		VINLDO1,2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5V, VINLDO3,4 = VLDO3,4 + 0.5 V (min. 2.5 V) to 6.5V, I_O = 10 mA	-1%		1%	
	Load regulation for LDO1, LDO2, LDO3, LDO4		I_O = 0 mA to 400 mA for LDO1, LDO2 I_O = 0 mA to 200 mA for LDO3, LDO4	-1%		1%	
	Regulation time for LDO1, LDO2, LDO3, LDO4		Load change from 10% to 90%		10		µs
PSRR	Power supply rejection ratio		f = 10 kHz; I_O = 50 mA; V_I = V_O + 1 V		70		dB

(1) Output voltage specification does not include tolerance of external voltage programming resistors.
(2) In Power Save Mode, operation is typically entered at I_{PSM} = V_I / 32 Ω.

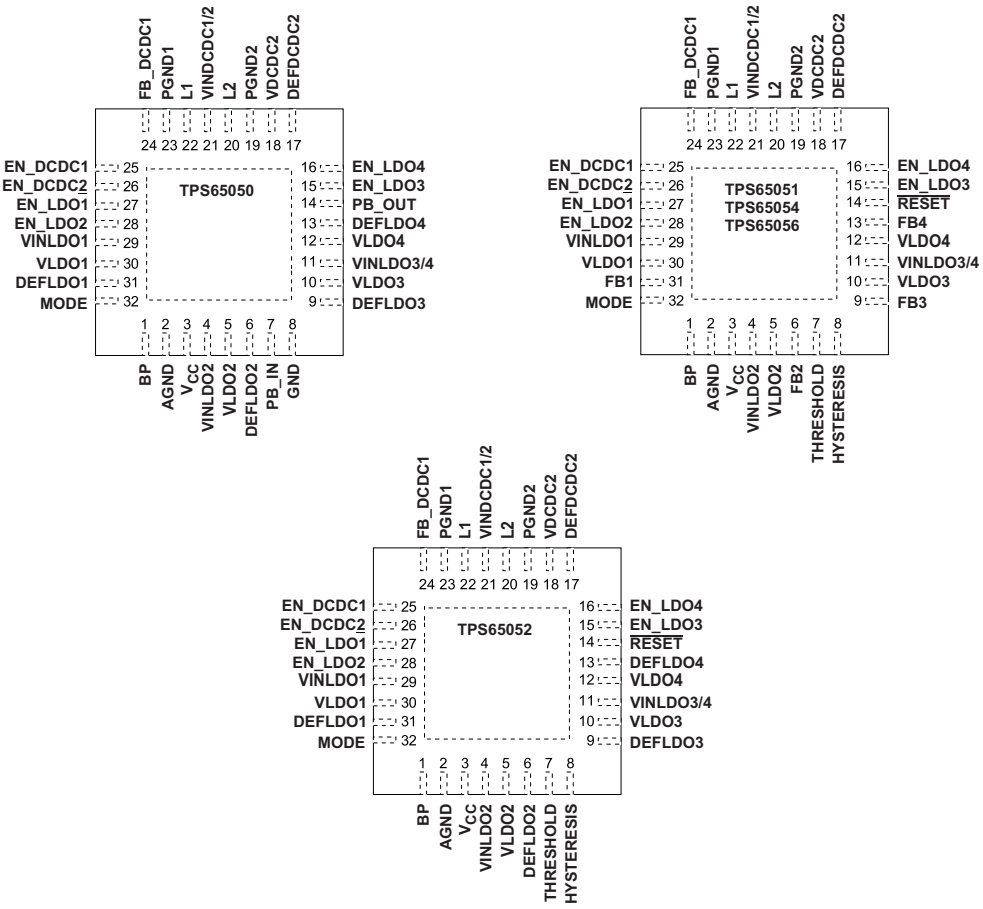
ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF. T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(DIS)}$	Internal discharge resistor at VLDO1, VLDO2, VLDO3, VLDO4	active when LDO is disabled		350		R
	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

PIN ASSIGNMENTS

RSM PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

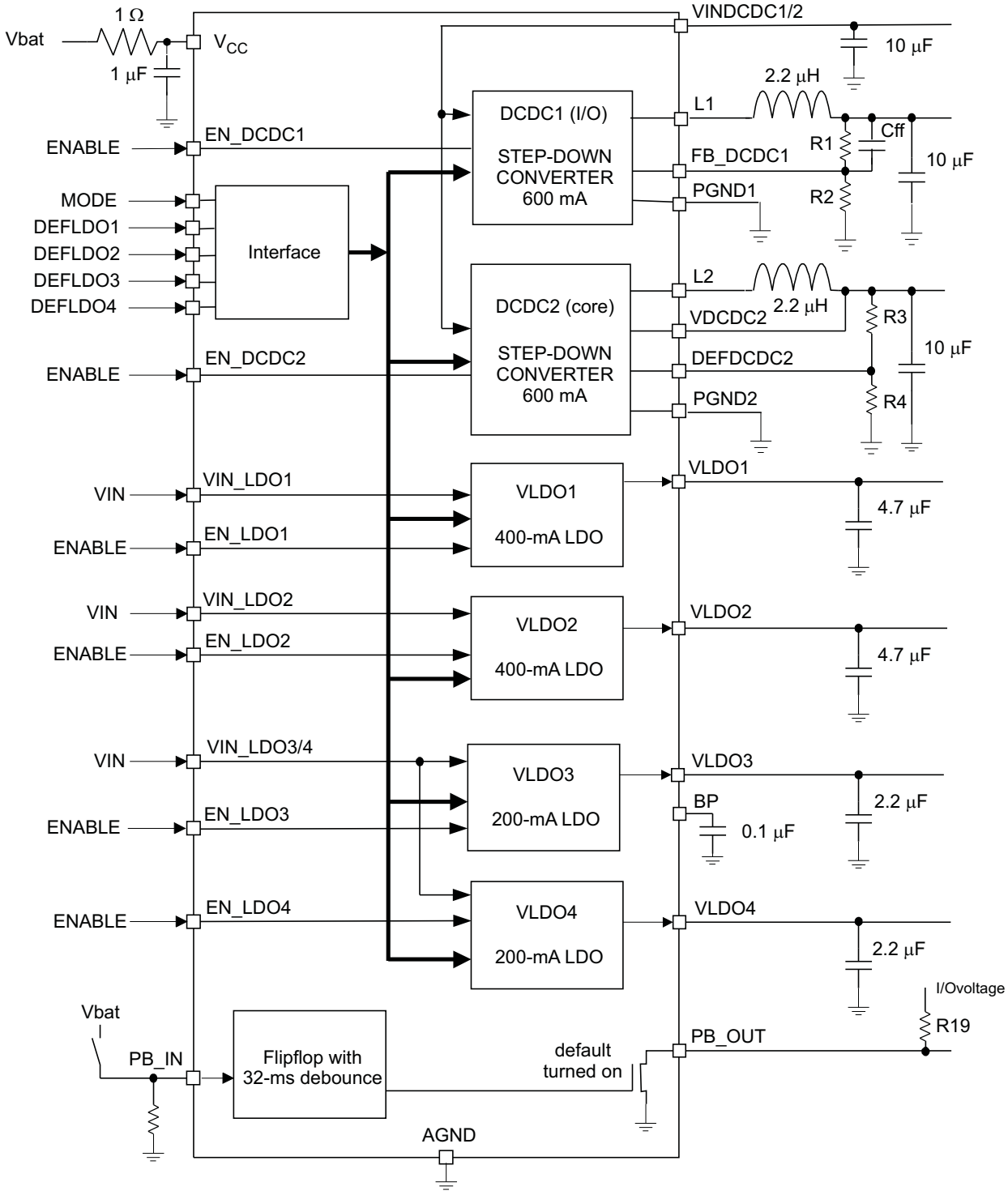
TERMINAL						I/O	DESCRIPTION
NAME	TPS65050	TPS65051	TPS65052	TPS65054	TPS65056		
V_{CC}	3	3	3	3	3	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. This pin must be connected to the same voltage supply as VINDCDC1/2.
FB_DCDC1	24	24	24	24	24	I	Input to adjust output voltage of converter 1 between 0.6 V and V_I. Connect external resistor divider between VOUT1, this pin, and GND.
MODE	32	32	32	32	32	I	Select between Power Safe Mode and forced PWM Mode for DCDC1 and DCDC2. In Power Safe Mode, PFM is used at light loads, PWM for higher loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then the device operates in Power Safe Mode.
VINDCDC1/2	21	21	21	21	21	I	Input voltage for VDCDC1 and VDCDC2 step-down converter. This must be connected to the same voltage supply as V_{CC}.
VDCDC2	18	18	18	18	18	I	Feedback voltage sense input, connect directly to the output of converter 2.
DEFDCDC2	17	17	17	17	17	I	TPS65050 and TPS65051: Feedback pin for converter 2. Connect DEFDCDC2 to the center of the external resistor divider. TPS65052 and TPS65056: Select pin of converter 2 output voltage. High = 1.3 V, Low = 1 V TPS65054: Select pin of converter 2 output voltage. High = 1.05 V, Low = 1.3 V
L1	22	22	22	22	22	O	Switch pin of converter 1. Connected to Inductor .

TERMINAL FUNCTIONS (continued)

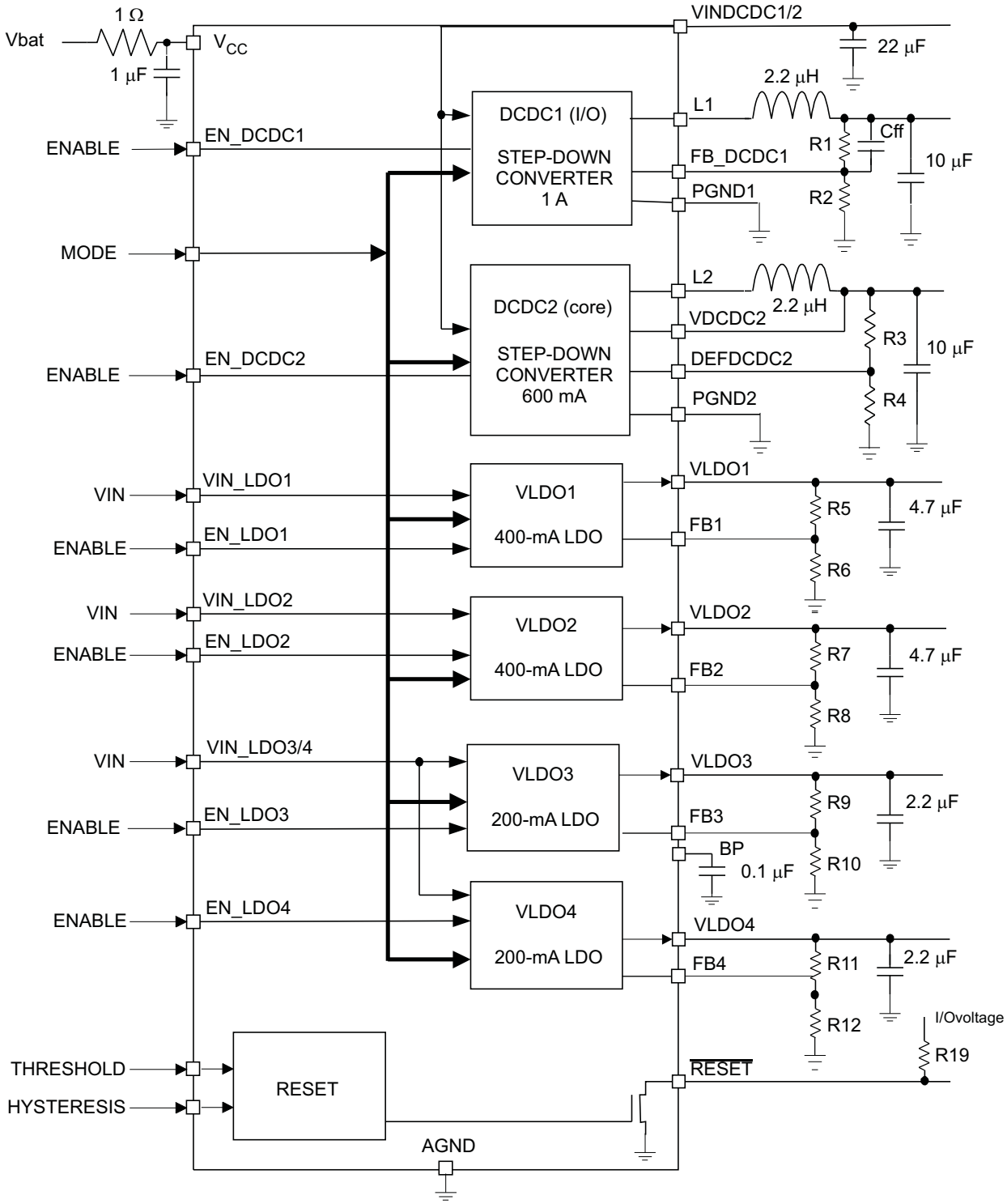
TERMINAL						I/O	DESCRIPTION
NAME	TPS65050	TPS65051	TPS65052	TPS65054	TPS65056		
PGND1	23	23	23	23	23	I	GND for converter 1
PGND2	19	19	19	19	19	I	GND for converter 2
AGND	2	2	2	2	2	I	Analog GND, connect to PGND and PowerPad™
L2	20	20	20	20	20	O	Switch Pin of converter 2. Connected to Inductor.
EN_DCDC1	25	25	25	25	25	I	Enable Input for converter 1, active high
EN_DCDC2	26	26	26	26	26	I	Enable Input for converter 2, active high
VINLDO1	29	29	29	29	29	I	Input voltage for LDO1
VINLDO2	4	4	4	4	4	I	Input voltage for LDO2
VINLDO3/4	11	11	11	11	11	I	Input voltage for LDO3 and LDO4
VLDO1	30	30	30	30	30	O	Output voltage of LDO1
VLDO2	5	5	5	5	5	O	Output voltage of LDO2
VLDO3	10	10	10	10	10	O	Output voltage of LDO3
VLDO4	12	12	12	12	12	O	Output voltage of LDO4
DEFLDO1	31	--	31	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4; LSB
FB1	--	31	--	31	31	I	Feedback input for the external voltage divider.
DEFLDO2	6	--	6	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4.
FB2	--	6	--	6	6	I	Feedback input for the external voltage divider.
DEFLDO3	9	--	9	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4.
FB3	--	9	--	9	9	I	Feedback input for the external voltage divider.
DEFLDO4	13	--	13	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4; MSB
FB4	--	13	--	13	13	I	Feedback input for the external voltage divider.
EN_LDO1	27	27	27	27	27	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	28	28	28	28	28	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	15	15	15	15	15	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.
EN_LDO4	16	16	16	16	16	I	Enable input for LDO4. Logic high enables the LDO, logic low disables the LDO.
THRESHOLD	--	7	7	7	7	I	Reset input
PB_IN	7	--	--	--	--	I	Input for the pushbutton ON-OFF function
HYSTERESIS	--	8	8	8	8	I	Input for hysteresis on reset threshold
GND	8	--	--	--	--	-	Connect to GND
$\overline{\text{RESET}}$	--	14	14	14	14	O	Open drain active low reset output, 100 ms reset delay time.
PB_OUT	14	--	--	--	--	O	Open drain output. Active low after the supply voltage (V_{CC}) exceeded the undervoltage lockout threshold. The pin can be toggled pulling PB_IN high.
BP	1	1	1	1	1	I	Input for bypass capacitor for internal reference.
PowerPAD™	--	--	--	--	--		Connect to GND

FUNCTIONAL BLOCK DIAGRAM

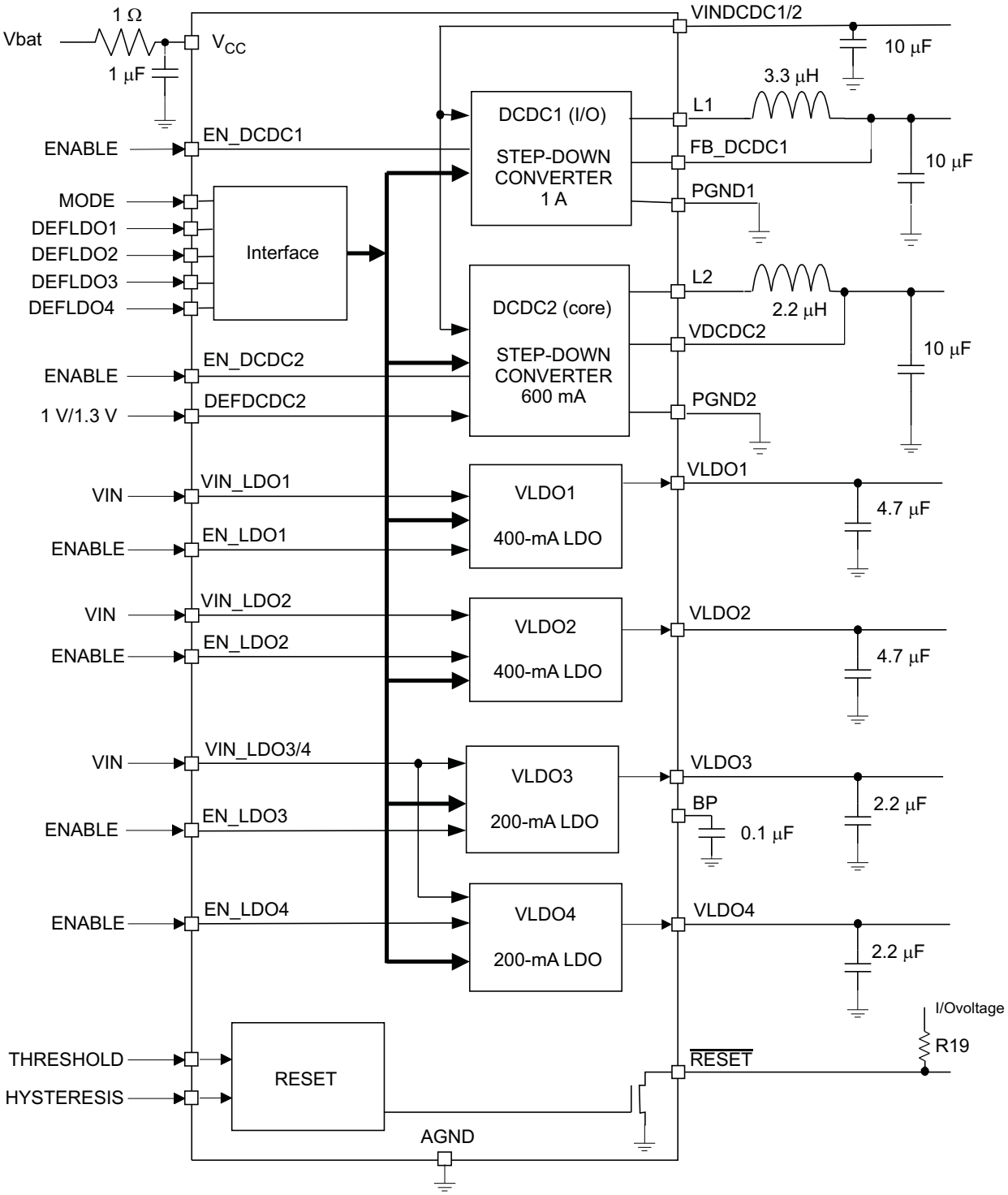
TPS65050



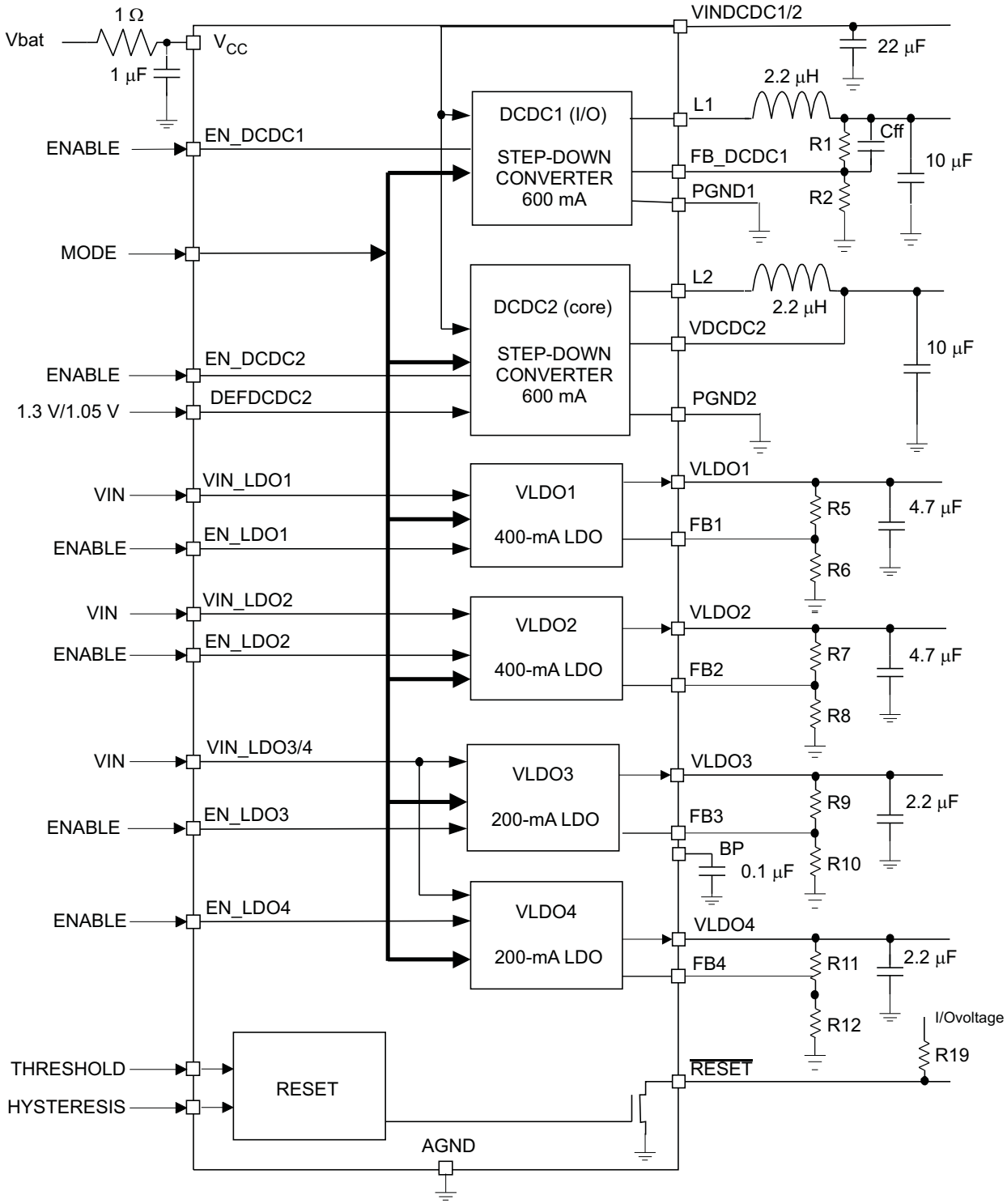
TPS65051


1 Ω
Vbat
VCC
1 µF
ENABLE
EN_DCDC1
MODE
ENABLE
EN_DCDC2
VIN
VIN_LDO1
ENABLE
EN_LDO1
VIN
VIN_LDO2
ENABLE
EN_LDO2
VIN
VIN_LDO3/4
ENABLE
EN_LDO3
ENABLE
EN_LDO4
THRESHOLD
HYSTERESIS
RESET
AGND
DCDC1 (I/O)
STEP-DOWN
CONVERTER
1 A
DCDC2 (core)
STEP-DOWN
CONVERTER
600 mA
VLDO1
400-mA LDO
VLDO2
400-mA LDO
VLDO3
200-mA LDO
VLDO4
200-mA LDO
VINDCDC1/2
22 µF
2.2 µH
L1
R1
Cff
10 µF
FB_DCDC1
R2
PGND1
L2
2.2 µH
VDCDC2
R3
10 µF
DEFDCDC2
R4
PGND2
VLDO1
R5
4.7 µF
FB1
R6
VLDO2
R7
4.7 µF
FB2
R8
VLDO3
R9
2.2 µF
FB3
BP
0.1 µF
R10
VLDO4
R11
2.2 µF
FB4
R12
I/Ovoltage
R19
RESET

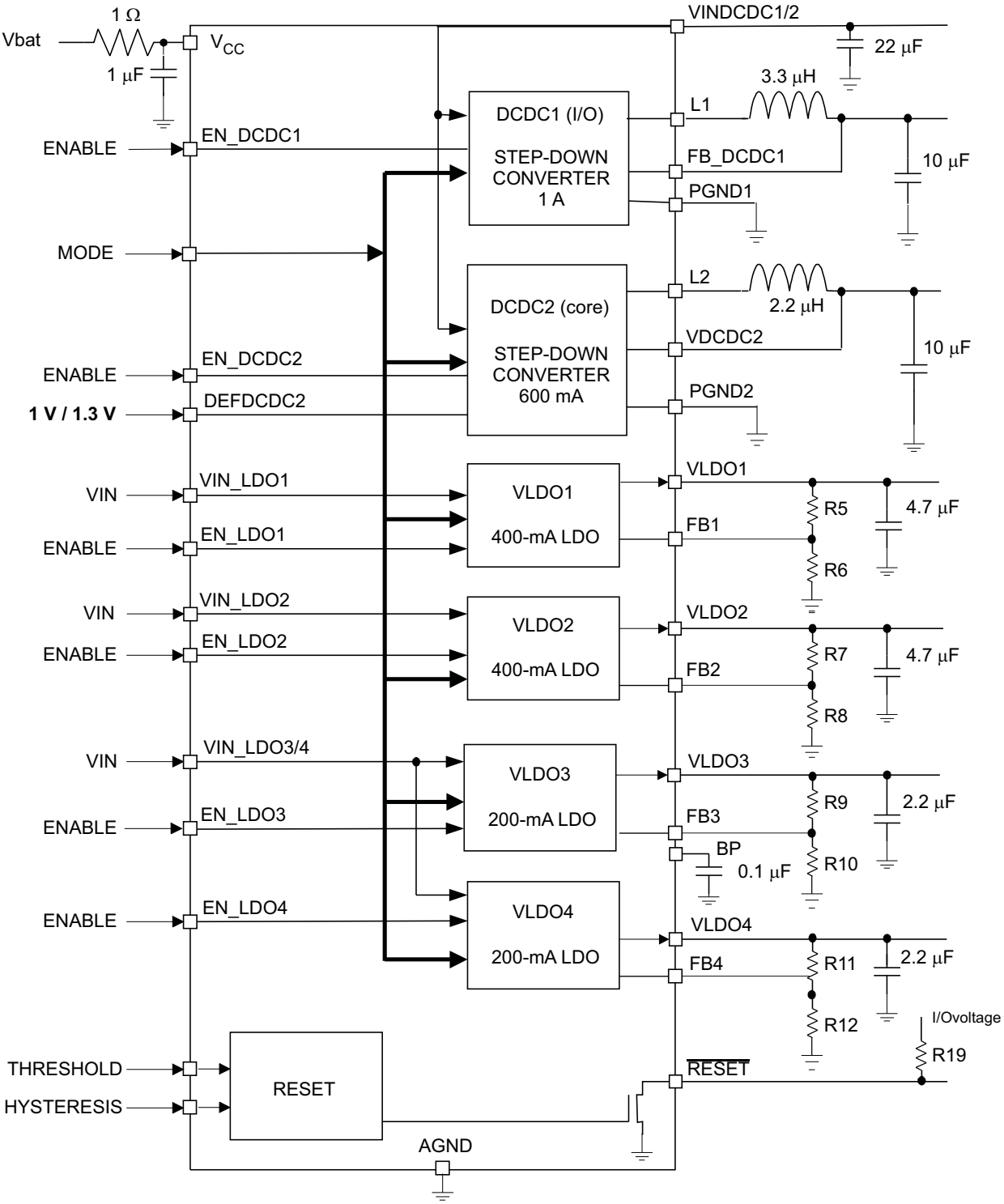
TPS65052


1 Ω
Vbat
VCC
1 µF
VINDCDC1/2
10 µF
3.3 µH
L1
DCDC1 (I/O)
STEP-DOWN
CONVERTER
1 A
FB_DCDC1
PGND1
10 µF
EN_DCDC1
ENABLE
MODE
DEFLDO1
DEFLDO2
DEFLDO3
DEFLDO4
Interface
L2
2.2 µH
DCDC2 (core)
STEP-DOWN
CONVERTER
600 mA
VDCDC2
PGND2
10 µF
EN_DCDC2
ENABLE
DEFDCDC2
1 V/1.3 V
VLDO1
4.7 µF
VIN_LDO1
VIN
EN_LDO1
ENABLE
VLDO1
400-mA LDO
VLDO2
4.7 µF
VIN_LDO2
VIN
EN_LDO2
ENABLE
VLDO2
400-mA LDO
VLDO3
BP
0.1 µF
2.2 µF
VIN_LDO3/4
VIN
EN_LDO3
ENABLE
VLDO3
200-mA LDO
VLDO4
2.2 µF
EN_LDO4
ENABLE
VLDO4
200-mA LDO
I/Ovoltage
R19
RESET
THRESHOLD
HYSTERESIS
RESET
AGND

TPS65054


1 Ω
Vbat
1 µF
VCC
VINDCDC1/2
22 µF
2.2 µH
L1
DCDC1 (I/O)
STEP-DOWN
CONVERTER
600 mA
ENABLE
EN_DCDC1
FB_DCDC1
PGND1
R1
R2
Cff
10 µF
MODE
L2
2.2 µH
DCDC2 (core)
STEP-DOWN
CONVERTER
600 mA
VDCDC2
ENABLE
EN_DCDC2
1.3 V/1.05 V
DEFDCDC2
PGND2
10 µF
VIN
VIN_LDO1
VLDO1
400-mA LDO
VLDO1
ENABLE
EN_LDO1
FB1
R5
R6
4.7 µF
VIN
VIN_LDO2
VLDO2
400-mA LDO
VLDO2
ENABLE
EN_LDO2
FB2
R7
R8
4.7 µF
VIN
VIN_LDO3/4
VLDO3
200-mA LDO
VLDO3
ENABLE
EN_LDO3
FB3
R9
R10
BP
0.1 µF
2.2 µF
ENABLE
EN_LDO4
VLDO4
200-mA LDO
VLDO4
FB4
R11
R12
2.2 µF
I/Ovoltage
R19
THRESHOLD
HYSTERESIS
RESET
RESET
AGND

TPS65056


1 Ω
Vbat
VCC
1 µF
VINDCDC1/2
22 µF
3.3 µH
L1
DCDC1 (I/O)
STEP-DOWN
CONVERTER
1 A
FB_DCDC1
PGND1
10 µF
ENABLE
EN_DCDC1
MODE
L2
2.2 µH
DCDC2 (core)
STEP-DOWN
CONVERTER
600 mA
VDCDC2
PGND2
10 µF
ENABLE
EN_DCDC2
1 V / 1.3 V
DEFDCDC2
VIN
VIN_LDO1
ENABLE
EN_LDO1
VLDO1
400-mA LDO
FB1
VLDO1
R5
R6
4.7 µF
VIN
VIN_LDO2
ENABLE
EN_LDO2
VLDO2
400-mA LDO
FB2
VLDO2
R7
R8
4.7 µF
VIN
VIN_LDO3/4
ENABLE
EN_LDO3
VLDO3
200-mA LDO
FB3
BP
0.1 µF
VLDO3
R9
R10
2.2 µF
ENABLE
EN_LDO4
VLDO4
200-mA LDO
FB4
VLDO4
R11
R12
2.2 µF
I/Ovoltage
R19
THRESHOLD
HYSTERESIS
RESET
RESET
AGND

TYPICAL CHARACTERISTICS

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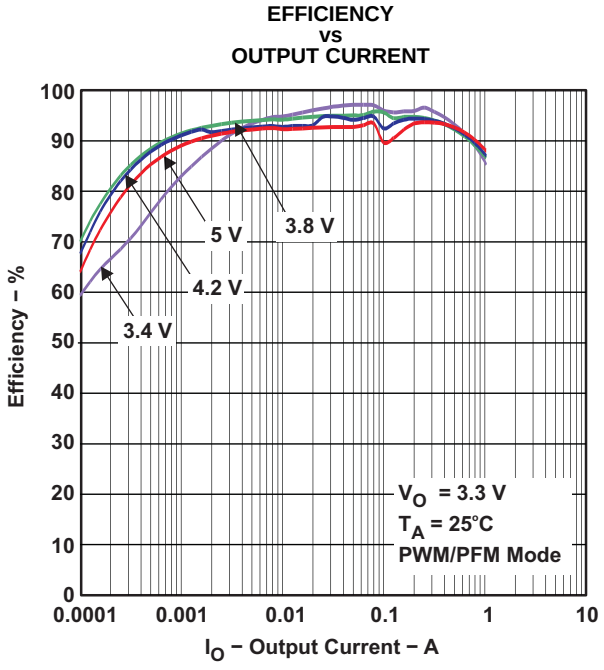


Figure 1.

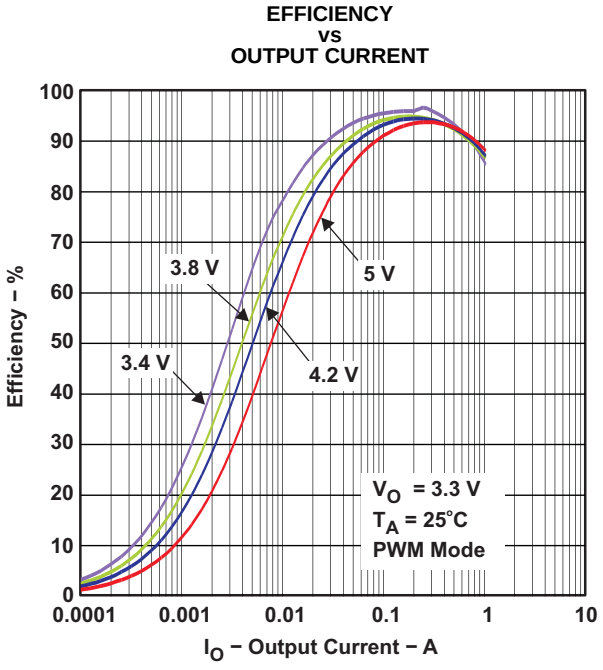


Figure 2.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
OUTPUT CURRENT

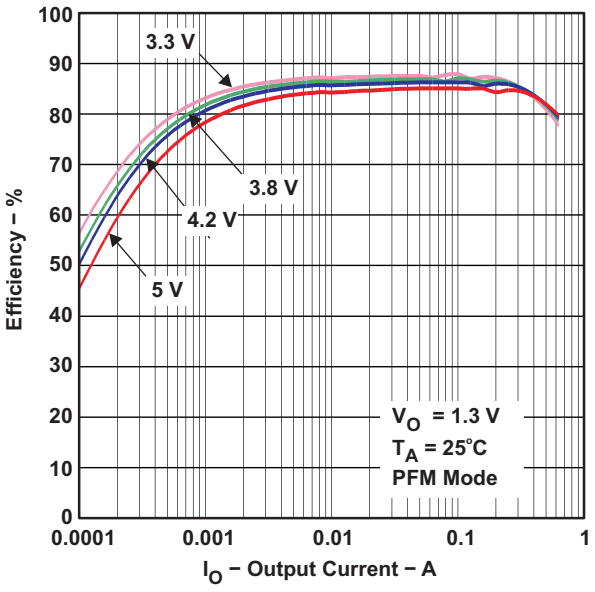


Figure 3.

EFFICIENCY
vs
OUTPUT CURRENT

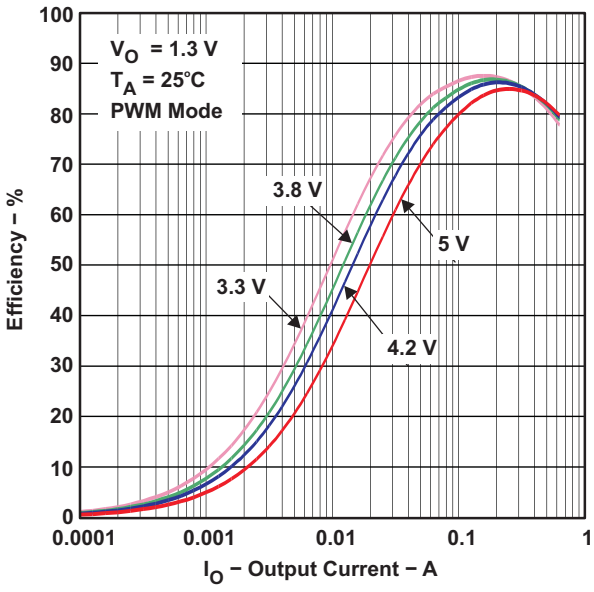


Figure 4.

OUTPUT VOLTAGE RIPPLE
PWM/PFM MODE = LOW

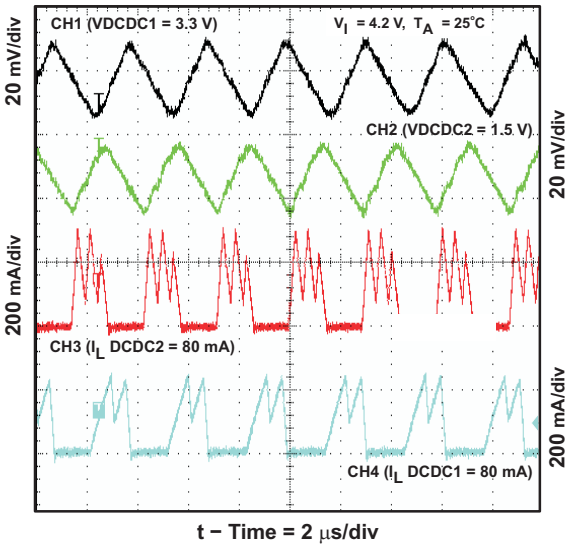


Figure 5.

OUTPUT VOLTAGE RIPPLE
PWM MODE = HIGH

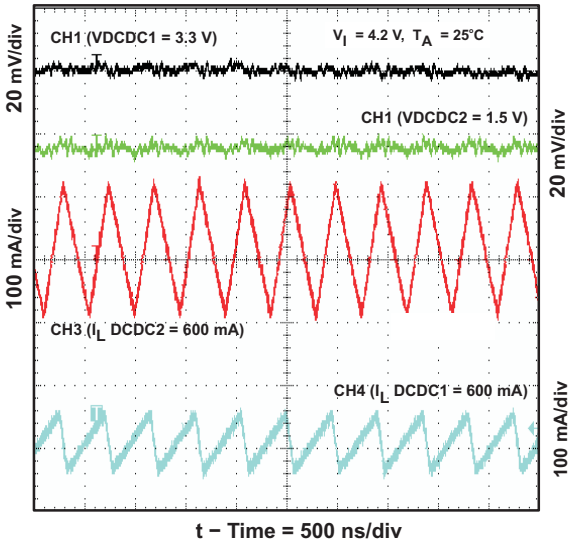
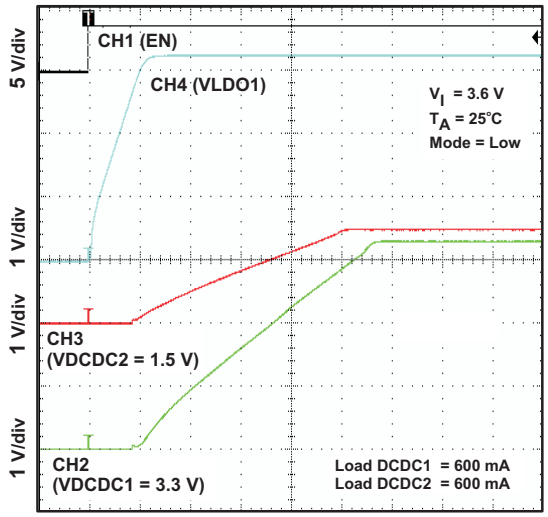


Figure 6.

TYPICAL CHARACTERISTICS (continued)

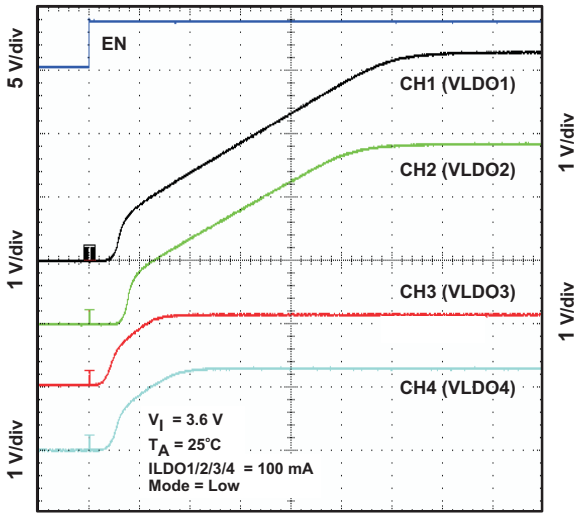
DCDC1 STARTUP TIMING



t − Time = 200 µs/div

Figure 7.

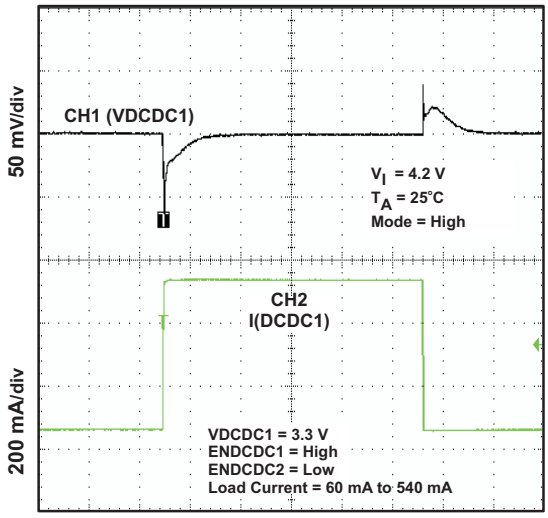
LDO1 TO LDO4 STARTUP TIMING



t − Time = 20 µs/div

Figure 8.

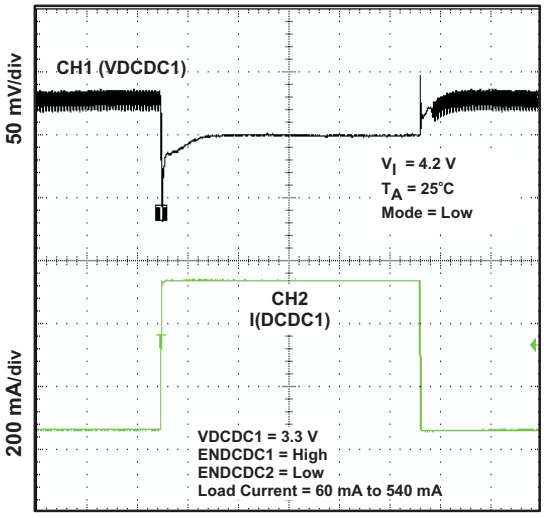
DCDC1 LOAD TRANSIENT RESPONSE



t − Time = 100 µs/div

Figure 9.

DCDC1 LOAD TRANSIENT RESPONSE



t − Time = 100 µs/div

Figure 10.

TYPICAL CHARACTERISTICS (continued)

DCDC2 LOAD TRANSIENT RESPONSE

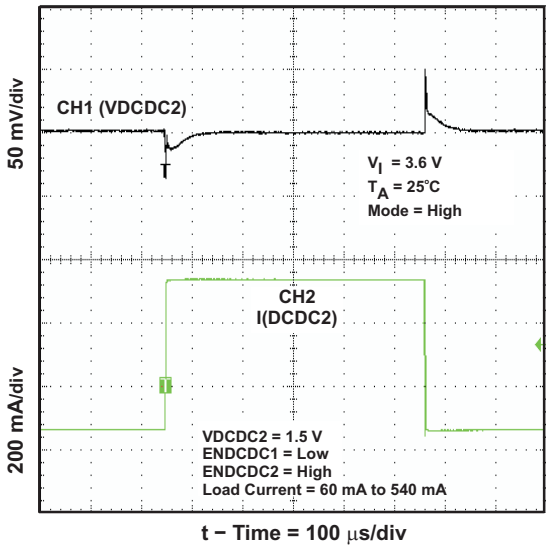


Figure 11.

DCDC2 LOAD TRANSIENT RESPONSE

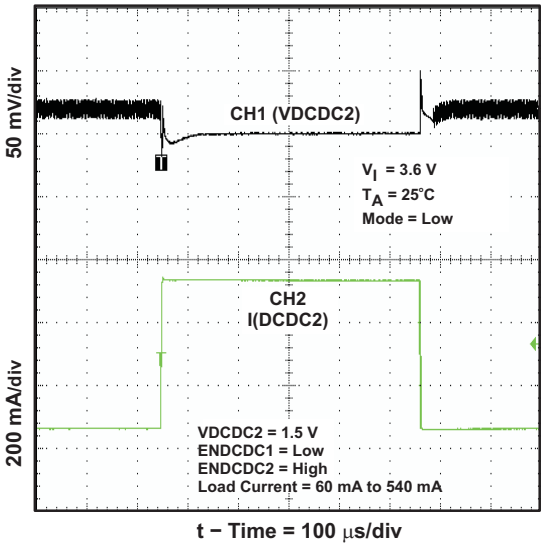


Figure 12.

DCDC1 LINE TRANSIENT RESPONSE

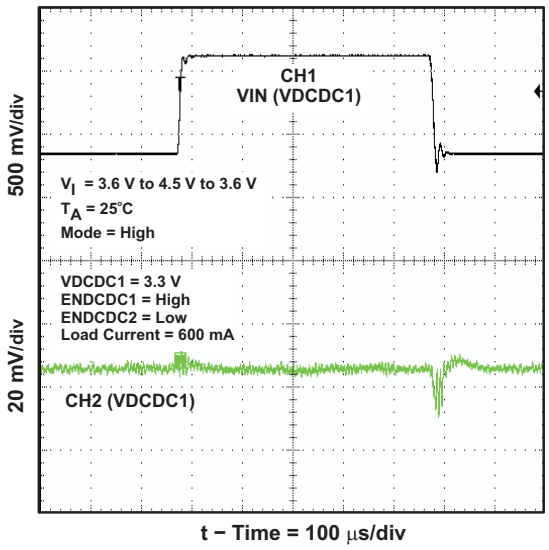


Figure 13.

DCDC2 LINE TRANSIENT RESPONSE

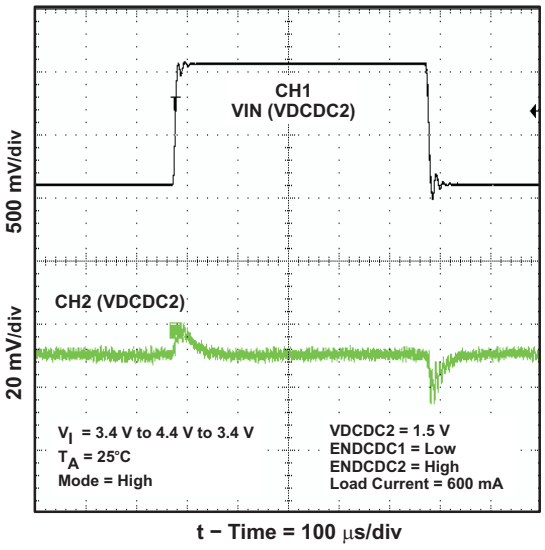


Figure 14.

TYPICAL CHARACTERISTICS (continued)

LDO1 LOAD TRANSIENT RESPONSE

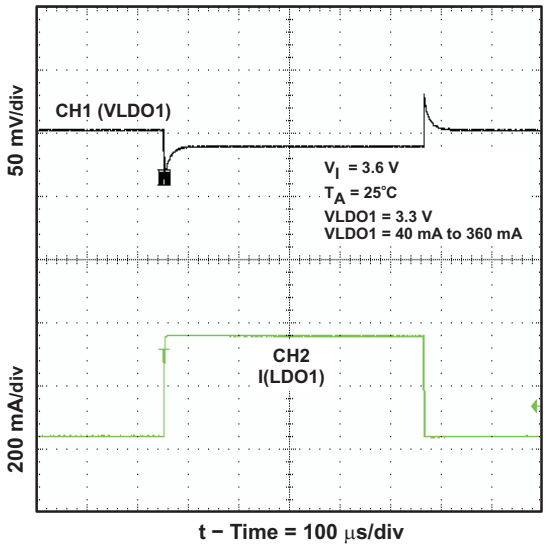


Figure 15.

LDO4 LOAD TRANSIENT RESPONSE

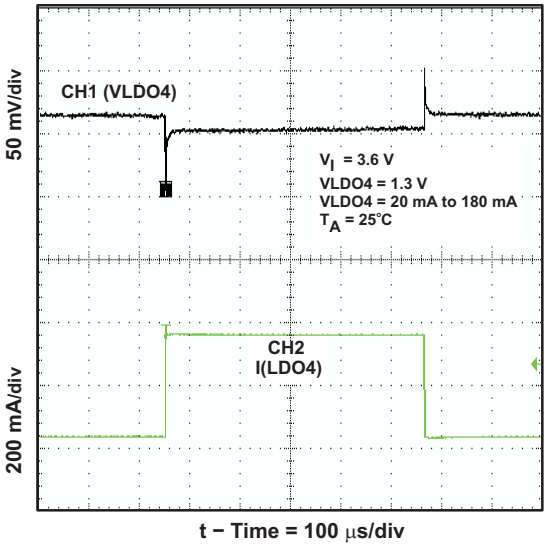


Figure 16.

LDO1 LINE TRANSIENT RESPONSE

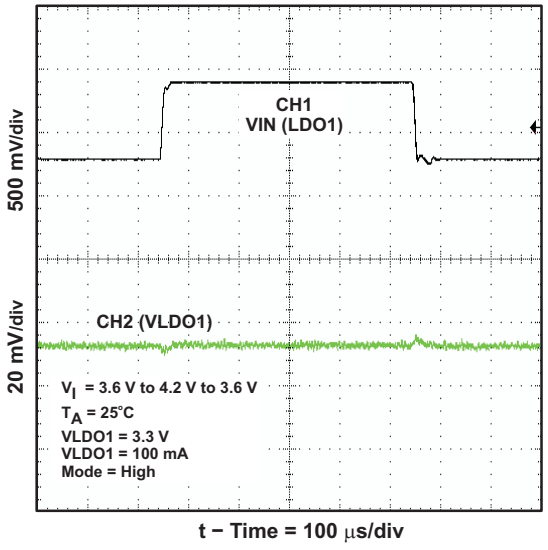


Figure 17.

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

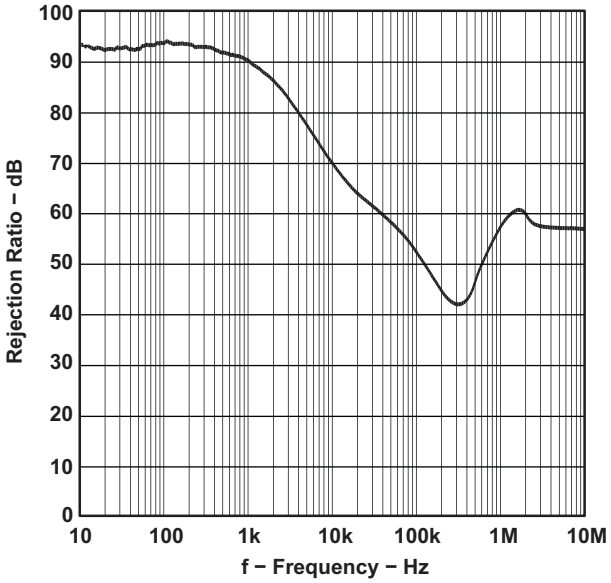


Figure 18.

DETAILED DESCRIPTION

Operation

The TPS6505x include each two synchronous step-down converters. The converters operate with 2.25-MHz (typical) fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation).

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on, and the inductor current ramps up until the current comparator trips, and the control logic turns off the switch. The current limit comparator turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time, which prevents shoot through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal turning off the N-channel rectifier, and turning on the on the P-channel switch.

The two DC/DC converters operate synchronized to each other, with converter 1 as the master. A 180° phase shift between converter 1 and converter 2 decreases the input RMS current. Therefore, smaller input capacitors can be used.

DCDC1 Converter

The converter 1 output voltage is set by an external resistor divider connected to FB_DCDC1 pin for TPS65050, TPS65051 and TPS65054. For TPS65052, the output voltage is fixed to 3.3 V and this pin needs to be directly connected to the output. See the *Application Information* section for more details. The maximum output current on DCDC1 is 600 mA for TPS65050 and TPS65054. For TPS65051, TPS65052 and TPS65056, the maximum output current is 1 A.

DCDC2 Converter

The VDCDC2 pin must be directly connected to the DCDC2 converter output voltage. The DCDC2 converter output voltage is selected via the DEFDCDC2 pin.

TPS65050 and TPS65051: The output voltage is set with an external resistor divider. Connect the DEFDCDC2 pin to the external resistor divider.

TPS65052, TPS65054 and TPS65056: The DEFDCDC2 pin can either be connected to GND, or to V_{CC}. The converter 2 output voltage defaults to:

Device	DEFDCDC2 = low	DEFDCDC2 = high
TPS65052 , TPS65056	1 V	1.3 V
TPS65054	1.3 V	1.05 V

Power-Save Mode

The Power Save Mode is enabled with the Mode pin set to 0. If the load current decreases, the converters enters Power Save Mode operation automatically. During Power Save Mode, the converters operate with reduced switching frequency in PFM mode, and with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

To optimize the converter efficiency at light load, the average current is monitored. If in PWM mode, the inductor current remains below a certain threshold, then Power Save Mode is entered. The typical threshold is calculated according to Equation 1:

$$I_{(PFM_enter)} = \frac{VINDCDC}{32\ \Omega} \quad (1)$$

A. Average output current threshold to enter PFM mode.

$$I_{(PSMDCDC_leave)} = \frac{VINDCDC}{24\ \Omega} \quad (2)$$

A. Average output current threshold to leave PFM mode.

During the Power Save Mode, the output voltage is monitored with a comparator. As the output voltage falls below the skip comparator threshold (skip comp), the P-channel switch turns on, and the converter effectively delivers a constant current. If the load is below the delivered current, the output voltage rises until the skip comp threshold is crossed again, then all switching activity ceases, reducing the quiescent current to a minimum until the output voltage has dropped below the threshold. If the load current is greater than the delivered current, the output voltage falls until it crosses the skip comparator low (Skip Comp Low) threshold set to 1% below nominal V_O, then Power Save Mode is exited, and the converter returns to PWM mode

These control methods reduce the quiescent current to 12 µA per converter, and the switching frequency to a minimum achieving the highest converter efficiency. The PFM mode operates with low output voltage ripple. The ripple depends on the comparator delay, and the size of the output capacitor; increasing capacitor values decreases the output ripple voltage.

The Power Save Mode can be disabled by driving the MODE pin high. In forced PWM mode, both converters operate with fixed frequency PWM mode regardless of the load.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is activated in Power Save Mode operation when the converter runs in PFM Mode. It provides more headroom for both, the voltage drop at a load step and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operate in PFM Mode, the output voltage is regulated typically 1% higher than the nominal value. In the event of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to -1% below the nominal value and enters PWM mode. During a release from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.

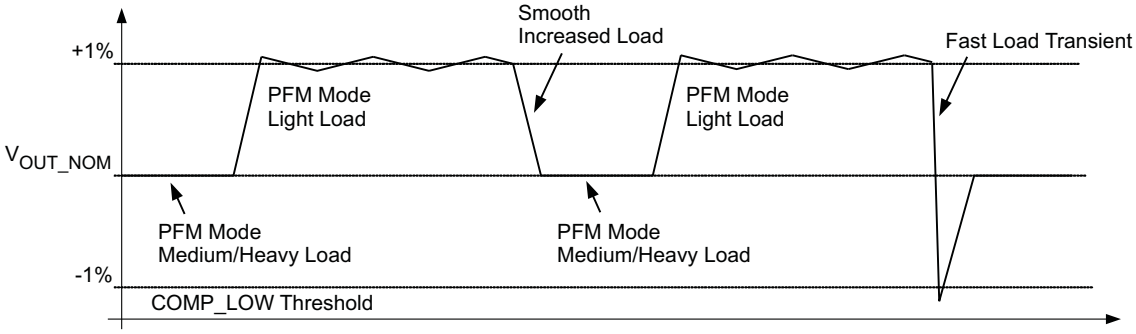


Figure 19. Dynamic Voltage Positioning

Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 20.

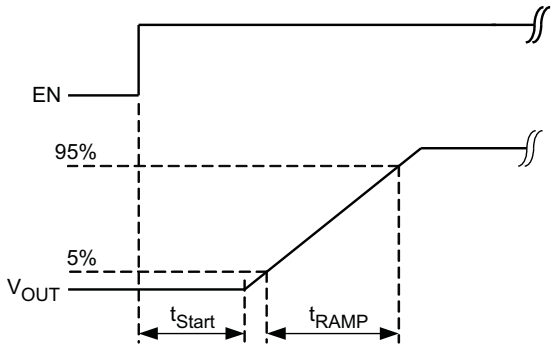


Figure 20. Soft Start

100% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. (i.e. The minimum input voltage to maintain regulation depends on the load current and output voltage) and can be calculated as:

$$V_I(\min) = V_O(\max) + I_O(\max) \times (r_{DS(on)}(\max) + R_L) \quad (3)$$

with:

- I_O max = maximum output current plus inductor ripple current
- $r_{DS(on)}$ max = maximum P-channel switch $r_{DS(on)}$.
- R_L = DC resistance of the inductor
- V_O (max) = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables all internal circuitry. The undervoltage lockout threshold, sensed at the V_{CC} pin is typically 1.8 V, max 2 V.

Mode Selection

The MODE pin allows mode selection between forced PWM Mode and power Safe Mode for both converters. Connecting this pin to GND enables the automatic PWM and power save mode operation. The converters operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads. For additional flexibility, it is possible to switch from power save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

Enable

To start up each converter independently, the device has a separate enable pin for each DC/DC converter and for each LDO. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4 are set to high, the corresponding converter starts up with soft start as previously described.

Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in the electrical characteristics. In this mode, the P and N-Channel MOSFETs are turned-off, the and the entire internal control circuitry is switched-off. If disabled, the outputs of the LDOs are pulled low by internal 350Ω resistors, actively discharging the output capacitor. For proper operation, the enable pins must be terminated and must not be left unconnected.

$\overline{\text{RESET}}$

The TPS65051, TPS65052, TPS65054 and TPS65056 contain circuitry that can generate a reset pulse for a processor with a 100 ms delay time. The input voltage at a comparator is sensed at an input called threshold. When the voltage exceeds the threshold, the output goes high with a 100-ms delay time. A hysteresis can be defined with an external resistor connected to the hysteresis input. This circuitry is functional as soon as the supply voltage at V_{CC} exceeds the undervoltage lockout threshold. Therefore, the TPS6505x has a shutdown current (all DCDC converters and LDOs are off) of 9 µA in order to supply bandgap and comparator.

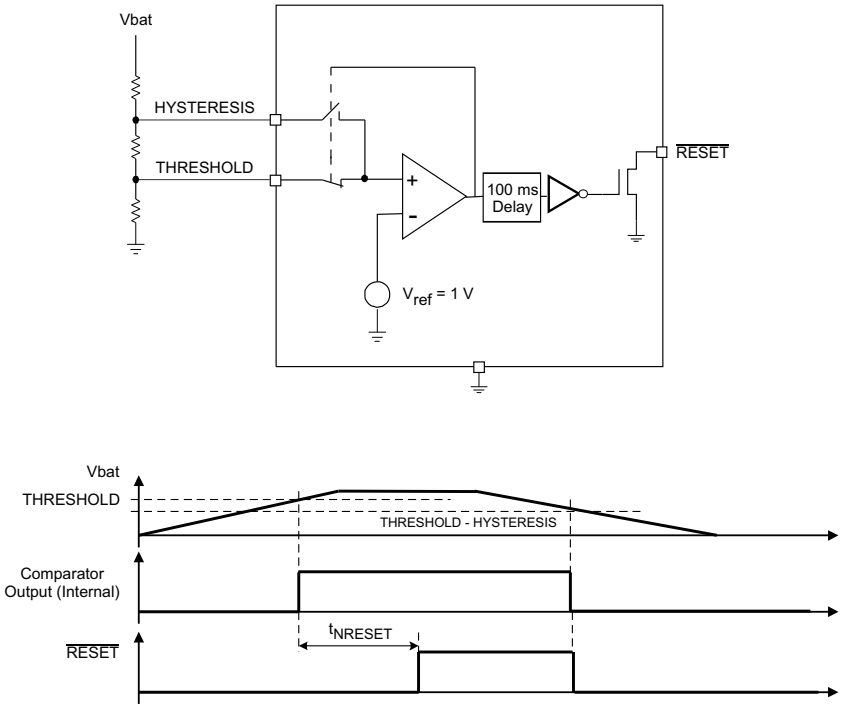


Figure 21. $\overline{\text{RESET}}$ Pulse Circuit

Push-Button ON-OFF (PB-ON-OFF)

The TPS65050 provides a PB-ON-OFF functionality instead of supervising a voltage with the threshold and hysteresis inputs. The output at PB_OUT is held low after voltage is applied at V_{CC}. Only after the input at PB-IN is pulled high once, the output driver at PB_OUT goes to its inactive state, driven high with its external pullup resistor. Further low-high pulses at PB-IN toggles the status of the PB_OUT output, and can be used to shutdown and start the converter with a single push on a button by connecting the PB_OUT output to the enable input of the converters.

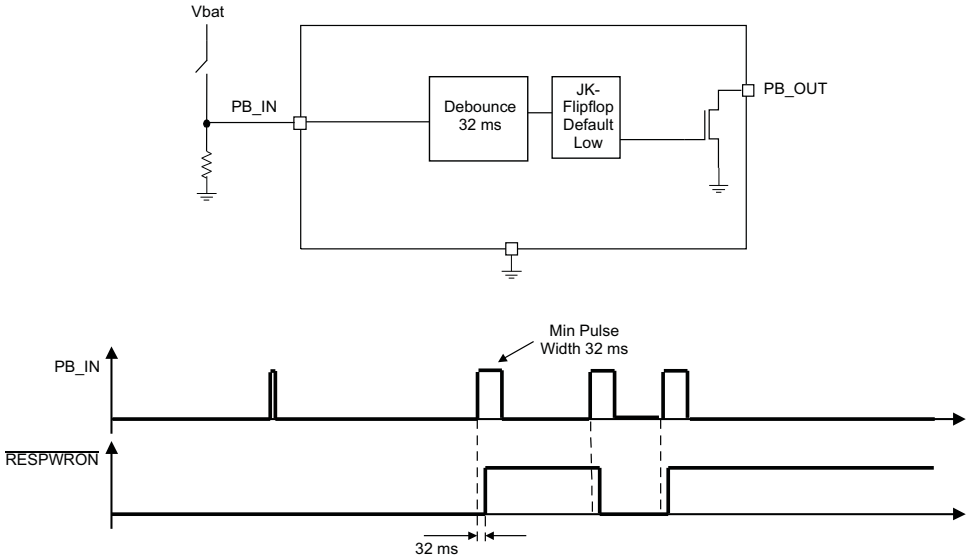


Figure 22. Push-Button Circuit

Short-Circuit Protection

All outputs are short-circuit protected with a maximum output current as defined in the *Electrical Characteristics*.

Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typically) for the DC/DC converters, the device goes into thermal shutdown. In this mode, the P and N-Channel MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the DC/DC converters disables both converters simultaneously.

The thermal shutdown temperature for the LDOs are set to typically 140°C. Therefore, a LDO which may be used to power an external voltage never heats up the chip high enough to turn off the DC/DC converters. If one LDO exceeds the thermal shutdown temperature, all LDOs turns off simultaneously.

Low Dropout Voltage Regulators

The low dropout voltage regulators are designed to operate well with small ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 280 mV at rated output current. Each LDO supports a current limit feature. The LDOs are enabled by the EN_LDO1, ENLDO2, EN_LDO3 and EN_LDO4 pin. In TPS65050 and TPS65052, the output voltage of the LDOs is set using 4 pins. The DEFLDO1 to DEFLDO4 pins can either be connected to GND or Vbat (V_{CC}) to define a set of output voltages for LDO1 to LDO4 according to table 1. Connecting the DEFLDOx pins to a voltage different from GND or V_{CC} causes increased leakage current into V_{CC}. In TPS65051 and TPS65054, the output voltage of the LDOs is set using external resistor dividers.

TPS65050 and TPS65052 default voltage options adjustable with DEFLDO4…DEFLDO1 according to Table 1.

Table 1. Default Options

DEFLDO1	DEFLDO2	DEFLDO3	DEFLDO4	VLDO1	VLDO2	VLDO3	VLDO4
				400 mA LDO	400 mA LDO	200 mA LDO	200 mA LDO
				1.8 V - 5.5 V Input	1.8 V - 5.5 V Input	1.5 V - 5.5 V Input	1.5 V - 5.5 V Input
0	0	0	0	3.3 V	3.3 V	1.85 V	1.85 V
0	0	0	1	3.3 V	3.3 V	1.5 V	1.5 V
0	0	1	0	3.3 V	2.85 V	2.85 V	2.7 V
0	0	1	1	3.3 V	2.85 V	2.85 V	2.5 V
0	1	0	0	3.3 V	2.85 V	2.85 V	1.85 V
0	1	0	1	3.3 V	2.85 V	1.85 V	1.85 V
0	1	1	0	3.3 V	2.85 V	1.5 V	1.5 V
0	1	1	1	3.3 V	2.85 V	1.5 V	1.3 V
1	0	0	0	3.3 V	2.85 V	1.1 V	1.3 V
1	0	0	1	2.85 V	2.85 V	1.85 V	1.85 V
1	0	1	0	2.7 V	3.3 V	1.2 V	1.2 V
1	0	1	1	2.5 V	3.3 V	1.5 V	1.5 V
1	1	0	0	2.5 V	3.3 V	1.5 V	1.3 V
1	1	0	1	1.85 V	1.85 V	1.35 V	1.35 V
1	1	1	0	1.8 V	2.5 V	3.3 V	2.85 V
1	1	1	1	1.2 V	1.8 V	1.1 V	1.3 V

APPLICATION INFORMATION

Output Voltage Setting

Converter 1 (DCDC1)

The output voltage of converter 1 can be set by an external resistor network. The output voltage can be calculated using Equation 4.

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

with an internal reference voltage V_{ref}, 0.6 V .

Setting the total resistance of R1 + R2 to less than 1 MΩ is recommended. The resistor network connects to the input of the feedback amplifier, therefore, requiring a small feedforward capacitor in parallel to R1. A typical value of 47 pF is sufficient.

Converter 2 (DCDC2)

The output voltage of converter 2 can be selected as following:

- Adjustable output voltage defined with external resistor network on pin DEFDCDC2. This option is available for TPS65050 and TPS65051.
- Two default fixed output voltages selectable by pin DEFDCDC2, see Table 2. This option is available for TPS65052 and TPS65054.

Table 2. Default Fixed Output Voltages

Converter 2	DEFDCDC2 = low	DEFDCDC2 = high
TPS65050	--	--
TPS65051	--	--
TPS65052	1 V	1.3 V
TPS65054	1.3 V	1.05 V
TPS65056	1 V	1.3 V

The adjustable output voltage can be calculated similar to the DCDC1 converter. Setting the total resistance of R3 + R4 to less than 1 MΩ is recommended. Route the DEFDCDC2 line separate from noise sources, such as the inductor or the L2 line. The VDCDC2 line needs to be directly connected to the output capacitor. As the VDCDC2 line is the feedback to the internal amplifier, no feedforward capacitor at R3 is needed.

Using an external resistor divider at DEFDCDC2:

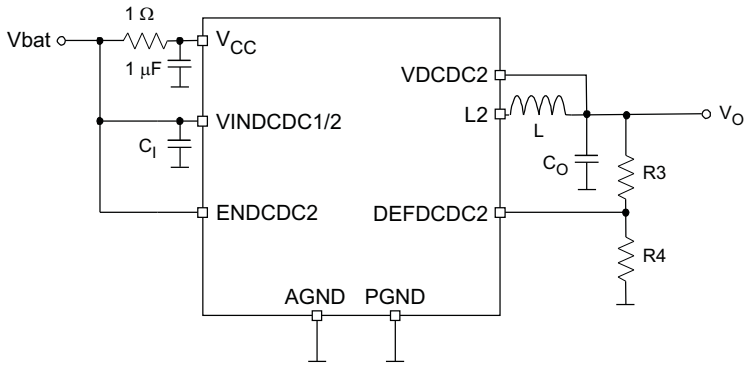


Figure 23. External Resistor Divider

$V_{(DEFDCDC2)}$ = 0.6 V

$$V_O = V_{(DEFDCDC2)} \times \frac{R3 + R4}{R4} \qquad R3 = R4 \times \left(\frac{V_O}{V_{(DEFDCDC2)}} \right) - R4 \tag{5}$$

See Table 3 for typical resistor values:

Table 3. Typical Resistor Values

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE	Typical CFF
3.3 V	680 kΩ	150 kΩ	3.32 V	47 pF
3 V	510 kΩ	130 kΩ	2.95 V	47 pF
2.85 V	560 kΩ	150 kΩ	2.84 V	47 pF
2.5 V	510 kΩ	160 kΩ	2.51 V	47 pF
1.8 V	300 kΩ	150 kΩ	1.8 v	47 pF
1.6 V	200 kΩ	120 kΩ	1.6 V	47 pF
1.5 V	300 kΩ	200 kΩ	1.5 V	47 pF
1.2 V	330 kΩ	330 kΩ	1.2 V	47 pF

Output Filter Design (Inductor and Output Capacitor)

Inductor Selection

The two converters operate with 2.2-µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency. The minimum inductor value is 1.5 µH, but an output capacitor of 22 µF minimum is needed in this case. For an output voltage above 2.8 V, an inductor value of 3.3 µH minimum is recommended. Lower values result in an increased output voltage ripple in PFM mode.

Equation 6 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 6. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L(max) = I_O(max) + \frac{\Delta I_L}{2} \tag{6}$$

with:

- f = Switching Frequency (2.25-MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_L$max = Maximum Inductor current

The highest inductor current occurs at maximum V_I. Open core inductors have a soft saturation characteristic, and they can normally handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consideration must be given to the difference in the core material from inductor to inductor which has an impact on the efficiency especially at high switching frequencies. See Table 4 and the typical applications for possible inductors.

Table 4. Tested Inductors

Inductor Type	Inductor Value	Supplier
LPS3010	2.2 µH	Coilcraft
LPS3015	3.3 µH	Coilcraft
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allow the use of small ceramic capacitors with a value of 22-µF (typical), without having large output voltage undershoots and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple, and are recommended.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{(RMSCout)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (7)$$

At nominal load current, the inductive converters operate in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \quad (8)$$

Where the highest output voltage ripple occurs at the highest input voltage V_I.

At light load currents, the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 5. Possible Capacitors

Capacitor Value	Size	Supplier	Type
2.2 µF	0805	TDK C2012X5R0J226MT	Ceramic
2.2 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic
10 µF	0603	Taiyo Yuden JMK107BJ106MA	Ceramic

Low Drop Out Voltage Regulators (LDOs)

The output voltage of all 4 LDOs in TPS65051, TPS65054 and TPS65056 are set by an external resistor network. The output voltage is calculated using Equation 9:

$$V_O = V_{ref} \times \left(1 + \frac{R5}{R6}\right) \quad (9)$$

with an internal reference voltage, V_{ref}, 1 V (typical)

Setting the total resistance of R5 + R6 to less than 1 MΩ is recommended. Typically, there is no feedforward capacitor needed at the voltage dividers for the LDOs.

$$V_O = V_{(FB_LDOs)} \times \frac{R5 + R6}{R6} \qquad R5 = R6 \times \left(\frac{V_O}{V_{(FB_LDOs)}}\right) - R6 \quad (10)$$

Typical resistor values:

Table 6. Typical Resistor Values

OUTPUT VOLTAGE	R5	R6	NOMINAL VOLTAGE
3.3 V	300 kΩ	130 kΩ	3.31 V
3 V	300 kΩ	150 kΩ	3 V
2.85 V	240 kΩ	130 kΩ	2.85 V
2.8 V	260 kΩ	200 kΩ	2.8 V
2.5 V	300 kΩ	200 kΩ	2.5 V
1.8 V	240 kΩ	300 kΩ	1.8 v
1.5 V	150 kΩ	300 kΩ	1.5 V
1.3 V	36 kΩ	120 kΩ	1.3 V
1.2 V	100 kΩ	510 kΩ	1.19 V
1.1 V	33 kΩ	330 kΩ	1.1 V

LAYOUT CONSIDERATIONS

Application Circuits

PB-ONOFF and Sequencing

The PB-ONOFF output can be used to enable one or several converters. After power up, the PB_OUT pin is low, and pulls down the enable pins connected to PB_OUT; EN_DCDC1, and EN_LDO1 in Figure 24. When PB_IN is pulled to V_{CC} for longer than 32 ms, the PB_OUT pin is turned off, hence the enable pins pulled high using a pull-up resistor to V_{CC}. This enables the DCDC1 converter and LDO1. The output voltage of DCDC1 ($V_{OUT}1$) is used as the enable signal for DCDC2 and LDO2 to LDO4. LDO1 with its output voltage of 3.3 V and LDO2 for an output voltage of 2.5 V are powered from the battery ($V_{(bat)}$) directly. To save power, the input voltage for the lower voltage rails at LDO3 and LDO4 are derived from the output of the step-down converters, keeping the voltage drop at the LDOs low to increase efficiency. As LDO3 and LDO4 are powered from the output of DCDC1, the total output current on $V_{OUT}1$, LDO3 and LDO4 must not exceed the maximum rating of DCDC1.

Figure 25 shows the power up timing for this application.

LAYOUT CONSIDERATIONS (continued)

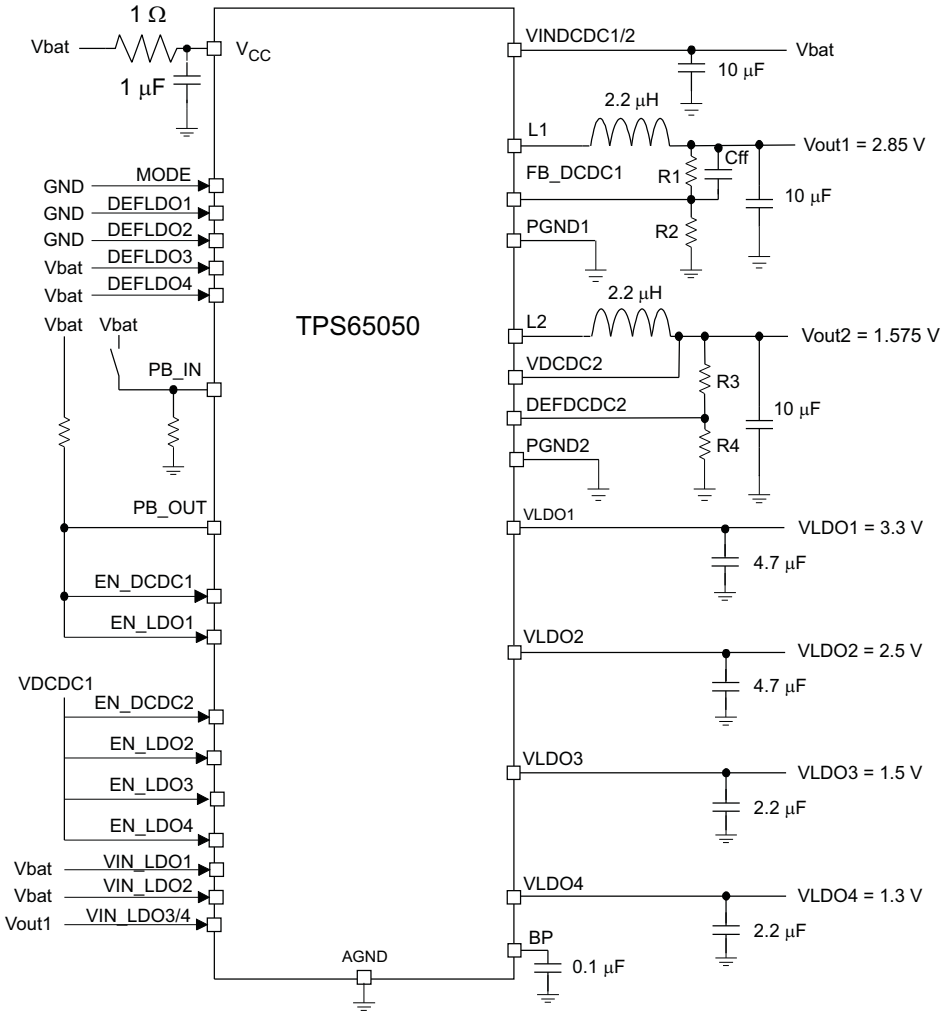


Figure 24. PB_ON/OFF Circuit

LAYOUT CONSIDERATIONS (continued)

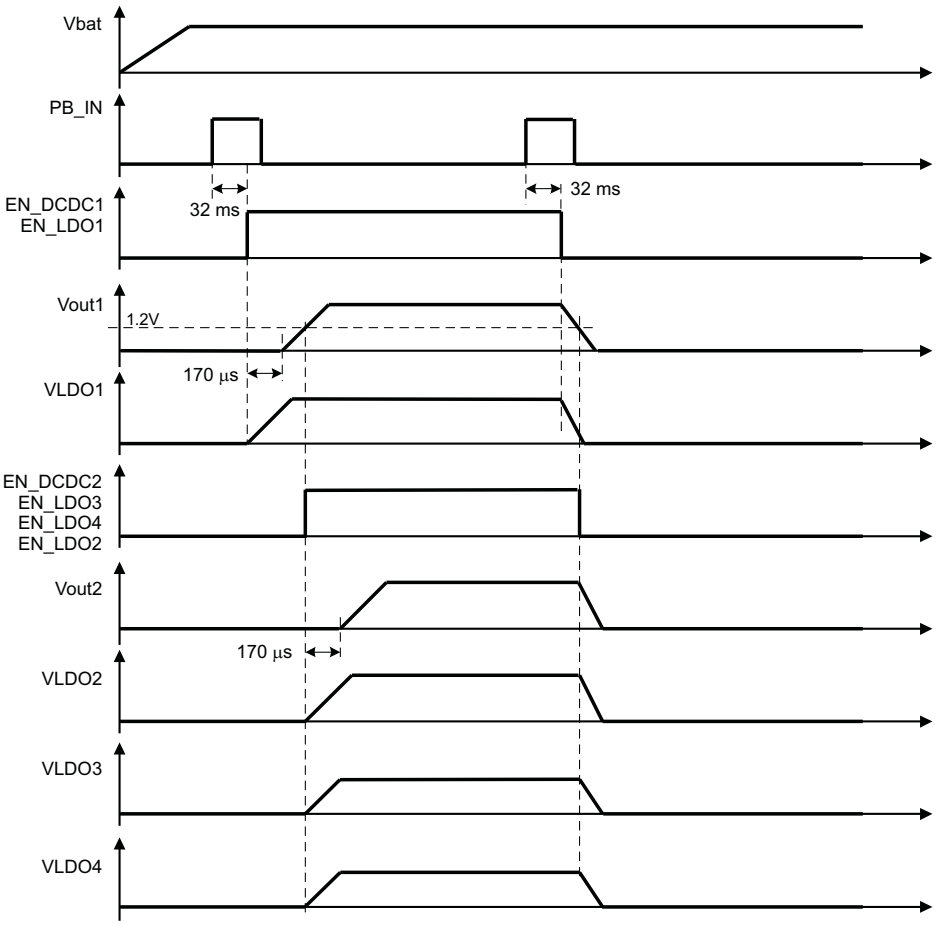


Figure 25. Power Up Timing

$\overline{\text{RESET}}$

TPS65051, TPS65052, TPS65054 and TPS65056 contain a comparator that are used to supervise a voltage connected to an external voltage divider, and generate a reset signal if the voltage is lower than the threshold. The rising edge is delayed by 100 ms at the open drain $\overline{\text{RESET}}$ output. The values for the external resistors R3 to R5 are calculated as follows:

V_L = lower voltage threshold

V_H = higher voltage threshold

V_{REF} = reference voltage (1 V)

Example:

- V_L = 3.3 V
- V_H = 3.4 V

  Set R5 = 100 kΩ

  → R3 + R4 = 240 kΩ

  → R4 = 3.03 kΩ

  → R3 = 237 kΩ

LAYOUT CONSIDERATIONS (continued)

$$R3 + R4 = R5 \times \left(\frac{V_H}{V_{ref}} - 1 \right)$$

$$R4 = R5 \times \frac{V_H - V_L}{V_L} \quad (11)$$

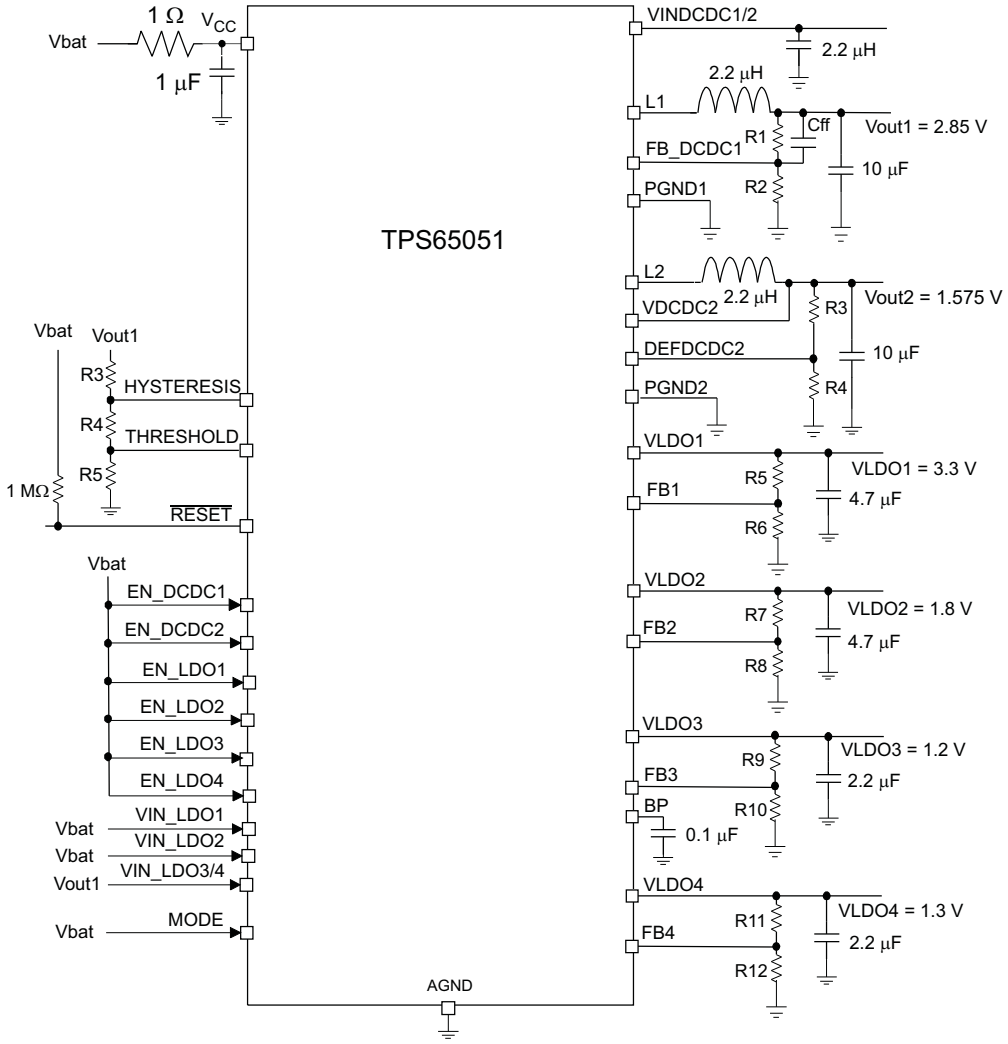


Figure 26. $\overline{\text{RESET}}$ Circuit

THERMAL PAD MECHANICAL DATA

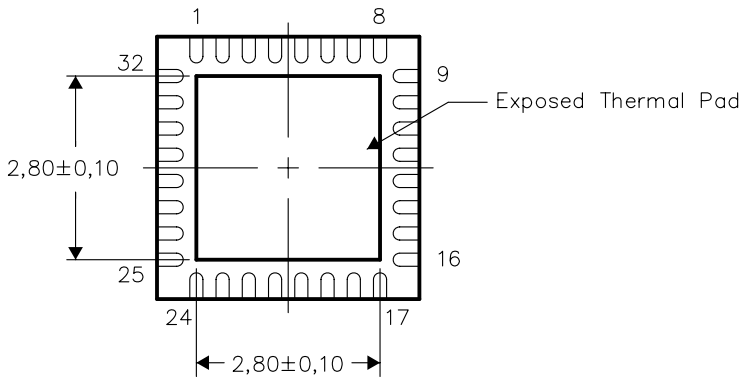
RSM (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



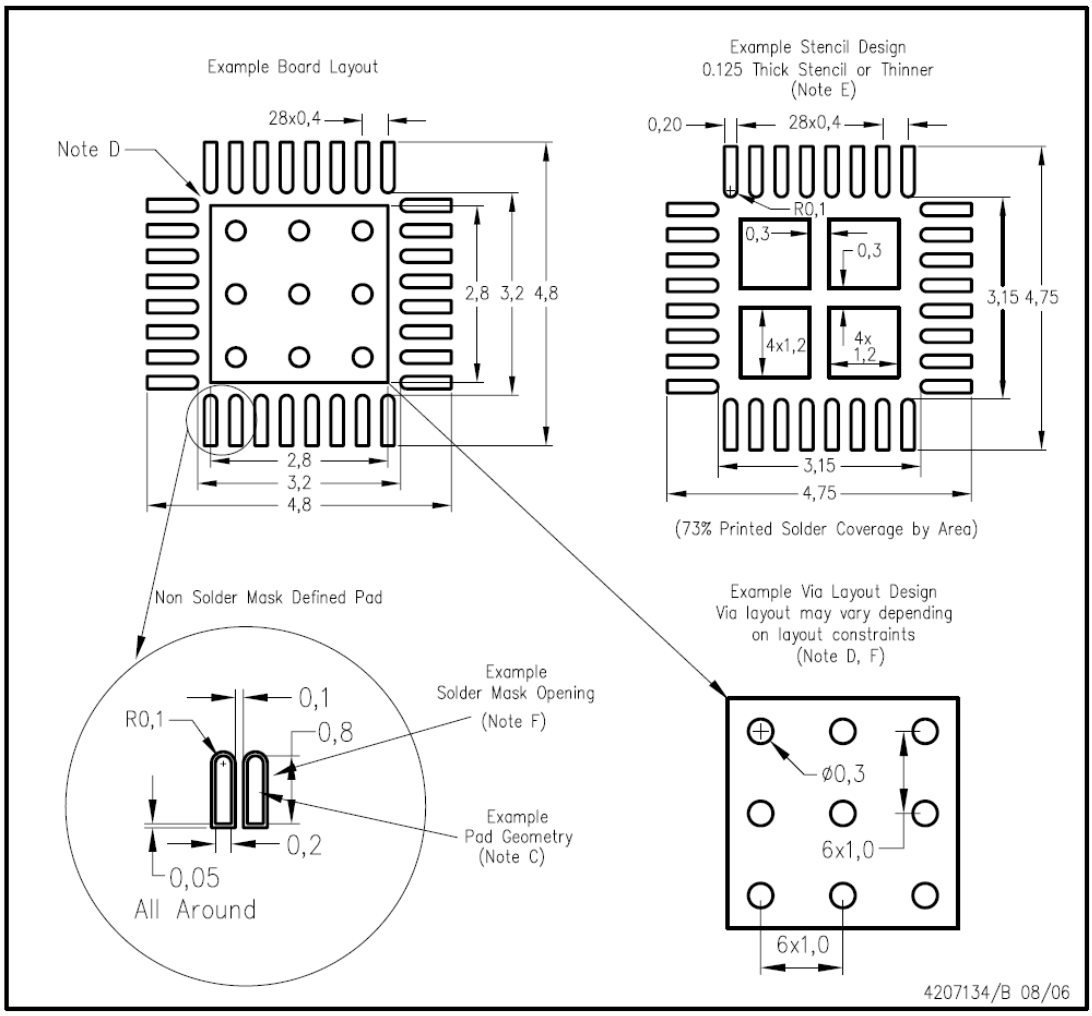
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

LAND PATTERN

RSM (S–PQFP–N32)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65050RSMR	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65050RSMRG4	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65050RSMT	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65050RSMTG4	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65051RSMR	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65051RSMRG4	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65051RSMT	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65051RSMTG4	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65052RSMR	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65052RSMRG4	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65052RSMT	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65052RSMTG4	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65054RSMR	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65054RSMRG4	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65054RSMT	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65054RSMTG4	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65056RSMR	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65056RSMRG4	ACTIVE	QFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65056RSMT	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65056RSMTG4	ACTIVE	QFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

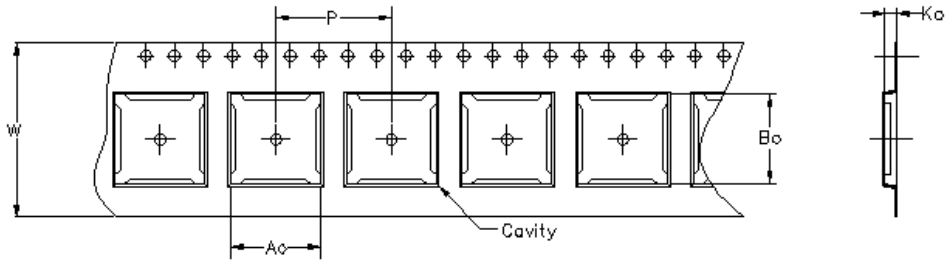
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

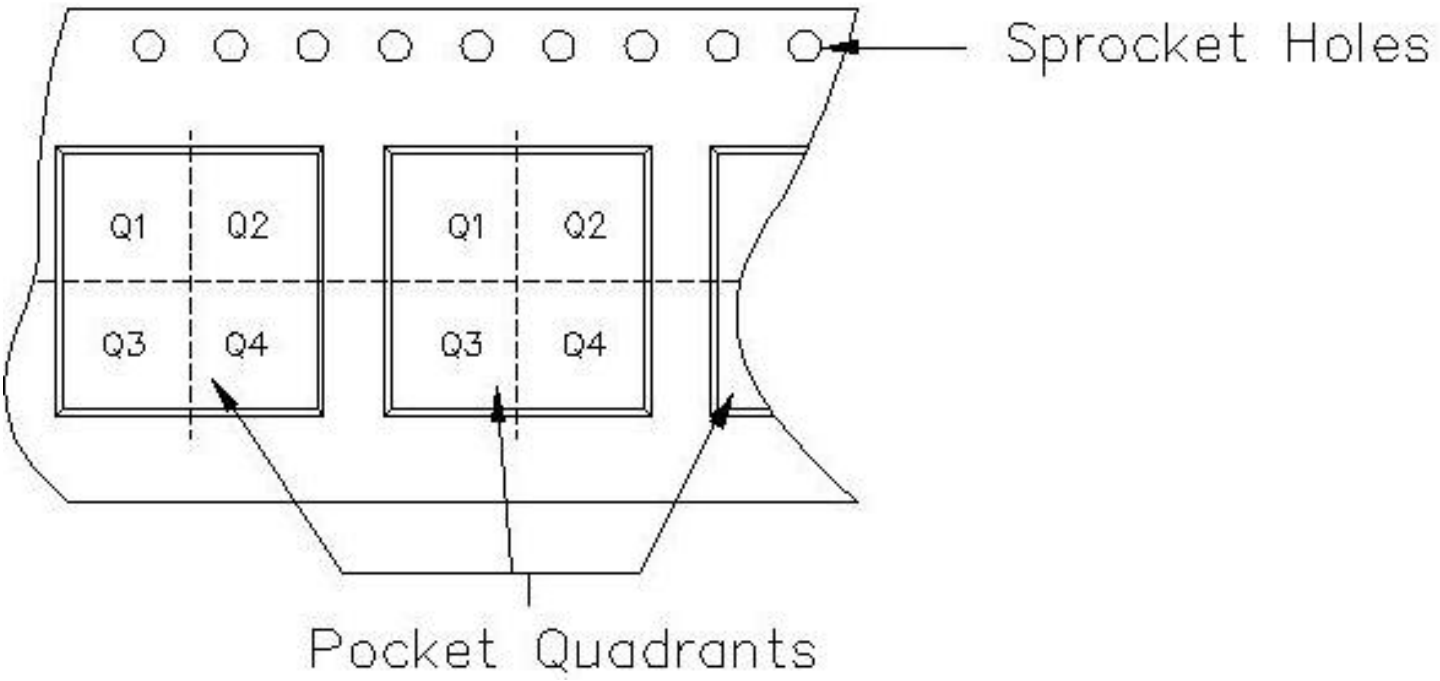
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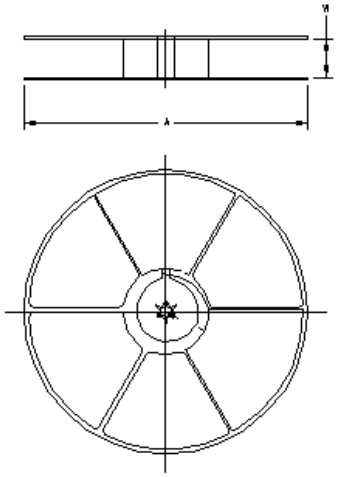
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



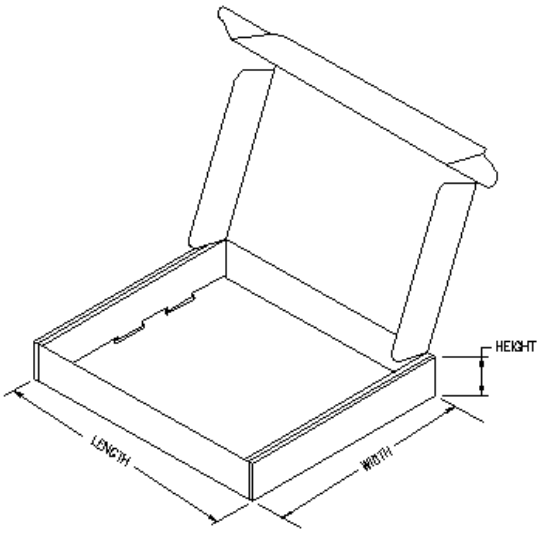
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65050RSMR	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65050RSMT	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65051RSMR	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65051RSMT	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65052RSMR	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65052RSMT	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65054RSMR	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65054RSMT	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65056RSMR	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP
TPS65056RSMT	RSM	32	FRB	330	12	4.3	4.3	1.5	12	12	PKGORNT2TR-MSP

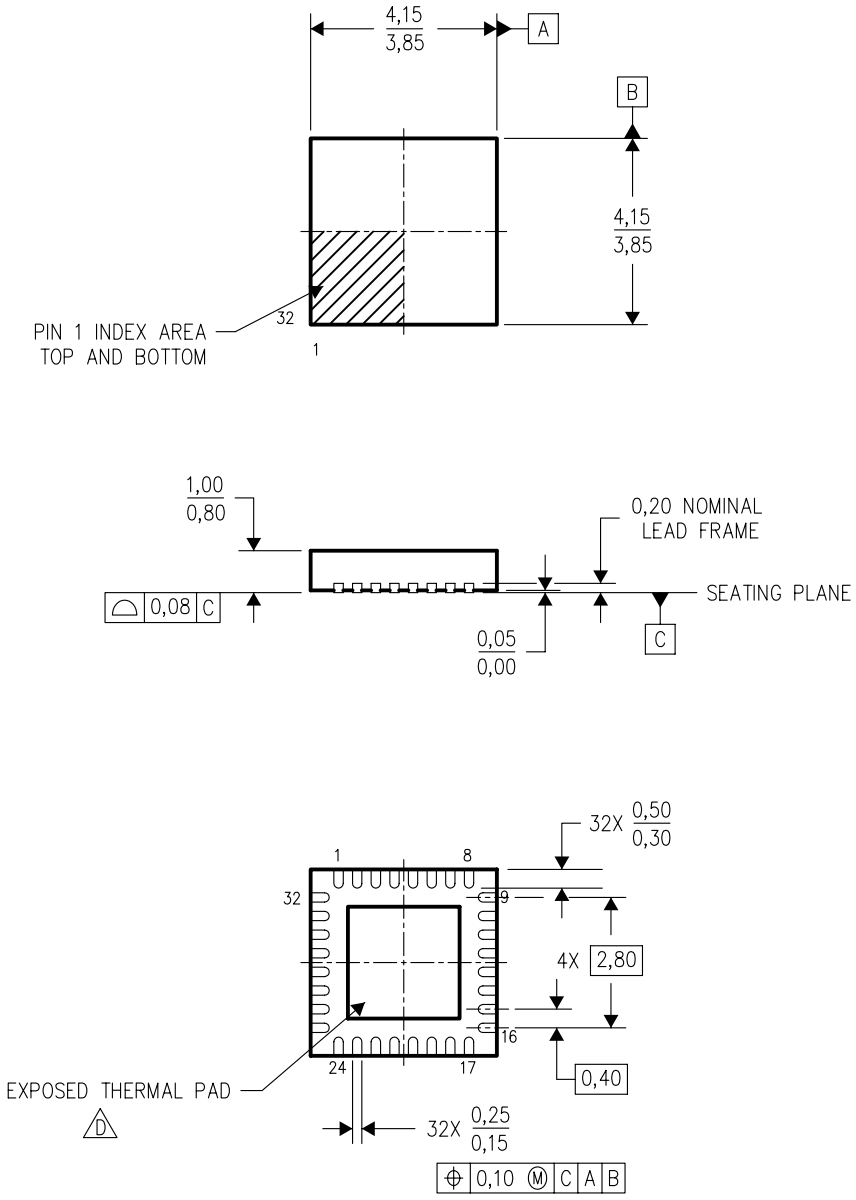


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS65050RSMR	RSM	32	FRB	342.9	336.6	20.6
TPS65050RSMT	RSM	32	FRB	342.9	336.6	20.6
TPS65051RSMR	RSM	32	FRB	342.9	336.6	20.6
TPS65051RSMT	RSM	32	FRB	342.9	336.6	20.6
TPS65052RSMR	RSM	32	FRB	342.9	336.6	20.6
TPS65052RSMT	RSM	32	FRB	342.9	336.6	20.6
TPS65054RSMR	RSM	32	FRB	342.9	336.6	20.6
TPS65054RSMT	RSM	32	FRB	342.9	336.6	20.6
TPS65056RSMR	RSM	32	FRB	342.9	336.6	20.6
TPS65056RSMT	RSM	32	FRB	342.9	336.6	20.6



RSM (S–PQFP–N32) PLASTIC QUAD FLATPACK



4207560/A 12/05

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

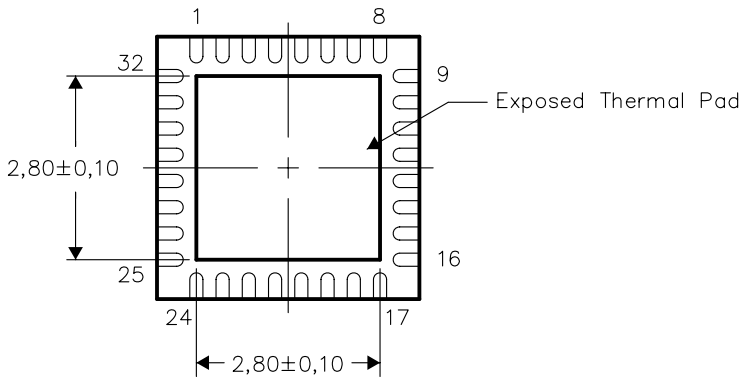
RSM (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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