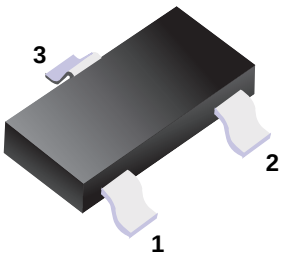
■ N-Channel Enhancement MOSFET

■ Features

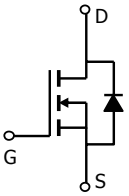
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

lead-free ROHS



1. Gate
2. Source
3. Drain

■ Simplified outline(SOT23-3L)



■ Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Description

The KF1002 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

V_{DSS}	$R_{DS(ON)}$ @10V (typ)	I_D
100V	185mΩ	2A

■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	2	A
Drain Current-Pulsed (Note 1)	I_{DM}	5	A
Maximum Power Dissipation	P_D	1.1	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

■ Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	120	℃/W

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=1A	-	185	220	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=1A	1	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	190	-	PF
Output Capacitance	C_{oss}		-	22	-	PF
Reverse Transfer Capacitance	C_{rss}		-	13	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V,I_D=1.3A,R_L=39Ω V_{GS}=10V,R_G=1Ω	-	6	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	10	-	nS
Turn-Off Fall Time	t_f		-	6	-	nS
Total Gate Charge	Q_g	V_{DS}=50V,I_D=1.3A, V_{GS}=10V	-	5.2		nC
Gate-Source Charge	Q_{gs}		-	0.75	-	nC
Gate-Drain Charge	Q_{gd}		-	1.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=1.3A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	2	A

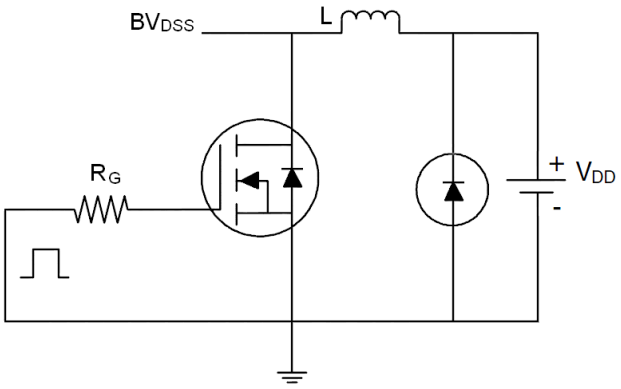
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

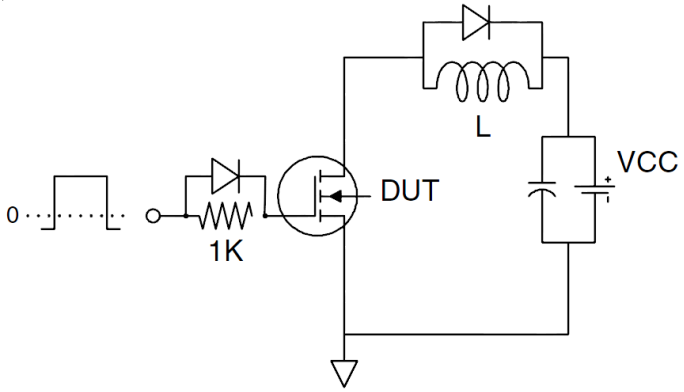
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Test Circuit

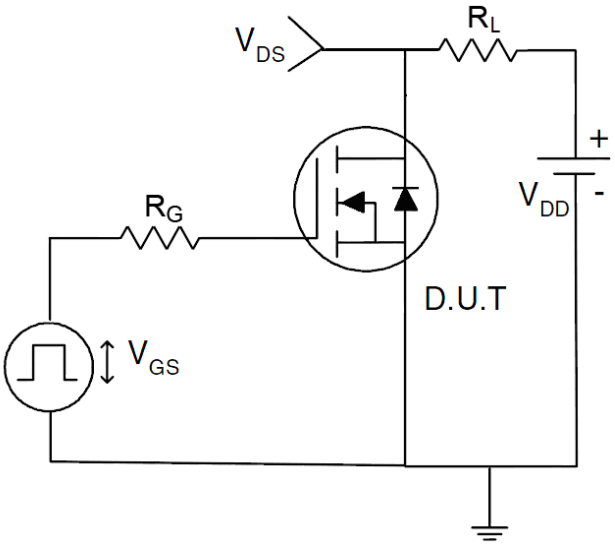
1）E_{AS} test circuit



2）Gate charge test circuit



3）Switch Time Test Circuit



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Typical Electrical and Thermal Characteristics (Curves)

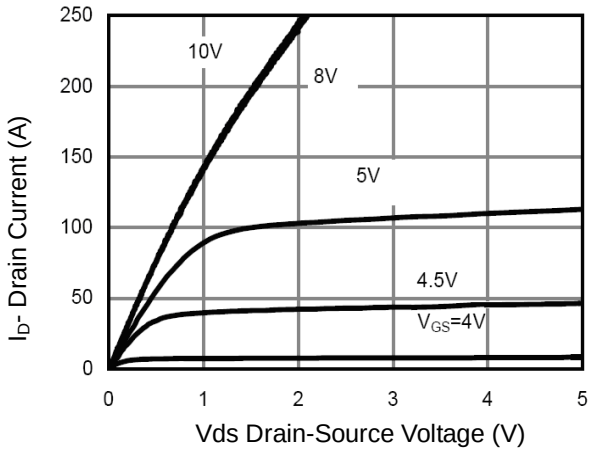


Figure 1 Output Characteristics

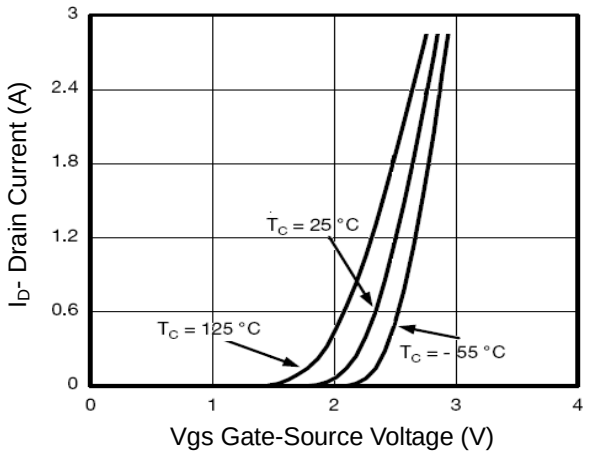


Figure 2 Transfer Characteristics

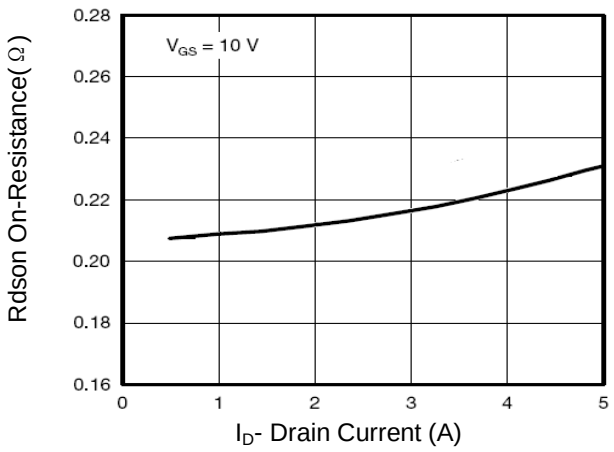


Figure 3 Rdson- Drain Current

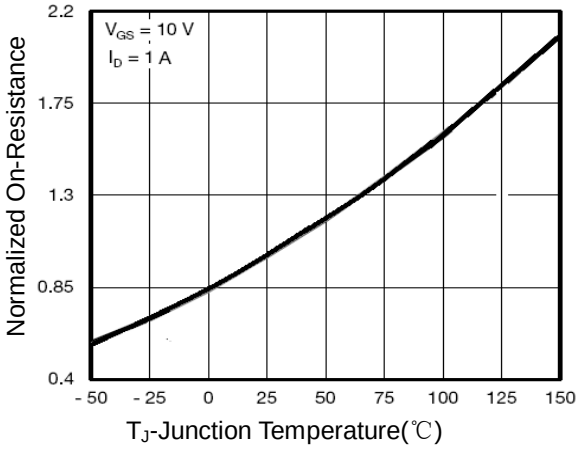


Figure 4 Rdson-JunctionTemperature

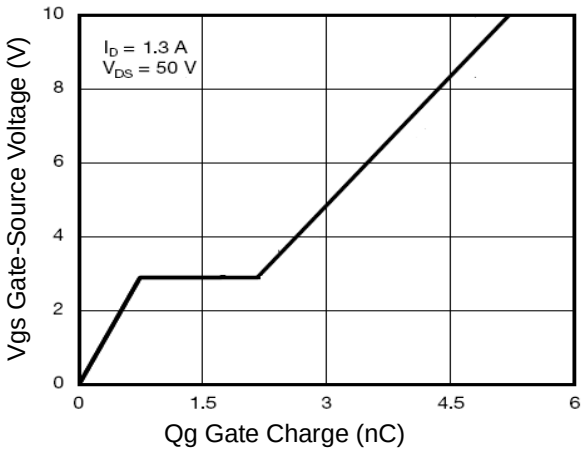


Figure 5 Gate Charge

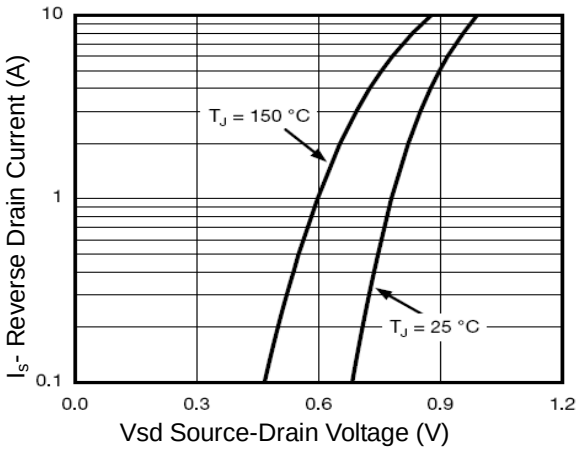


Figure 6 Source- Drain Diode Forward

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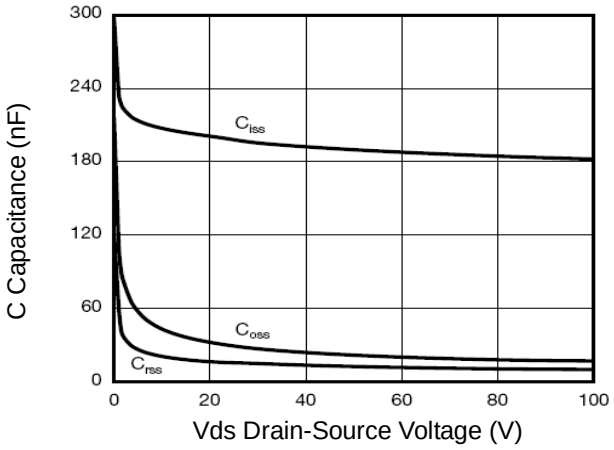


Figure 7 Capacitance vs Vds

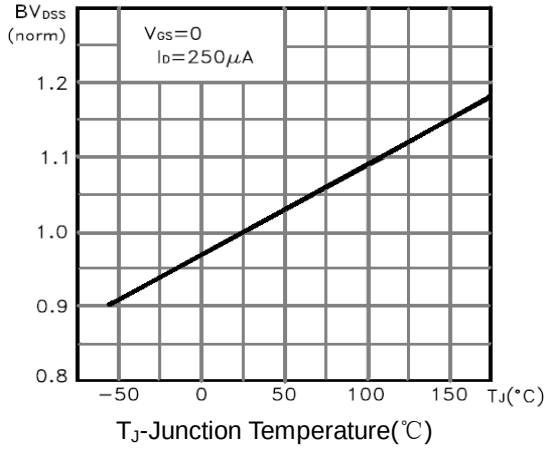


Figure 9 BV_{DSS} vs Junction Temperature

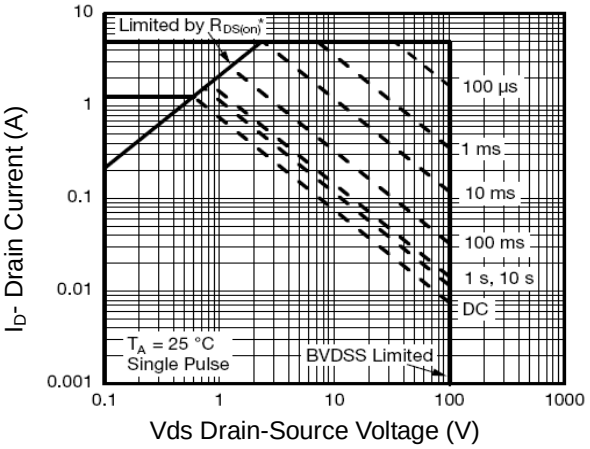


Figure 8 Safe Operation Area

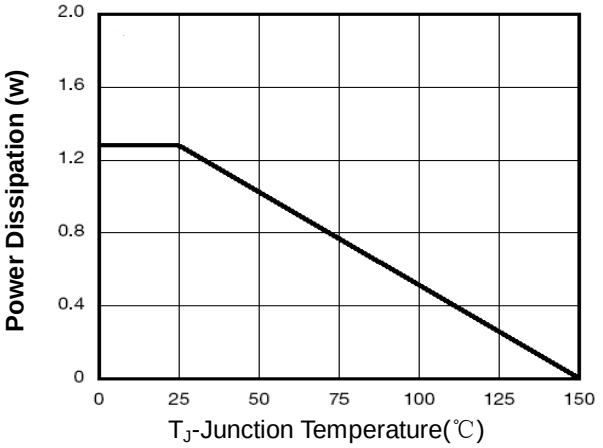


Figure 10 Power De-rating

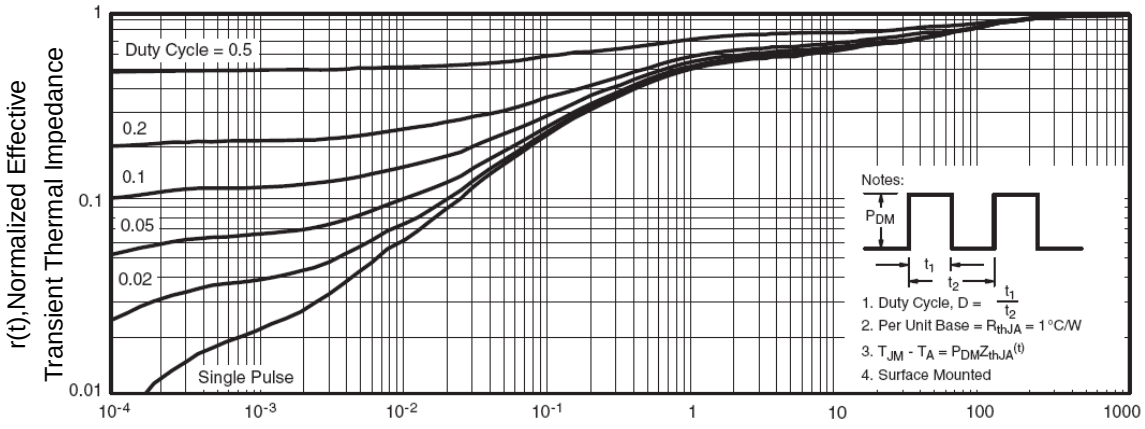
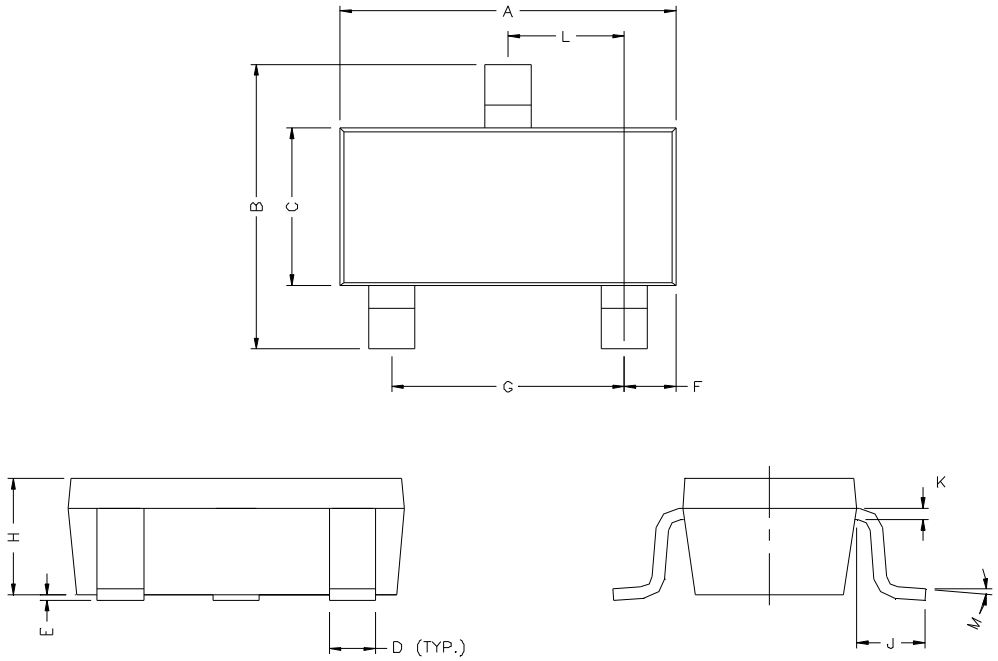


Figure 11 Normalized Maximum Transient Thermal Impedance

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Package Outline SOT23-3L



DIMENSIONS (mm are the original dimensions)

UNIT	A	B	C	D	E	F	G	H	K	J	L	M
mm	2.70 3.10	2.65 2.95	1.50 1.70	0.35 0.50	0 0.10	0.45 0.55	1.9	1.00 1.30	0.10 0.20	0.40 -	0.85 1.15	0° 10°

Summary of Packing Options

Package	Package Description	Packing Quantity	Industry Standard
SOT23-3L	Tape/Reel,7”reel	3000	EIA-481-1

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