# ADS816x 8-Channel, 16-Bit, 1-MSPS SAR ADC With Easy to Drive Analog Inputs

## 1 Features

- Compact Low Power Data Acquisition System:
  - MUX Breakout Enables Single External Driver Amplifier
  - Single-Supply Operation
  - 16-Bit SAR ADC
  - Low Drift Integrated Reference and Buffer
  - 0.5 × $V_{REF}$ Output for Analog Input DC Biasing
- Excellent AC and DC Performance:
  - SNR: 92-dB, THD: –110-dB
  - INL: ±0.3-LSB, 16-Bit No Missing Codes
- Low Leakage Multiplexer With Sequencer:
  - Multiple Channel Sequencing Options:
    - Manual Mode, On-the-Fly Mode, Auto Sequence Mode, Custom Channel Sequencing
  - Early Switching Enables Direct Sensor Interface
  - Fast Response Time with On-the-Fly Mode
- System Monitoring Features:
  - Per Channel Programmable Window Comparator
  - Alert Output for MCU Interrupt
  - False Trigger Avoidance With Programmable Hysteresis
- Enhanced-SPI Digital Interface:
  - 1-MSPS Throughput With 16-MHz SCLK
  - High-Speed, 70-MHz Digital Interface
- Wide Temperature Range: –40°C to +125°C

## 2 Applications

- Optical Line Cards
- Data Acquisition Cards
- Test and Measurement
- Patient Monitoring
- PLC Universal Analog Input Module

## 3 Description

The ADS816x is a family of 16-bit, 8-channel, high-precision successive approximation register (SAR) analog-to-digital converters (ADCs) operating from a single 5-V supply with 1-MSPS (ADS8168) and 250-kSPS (ADS8166) total throughput.

The input multiplexer supports extended settling time, which makes driving the analog inputs easier. The output of the multiplexer and ADC analog inputs are available as device pins. This configuration allows one ADC driver op amp to be used for all eight analog inputs of the multiplexer. The ADS816x simplifies processing of data with an enhanced channel sequencer, which reduces software complexity.

The ADS816x device family features a digital window comparator with programmable high and low alarm thresholds with hysteresis per analog input channel. The single op-amp solution with programmable alarm thresholds enables low power, low cost, and smallest form factor applications.

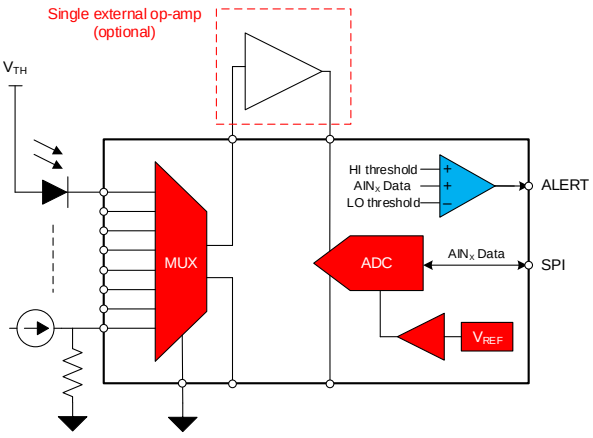
**Device Information**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ADS816x | VQFN (32) | 5.00 mm × 5.00 mm |

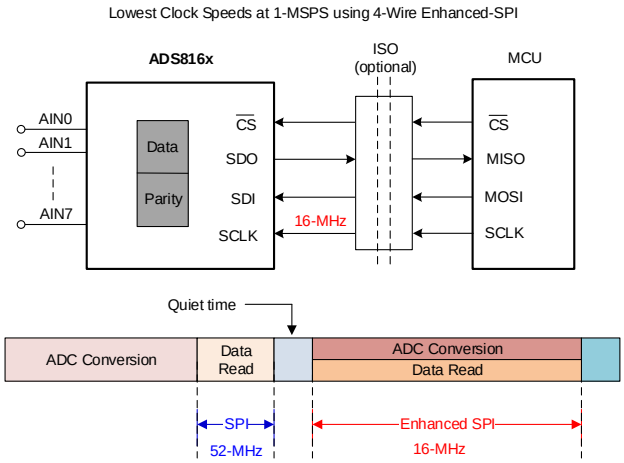
(1) For all package options refer to mechanical drawing section at the end of the datasheet.

ADVANCE INFORMATION

**ADS816x Application Topologies**




Small Form Factor Solution for Multiple Input Types



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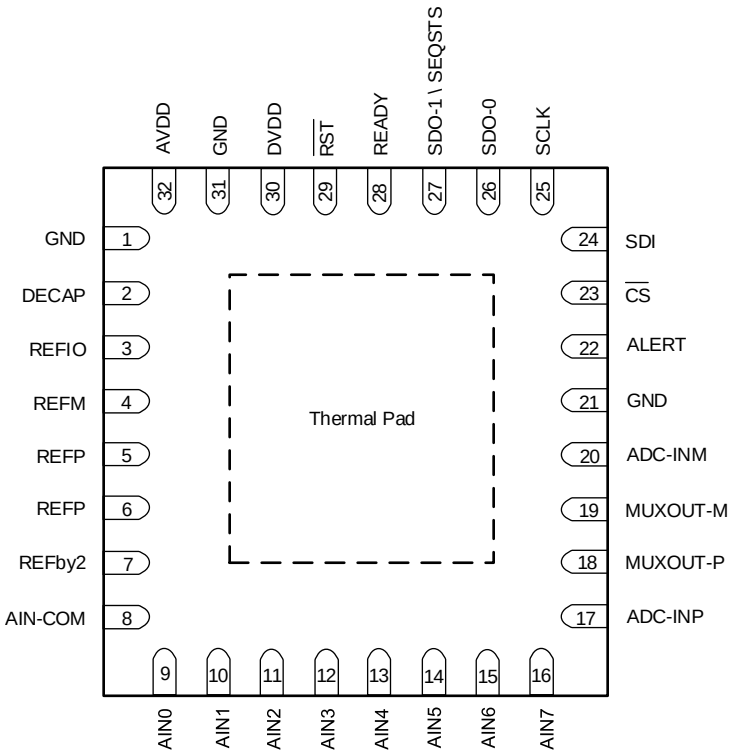
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (November 2017) to Revision A | Page |
|---|---|
| • Added ADS8166 to document | 1 |
| • Changed *Lookup Based Channel Sequencing* to *Custom Channel Sequencing* in *Low Leakage Multiplexer* sub-bullet | 1 |
| • Changed *Description* section for clarity | 1 |
| • Added minimum and maximum limits added throughout *Specifications* section | 5 |
| • Added *Typical Characteristics* section | 12 |
| • Changed *Detailed Description* section for clarity | 16 |

# 5 Pin Configuration and Functions

**RHB Package**
**32-Pin VQFN**
**Top View**




TOP VIEW

**Pin Functions**

| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADC-INM | 20 | Analog input | Negative ADC analog input. |
| ADC-INP | 17 | Analog input | Positive ADC analog input. |
| AIN0 | 9 | Analog input | Analog input channel 0. |
| AIN1 | 10 | Analog input | Analog input channel 1. |
| AIN2 | 11 | Analog input | Analog input channel 2. |
| AIN3 | 12 | Analog input | Analog input channel 3. |
| AIN4 | 13 | Analog input | Analog input channel 4. |
| AIN5 | 14 | Analog input | Analog input channel 5. |
| AIN6 | 15 | Analog input | Analog input channel 6. |
| AIN7 | 16 | Analog input | Analog input channel 7. |
| AIN-COM | 8 | Analog input | Common analog input. |
| ALERT | 22 | Digital output | Digital ALERT output; active high.<br>This pin is the output of the logical OR of the enabled channel ALERTs. |
| AVDD | 32 | Power supply | Analog power supply pin. Connect 1-µF capacitor to GND. |
| $\overline{CS}$ | 23 | Digital input | Chip-select input pin; active low.<br>The device starts conversion of the active input channel on the rising edge of $\overline{CS}$.<br>The device takes control of the data bus when $\overline{CS}$ is low.<br>The SDO-x pins go to Hi-Z when $\overline{CS}$ is high. |

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## Pin Functions (continued)

| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DECAP | 2 | Power supply | Connect 1-µF capacitor to GND for internal power supply. |
| DVDD | 30 | Power supply | Interface power supply pin. Connect 1-µF capacitor to GND. |
| GND | 1, 21, 31 | Power supply | Ground. |
| MUXOUT-M | 19 | Analog output | MUX negative analog output. |
| MUXOUT-P | 18 | Analog output | MUX positive analog output. |
| READY | 28 | Digital output | Multifunction output pin.<br>With $\overline{CS}$ held high, READY reflects the device conversion status. READY is low when a conversion is on-going.<br>With $\overline{CS}$ low, the status of READY depends on the output protocol selection. |
| REFby2 | 7 | Analog output | The output voltage on this pin is equal to half the voltage on REFP pin. Connect 1-µF capacitor to GND. |
| REFIO | 3 | Analog input/output | Reference voltage input; internal reference 4.096-V output. Connect 1-µF capacitor to GND. |
| REFM | 4 | Analog input | Reference ground potential; short to GND externally. |
| REFP | 5, 6 | Analog input/output | Reference buffer output, ADC reference input. Short pins 5 and 6 together. |
| $\overline{RST}$ | 29 | Digital input | Asynchronous reset input pin.<br>A low pulse on the $\overline{RST}$ pin resets the device. All register bits return to the default state. |
| SCLK | 25 | Digital input | Clock input pin for the serial interface.<br>All system-synchronous data transfer protocols are timed with respect to the SCLK signal. |
| SDI | 24 | Digital input | Serial data input pin.<br>This pin is used to feed data or commands into the device. |
| SDO-0 | 26 | Digital output | Serial communication pin: data output 0. |
| SDO-1/SEQSTS | 27 | Digital output | Multifunction output pin.<br>By default, this pin indicates the channel scanning status in the AUTO or PROGRAM sequence modes.<br>In dual SDO data transfer mode this pin acts as a serial communication pin: data output 1. |
| Thermal pad | | Supply | Exposed thermal pad; connect to GND. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| AVDD | -0.3 | 7 | V |
| DVDD | -0.3 | 7 | V |
| AINx(2), AIN-COM, MUXOUT-P, MUXOUT-M, ADC-INP, ADC-INM to GND | -0.3 | AVDD + 0.3 | V |
| REFP to REFM | -0.3 | AVDD + 0.3 | V |
| REFIO to REFM | -0.3 | AVDD + 0.3 | V |
| REFM to GND | -0.1 | 0.1 | V |
| Digital input pins to GND | -0.3 | DVDD + 0.3 | V |
| Digital output pins to GND | -0.3 | DVDD + 0.3 | V |
| Input current to any pin except supply pins | -10 | 10 | mA |
| Operating temperature, $T_J$ | -40 | 125 | °C |
| Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7 pins.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| AVDD | Internal reference | 4.5 | 5 | 5.5 | V |
| | External reference | 3 | 5 | 5.5 | V |
| DVDD | Operating | 1.65 | 3 | 5.5 | V |
| | Specified throughput | 2.35 | 3 | 5.5 | V |
| $T_A$ | Ambient temperature | -40 | 25 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | ADS816x RHB (VQFN) 32 | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 29.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 18.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 10.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 10.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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## 6.5 Electrical Characteristics

At AVDD = 5-V, DVDD = 1.65-V to 5.5-V, REFIO configured as output pin, and maximum throughput (unless otherwise noted). Minimum and maximum values at $T_A$ = -40°C to +125°C; typical values at $T_A$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUTS - SINGLE-ENDED CONFIGURATION** | | | | | | |
| FSR | Full-scale input range for selected input pair | | 0 | | $V_{REF}$ | V |
| $V_{IN}$ | Absolute input voltage (AINx(1) to REFM) | CHx_CHy_CFG(2) = 00b | -0.1 | | $V_{REF}$ + 0.1 | V |
| | Absolute input voltage (AINy(3) to REFM) | CHx_CHy_CFG = 01b | -0.1 | | 0.1 | V |
| | Absolute input voltage (AIN-COM) | | -0.1 | | 0.1 | V |
| $I_{LMUX\_OFF}$ | MUX input OFF leakage current | REFM < $V_{IN}$ < REFP | -750 | ±10 | 750 | nA |
| **ANALOG INPUTS - PSEUDO-DIFFERENTIAL CONFIGURATION** | | | | | | |
| FSR | Full-scale input range for selected input pair | | -$V_{REF}$/2 | | $V_{REF}$/2 | V |
| $V_{IN}$ | Absolute input voltage (AINx to REFM) | CHx_CHy_CFG = 00b | -0.1 | | $V_{REF}$ + 0.1 | V |
| | Absolute input voltage (AINy to REFM) | CHx_CHy_CFG = 10b | $V_{REF}$/2 - 0.1 | $V_{REF}$/2 | $V_{REF}$/2 + 0.1 | V |
| | Absolute input voltage (AIN-COM) | | $V_{REF}$/2 - 0.1 | $V_{REF}$/2 | $V_{REF}$/2 + 0.1 | V |
| **ANALOG INPUTS** | | | | | | |
| $C_{SH}$ | ADC Input capacitance | | | 60 | | pF |
| $C_{INMUX}$ | MUX Input capacitance | | | 13 | | pF |
| $I_{LMUX\_ON}$ | MUX input ON leakage current | REFM < $V_{IN}$ < REFP | -750 | ±10 | 750 | nA |
| **DC PERFORMANCE** | | | | | | |
| | Resolution | | | 16 | | Bits |
| NMC | No Missing Codes | | 16 | | | |
| INL | Integral nonlinearity | | -0.8 | ±0.35 | 0.8 | LSB |
| DNL | Differential nonlinearity | | -0.5 | ±0.2 | 0.5 | LSB |
| $V_{OS}$ | Input offset error | | -10 | ±0.5 | 10 | LSB |
| $dV_{OS}/dT$ | Input offset thermal drift | | | 0.25 | | µV/°C |
| $G_E$ | Gain error | Referred to REFIO | -0.06 | ±0.002 | 0.06 | %FSR |
| $dG_E/dT$ | Gain error thermal drift | Referred to REFIO | | ±1 | | ppm/°C |
| TNS | Transition noise | $V_{IN}$ = $V_{REF}$/2 | | 0.6 | | LSB |
| **AC PERFORMANCE** | | | | | | |
| SINAD | Signal-to-noise + distortion | $f_{IN}$ = 2-kHz | 92.1 | 93.5 | | dB |
| SNR | Signal-to-noise-ratio | $f_{IN}$ = 2-kHz | 92.2 | 93.6 | | dB |
| THD | Total harmonic distortion | $f_{IN}$ = 2-kHz | | -110 | | dB |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 2-kHz | | 112 | | dB |
| | Isolation Crosstalk | $f_{IN}$ = 100-kHz | | -115 | | dB |
| **REFERENCE BUFFER** | | | | | | |
| $V_{RO}$ | Reference buffer offset voltage | $V_{RO}$ = $V_{REFP}$ - $V_{REFIO}$, $T_A$ = 25°C | -250 | | 250 | µV |
| $C_{REFP}$ | Decoupling capacitor on REFP | | | 22 | | µF |
| $R_{ESR}$ | External series resistance | | 0 | | 1.3 | Ω |

(1) AINx refers to analog inputs AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.
(2) CHx_CHy_CFG bits set the analog input configuration as single-ended or pseudo-differential pair. Refer to AIN_CFG register for more details.
(3) AINy refers to analog inputs AIN1, AIN3, AIN5, and AIN7 when CHx_CHy_CFG = 01b or 10b. Refer to Multiplexer Configurations for more details.

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## Electrical Characteristics (continued)

At AVDD = 5-V, DVDD = 1.65-V to 5.5-V, REFIO configured as output pin, and maximum throughput (unless otherwise noted). Minimum and maximum values at $T_A$ = -40°C to +125°C; typical values at $T_A$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **REFby2 BUFFER** | | | | | | |
| $V_{REFby2}$ | REFby2 output voltage | | | $V_{REFP}$/2 | | V |
| $I_{REFby2}$ | DC Sourcing current from REFby2 | | | | 2 | mA |
| $C_{REFby2}$ | Decoupling capacitor on REFby2 | | 1 | | | µF |
| **INTERNAL REFERENCE OUTPUT** | | | | | | |
| $V_{REFIO}$ | REFIO output voltage(4) | $T_A$ = 25°C, REFIO configured as output pin | | 4.096 | | V |
| $dV_{REFIO}/dT$ | Internal reference temperature drift | | | 4 | 18 | ppm/°C |
| $C_{REFIO}$ | Decoupling capacitor on REFIO | REFIO configured as output | 1 | | | µF |
| **EXTERNAL REFERENCE INPUT** | | | | | | |
| $V_{REFIO}$ | REFIO input voltage | REFIO configured as input pin | 2.5 | | AVDD - 0.3 | V |
| $I_{REFIO}$ | REFIO input current | REFIO configured as input pin | | 0.1 | 1 | µA |
| $C_{REF}$ | Internal capacitance on REFIO pin | REFIO configured as input pin | | 10 | | pF |
| **SAMPLING DYNAMICS** | | | | | | |
| | Aperture delay | | | 4 | | ns |
| $t_{j\text{-}RMS}$ | Aperture Jitter | | | 2 | | ps RMS |
| $f_{-3\text{-}dB(small)}$ | Small-signal bandwidth | Measured at ADC inputs | | 23 | | MHz |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| $I_{AVDD}$ | Analog supply current | ADS8168, AVDD = 5-V | | 5.3 | 6.2 | mA |
| | | ADS8166, AVDD = 5-V | | 3 | 3.7 | |
| | | Static, no conversion | | 2.3 | | |
| | | Static, PD_REFBUF = 1 | | 1.6 | | |
| | | Static, PD_REF = 1 | | 800 | | µA |
| | | Static, PD_REFBUF, PD_REF and PD_REFby2 = 1 | | 180 | | µA |
| $I_{DVDD}$ | Digital supply current | DVDD = 3 V, $C_{LOAD}$ = 10-pF, no conversion | | 0.45 | | uA |

(4) Does not include the variation in voltage resulting from solder effects.

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## 6.6 Timing Requirements

At AVDD = 5-V, DVDD = 1.65-V to 5.5-V, and maximum throughput (unless otherwise noted). Minimum and maximum values at $T_A$ = -40°C to +125°C; typical values at $T_A$ = 25°C.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CONVERSION CYCLE** | | | | | | |
| $f_{CYCLE}$ | Sampling frequency | ADS8168 | | | 1000 | kHz |
| | | ADS8166 | | | 250 | kHz |
| $t_{CYCLE}$ | ADC cycle-time period | ADS8168 | 1 | | | µs |
| | | ADS8166 | 4 | | | µs |
| $t_{wh\_CSZ}$ | Pulse duration: $\overline{CS}$ high | | 30 | | | ns |
| $t_{wl\_CSZ}$ | Pulse duration: $\overline{CS}$ low | | 30 | | | ns |
| $t_{ACQ}$ | Acquisition time | | 300 | | | ns |
| $t_{qt\_ACQ}$ | Quite acquisition time | | 30 | | | ns |
| $t_{d\_CNVCAP}$ | Quiet aperture time | | 20 | | | ns |
| **ASYNCHRONOUS RESET AND LOW POWER MODES** | | | | | | |
| $t_{wl\_RST}$ | Pulse duration: $\overline{RST}$ low | | 100 | | | ns |
| **SPI-COMPATIBLE SERIAL INTERFACE** | | | | | | |
| $f_{CLK}$ | Serial clock frequency | 2.35-V ≤ DVDD ≤ 5.5-V, $V_{IH}$ > 0.7 DVDD, $V_{IL}$ < 0.3 DVDD | | | 70 | MHz |
| | | 1.65-V ≤ DVDD < 2.35-V, $V_{IH}$ ≥ 0.8 DVDD, $V_{IL}$ ≤ 0.2 DVDD | | | 20 | MHz |
| | | 1.65-V ≤ DVDD < 2.35-V, $V_{IH}$ ≥ 0.9 DVDD, $V_{IL}$ ≤ 0.1 DVDD | | | 68 | MHz |
| $t_{CLK}$ | Serial clock time period | | $1/f_{CLK}$ | | | ns |
| $t_{ph\_CK}$ | SCLK high time | | 0.45 | | 0.55 | $t_{CLK}$ |
| $t_{pl\_CK}$ | SCLK low time | | 0.45 | | 0.55 | $t_{CLK}$ |
| $t_{ph\_CSCK}$ | Setup time: $\overline{CS}$ falling to the first SCLK capture edge | | 15 | | | ns |
| $t_{su\_CKDI}$ | Setup time: SDI data valid to the SCLK capture edge | | 3 | | | ns |
| $t_{ht\_CKDI}$ | Hold time: SCLK capture edge to (previous) data valid on SDI | | 4 | | | ns |
| $t_{ht\_CKCS}$ | Delay time: last SCLK falling to $\overline{CS}$ rising | | 7.5 | | | ns |
| **SOURCE-SYNCHRONOUS SERIAL INTERFACE** | | | | | | |
| $f_{CLK}$ | Serial clock frequency | 2.35-V ≤ DVDD ≤ 5.5-V, SDR (DATA_RATE = 0b) | | | 70 | MHz |
| | | 2.35-V ≤ DVDD ≤ 5.5-V, DDR (DATA_RATE = 1b) | | | 35 | MHz |
| $t_{CLK}$ | Serial clock time period | | $1/f_{CLK}$ | | | ns |

ADVANCE INFORMATION

## 6.7 Switching Characteristics

At AVDD = 5-V, DVDD = 1.65-V to 5.5-V, and maximum throughput (unless otherwise noted). Minimum and maximum values at $T_A$ = -40°C to +125°C; typical values at $T_A$= 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CONVERSION CYCLE** | | | | | | |
| $t_{CONV}$ | Conversion time | ADS8168 | | | 640 | ns |
| | | ADS8166 | | | 2500 | |
| **ASYNCHRONOUS RESET, AND LOW POWER MODES** | | | | | | |
| $t_{d\_RST}$ | Delay time: $\overline{RST}$ rising to READY rising | | | | 3 | ms |
| $t_{PU\_ADC}$ | Power-up time for converter module | Change PD_ADC = 1b to 0b | 1 | | | ms |
| $t_{PU\_REFIO}$ | Power-up time for internal reference | Change PD_REF = 1b to 0b | 5 | | | ms |
| $t_{PU\_REFBUF}$ | Power-up time for internal reference buffer | Change PD_REFBUF = 1b to 0b | 10 | | | ms |
| $t_{PU\_Device}$ | Power-up time for device | | 10 | | | ms |
| **SPI-COMPATIBLE SERIAL INTERFACE** | | | | | | |
| $t_{den\_CSDO}$ | Delay time: $\overline{CS}$ falling to data enable | | | | 15 | ns |
| $t_{dz\_CSDO}$ | Delay time: $\overline{CS}$ rising to SDO going to Hi-Z | | | | 15 | ns |
| $t_{d\_CKDO}$ | Delay time: SCLK launch edge to (next) data valid on SDO | | | | 19 | ns |
| $t_{d\_CSRDY\_t}$ | Delay time: $\overline{CS}$ falling to READY falling | | | | 15 | ns |
| **SOURCE-SYNCHRONOUS SERIAL INTERFACE (External Clock)** | | | | | | |
| $t_{d\_CKSTR\_r}$ | Delay time: SCLK launch edge to READY rising | | | | 23 | ns |
| $t_{d\_CKSTR\_f}$ | Delay time: SCLK launch edge to READY falling | | | | 23 | ns |
| $t_{off\_STRDO\_f}$ | Time offset: READY falling to (next) data valid on SDO | | -2 | | 2 | ns |
| $t_{off\_STRDO\_r}$ | Time offset: READY rising to (next) data valid on SDO | | -2 | | 2 | ns |
| $t_{ph\_STR}$ | Strobe output high time | 2.35-V ≤ DVDD ≤ 5.5-V | 0.45 | | 0.55 | $t_{STR}$ |
| $t_{pl\_STR}$ | Strobe output low time | 2.35-V ≤ DVDD ≤ 5.5-V | 0.45 | | 0.55 | $t_{STR}$ |

ADVANCE INFORMATION

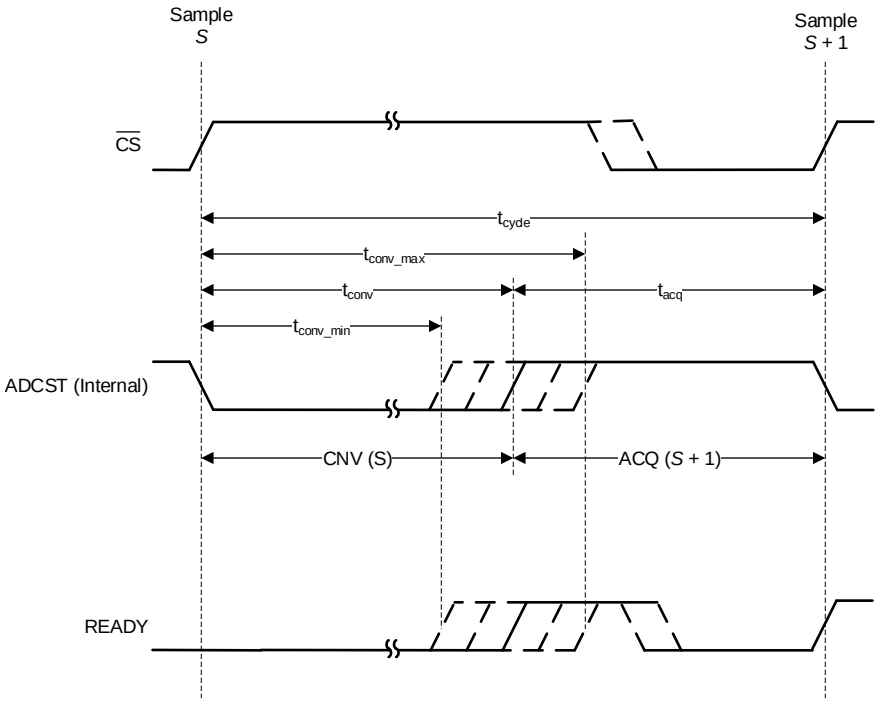



**Figure 1. Conversion Cycle Timing**

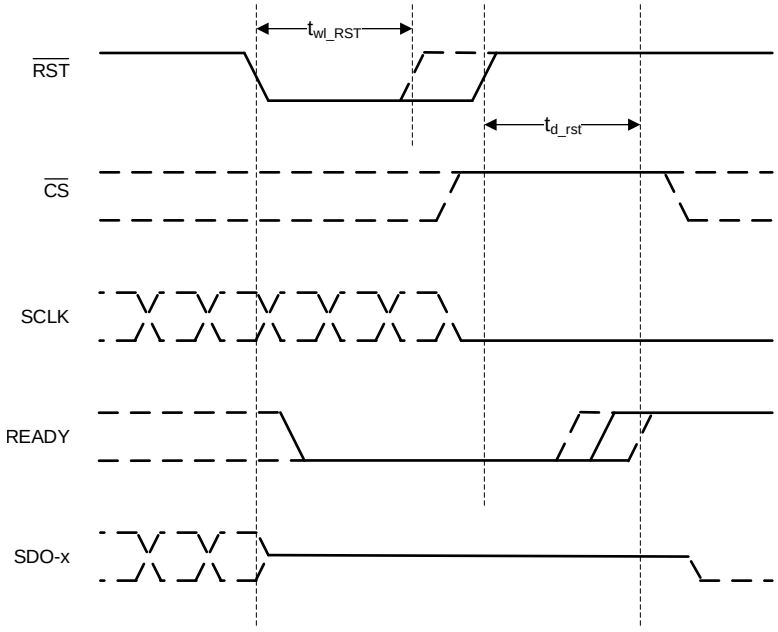
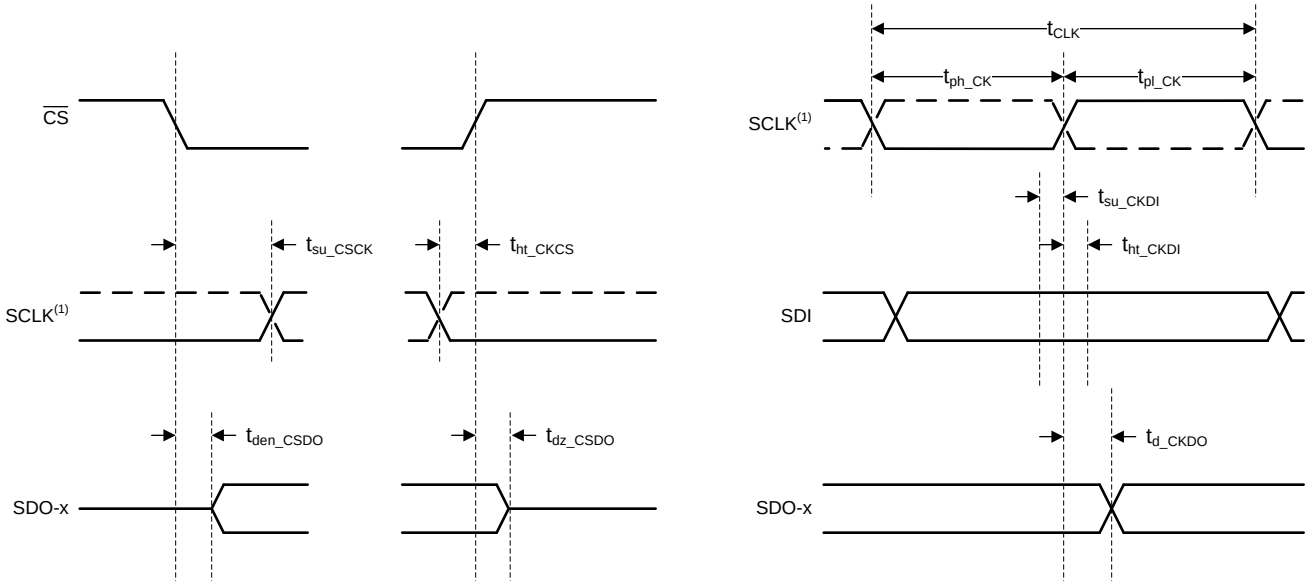



**Figure 2. Asynchronous Reset Timing**

ADVANCE INFORMATION




(1) The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

**Figure 3. SPI-Compatible Serial Interface Timing**

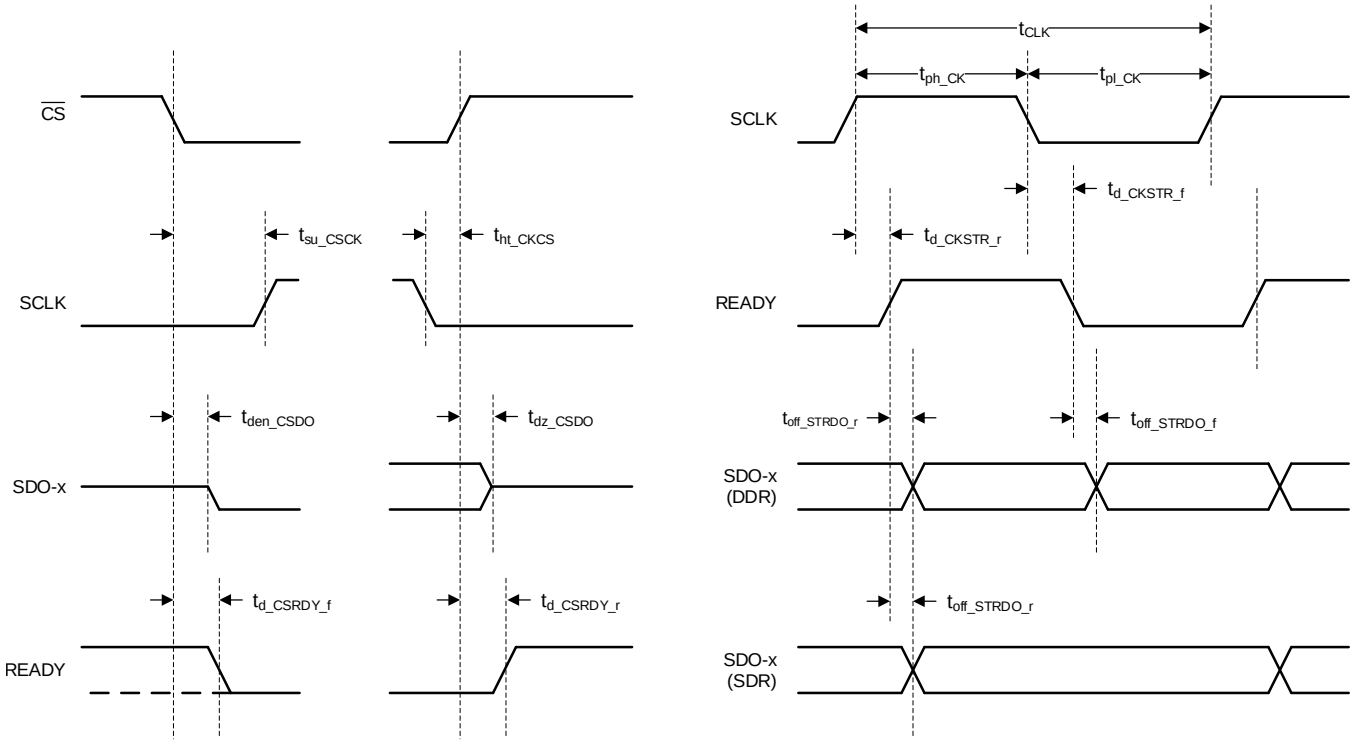
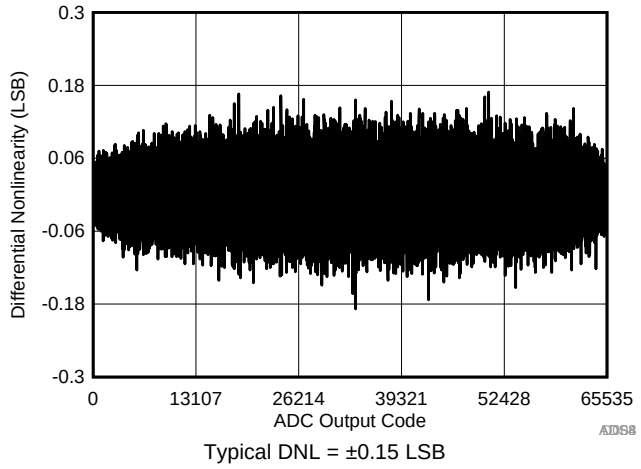



**Figure 4. Source-Synchronous Serial Interface Timing**

ADVANCE INFORMATION

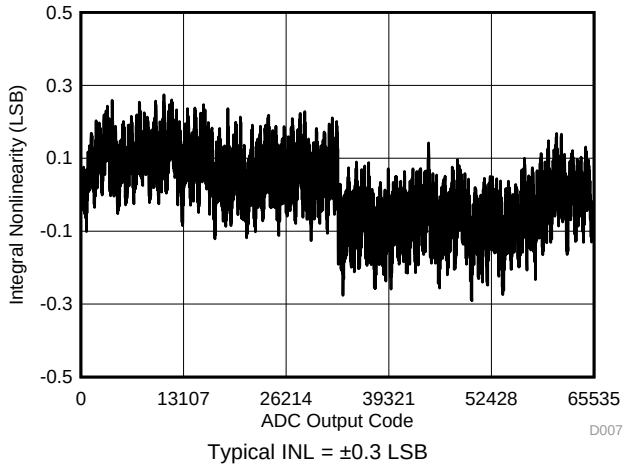
## 6.8 Typical Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)




Typical DNL = ±0.15 LSB

**Figure 5. Typical DNL**




Typical INL = ±0.3 LSB

**Figure 6. Typical INL**

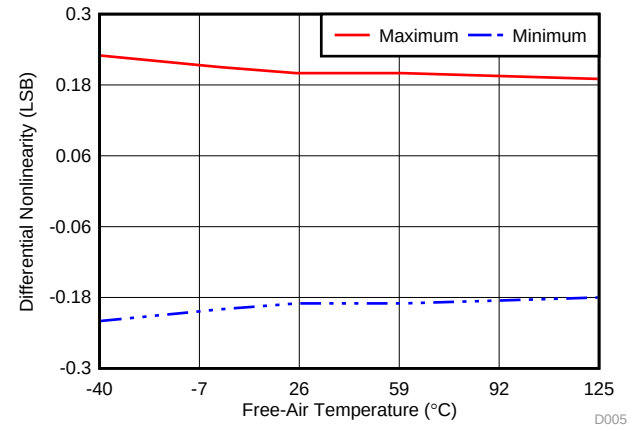



**Figure 7. DNL vs Temperature**

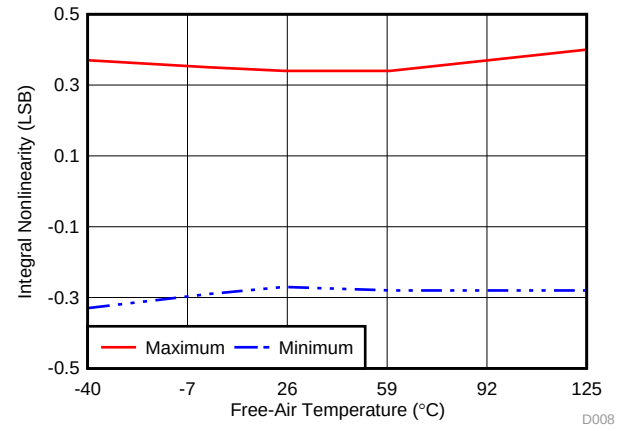



**Figure 8. INL vs Temperature**

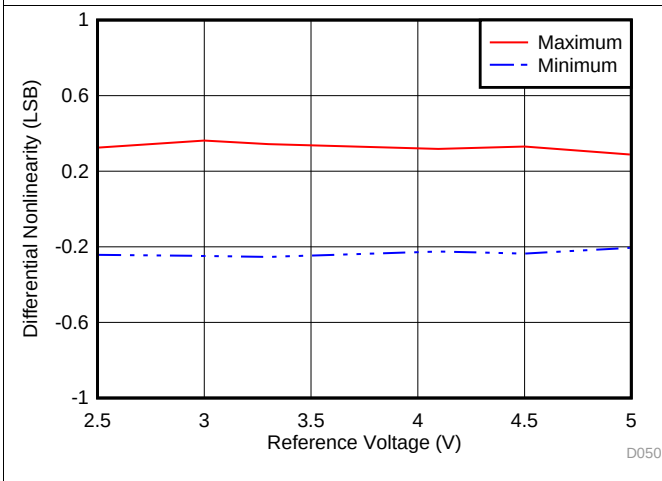



**Figure 9. DNL vs Reference Voltage**

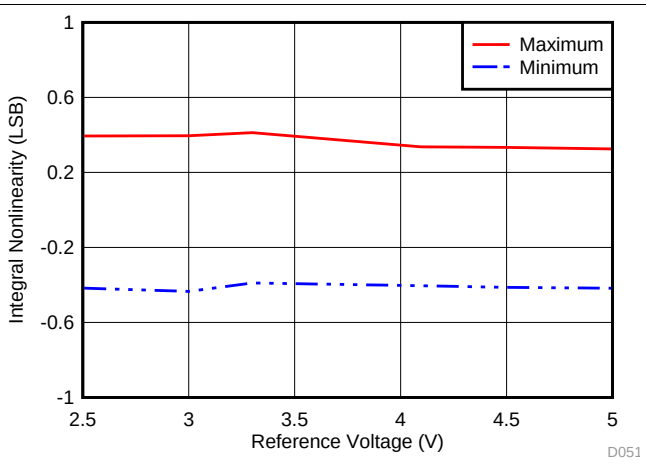
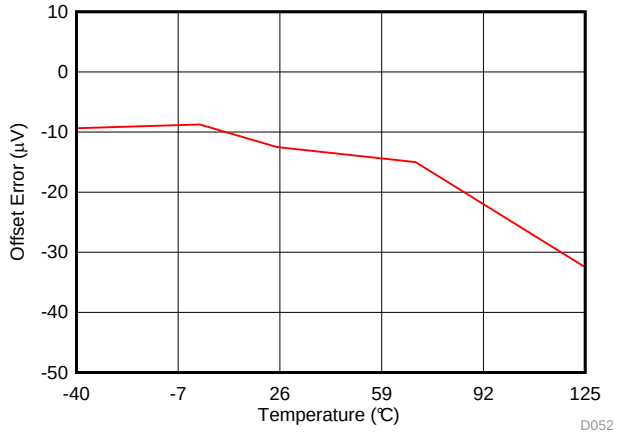



**Figure 10. INL vs Reference Voltage**

ADVANCE INFORMATION

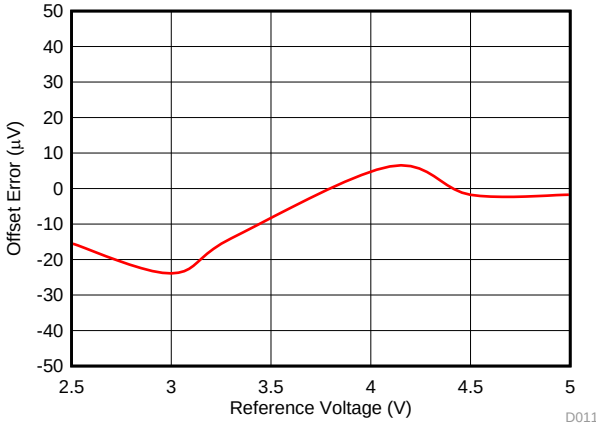
## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)



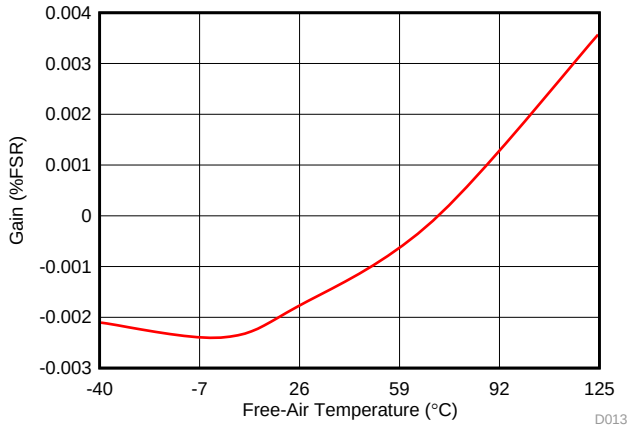

REF_SEL[2:0] = 000b

**Figure 11. Offset vs Temperature**



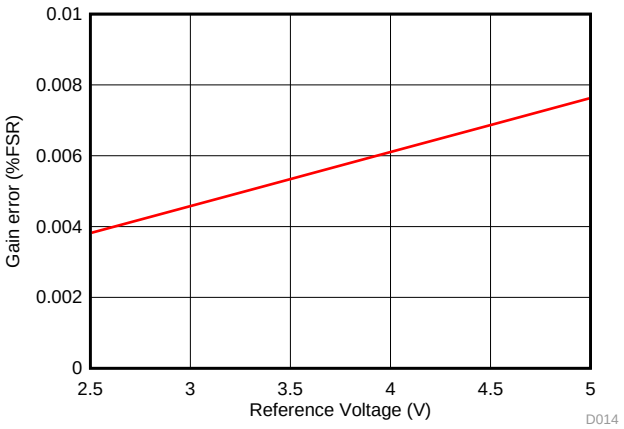

With appropriate REF_SEL[2:0], see OFST_CAL

**Figure 12. Offset vs Reference Voltage**



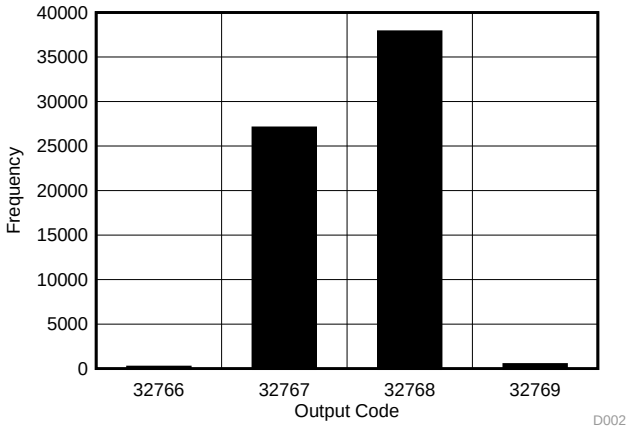

EN_MARG = 0b

**Figure 13. Gain Error (ADC + REFBUF) vs Temperature**



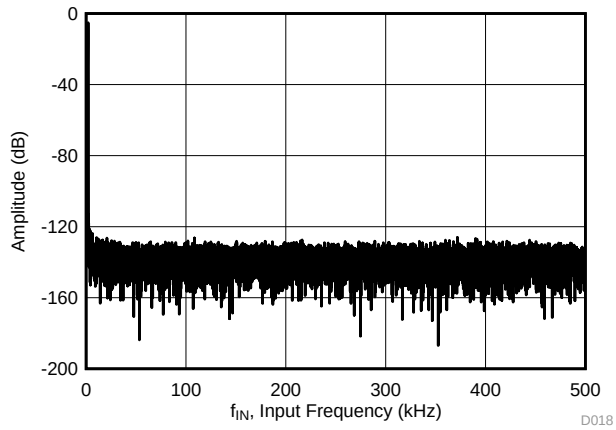

EN_MARG = 0b

**Figure 14. Gain Error (ADC + REFBUF) vs Reference Voltage**




Standard deviation = 0.51 LSB

**Figure 15. DC Input Histogram**



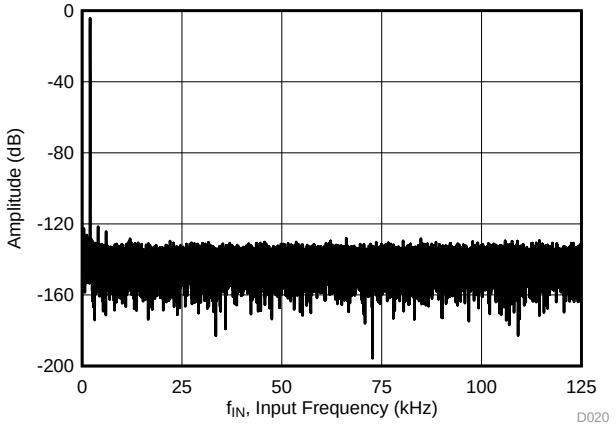

$f_{IN}$ = 2 kHz, SNR = 93.8 dB, THD = –112.7 dB

**Figure 16. Typical FFT: ADS8168**

ADVANCE INFORMATION

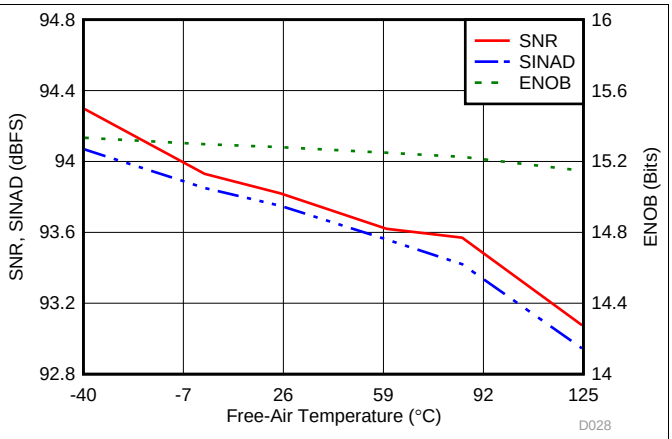
## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)



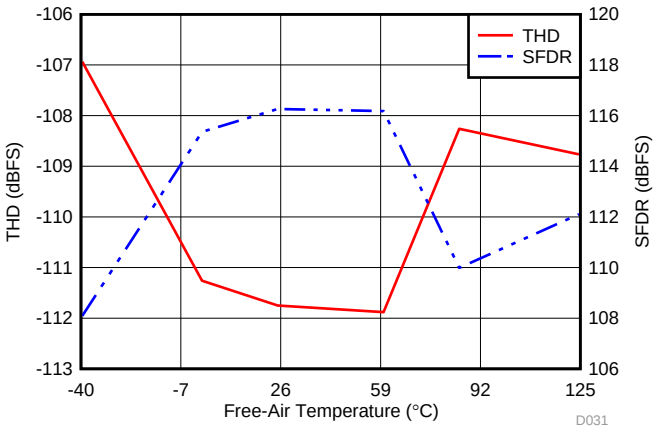

$f_{IN}$ = 2 kHz, SNR = 93.8 dB, THD = –111.4 dB

**Figure 17. Typical FFT: ADS8166**



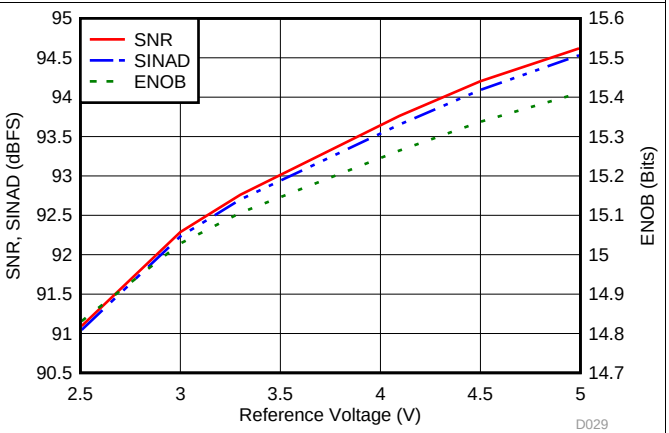

$f_{IN}$ = 2 kHz

**Figure 18. Noise Performance vs Temperature**



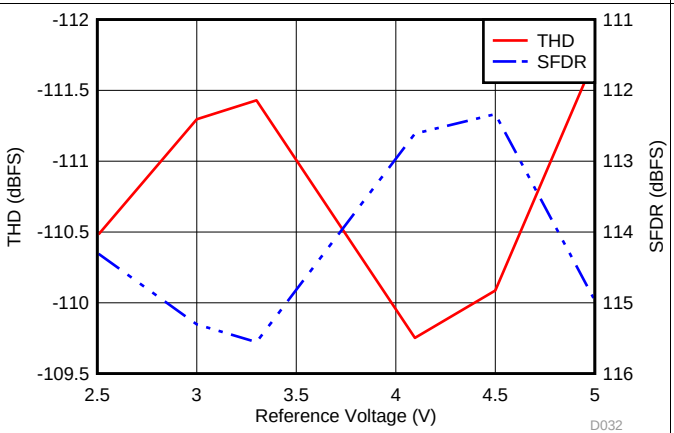

$f_{IN}$ = 2 kHz

**Figure 19. Distortion Performance vs Temperature**




$f_{IN}$ = 2 kHz

**Figure 20. Noise Performance vs Reference Voltage**




$f_{IN}$ = 2 kHz

**Figure 21. Distortion Performance vs Reference Voltage**

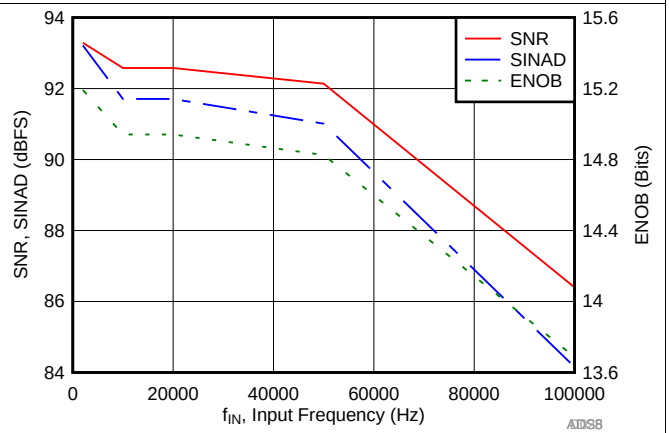



**Figure 22. Noise Performance vs Input Frequency**

ADVANCE INFORMATION

## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)

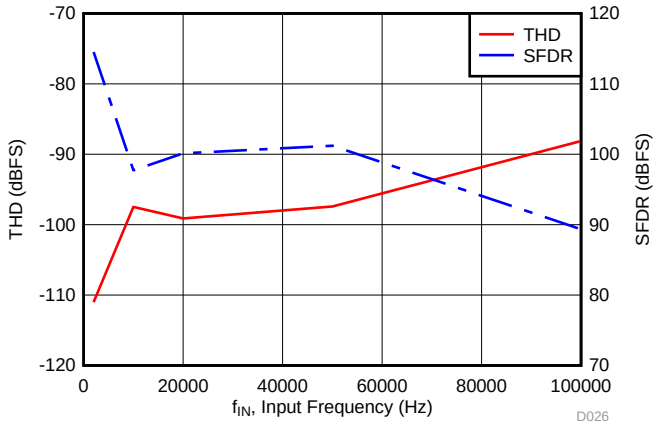



**Figure 23. Distortion Performance vs Input Frequency**

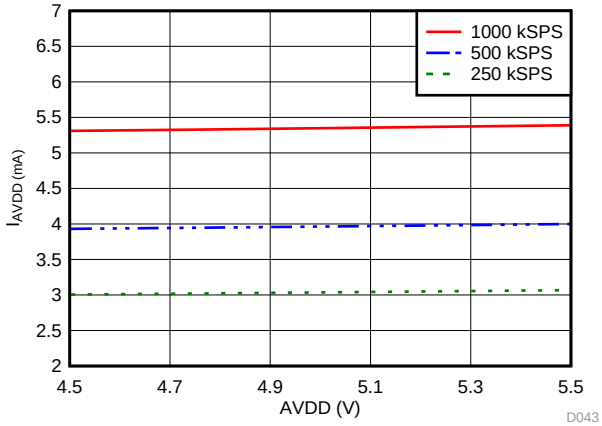
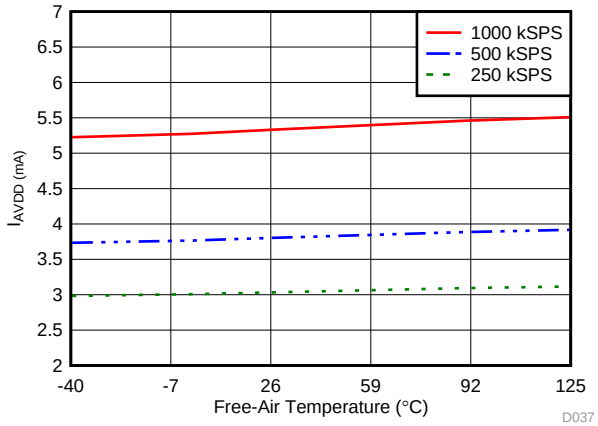



**Figure 24. Analog Supply Current vs Supply Voltage**




AVDD = 5 V

**Figure 25. Analog Supply Current vs Temperature**

ADVANCE INFORMATION

# 7 Detailed Description

## 7.1 Overview

The ADS816x is a family of 16-bit successive approximation register (SAR), analog-to-digital converters (ADCs) based on charge redistribution architecture with an analog multiplexer. This device integrates a reference, reference buffer, REFby2, LDO, and features high performance at full throughput and low power consumption.

This device family supports unipolar, single-ended and pseudo-differential, analog input signals. The analog multiplexer is optimized for low distortion and extended settling time. The internal reference generates low-drift 4.096-V reference output. The integrated reference buffer supports the burst mode of data acquisition for external reference voltages in the range 2.5 V to 5 V. For DC level shifting of the analog input signals, the device has a REFby2 output. The REFby2 output is derived from the output of the integrated reference buffer (REFP pin).

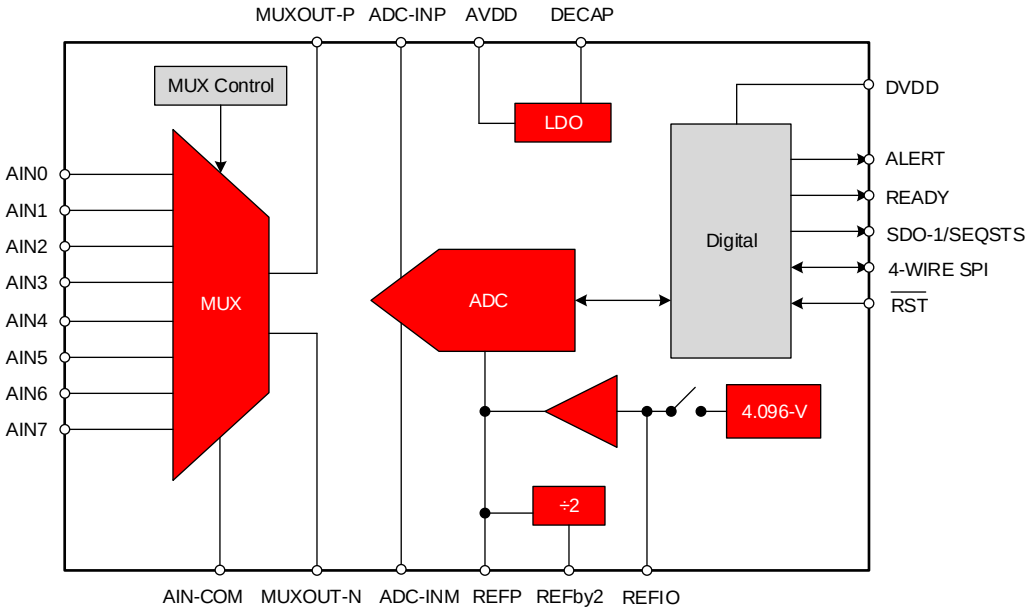
When a conversion is initiated, the differential input between the ADC-INP and ADC-INM pins is sampled on the internal capacitor array. The device uses an internal clock to perform conversions. During the conversion process, both analog inputs of the ADC are disconnected from the internal circuit. At the end of conversion process, the device reconnects the sampling capacitors to the ADC-INP and ADC-INM pins and enters an acquisition phase.

The integrated LDO allows the device to operate on a single supply, AVDD. The device consumes only 26.5 mW or 15 mW of power when operating at 1 MSPS (ADS8168) or 250 kSPS (ADS8166), respectively, with the internal reference, reference buffer, REFby2 buffer, and LDO enabled.

The enhanced-SPI digital interface is backward-compatible with traditional SPI protocols. Configurable features boost analog performance and simplify board layout, timing, firmware, and support full throughput at lower clock speeds. This features simplifies using a variety of microcontrollers as well as digital signal processors (DSPs) and field-programmable gate arrays (FPGAs).

The ADS816x enables optical line cards, optical modules, test and measurement, medical, and industrial applications to achieve fast, low-noise, low-distortion, low-power data acquisition in a small form factor.

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

The ADS816x is comprised of five modules: the converter (SAR ADC), multiplexer (MUX), the reference module, the enhanced-SPI interface, and the low-dropout regulator (LDO); see the *Functional Block Diagram*.

The LDO module is powered by the AVDD supply, and generates the bias voltage for internal circuit blocks of the device. The reference buffer drives the capacitive switching load present at the reference pins during the conversion process. The multiplexer selects among 8 analog input channels as input for the converter module. The converter module samples and converts the analog input into an equivalent digital output code. The enhanced-SPI interface module facilitates communication and data transfer between the device and the host controller.

### 7.3.1 Analog Multiplexer

Figure 26 shows the small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by resistance ($R_{S1}$ and $R_{S2}$, typically 50-Ω) in series with an ideal switch (SW). The sampling capacitors, $C_{S1}$ and $C_{S2}$, are typically 60-pF.

The multiplexer ON-resistance ($R_{MUX}$), typically 40-Ω is seen in series between the ON channel and MUXOUT-P or MUXOUT-M. Analog input of the multiplexer has typically 13-pF ON-channel capacitance ($C_{MUX}$).

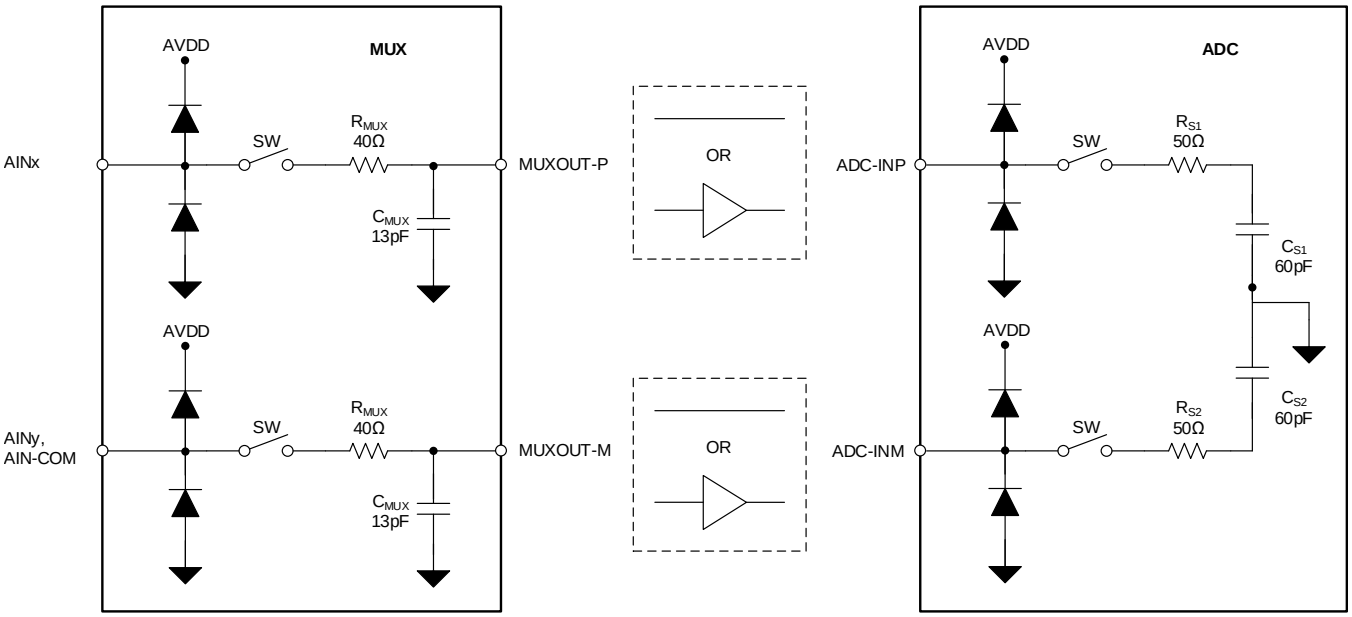


**Figure 26. Input Sampling Stage Equivalent Circuit**

During the input signal acquisition phase, the ADC-INP and ADC-INM inputs are individually sampled on $C_{S1}$ and $C_{S2}$, respectively. During the conversion process, the device converts for the voltage difference between the two sampled values: $V_{ADC-INP} - V_{ADC-INM}$.

Each analog input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

#### *7.3.1.1 Multiplexer Configurations*

The ADS816x supports single-ended and pseudo-differential analog input signals. The flexible analog input channel configuration supports various sensor types. The analog inputs can be configured as illustrated in Figure 27.

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## Feature Description (continued)

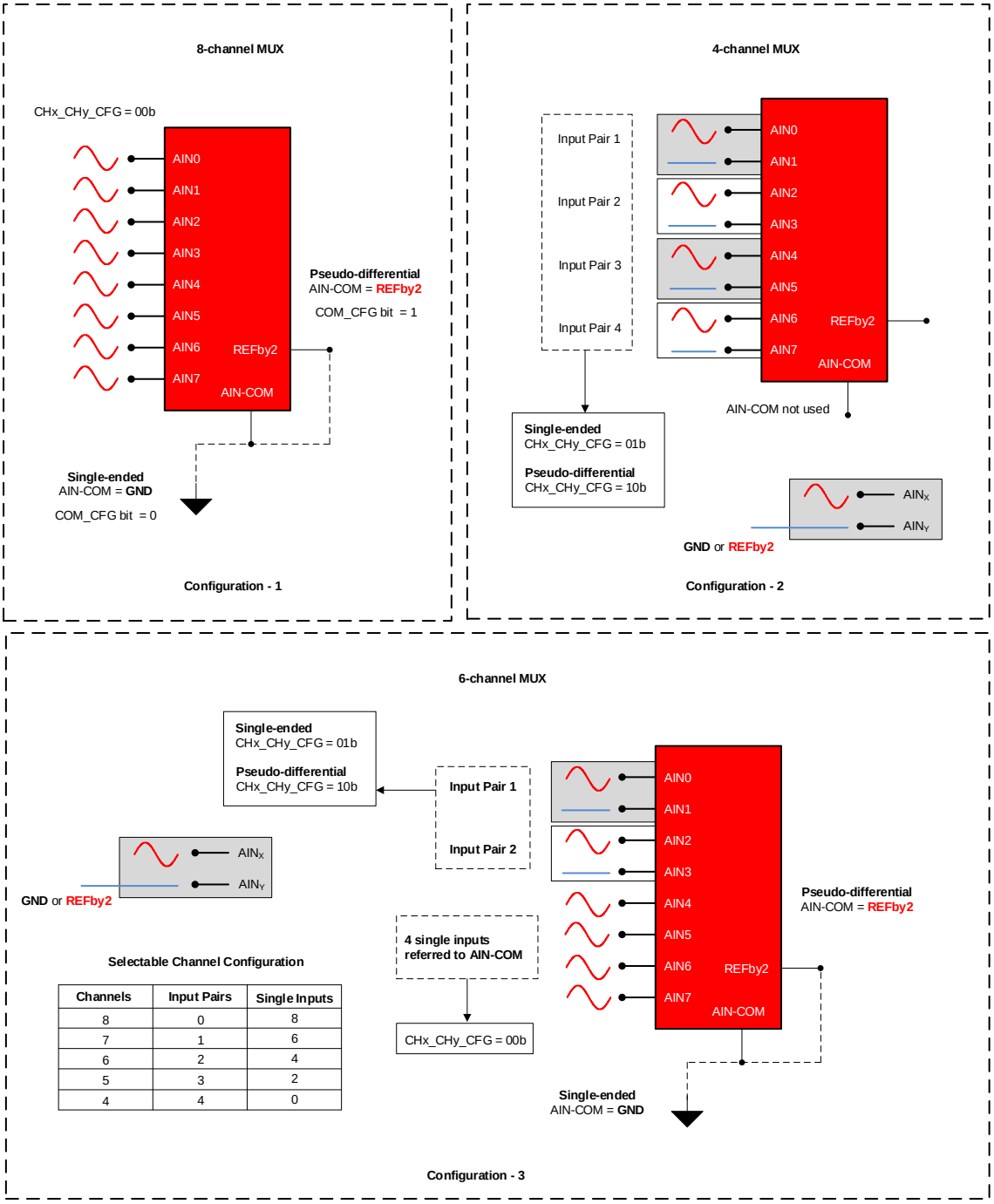


**Figure 27. Analog Input Configurations**

The analog inputs can be configured as:

- **Configuration 1**: Eight-channel MUX, AIN_CFG = 00h. The AIN-COM input range is decided by the COM_CFG register.
  - Single-ended inputs with AIN-COM input as GND (COM_CFG = 00h).
  - Pseudo-differential inputs with AIN-COM input as $V_{REF}$ / 2 (COM_CFG = 01h).
- **Configuration 2**: Four-channel MUX.

## Feature Description (continued)

  - The AIN_CFG register selects the analog input range of individual pairs(1)(2).
- **Configuration 3**: Single-ended and pseudo-differential inputs.
  - Among the eight analog inputs of the MUX, some can be configured as pairs while the others are configured as individual channels. See Table 1 for options with channel configuration.
  - For channels configured as pairs, the AIN_CFG register selects the single-ended or pseudo-differential configuration for individual pairs.
  - For individual channels, the COM_CFG register decides the single-ended or pseudo-differential configuration.

**Table 1. Channel Configuration Options**

| SR. NO. | TOTAL CHANNELS | INPUT PAIRS | INDIVIDUAL CHANNELS |
|---|---|---|---|
| 1 | 8 | 0 | 8 |
| 2 | 7 | 1 | 6 |
| 3 | 6 | 2 | 4 |
| 4 | 5 | 3 | 2 |
| 5 | 4 | 4 | 0 |

(1) Channel pairs can be formed as [AIN0 - AIN1], [AIN2 - AIN3], [AIN4 - AIN5], and [AIN6 - AIN7].
(2) When channels are configured as pairs, AIN0, AIN2, AIN4, and AIN6 are positive inputs.

**NOTE**

COM_CFG register sets the input voltage range of the AIN-COM pin. AIN-COM pin must be connected to GND (COM_CFG = 0b) or REFby2 (COM_CFG = 1b) externally. When using the MUX in a four-channel configuration, the COM_CFG register has no effect; connect the AIN-COM pin to GND to avoid noise pick-up.

### *7.3.1.2 Multiplexer With Minimum Crosstalk*

For precision measurement in a multi-channel system, coupling from one channel to another, i.e. crosstalk, can distort the measurement. In conventional multiplexers, as shown in Figure 28, the OFF channel parasitic capacitance between the drain and source of the switch ($C_{DSY}$) couples the OFF channel signal to the ON channel.

The ADS816x device family uses a seven-switch structure, as shown in Figure 28. In this switch architecture, the off channel parasitic capacitance is connected to ground which significantly reduces coupling. Care must be taken to avoid signal coupling on the printed circuit board (PCB), as described in the *Layout* section.

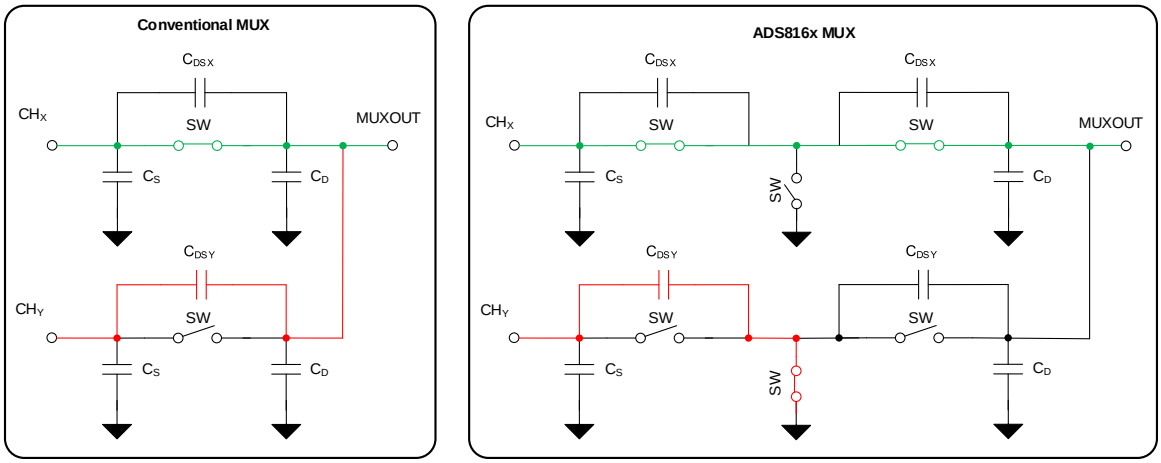


**Figure 28. Isolation Crosstalk in Conventional MUX versus the ADS816x**

#### 7.3.1.3 Early Switching for Direct Sensor Interface

Figure 29 shows the small signal equivalent model of the ADS816x analog inputs. The multiplexer input has a switch resistance ($R_{MUX}$) and parasitic capacitance ($C_{MUX}$). The parasitic capacitance causes a charge kick-back on the MUX analog input just as the ADC sampling capacitor causes a charge kick-back on ADC inputs.

In conventional multichannel SAR ADCs, the acquisition time of the ADC is also the settling time available at the analog inputs of the multiplexer because they are internally connected. Hence high-bandwidth op-amps are required at the analog inputs of the multiplexer to settle the charge kick-back. Multiple high bandwidth op-amps would significantly increase power dissipation, cost, and size of the solution.

The analog inputs of the ADS816x device family provide a long settling time ($t_{CYCLE}$ - 100-ns) resulting in long acquisition time at MUX inputs when using driver amplifier between MUX outputs and ADC inputs. The low parasitic capacitance together with enhanced settling time eliminate the need to use an op-amp at the multiplexer input in most applications.

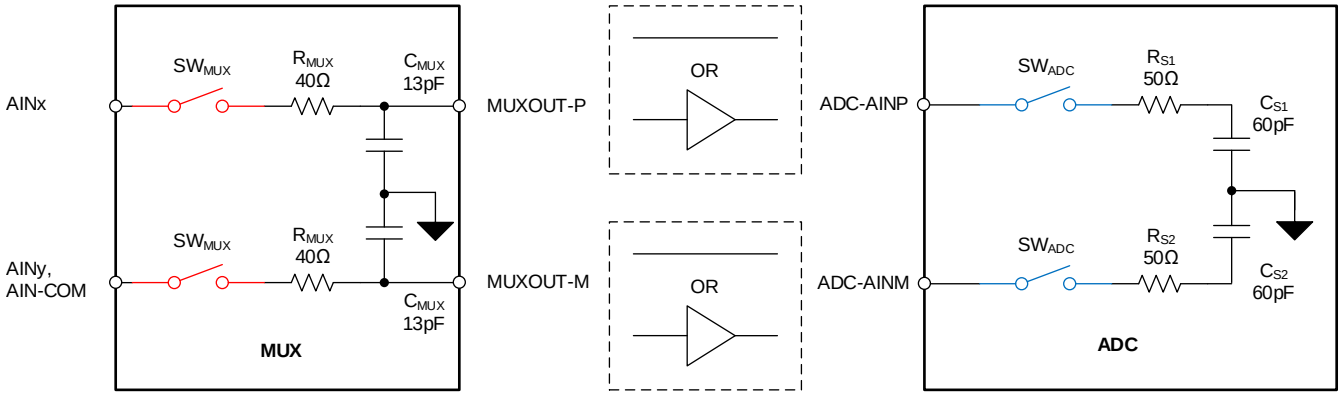


**Figure 29. Synchronous and Timed Switching of the MUX and ADC Input Switches**

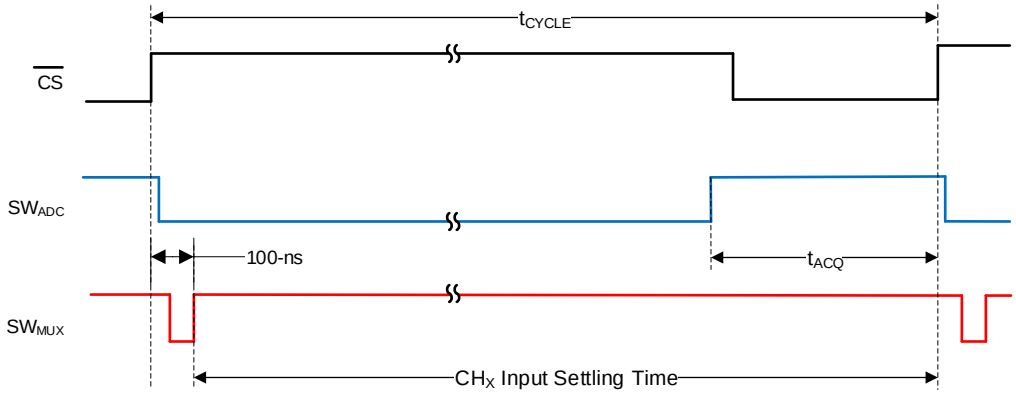


**Figure 30. Early Switching of the MUX Enables a Long Acquisition Phase**

To achieve better accuracy and noise performance, it is desirable to average several output codes of a particular MUX input channel without switching the MUX. As shown in Figure 39 and Figure 41, the output of the multiplexer does not create a charge kick-back as long as SDI = 0 i.e. the NOP command. Multiplexer does not switch during subsequent conversions except for the first time when a channel is selected. Hence high impedance sources such as voltage from resistor dividers can be connected to analog inputs of the multiplexer without an op-amp.

### 7.3.2 Reference

The ADS816x has a precision, low-drift reference internal to the device. See the *Internal Reference* section for details about using the internal reference.

For best ENOB performance, the input signal range must be equal to the full-scale input range of the ADC. To maximize ENOB, an external reference voltage source can be used as described in the *External Reference* section.

### 7.3.2.1 Internal Reference

The device features an internal reference source with a nominal output value of 4.096 V. On power-up, the internal reference is enabled by default. A minimum 1-µF decoupling capacitor is recommended to be placed between the REFIO and REFM pins as shown in Figure 31. The capacitor must be placed as close to the REFIO pin as possible. The output impedance of the internal band-gap circuit creates a low-pass filter with this capacitor to band-limit the noise of the reference. The internal reference is also temperature compensated to provide excellent temperature drift over an extended industrial temperature range of –40°C to +125°C. By default the internal reference is ON and the voltage at REFIO is 4.096 V. The REFIO pin has ESD protection diodes to the AVDD and GND pins.

The initial accuracy specification for the internal reference can be degraded if the die is exposed to any mechanical or thermal stress. Heating the device when being soldered to a PCB and any subsequent solder reflow is a primary cause for shifts in the internal reference voltage output. The main cause of thermal hysteresis is a change in die stress and is therefore a function of the package, die-attach material, and molding compound, as well as the layout of the device itself.

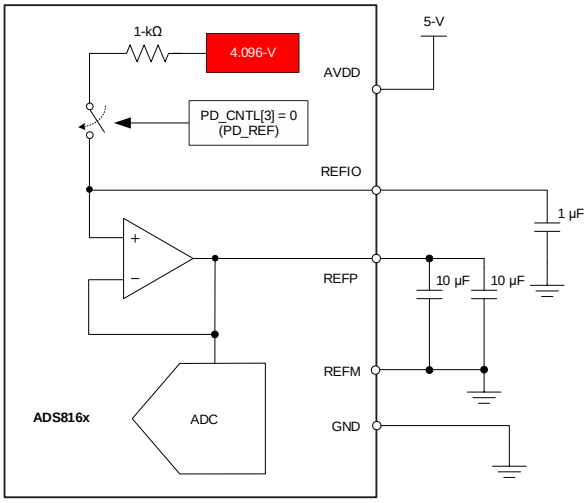


**Figure 31. Device Connections for Using Internal 4.096-V Reference**

### 7.3.2.2 External Reference

Figure 32 shows the connections for using the device with external reference. A reference without low impedance output buffer can be used because the input leakage current of the internal reference buffer is less than 1 µA.

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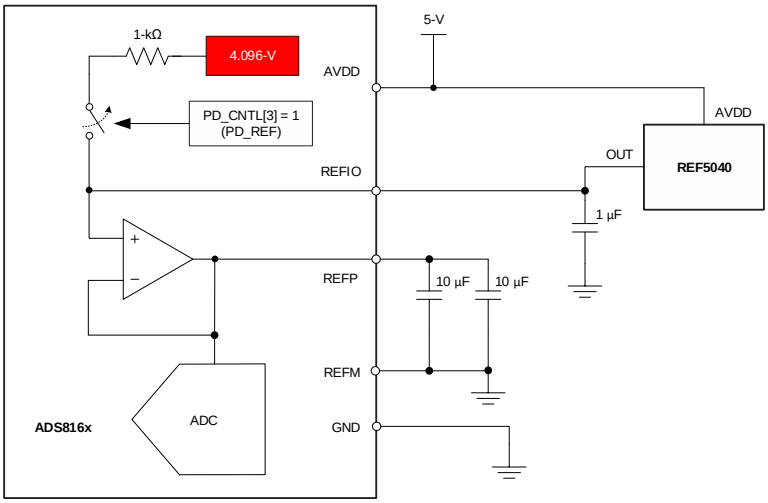


**Figure 32. Device Connections for Using External Reference**

### 7.3.3 Reference Buffer

On the $\overline{CS}$ rising edge, the ADC starts converting the sampled analog input channel, and the internal capacitors are switched to the REFP pins as per the successive approximation algorithm. Most of the switching charge required during the conversion process is provided by external decoupling capacitor $C_{REFP}$. If the charge lost from the $C_{REFP}$ is not replenished before the next $\overline{CS}$ rising edge, the voltage on REFP pins is less than $V_{REFP}$. The subsequent conversion occurs with this different reference voltage, and causes a proportional error in the output code. The internal reference buffer of the device maintains the voltage on REFP pins within 0.5-LSB of $V_{REFP}$. All the performance characteristics of the device are specified with the internal reference buffer and specified value of $C_{REFP}$.

In burst-mode of operation, the ADC samples the selected analog input channel for a long duration of time and then performs a burst of conversions. During the sampling time, the sampling capacitor ($C_S$) is connected to the differential input pins and no charge is drawn from the REFP pins. However, during the very first conversion cycle, there is a step change in the current drawn from the REFP pins. This sudden change in load triggers a transient settling response in the reference buffer. For a fixed input voltage, any transient settling error at the end of the conversion cycle results in a change in output codes over the subsequent conversions. The internal reference buffer of the ADS8168, when used with the recommended value of $C_{REFP}$, keeps the transient settling error at the end of each conversion cycle within 0.5 LSB. Therefore, the device supports burst-mode of operation with every conversion result being as per the datasheet specifications.

Figure 33 shows the block diagram of the internal reference and reference buffer.

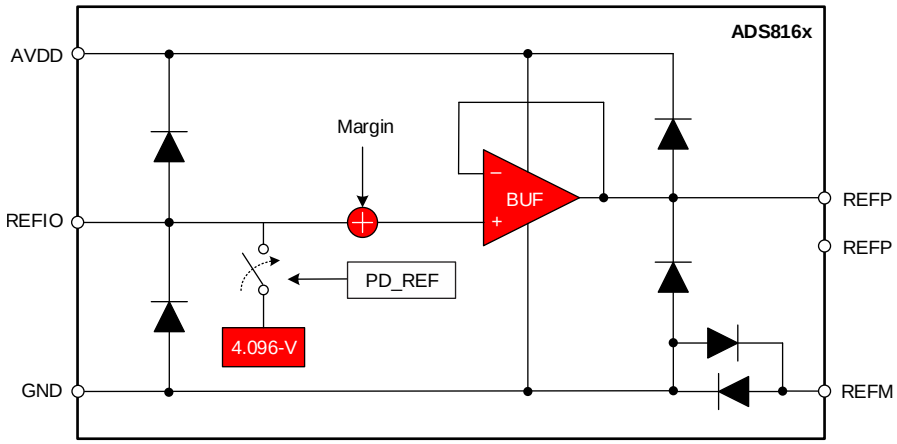


**Figure 33. Internal Reference and Reference Buffer Block Diagram**

For the minimum ADC input offset error ($V_{OS}$), set the REF_SEL[2:0] bits to the value closest to $V_{REF}$ (see the OFST_CAL register). The internal reference buffer has a typical gain of 1 V/V with minimal offset error ($V_{(RO)}$), and the output of the buffer is available between the REFP and the REFM pins. Set the REF_OFST[4:0] (see the REF_MRG1 register) bits to add or subtract an intentional offset voltage as described in Table 22.

Short the two REFP pins externally. Short the REFM pin to GND externally. As shown in Figure 32, place a decoupling capacitor $C_{REFP}$ between the REFP and the REFM pins as close to the device as possible. See the *Layout* section for layout recommendations.

### 7.3.4 REFby2 Buffer

To use the maximum dynamic range of the ADC, the input signal must be biased around the mid-scale of the ADC's input range. In the ADS8168, where absolute input range is 0-V to reference voltage ($V_{REF}$), mid-scale is $V_{REF}$ / 2. The REFby2 buffer generates the $V_{REF}$ / 2 signal for mid-scale shifting of the input signal. REFBy2 can be used in various types of sensor signal conditioning circuits, as shown in Figure 34.

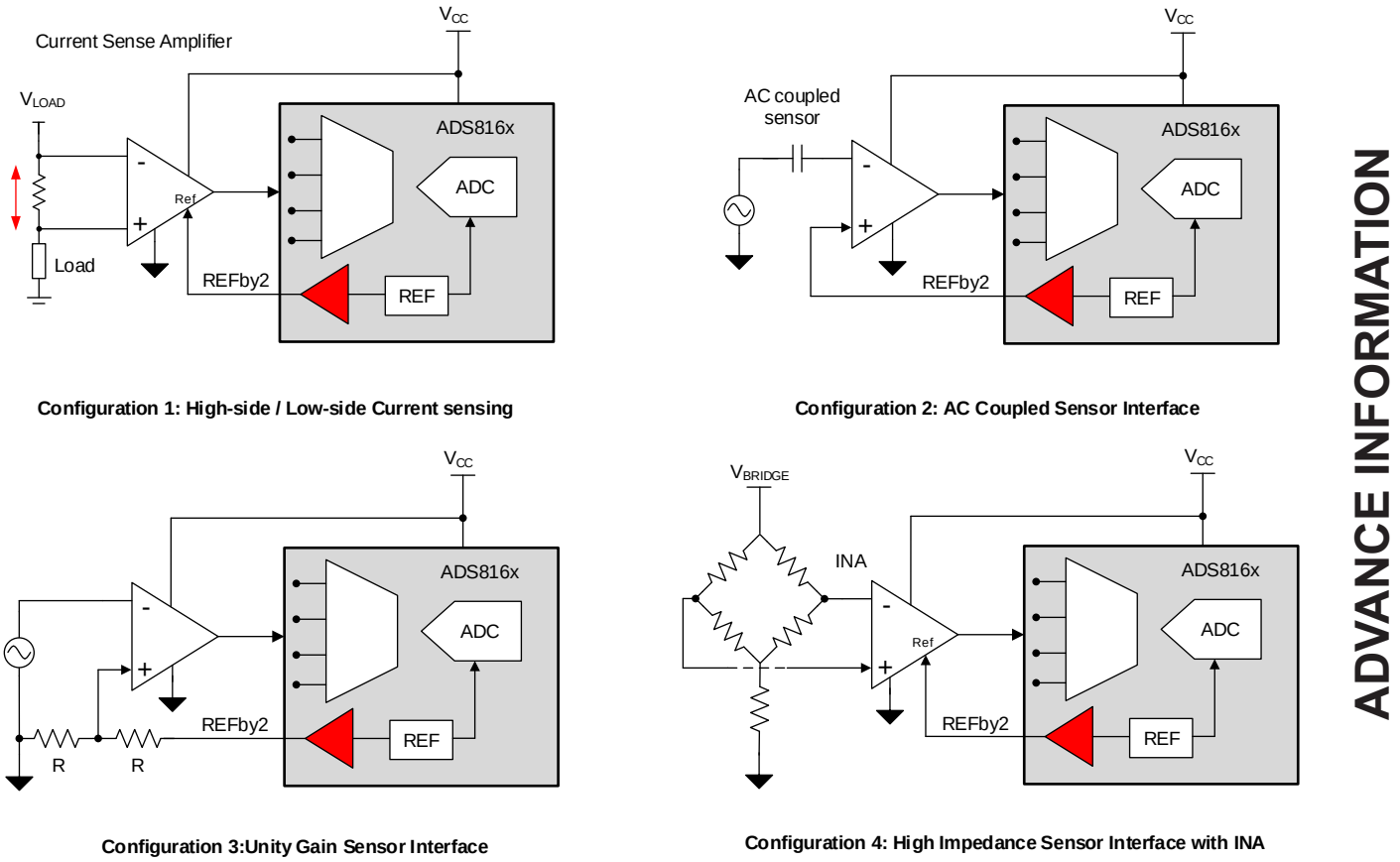


**Figure 34. Signal Conditioning with REFby2 Buffer**

A resistor divider at the output of reference buffer generates the $V_{REF}$ / 2 as illustrated in Figure 35. When not using the internal reference buffer (see the PD_CNTL register), voltage applied at the REFP pin is applied to resistor divider. The output of the resistor divider is buffered and available at the REFby2 pin.

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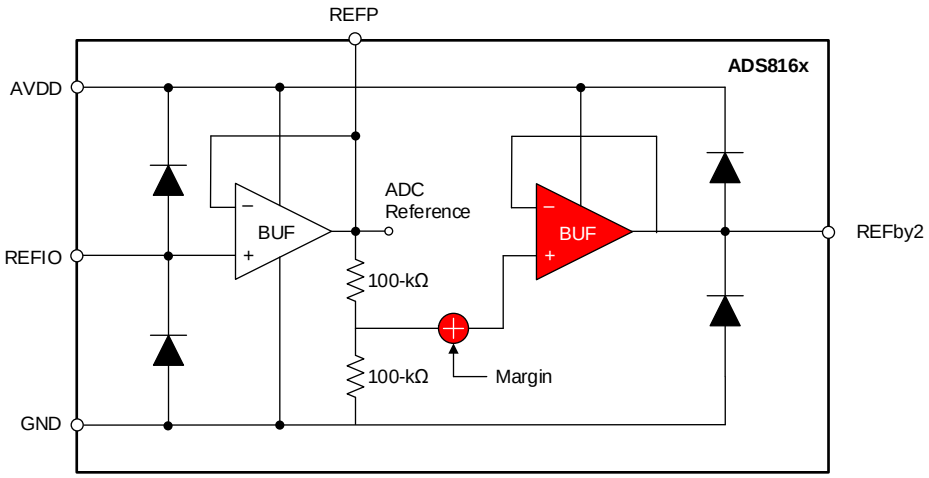


**Figure 35. REFby2 Buffer Model**

The REFby2 buffer is capable of sourcing up to 2-mA DC current. The REFby2 pin has ESD diode connections to AVDD and GND.

### 7.3.5 Converter Module

The converter module samples the analog input signal (provided between the ADC-INP and ADC-INM pins), compares this signal with the reference voltage (between the REFP pins and REFM pin), and generates an equivalent digital output code.

The converter module receives $\overline{\text{RST}}$ and $\overline{\text{CS}}$ inputs from the interface module, and outputs the conversion result back to the interface module.

#### *7.3.5.1 Internal Oscillator*

The device features an internal oscillator (OSC) that provides the conversion clock. Conversion duration varies, but is bounded by the minimum and maximum value of $t_{conv}$.

#### *7.3.5.2 ADC Transfer Function*

The device supports single-ended and pseudo-differential analog inputs. The device output is in straight binary format. Figure 36 and Table 2 show the ideal transfer characteristics for a 16-bit ADC with unipolar inputs.

The least significant bit (LSB) for the ADC is given by Equation 1:

$$1\ \text{LSB} = V_{REF} / 2^{16} \quad (1)$$

ADVANCE INFORMATION

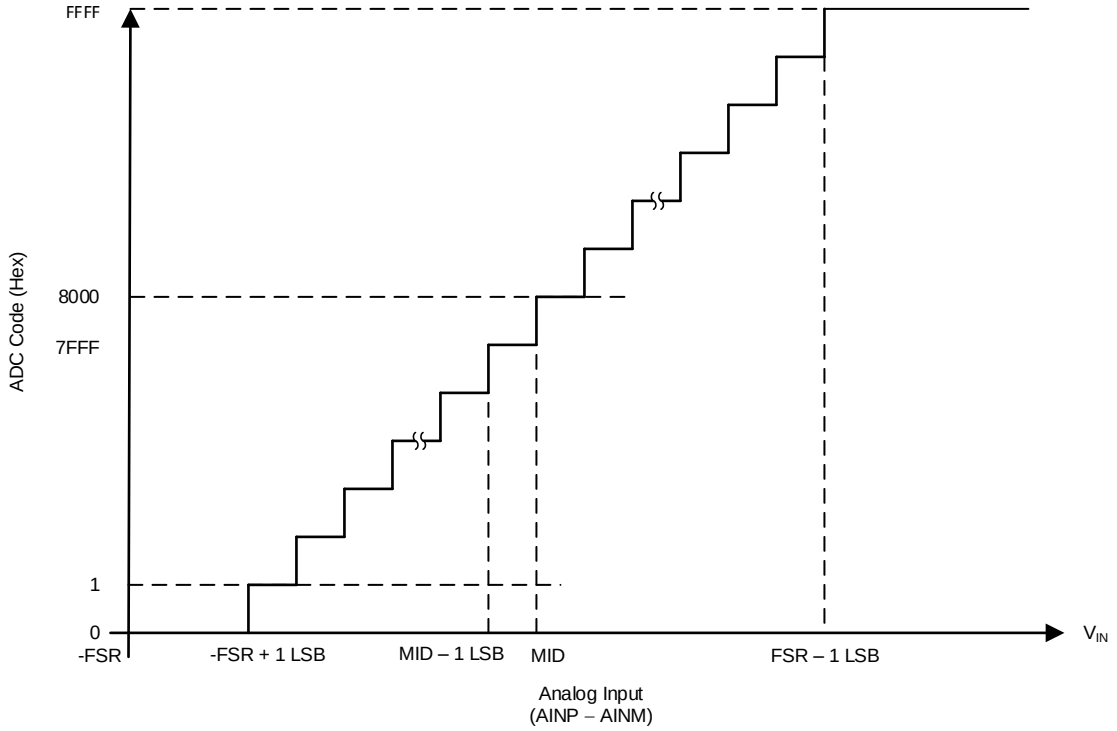


**Figure 36. Converter Transfer Characteristics**

**Table 2. Transfer Characteristics**

| DESCRIPTION | SINGLE-ENDED INPUT VOLTAGE $V_{REF}$ = 4.096V | PSEUDO-DIFFERENTIAL INPUT VOLTAGE $V_{REF}$ = 4.096V | OUTPUT CODE (HEX) |
|---|---|---|---|
| FSR – 1 LSB | 4.0959375 V | 2.0479375 V | FFFF |
| MID + 1 LSB | 2.0480625 V | 0.0000625 V | 8001 |
| MID | 2.048 V | 0 V | 8000 |
| MID – 1 LSB | 2.0479375 V | –0.0000625 V | 7FFF |
| –FSR + 1 LSB | 0.0000625 V | –2.0479375 V | 0001 |
| –FSR | 0 V | –2.048 V | 0000 |

### 7.3.6 LDO

To enable single-supply operation, the device features an internal low-dropout regulator (LDO). The LDO is powered by the AVDD supply, and the 2.85-V (nominal) output is available on the DECAP pin. This LDO output powers the critical analog blocks within the device, and must not be used for any other external purposes.

Decouple the DECAP pin with the GND pin by placing a 1-μF, X7R-grade, ceramic capacitor with a 6.3-V rating, as shown in Figure 37. There is no upper limit on the value of the decoupling capacitor; however, a larger decoupling capacitor results in higher power-up time for the device. See the *Layout* section for layout recommendations.

ADVANCE INFORMATION

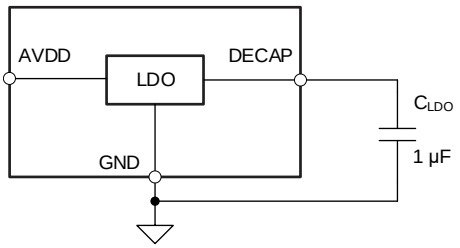


**Figure 37. Internal LDO Connections**

## 7.4 Device Functional Modes

The multiplexer includes a sequence control logic that supports various features as described in the *Channel Selection Using Internal Multiplexer* section.

### 7.4.1 Channel Selection Using Internal Multiplexer

The ADS8168 includes an eight channel, linear, and low leakage current analog multiplexer. The multiplexer performs break-before-make operation when switching channels. There are four modes of switching the multiplexer input channels:

- Manual mode
- On-the-fly mode
- Auto channel sequence mode
- Custom channel sequencing mode

These modes can be selected by configuring the SEQ_MODE[1:0] bits in the DEVICE_CFG register. On power-up the default mode is manual mode; SEQ_MODE[1:0] = 00b, and default input channel is AIN0. The multiplexer configuration registers can be accessed over SPI as shown in Figure 46. The SPI interface eliminates the need for separate MUX control lines.

#### *7.4.1.1 Manual Mode*

In Manual Mode of operation, the channel ID of desired analog input is configured in the CHANNEL_ID register. On power-up or after device reset, AIN0 is selected; CHANNEL_ID[2:0] = 000b. Manual mode can be enabled, from any other sequencing mode, by programming the SEQ_MODE[1:0] = 00b in the DEVICE_CFG register. The timing information for changing channels in manual mode is shown in Figure 38.

The channel information can be updated in a MCU friendly 3-byte access. As the 24-bits of channel configuration are sent over SDI, conversion data is clocked out over SDO. The data on SDO is MSB aligned and the first 16-clocks correspond to 16-bits of conversion data. The last 8-bits of SDO can be ignored by the MCU.

## Device Functional Modes (continued)

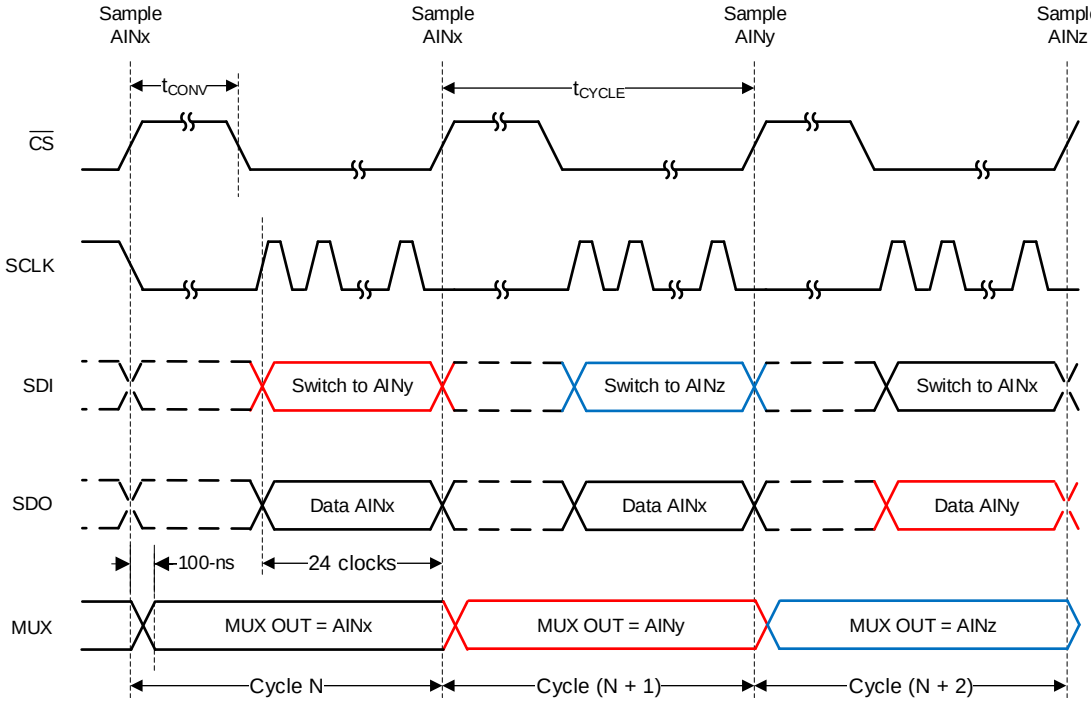


**Figure 38. Manual Mode Timing Diagram**

As can be inferred from Figure 38, the command to switch to $CH_B$ is sent in the $N^{th}$ cycle and the data corresponding to channel $CH_B$ is available in the $(N + 2)^{th}$ cycle. This is because, on the rising edge of $\overline{CS}$, the SDI commands are processed and ADC starts conversion. This causes the conversion to be done on the previous channel ($CH_A$) and not on the updated channel ID ($CH_B$).

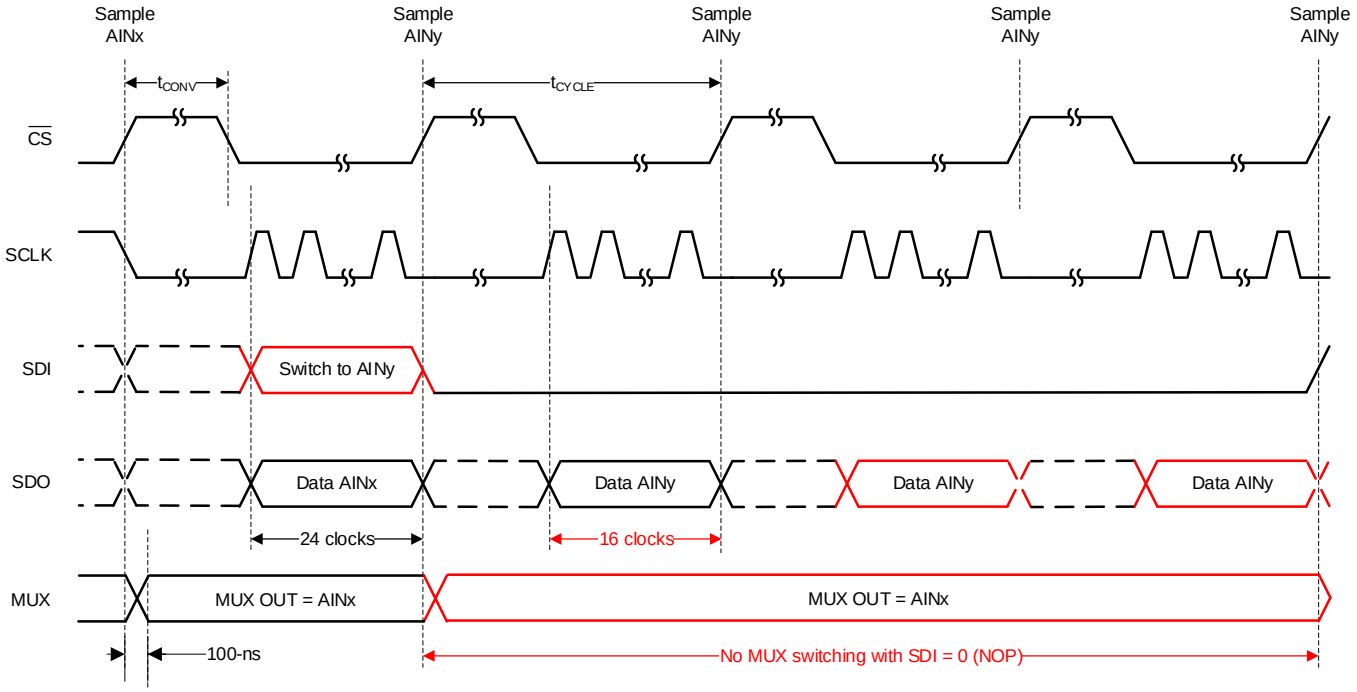


**Figure 39. Manual Mode With No Channel Switching Timing Diagram**

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## Device Functional Modes (continued)

As shown in Figure 39, after selecting $CH_B$ the output of the multiplexer does not create a charge kick-back as long as SDI = 0 (that is, the NOP command). Therefore, high-impedance sources such as voltage from resistor dividers can be connected to analog inputs of the multiplexer without an op amp.

### *7.4.1.2 On-The-Fly Mode*

There is a latency of 1 cycle when switching channels using register access, as in Manual Mode. The newly selected channel data is available 2 cycles after selecting the desired channel. The ADS816x device family supports on-the-fly switching of analog input channels of the multiplexer. This mode can be enabled by programming SEQ_MODE[1:0] = 01b in the DEVICE_CFG register. When enabled, the analog input channel for next conversion is determined by the first 5-bits sent over SDI. Desired analog input channel can be selected by setting MSB = 1 and the following 4-bits as channel ID. If the MSB = 0 then the SDI bit stream is decoded as a normal frame on the rising edge of $\overline{CS}$.

**Table 3. On-the-Fly Mode Channel Selection Commands**

| SDI BITS [15:11] | SDI BITS [10:0] | DESCRIPTION |
|---|---|---|
| 1 0000 | Don't care | Select analog input 0 |
| 1 0001 | Don't care | Select analog input 1 |
| 1 0010 | Don't care | Select analog input 2 |
| 1 0011 | Don't care | Select analog input 3 |
| 1 0100 | Don't care | Select analog input 4 |
| 1 0101 | Don't care | Select analog input 5 |
| 1 0110 | Don't care | Select analog input 6 |
| 1 0111 | Don't care | Select analog input 7 |
| 1 1000 to 1 1111 | Don't care | Error bit is set; select analog input 0 |

To set the device in on-the-fly mode, configure EN_ON_THE_FLY = 1b in ON_THE_FLY_CFG register using a 3-byte register access as shown in Figure 40. Once in this mode, 16-bit data transfer can be used thereby reducing the required clock speed.

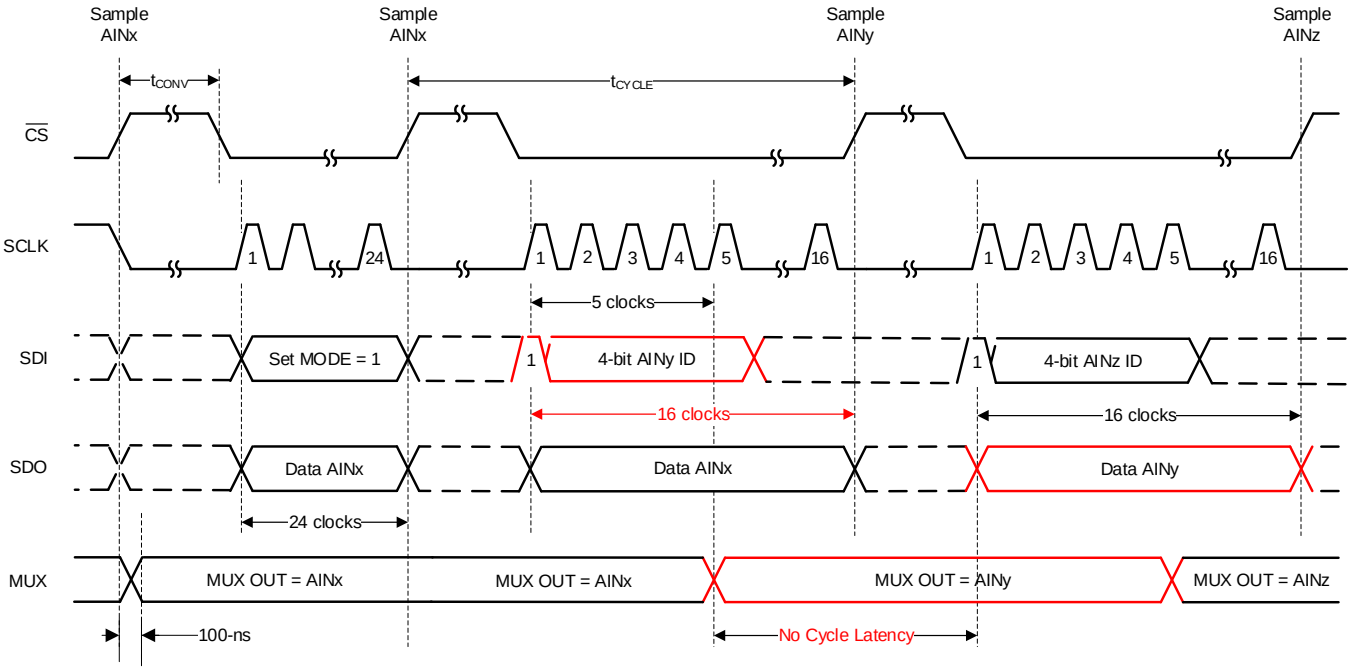


**Figure 40. On-the-Fly Mode With No MUX Channel Selection Latency**

As shown in Figure 41 after selecting $CH_B$ the output of the multiplexer does not create a charge kick-back as long as SDI = 0 (that is, the NOP command). Hence high impedance sources such as voltage from resistor dividers can be connected to analog inputs of the multiplexer without an op amp.

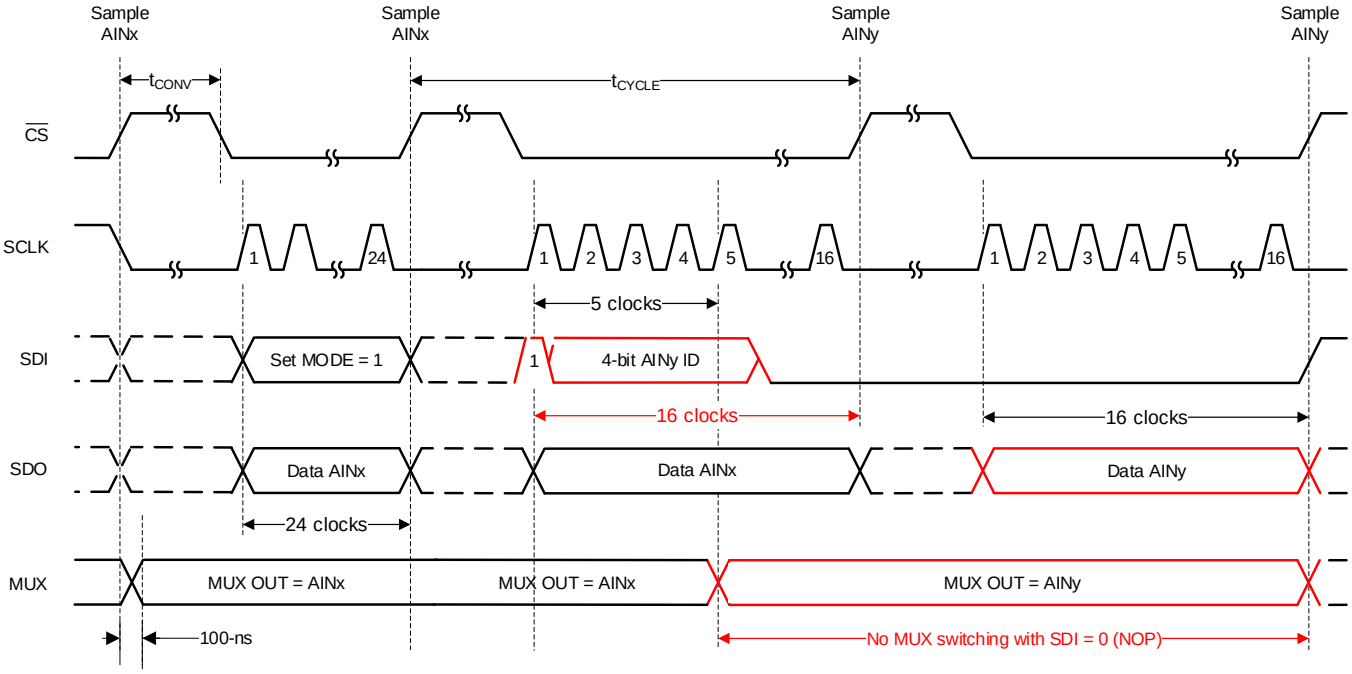


**Figure 41. On-the-Fly Mode With No Channel Switching Timing Diagram**

### *7.4.1.3 Auto Sequence Mode*

In auto sequence mode, the internal channel sequencer can selectively scan channels from AIN0 through AIN7 in ascending order. To select auto sequence mode, configure SEQ_MODE = 10b in the DEVICE_CFG register using a 3-byte register access. One or more channels, among AIN[7:0], can be enabled by configuring the AUTO_SEQ_CFG1 register. By default all analog input channels are enabled. After enabling the desired channels, the sequence can be started by setting SEQ_START = 1b. The ADC auto-increments through the enabled channels after every $\overline{CS}$ rising edge. Upon setting SEQ_START = 1b, the SDO-1/SEQSTS pin is at logic 1 until the last channel conversion frame is complete as shown in Figure 42. After the last enabled channel conversion is complete, channel AIN0 is selected and SDO-1/SEQSTS is in high impedance state.

ADVANCE INFORMATION

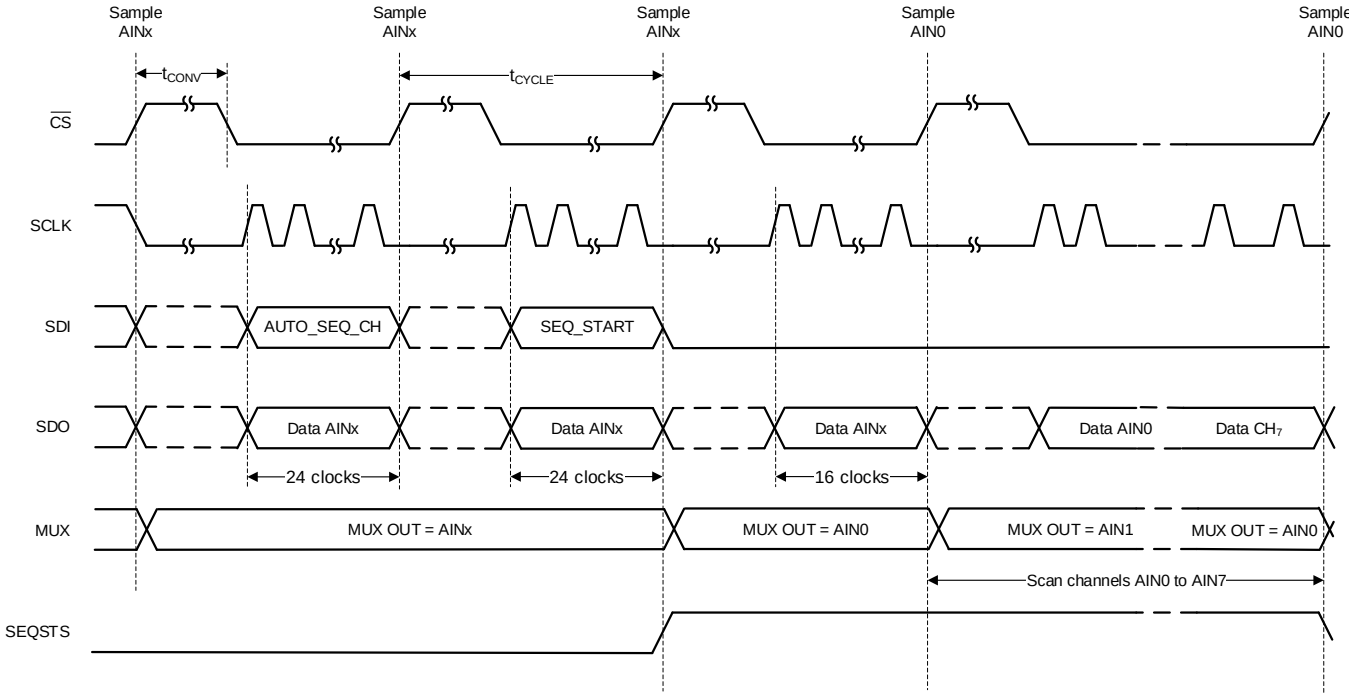


**Figure 42. Starting a sequence in Auto Sequence Mode**

As an example, Figure 43 shows the timing diagram when the device is scanning AIN2 and AIN6 in Auto Sequence mode. At the end of conversion of AIN6, SDO-1/SEQSTS is Hi-Z and AIN0 is selected as the active channel. At the end of sequence, if more conversion frames are launched the device will return valid data corresponding to AIN0.

To use the device in auto sequence mode follow these steps

- Set SEQ_MODE[1:0] = 10b.
- Configure the AUTO_SEQ_CFG1 register. In Figure 43, AUTO_SEQ_CFG1 = 0x84.
- SEQ_START = 1b to start executing the sequence.

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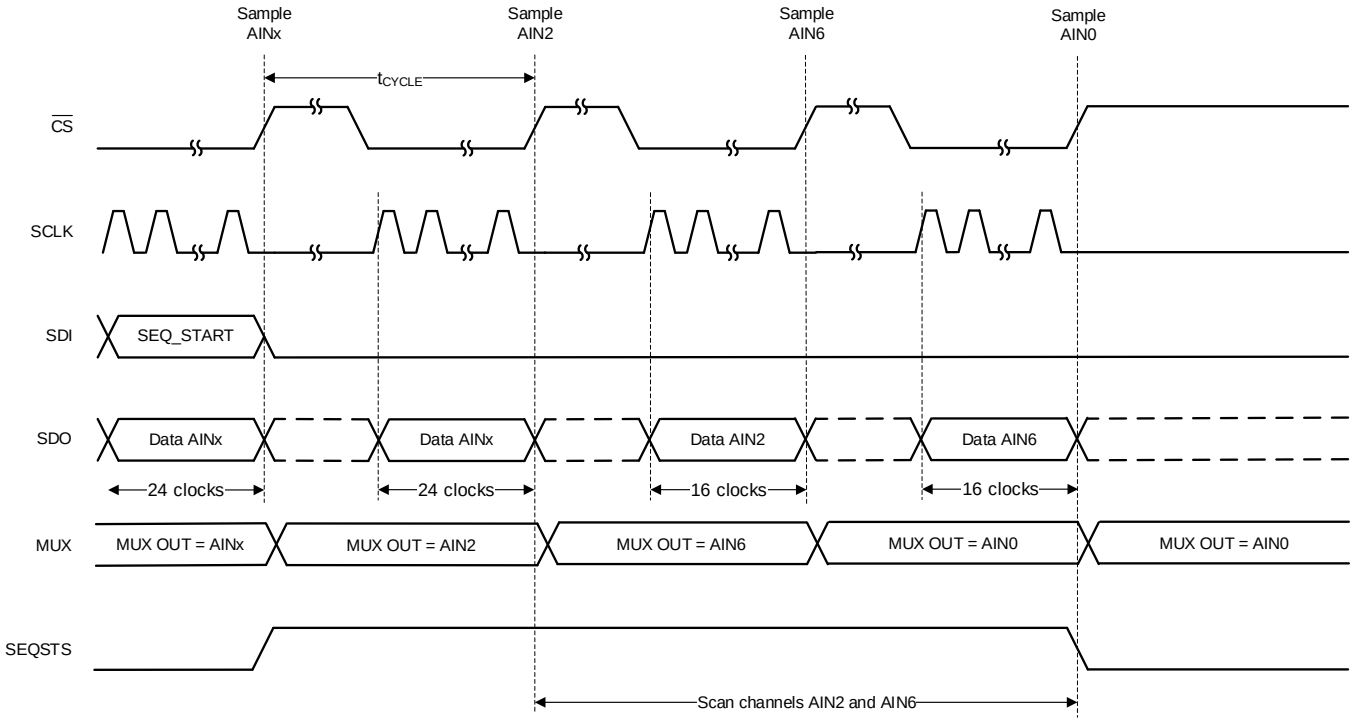


**Figure 43. Example: Scanning Channels 2 and 6 in Auto Sequence Mode**

To repeat a channel sequence indefinitely, set AUTO_REPEAT = 1b. When AUTO_REPEAT bit is enabled, the MUX will scan through the channels enabled in the AUTO_SEQ_CFG1 register and repeat the sequence after the last channel data has been converted as shown in Figure 44.

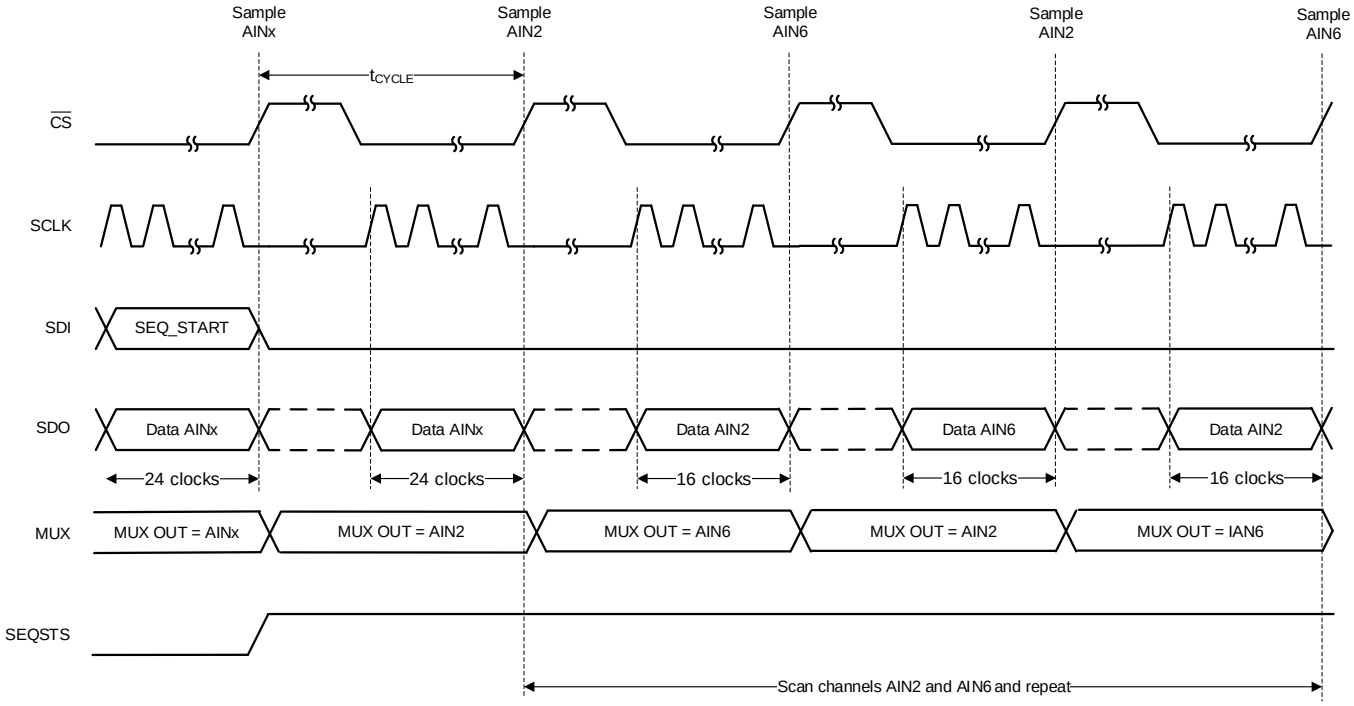


**Figure 44. Example: Scanning Channels 2 and 6 in Auto Sequence Mode With AUTO_REPEAT = 1**

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Figure 44 shows the timing diagram when the device is scanning AIN2 and AIN6 in Auto Sequence mode with AUTO_REPEAT = 1b. At the end of conversion of AIN6, AIN2 is selected as the active channel and the device continues scanning through the enabled channels again.

To use the device in auto sequence with the repeat mode enabled follow these steps

- Set SEQ_MODE[1:0] = 10b.
- Configure the AUTO_SEQ_CFG1 register. In Figure 43, AUTO_SEQ_CFG1 = 0x84.
- AUTO_REPEAT = 1b.
- SEQ_START = 1b to start executing the sequence.

To terminate an on-going channel sequence set SEQ_ABORT = 1. When SEQ_ABORT is set, the auto sequence stops and AIN0 is selected as the active input channel.

#### *7.4.1.4 Custom Channel Sequencing Mode*

In custom channel sequencing mode the internal channel sequencer can selectively scan channels from AIN0 through AIN7 in an order as defined by the user in a programmable lookup table as illustrated in Table 4. The device can be configured in custom channel sequencing mode by programming SEQ_MODE[1:0] = 11b in the DEVICE_CFG register using a 3-byte register access. The channel scanning sequence is programmed by configuring the channel IDs in the register as space as shown in Table 4. Associated with every channel ID, a channel sample count can also be programmed. By default the channel sample count is 1 which means the sequence executes in the order of programmed channel IDs. If channel sample count is > 1 the corresponding channel is sampled and converted programmed number of times before switching to the next channel.

**Table 4. Custom Channel Sequencing Configuration Space**

| REGISTER ADDRESS | CHANNEL ID[2:0] | REGISTER ADDRESS | CHANNEL SAMPLE COUNT[7:0] |
|---|---|---|---|
| 0x8C | Index 0 : 3-bit channel ID (default = 0) | 0x8D | Index 0 : 8-bit sample count (default = 1) |
| 0x8E | Index 1 : 3-bit channel ID (default = 0) | 0x8F | Index 1 : 8-bit sample count (default = 1) |
| 0x90 | Index 2 : 3-bit channel ID (default = 0) | 0x91 | Index 2 : 8-bit sample count (default = 1) |
| 0x92 | Index 3 : 3-bit channel ID (default = 0) | 0x93 | Index 3 : 8-bit sample count (default = 1) |
| 0x94 | Index 4 : 3-bit channel ID (default = 0) | 0x95 | Index 4 : 8-bit sample count (default = 1) |
| 0x96 | Index 5 : 3-bit channel ID (default = 0) | 0x97 | Index 5 : 8-bit sample count (default = 1) |
| 0x98 | Index 6 : 3-bit channel ID (default = 0) | 0x99 | Index 6 : 8-bit sample count (default = 1) |
| 0x9A | Index 7 : 3-bit channel ID (default = 0) | 0x9B | Index 7 : 8-bit sample count (default = 1) |
| 0x9C | Index 8 : 3-bit channel ID (default = 0) | 0x9D | Index 8 : 8-bit sample count (default = 1) |
| 0x9E | Index 9 : 3-bit channel ID (default = 0) | 0x9F | Index 9 : 8-bit sample count (default = 1) |
| 0xA0 | Index 10 : 3-bit channel ID (default = 0) | 0xA1 | Index 10 : 8-bit sample count (default = 1) |
| 0xA2 | Index 11 : 3-bit channel ID (default = 0) | 0xA3 | Index 11 : 8-bit sample count (default = 1) |
| 0xA4 | Index 12 : 3-bit channel ID (default = 0) | 0xA5 | Index 12 : 8-bit sample count (default = 1) |
| 0xA6 | Index 13 : 3-bit channel ID (default = 0) | 0xA7 | Index 13: 8-bit sample count (default = 1) |
| 0xA8 | Index 14 : 3-bit channel ID (default = 0) | 0xA9 | Index 14 : 8-bit sample count (default = 1) |
| 0xAA | Index 15: 3-bit channel ID (default = 0) | 0xAB | Index 15 : 8-bit sample count (default = 1) |

For application specific scanning requirements, start and stop pointers can be used to define the channel scanning sequence. Start index can be programmed in the CCS_START_INDEX register and the stop index can be programmed in the CCS_STOP_INDEX register. The 4-bit index corresponds to the configuration index as shown in Table 4. The sequence starts executing from the index programmed in CCS_START_INDEX (default 0) and stop or loop-back from CCS_STOP_INDEX (default 15). The channel scanning sequence can be looped-back to the start index from stop index by setting the CCS_SEQ_LOOP register = 1b.

After configuring the channel scanning order, start index, and stop index the scanning can be initiated by setting the SEQ_START bit = 1b. The ADC scans through the enabled channels after every $\overline{CS}$ rising edge as defined by the channel scanning order. Upon setting SEQ_START = 1b, the SDO-1/SEQSTS pin is pulled high until the last channel conversion frame is complete as shown in Figure 42. After the last enabled channel conversion is complete, channel AIN0 is selected and SEQSTS/SDO-1 goes to tristate as shown in Figure 43.

As an example, Figure 43 shows the timing diagram when the channel configuration is set as in Table 5. At the end of conversion of AIN6, SEQSTS/SDO-1 is tristate and AIN0 is selected as the active channel. At the end of sequence, if more conversion frames are launched the device will return valid data corresponding to AIN0.

To use the device in easy capture mode follow these steps:

- Set SEQ_MODE[1:0] = 3.
- Configure the channel sequence by setting up registers 0x000C - 0x002B.
- Configure the CCS_START_INDEX register and the CCS_STOP_INDEX register. In Figure 43, CCS_START_INDEX = 0 and CCS_STOP_INDEX = 1.
- Configure CCS_SEQ_LOOP register = 1 for indefinitely looping the sequence. In Figure 43, CCS_SEQ_LOOP register = 0b.
- SEQ_START = 1b to start executing the sequence.

**Table 5. Custom Channel Sequencing Configuration Example**

| REGISTER ADDRESS | CHANNEL ID[2:0] | REGISTER ADDRESS | CHANNEL SAMPLE COUNT[7:0] |
|---|---|---|---|
| 0x8C | 010b (Channel 2) | 0x8D | 1 |
| 0x8E | 110b (Channel 6) | 0x8F | 1 |

### 7.4.2 Digital Window Comparator

The ADS8168 has a programmable digital window comparator for every analog input channel. The integrated digital window comparator enables the host not to read ADC data over serial interface for comparison purposes. In monitoring applications, the ADC can compare channel data with the set thresholds and alert the system host using ALERT pin. Also, it saves processing cycles by not requiring the high and low comparison in software.

The window comparison is achieved by comparing the channel output code with a programmable high and low digital threshold. Each analog input channel has a programable hysteresis which is applicable to both the high and low thresholds of the corresponding channel as shown in Figure 45. Hence the following configurations are available per analog input channel:

- Low threshold
- High threshold
- Hysteresis

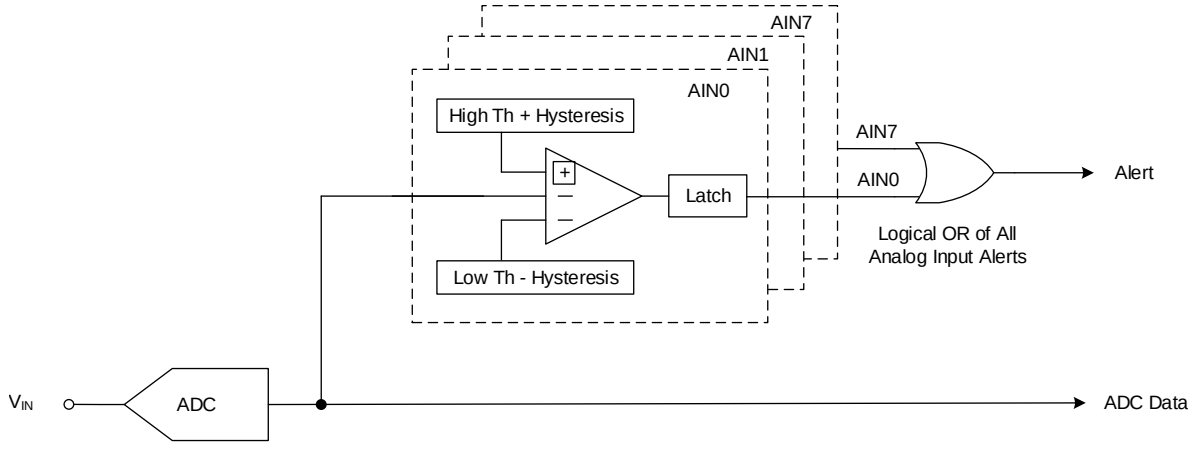


**Figure 45. Digital Window Comparator**

The thresholds and hysteresis can be configured independently for every analog input channel. The ALERT output of the device is a logical OR of all the enabled alert outputs corresponding to the analog inputs. It is possible to selectively enable the window comparator for the analog inputs by configuring the ALERT_CFG.

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The status of alert of individual analog input channel can be read from the ALERT_STATUS register. Further information about high or low threshold ALERT can be read by reading the ALERT_HI_STATUS register and the ALERT_LO_STATUS register, respectively. When monitoring only a low threshold, the high threshold can be set to ADC positive full-scale code. Similarly, when monitoring only a high threshold, the low threshold can be set to negative full-scale code.

## 7.5 Programming

### 7.5.1 Data Transfer Protocols

#### *7.5.1.1 Enhanced-SPI Interface*

The device features an enhanced-SPI interface that allows the host controller to operate at slower SCLK speeds and still achieve the required cycle time with a faster response time.

- For any data write operation, the host controller can use any of the four legacy, SPI-compatible protocols to configure the device, as described in the *Protocols for Configuring the Device* section. See the *Register Read/Write Operation* section for details about register read or write operation.
- For reading ADC conversion data or register data from the device, the enhanced-SPI interface module offers the following options:
  - SPI protocol with a single data output line: SDO-0 (see the *SPI Protocols With a Single SDO* section)
  - SPI protocol with dual data output lines: SDO-1 and SDO-0 (see the *SPI Protocols With Dual SDO* section)
  - Clock re-timer data transfer (see the *Clock Re-Timer Data Transfer* section)

##### 7.5.1.1.1 Protocols for Configuring the Device

As described in Table 6, the host controller can use any of the four SPI protocols i.e SPI-00, SPI-01, SPI-10, or SPI-11 to write data into the device.

**Table 6. SPI Protocols for Configuring the Device**

| PROTOCOL | SCLK POLARITY (At $\overline{CS}$ Falling Edge) | SCLK PHASE (Capture Edge) | SDI_MODE[1:0] | SDO_MODE[1:0] | DIAGRAM |
|---|---|---|---|---|---|
| SPI-00 | Low | Rising | 00h | 00h | Figure 47 |
| SPI-01 | Low | Falling | 01h | 00h | Figure 47 |
| SPI-10 | High | Falling | 02h | 00h | Figure 48 |
| SPI-11 | High | Rising | 03h | 00h | Figure 48 |

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations. To select a different SPI-compatible protocol, program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol. Note that the SPI protocol selected by the configuration of the SDI_MODE[1:0] is applicable to both read and write operations.

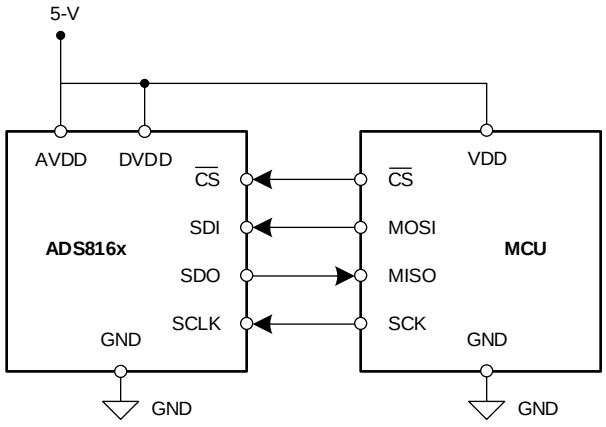


**Figure 46. 4-Wire SPI Interface Connection Diagram**

Figure 47 and Figure 48 detail the four protocols using an optimal data frame.

**NOTE**

As explained in the *Register Read/Write Operation* section, a valid register read or write operation to the device requires 24 SCLKs to be provided within a data transfer frame. When reading ADC conversion data, minimum 16 SCLKs are required within a data transfer frame.

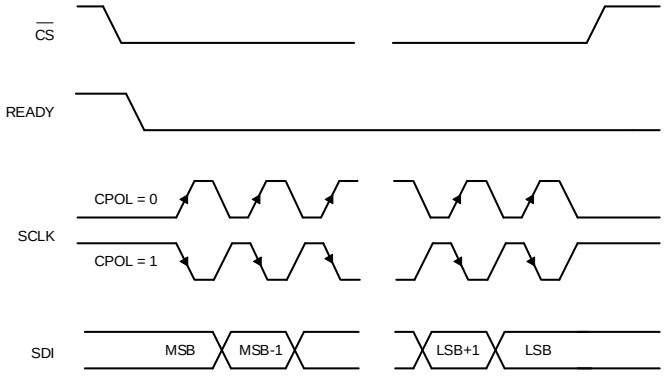


**Figure 47. Standard SPI Timing Protocol (CPHA = 0)**

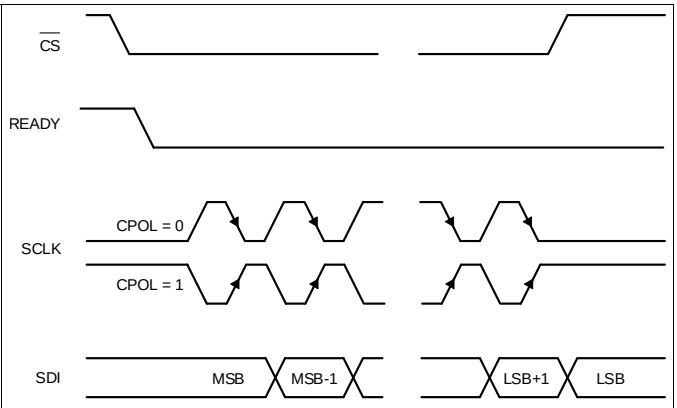


**Figure 48. Standard SPI Timing Protocol (CPHA = 1)**

#### 7.5.1.1.2 Protocols for Reading From the Device

The protocols for the data read operation can be broadly classified into three categories:

1. SPI protocols (SPI-00, SPI-01, SPI-10, and SPI-11) with Single SDO; for example, SDO-0
2. SPI protocols (SPI-00, SPI-01, SPI-10, and SPI-11)with Dual SDO; for example, SDO-1 and SDO-0
3. Source-synchronous protocol for data transfer

##### *7.5.1.1.2.1 SPI Protocols With a Single SDO*

As shown in Table 7, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00, SPI-01, SPI-10, or SPI-11) to read data from the device.

**Table 7. SPI Protocols for Reading From the Device**

| PROTOCOL | SCLK POLARITY (At $\overline{CS}$ Falling Edge) | SCLK PHASE (Capture Edge) | MSB BIT LAUNCH EDGE | SDI_MODE[1:0] | SDO_MODE[1:0] | DIAGRAM |
|---|---|---|---|---|---|---|
| SPI-00 | Low | Rising | $\overline{CS}$ falling | 00h | 00h | Figure 49 |
| SPI-01 | Low | Falling | 1st SCLK rising | 01h | 00h | Figure 49 |
| SPI-10 | High | Falling | $\overline{CS}$ falling | 02h | 00h | Figure 50 |
| SPI-11 | High | Rising | 1st SCLK falling | 03h | 00h | Figure 50 |

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00 protocol for data read and data write operations. To select a different SPI-compatible protocol for both the data transfer operations:

1. Program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00 protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol.
2. Set the SDO_MODE[1:0] bits = 00b in the SDO_CNTL1 register.

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**NOTE**

The SPI transfer protocol selected by configuring the SDI_MODE[1:0] bits in the SDI_CNTL register determines the data transfer protocol for both write and read operations.

When using any of the SPI-compatible protocols, the READY output remains low throughout the data transfer frame.

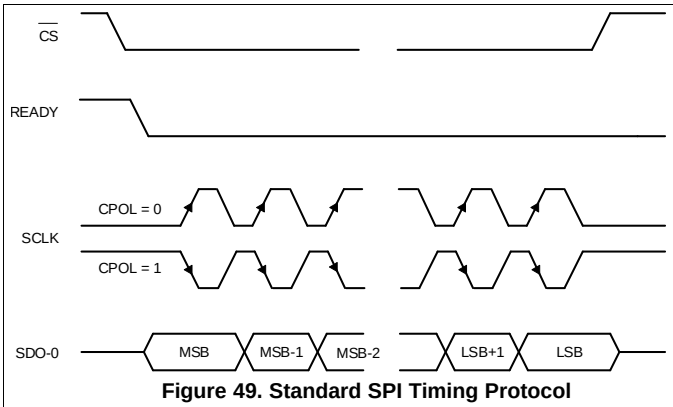


**Figure 49. Standard SPI Timing Protocol (CPHA = 0, Single SDO-0)**

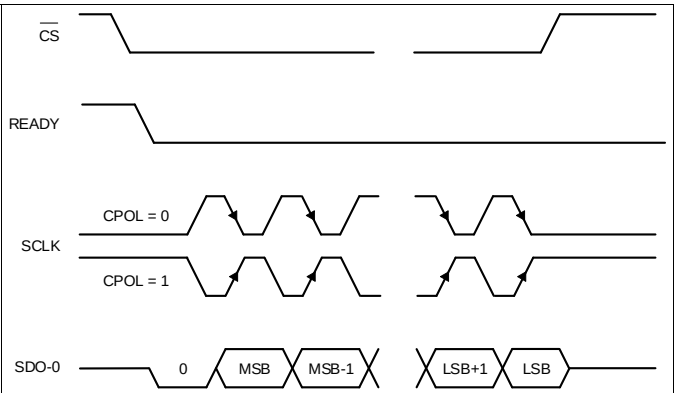


**Figure 50. Standard SPI Timing Protocol (CPHA = 1, Single SDO-0)**

#### 7.5.1.1.2.2 SPI Protocols With Dual SDO

The device provides an option to increase the SDO bus width from one bit (default, single SDO-0) to two bits (dual SDO) when operating with any of the data transfer protocols. In order to operate the device in dual SDO mode, the SDO_WIDTH bit in the SDO_CNTL1 register must be set to 1b. In this mode, the SDO-1/SEQSTS pin functions as SDO-1.

In dual SDO mode, two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK launch edge, as shown in Figure 51 and Figure 52.

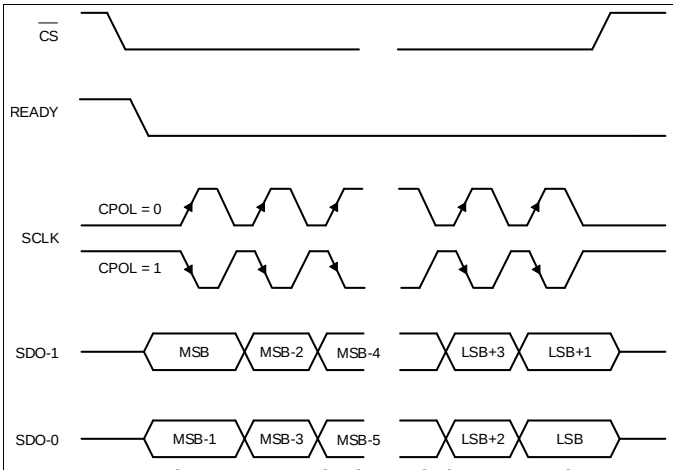


**Figure 51. Standard SPI Timing Protocol (CPHA = 0, Dual SDO)**

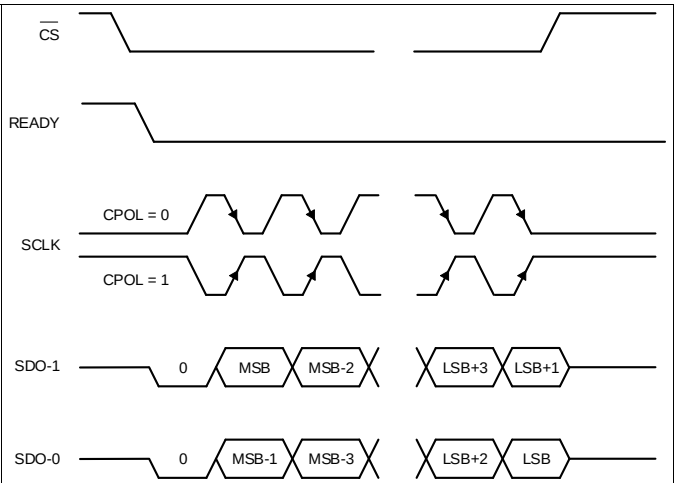


**Figure 52. Standard SPI Timing Protocol (CPHA = 1, Dual SDO)**

#### 7.5.1.1.2.3 Clock Re-Timer Data Transfer

In clock re-timer data transfer mode, the device provides an output clock that is synchronous with the output data. Furthermore, the host controller can also select the data bus width in this mode of operation. In all modes of operation, the READY pin provides the output clock, synchronous to the device data output.

The clock re-timer data transfer allows the width of the output bus to be configured, similar to the SPI protocols.

#### 7.5.1.1.2.3.1 Output Bus Width Options

The device provides an option to increase the SDO-x bus width from one bit (default, single SDO-x) to two bits (dual SDO-x) when operating with clock re-timer data transfer. In order to operate the device in dual SDO mode, the SDO_WIDTH bit in the SDO_CNTL1 register must be set to 1b. In this mode, the SDO-1/SEQSTS pin functions as SDO-1.

**NOTE**

For any particular data transfer, SPI or Clock Re-timer, the device follows the same timing specifications for single and dual SDO modes. The only difference is that in the dual SDO mode the device requires half as many clock cycles to output the same number of bits when in single SDO mode, thus reducing the minimum required clock frequency for a certain sampling rate of the ADC.

### 7.5.2 Register Read/Write Operation

This device features configuration registers (as described in the *Interface and Hardware Configuration Registers* section). To access the internal configuration registers, these devices support the commands listed in Table 8.

**Table 8. Supported Commands**

| B[23:19] | B[18:8] | B[7:0] | COMMAND ACRONYM | COMMAND DESCRIPTION |
|---|---|---|---|---|
| 00000 | 00000000000 | 00000000 | NOP | No operation |
| 00001 | <11-bit address> | <8-bit data> | WR_REG | Write <8-bit data> to the <11-bit address> |
| 00010 | <11-bit address> | 00000000 | RD_REG | Read contents from the <11-bit address> |
| 00011 | <11-bit address> | <8-bit unmasked bits> | SET_BITS | Set <8-bit unmasked bits> from <11-bit address> |
| 00100 | <11-bit address> | <8-bit unmasked bits> | CLR_BITS | Clear <8-bit unmasked bits> from <11-bit address> |
| Remaining combinations | xxxxxxxxx | xxxxxxxx | Reserved | These commands are reserved and treated by the device as no operation |

The ADS816x device family supports two types of data transfer operations: *data write* (the host controller configures the device), and *data read* (the host controller reads data from the device).

Any data write to the device is always synchronous to the external clock provided on the SCLK pin. The WR_REG command writes the 8-bit data into the 11-bit address specified in the command string. The CLR_BITS command clears the specified bits (identified by 1) at the 11-bit address (without affecting the other bits), and the SET_BITS command sets the specified bits (identified by 1) at the 11-bit address (without affecting the other bits).

Figure 53 shows the digital waveform for register read operation. Register read operation consists of two frames: one frame to initiate a register read and second frame to read data from register address provided in the first frame. As shown in Figure 53, during the first 24-bit frame, read command (00010b), 11-bit register address and 8-bit dummy data are sent over SDI. When $\overline{CS}$ goes from low to high, this read command is decoded and the requested register data is available for reading during the next frame. During the second frame, the first 8 bits on SDO correspond to the requested register read. During the second frame SDI can be used to initiate another operation or can be set to 0.

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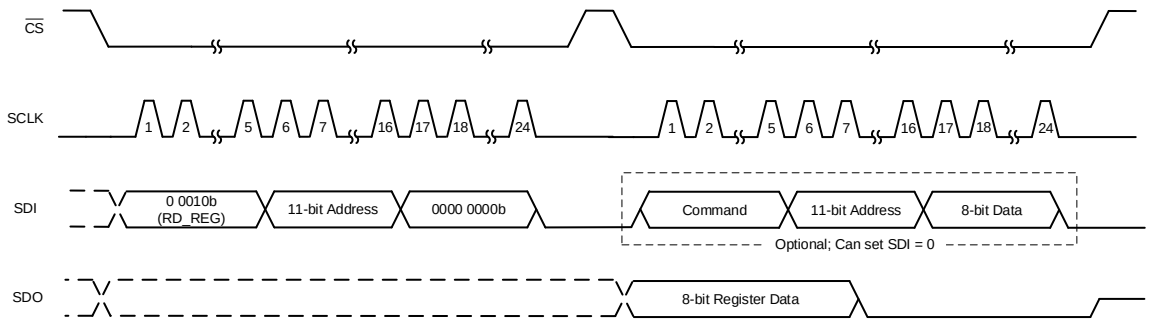


**Figure 53. Register Read Operation**

For writing data to the register one 24-bit frame is required as shown in Figure 54. The 24-bit data on SDI consists of 5-bit write command (00001b), 11-bit register address and 8-bit data. On $\overline{CS}$ rising edge the write command is decoded and the specified register is updated with the 8-bit data specified during register write operation.

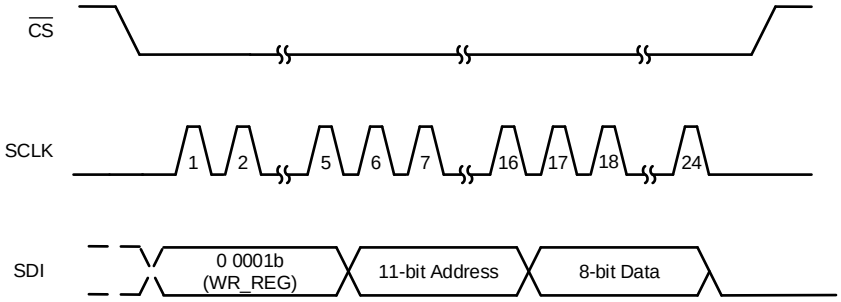


**Figure 54. Register Write Operation**

Table 9 lists the access codes for the ADS8168 registers.

**Table 9. ADS8168 Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| R | R | Read |
| R-W | R/W | Read or write |
| W | W | Write |
| *-n* | | Value after reset or the default value |

## 7.6 Register Maps

### 7.6.1 Interface and Hardware Configuration Registers

The device features following hardware configuration registers, mapped as described in Table 10.

**Table 10. Configuration Registers Mapping**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 000h | REG_ACCESS | Enables read/write access to device configuration registers specified in *Interface and Hardware Configuration Registers* |
| 004h | PD_CNTL | Enable/Disable control for reference, reference buffer, REFby2 buffer, and the ADC |
| 008h | SDI_CNTL | SPI-00/01/10/11 protocol selection. |
| 00Ch | SDO_CNTL1 | SDO output protocol selection |
| 00Dh | SDO_CNTL2 | Output data rate selection |

## Register Maps (continued)

**Table 10. Configuration Registers Mapping (continued)**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 00Eh | SDO_CNTL3 | Reserved |
| 00Fh | SDO_CNTL4 | Configuration for SEQSTS pin when not using SDO-1 for data transfer. |
| 010h | DATA_CNTL | Output data word configuration |
| 011h | PARITY_CNTL | Parity configuration register |

### *7.6.1.1 REG_ACCESS Register (address = 00h) [reset = 00h]*

This register enables/disables write access to the device configuration registers specified in Table 10.

**Figure 55. REG_ACCESS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REG_ACCESS_BITS | | | | | | | |
| R/W-0000 0000b | | | | | | | |

**Table 11. REG_ACCESS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | REG_ACCESS_BITS | R/W | 0000 0000b | Enables or disables write access to the device configuration registers specified in Table 10.<br>Write 1010 1010b to this register to enable write access.<br>Write access is disabled for all values other than REG_ACCESS_BITS = 1010 1010b. |

### *7.6.1.2 PD_CNTL Register (address = 04h) [reset = 00h]*

This register controls the low-power modes offered by the device. Write access to this register are disabled on power-up. To enable write access, configure the REG_ACCESS register.

**Figure 56. PD_CNTL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | PD_REFby2 | PD_REF | PD_REFBUF | PD_ADC | 0 |
| R-0b | R-0b | R-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R-0b |

**Table 12. PD_CNTL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | R | 000b | Reserved bits. Reads return 000b. |
| 4 | PD_REFby2 | R/W | 0b | This bit powers down the internal reference-by-2 buffer.<br>0b = REFby2 buffer is powered up<br>1b = REFby2 buffer is powered down |
| 3 | PD_REF | R/W | 0b | This bit powers down the internal reference.<br>0b = Internal reference is powered up<br>1b = Internal reference is powered down |
| 2 | PD_REFBUF | R/W | 0b | This bit powers down the internal reference buffer.<br>0b = Internal reference buffer is powered up<br>1b = Internal reference buffer is powered down |
| 1 | PD_ADC | R/W | 0b | This bit powers down the converter module.<br>0b = converter module is powered up<br>1b = converter module is powered down |
| 0 | 0 | R | 0b | Reserved bits. Do not write. Reads return 0b. |

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To power-down the converter module, set the PD_ADC bit in the PD_CNTL register. The converter module powers down on the rising edge of $\overline{CS}$. To power-up the converter module, reset the PD_ADC bit in the PD_CNTL register. The converter module starts to power-up on the rising edge of $\overline{CS}$. Wait for $t_{PU\_ADC}$ before initiating any conversion or data transfer operation.

To power-down the internal reference buffer, set the PD_REFBUF bit in the PD_CNTL register. The internal reference buffer powers down on the rising edge of $\overline{CS}$.

To power-down the internal reference, set the PD_REF bit in the PD_CNTL register. The internal reference powers down on the rising edge of $\overline{CS}$.

#### 7.6.1.3 SDI_CNTL Register (address = 008h) [reset = 00h]

This register selects the SPI protocol for writing data to the device. Write access to this register are disabled on power-up. To enable write access, configure the REG_ACCESS register.

**Figure 57. SDI_CNTL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | SDI_MODE[1:0] | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-00b | |

**Table 13. SDI_CNTL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R | 000000b | Reserved bits. Do not write. Reads return 000000b. |
| 1-0 | SDI_MODE[1:0] | R/W | 00b | These bits select the protocol for writing data into the device.<br>00b = Standard SPI with CPOL = 0 and CPHASE = 0<br>01b = Standard SPI with CPOL = 0 and CPHASE = 1<br>10b = Standard SPI with CPOL = 1 and CPHASE = 0<br>11b = Standard SPI with CPOL = 1 and CPHASE = 1 |

#### 7.6.1.4 SDO_CNTL1 Register (address = 0Ch) [reset = 00h]

This register configures the protocol for reading data from the device. Write access to this register are disabled on power-up. To enable write access, configure the REG_ACCESS register.

**Figure 58. SDO_CNTL1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | OUTDATA_uC_MODE | DATA_RIGHT_ALIGNED | BYTE_INTERLEAVE | 0 | SDO_WIDTH | SDO_MODE[1:0] | |
| R-0b | R/W-0b | R/W-0b | R/W-0b | R-0b | R/W-0b | R/W-00b | |

**Table 14. SDO_CNTL1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R | 0b | Reserved bit. Do not write. Read returns 0b. |
| 6 | OUTDATA_uC_MODE | R/W | 0b | Enables MCU/Processor friendly data interface.<br>0b = Length of output data is determined by DATA_OUT_FORMAT field in the DATA_CNTL register.<br>1b = Length of output data is fixed to<br>16-bits : when length based on DATA_OUT_FORMAT is ≤ 16.<br>32-bits : when length based on DATA_OUT_FORMAT is > 16. |
| 5 | DATA_RIGHT_ALIGNED | R/W | 0b | This bit is ignored if OUTDATA_uC_MODE = 0b. When OUTDATA_uC_MODE = 1b:<br>0b = Data frame left aligned. The SDOs will output device data bits followed by 0s in a 32-bit output frame.<br>1b = Data frame right aligned. The SDOs will output 0s followed by device data bits in a 32-bit output frame. |

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**Table 14. SDO_CNTL1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4 | BYTE_INTERLEAVE | R/W | 0b | This bit is ignored if OUTDATA_uC_MODE = 0b or SDO_WIDTH = 0b. When OUTDATA_uC_MODE = 1b and SDO_WIDTH = 1b:<br>0b = Bit mode. SDO-1 will output (MSB, MSB - 2 ..., LSB + 1) and SDO-0 will output (MSB - 1, MSB - 3, ..., LSB).<br>1b = Byte mode. If total number of bits to be read from the device is N (conversion result, parity, channel ID, etc.);<br>When N ≤16: SDO-1 will output 8 MSB bits and SDO-0 will output (N-8) bits.<br>When 16 < N ≤ 32: SDO-1 will output 16 MSB bits and SDO-0 will output (N-16) bits. |
| 3 | 0 | R | 0b | Reserved bit. Do not write. Read returns 0b. |
| 2 | SDO_WIDTH | R/W | 0b | This bit sets the width of the output bus.<br>0b = Data bits are output only on SDO-0<br>1b = Data bits are output on SDO-0 (MSB - 1, MSB - 3 ..., LSB) and SDO-1 (MSB, MSB - 2 ..., LSB + 1) |
| 1-0 | SDO_MODE[1:0] | R/W | 00b | These bits select the protocol for reading data from the device.<br>00b = SDO follows the SPI protocol selected in the SDI_CNTL register<br>01b = SDO follows the SPI protocol selected in the SDI_CNTL register but with *Early Data Launch* feature enabled. See .<br>10b = Invalid configuration, not supported by the device<br>11b = SDO follows the Clock Re-Timer Data Transfer |

### 7.6.1.5 SDO_CNTL2 Register (address = 0Dh) [reset = 00h]

This register configures the output data rates, SDR or DDR, when using the clock re-timer data transfer. Write access to this register are disabled on power-up. To enable write access, configure the REG_ACCESS register.

**Figure 59. SDO_CNTL2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DATA_RATE |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

**Table 15. SDO_CNTL2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 000 0000 | R | 000 0000b | Reserved bit. Do not write. Reads return 000 0000b. |
| 0 | DATA_RATE | R/W | 0b | This bit is ignored if SDO_MODE[1:0] = 0xb. When SDO_MODE[1:0] = 11b:<br>0b = SDOs are updated at single data rate (SDR) with respect to the output clock<br>1b = SDOs are updated at double data rate (DDR) with respect to the output clock |

### 7.6.1.6 SDO_CNTL3 Register (address = 0Eh) [reset = 00h]

The bits in this register are reserved.

**Figure 60. SDO_CNTL3 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b |

**Table 16. SDO_CNTL3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | 0000 0000 | R | 0000 0000b | Reserved bits. Do not write. Reads return 0000 0000b. |

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### 7.6.1.7 SDO_CNTL4 Register (address = 0Fh) [reset = 00h]

This register configures the behaviour of SEQ_STS pin when not using dual SDO mode (SDO_WIDTH = 0b). Write access to this register are disabled on power-up. To enable write access, configure the REG_ACCESS register.

**Figure 61. SDO_CNTL4 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEQSTS_CFG |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

**Table 17. SDO_CNTL4 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 000 0000 | R | 000 0000b | Reserved bits. Do not write. Reads return 000 0000b. |
| 0 | SEQSTS_CFG | R/W | 0b | This pin decides the behaviour of SDO-1 when SDO_WIDTH = 0b.<br>0b = SDO-1 is tristate.<br>1b = SDO-1 will indicate sequence active status. |

### 7.6.1.8 DATA_CNTL Register (address = 010h) [reset = 00h]

This register configures the contents of the output data word. Write access to this register are disabled on power-up. To enable write access, configure the REG_ACCESS register.

**Figure 62. DATA_CNTL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | DATA_OUT_FORMAT[1:0] | | 0 | 0 | 0 | DATA_VAL |
| R-0b | R-0b | R/W-00b | | R-0b | R-0b | R-0b | R/W-0b |

**Table 18. DATA_CNTL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 00 | R | 000b | Reserved bits. Reads return 00b. |
| 5-4 | DATA_OUT_FORMAT[1:0] | R/W | 00b | These bits control the composition of the output data frame.<br>00b = ADC conversion result.<br>01b = ADC conversion result + 4-bit channel ID.<br>10b = ADC conversion result + 4-bit channel ID + 4-bit device status (DEVICE_CFG[3:0]) + 2-bit channel configuration.<br>11b = Reserved.<br>Parity bits can be appended to data output frame. See the PARITY_CNTL register for details. |
| 3-1 | 000 | R | 000b | Reserved bits. Reads return 00b. |
| 0 | DATA_VAL | R/W | 0b | Setting this bit enables debug mode for SDO capture.<br>0b = Normal operation. Device data output on SDO.<br>1b = Device will output fixed 1010 0110 patten. This is useful for debugging data capture from the device. |

### 7.6.1.9 PARITY_CNTL Register (address = 11h) [reset = 00h]

This register enables/disables computing parity status for the output from the device. Write access to this register are disabled on power-up. To enable write access, configure the REG_ACCESS register.

**Figure 63. PARITY_CNTL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | PARITY_EN | 0 | 0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b | R-0b | R-0b |

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**Table 19. PARITY_CNTL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 0000 | R | 0 0000b | Reserved bits. Do not write. Reads return 0 0000b. |
| 2 | PARITY_EN | R/W | 0b | Enables parity computation on the data output bits.<br>0b = Parity disabled.<br>1b = 1-bit parity appended to data output frame. Length of data is 1-bit more than length specified by DATA_OUT_FORMAT. |
| 1-0 | 00 | R | 00b | Reserved bits. Do not write. Reads return 00b. |

### 7.6.2 Device Calibration Registers

The device features following calibration registers, mapped as described in Table 20.

**Table 20. Calibration Registers Mapping**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 018h | OFST_CAL | Setting for optimum ADC offset calibration when using external reference input |
| 019h | REF_MRG1 | Margin setting for reference buffer to compensate for initial accuracy of the reference voltage |
| 01Ah | REF_MRG2 | Enable margin setting of reference buffer as configured in REF_MRG1 |
| 01Bh | REFby2_MRG | REFby2 buffer margin configuration |

#### *7.6.2.1 OFST_CAL Register (address = 018h) [reset = 00h]*

This register selects optimal offset calibration when using external reference input. When using internal reference, do not write into this register. See the *Reference Buffer* section for more details.

**Figure 64. OFST_CAL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | REF_SEL[2:0] | | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R/W-000b | | |

**Table 21. OFST_CAL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R | 0 0000b | Reserved bits. Reads return 0 0000b. |
| 2-0 | REF_SEL[2:0] | R/W | 000b | These bits select the external reference range for optimal offset.<br>000b = Optimum offset calibration for $V_{REF}$ = 5.0 V<br>001b = Optimum offset calibration for $V_{REF}$ = 4.5 V<br>010b = Optimum offset calibration for $V_{REF}$ = 4.096 V<br>011b = Optimum offset calibration for $V_{REF}$ = 3.3 V<br>100b = Optimum offset calibration for $V_{REF}$ = 3.0 V<br>101b = Optimum offset calibration for $V_{REF}$ = 2.5 V<br>110b = Optimum offset calibration for $V_{REF}$ = 5.0 V<br>111b = Optimum offset calibration for $V_{REF}$ = 5.0 V |

#### *7.6.2.2 REF_MRG1 Register (address = 019h) [reset = 00h]*

This register selects the margining to be added to or subtracted from the reference buffer output; see the *Reference Buffer* section.

**Figure 65. REF_MRG1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | REF_OFST[4:0] | | | | |
| R-0b | R-0b | R-0b | R/W-00000b | | | | |

**Table 22. REF_MRG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | R | 000b | Reserved bits. Reads return 000b. |
| 4-0 | REF_OFST[4:0] | R/W | 00000b | These bits select the reference offset value as per Table 23. |

**Table 23. REF_OFST[4:0] settings**

| REF_OFST[4:0] | $\Delta V_{REFBUFOUT}$ (typical) |
|---|---|
| 00000b | 0 mV |
| 00001b | 280 µV |
| 00010b | 580 µV |

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**Table 23. REF_OFST[4:0] settings (continued)**

| REF_OFST[4:0] | $\Delta V_{REFBUFOUT}$ (typical) |
|---|---|
| 00011b | 840 µV |
| 00100b | 1.12 mV |
| 00101b | 1.4 mV |
| 00110b | 1.68 mV |
| 00111b | 1.96 mV |
| 01000b | 2.24 mV |
| 01001b | 2.52 mV |
| 01010b | 2.8 mV |
| 01011b | 3.08 mV |
| 01100b | 3.36 mV |
| 01101b | 3.64 mV |
| 01110b | 3.92 mV |
| 01111b | 4.2 mV |
| 10000b | –4.5 mV |
| 10001b | –4.22 mV |
| 10010b | –3.94 mV |
| 10011b | –3.66 mV |
| 10100b | –3.38 mV |
| 10101b | –3.1 mV |
| 10110b | –2.82 mV |
| 10111b | –2.54 mV |
| 11000b | –2.26 mV |
| 11001b | –1.98 mV |
| 11010b | –1.7 mV |
| 11011b | –1.42 mV |
| 11100b | –1.14 mV |
| 11101b | –860 µV |
| 11110b | –580 µV |
| 11111b | –280 µV |

### *7.6.2.3 REF_MRG2 Register (address = 01Ah) [reset = 00h]*

This register enables/disables the reference buffer margin configuration in the REF_MRG1 register.

**Figure 66. REF_MRG2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | EN_MARG |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

**Table 24. REF_MRG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 000 0000b | Reserved bits. Reads return 000 0000b. |
| 0 | EN_MARG | R/W | 0b | This bit enables reference buffer margining feature.<br>0b = Margining is disabled<br>1b = Margining is enabled |

### *7.6.2.4 REFby2_MRG Register (address = 01Bh) [reset = 00h]*

This register selects the margining to be added to or subtracted from the REFFby2 buffer output; see the *REFby2 Buffer* section.

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**Figure 67. REFby2_MRG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | REFby2_OFST[2:0] | | | 0 | 0 | 0 | EN_REFby2_MARG |
| R-0b | R/W-000b | | | R-0b | R-0b | R-0b | R/W-0b |

**Table 25. REFby2_MRG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R | 0b | Reserved bit. Do not write. Reads return 0b. |
| 6-4 | REFBY2_OFST[2:0] | R/W | 000b | These bits select the REFby2 offset value as per Table 26. |
| 3-1 | 0 | R | 000b | Reserved bits. Do not write. Reads return 000b. |
| 0 | EN_REFby2_MARG | R/W | 0b | This bit enables REFby2 buffer margining feature.<br>0b = Margining is disabled<br>1b = Margining is enabled |

**Table 26. REFby2_OFST[2:0] settings**

| REFby2_OFST[2:0] | $V_{REFby2}$(1) AT $V_{REF}$ = 4.096 V | $V_{REFby2}$(1) AT $V_{REF}$ = 5 V |
|---|---|---|
| EN_REFby2_MARG = 0b | 2.04800 V | 2.50000 V |
| 000b | 2.12611 V | 2.59155 V |
| 001b | 2.13008 V | 2.59640 V |
| 010b | 2.13406 V | 2.60124 V |
| 011b | 2.13804 V | 2.60610 V |
| 100b | 2.14203 V | 2.61096 V |
| 101b | 2.14602 V | 2.61581 V |
| 110b | 2.14999 V | 2.62065 V |
| 111b | 2.15397 V | 2.62550 V |

(1) The actual $V_{REFby2}$ value may vary by ±10% from Table 26.

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### 7.6.3 Analog Input Configuration Registers

The device features following channel configuration registers, mapped as described in Table 20.

**Table 27. Analog Input Configuration Registers Mapping**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 024h | AIN_CFG | Analog input signal configuration selection |
| 027h | COM_CFG | AIN-COM pin configuration |

#### *7.6.3.1 AIN_CFG Register (address = 024h) [reset = 00h]*

This register configures the analog inputs as single-ended or pseudo-differential with or without common input.

**Figure 68. AIN_CFG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH7_CH6_CFG[1:0] | | CH5_CH4_CFG[1:0] | | CH3_CH2_CFG[1:0] | | CH1_CH0_CFG[1:0] | |
| R/W-00b | | R/W-00b | | R/W-00b | | R/W-00b | |

**Table 28. AIN_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | CH1_CH0_CFG[1:0] | R/W | 00b | 00b = AIN0 and AIN1 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation.<br>01b = AIN0 and AIN1 will be a single-ended pair. AIN0 will connect to MUXOUT-P and AIN1 will connect to MUXOUT-M.<br>10b = AIN0 and AIN1 will be a pseudo-differential pair. AIN0 will connect to MUXOUT-P and AIN1 will connect to MUXOUT-M.<br>11b = Same as 00b. AIN0 and AIN1 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation. |
| 5-4 | CH3_CH2_CFG[1:0] | R/W | 00b | 00b = AIN2 and AIN3 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation.<br>01b = AIN2 and AIN3 will be a single-ended pair. AIN2 will connect to MUXOUT-P and AIN3 will connect to MUXOUT-M.<br>10b = AIN2 and AIN3 will be a pseudo-differential pair. AIN2 will connect to MUXOUT-P and AIN3 will connect to MUXOUT-M.<br>11b = Same as 00b. AIN2 and AIN3 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation. |
| 3-2 | CH5_CH4_CFG[1:0] | R/W | 00b | 00b = AIN4 and AIN5 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation.<br>01b = AIN4 and AIN5 will be a single-ended pair. AIN4 will connect to MUXOUT-P and AIN5 will connect to MUXOUT-M.<br>10b = AIN4 and AIN5 will be a pseudo-differential pair. AIN4 will connect to MUXOUT-P and AIN5 will connect to MUXOUT-M.<br>11b = Same as 00b. AIN4 and AIN5 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation. |
| 1-0 | CH7_CH6_CFG[1:0] | R/W | 00b | 00b = AIN6 and AIN7 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation.<br>01b = AIN6 and AIN7 will be a single-ended pair. AIN6 will connect to MUXOUT-P and AIN7 will connect to MUXOUT-M.<br>10b = AIN6 and AIN7 will be a pseudo-differential pair. AIN6 will connect to MUXOUT-P and AIN7 will connect to MUXOUT-M.<br>11b = Same as 00b. AIN6 and AIN7 will be 2 separate channels. MUXOUT-M pin connected to AIN-COM pin. Refer to COM_CFG for selecting single-ended or pseudo-differential operation. |

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### 7.6.3.2 COM_CFG Register (address = 027h) [reset = 00h]

This register selects single-ended or pseudo-differential operation of analog input channels which are not configured as pairs (see the AIN_CFG register). Depending on the contents of this register, AIN-COM must be connected to either GND or REFby2 on the PCB.

**Figure 69. COM_CFG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | COM_CFG |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

**Table 29. COM_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 000 0000b | Reserved bits. Reads return 000 0000b. |
| 0 | COM_CFG | R/W | 0b | This bit selects the analog input channel configuration when = 00b or 11b in the AIN_CFG register:<br>0b = All individual channels are single-ended inputs. Connect AIN-COM pin to GND.<br>1b = All individual channels are pseudo differential inputs. Connect AIN-COM pin to REFby2. |

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### 7.6.4 Channel Sequence Configuration Registers Map

The device features following channel configuration registers, mapped as described in Table 30.

**Table 30. Channel Sequence Configuration Registers Mapping**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 01Ch | DEVICE_CFG | MUX sequence configuration and device status bits |
| 01Dh | CHANNEL_ID | Analog input channel selection in manual mode |
| 01Eh | SEQ_START | Control for starting the multiplexer sequence |
| 01Fh | SEQ_STOP | Control for aborting the multiplexer sequence |
| 02A | ON_THE_FLY_CFG | Enable/disable on-the-fly mode |
| 080h | AUTO_SEQ_CFG1 | Channel selection register for auto sequence mode |
| 082h | AUTO_SEQ_CFG2 | Control for repeating the channels in auto sequence mode |

#### *7.6.4.1 DEVICE_CFG Register (address = 01Ch) [reset = 00h]*

This register selects the mode of channel sequencing and reading this register returns device status information.

**Figure 70. DEVICE_CFG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | ALERT_STATUS | ERROR_STATUS | SEQ_MODE[1:0] | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-00b | |

**Table 31. DEVICE_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved bits. Do not write. Reads return 0000b. |
| 3 | ALERT_STATUS | R | 0b | Read only. This bit reflects the ALERT pin logic level. |
| 2 | ERROR_STATUS | R | 0b | Read only. Indicates device configuration error:<br>0b = No error.<br>1b = Error in configuration. |
| 1-0 | SEQ_MODE[1:0] | R/W | 00b | Sets the MUX channel selection operation:<br>00b = manual mode<br>01b = on-the-fly mode<br>10b = auto aequence mode<br>11b = custom channel sequencing mode |

The ALERT_STATUS, ERROR_STATUS and SEQ_MODE[1:0] bits can be collectively decoded to indicate events as shown in Table 32.

**Table 32. Decoding DEVICE_CFG Read Value**

| ALERT_STATUS | ERROR_STATUS | SEQ_MODE[1:0] | EVENT DESCRIPTION |
|---|---|---|---|
| 0 | 0 | 00 | No ALERT, no error, manual mode. |
| 0 | 0 | 01 | No ALERT, no error, on-the-fly mode. |
| 0 | 0 | 10 | No ALERT, no error, auto sequence mode. |
| 0 | 0 | 11 | No ALERT, no error, custom channel sequencing mode. |
| 0 | 1 | 00 | No ALERT, error, manual mode |
| 0 | 1 | 01 | No ALERT, error, on-the-fly mode |
| 0 | 1 | 10 | No ALERT, error, auto sequence mode |
| 0 | 1 | 11 | No ALERT, error, custom channel sequencing mode |
| 1 | 0 | 00 | ALERT, no error, manual mode |
| 1 | 0 | 01 | ALERT, no error, on-the-fly mode |
| 1 | 0 | 10 | ALERT, no error, auto sequence mode |
| 1 | 0 | 11 | ALERT, no error, custom channel sequencing mode |

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**Table 32. Decoding DEVICE_CFG Read Value (continued)**

| ALERT_STATUS | ERROR_STATUS | SEQ_MODE[1:0] | EVENT DESCRIPTION |
|---|---|---|---|
| 1 | 1 | 00 | ALERT, error, manual mode |
| 1 | 1 | 01 | ALERT, error, on-the-fly mode |
| 1 | 1 | 10 | ALERT, error, auto sequence mode |
| 1 | 1 | 11 | ALERT, error, custom channel sequencing mode |

### 7.6.4.2 CHANNEL_ID Register (address = 01Dh) [reset = 00h]

This register selects the analog input channel; see the *Manual Mode* section.

**Figure 71. CHANNEL_ID Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | CHANNEL_ID[2:0] | | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R/W-000b | | |

**Table 33. CHANNEL_ID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R | 0 0000b | Reserved bits. Reads return 0 0000b. |
| 2-0 | CHANNEL_ID[2:0] | R/W | 000b | These bits select the analog input channel as per Table 34. |

**Table 34. Analog input channel selection settings**

| CHANNEL_ID[2:0] | ANALOG INPUT SELECTED |
|---|---|
| 000b | AIN0 |
| 001b | AIN1 |
| 010b | AIN2 |
| 011b | AIN3 |
| 100b | AIN4 |
| 101b | AIN5 |
| 110b | AIN6 |
| 111b | AIN7 |

**NOTE**

Writing to the CHANNEL_ID register, when the device is actively operating in auto sequence mode or custom channel sequencing mode, aborts the on-going sequence and DEVICE_CFG is set to manual mode.

### 7.6.4.3 SEQ_START Register (address = 01Eh) [reset = 00h]

This register starts the channel selection sequence when in auto channel sequence mode or custom channel sequencing mode. Writing to this register has no effect when in manual mode or on-the-fly mode.

**Figure 72. SEQ_START Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEQ_START |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | W-0b |

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**Table 35. SEQ_START Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | - | - | Reserved bits. Do not write. |
| 0 | SEQ_START | W | 0b | This bit starts channel scanning sequence when SEQ_MODE[1:0] = auto channel sequence mode or custom channel sequencing mode.<br>0b = No effect. This does not stop an on-going sequence.<br>1b = Start channel sequence. |

### *7.6.4.4 SEQ_ABORT Register (address = 01Fh) [reset = 00h]*

This register stops the channel selection sequence when in auto channel sequence mode or custom channel sequencing mode. Writing to this register has no effect when in manual mode or on-the-fly mode.

**Figure 73. SEQ_ABORT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEQ_ABORT |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | W-0b |

**Table 36. SEQ_ABORT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | - | - | Reserved bits. Do not write. |
| 0 | SEQ_ABORT | W | 0b | This bit stops channel scanning sequence when SEQ_MODE[1:0] = auto channel sequence mode or custom channel sequencing mode.<br>0b = No effect.<br>1b = Stop channel sequence. |

### *7.6.4.5 ON_THE_FLY_CFG Register (address = 02Ah) [reset = 00h]*

This register enables on-the-fly mode mode of operation. This mode of operation helps in selecting analog input channels without having to write to device configuration registers.

**Figure 74. ON_THE_FLY_CFG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | EN_ON_THE_FLY |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

**Table 37. ON_THE_FLY_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 000 0000b | Reserved bits. Reads return 000 0000b. |
| 0 | EN_ON_THE_FLY | R/W | 0b | This bit enables the on-the-fly mode.<br>0b = On-the-fly mode disabled.<br>1b = On-the-fly mode enabled. First five bits on SDI select the analog input channel for next conversion, Figure 40. |

### *7.6.4.6 AUTO_SEQ_CFG1 Register (address = 080h) [reset = 00h]*

This register selects the channels enabled for auto channel sequence mode.

**Figure 75. AUTO_SEQ_CFG1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EN_AIN7 | EN_AIN6 | EN_AIN5 | EN_AIN4 | EN_AIN3 | EN_AIN2 | EN_AIN1 | EN_AIN0 |
| R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

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**Table 38. AUTO_SEQ_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | EN_AIN7 | R/W | 0b | Enable analog input channel 7 in the auto channel sequence mode, see the *Auto Sequence Mode* section.<br>0b = AIN7 not enabled in scanning sequence.<br>1b = AIN7 enabled in scanning sequence. |
| 6 | EN_AIN6 | R/W | 0b | Enable analog input channel 6 in the auto channel sequence mode.<br>0b = AIN6 not enabled in scanning sequence.<br>1b = AIN6 enabled in scanning sequence. |
| 5 | EN_AIN5 | R/W | 0b | Enable analog input channel 5 in the auto channel sequence mode.<br>0b = AIN5 not enabled in scanning sequence.<br>1b = AIN5 enabled in scanning sequence. |
| 4 | EN_AIN4 | R/W | 0b | Enable analog input channel 4 in the auto channel sequence mode.<br>0b = AIN4 not enabled in scanning sequence.<br>1b = AIN4 enabled in scanning sequence. |
| 3 | EN_AIN3 | R/W | 0b | Enable analog input channel 3 in the auto channel sequence mode.<br>0b = AIN3 not enabled in scanning sequence.<br>1b = AIN3 enabled in scanning sequence. |
| 2 | EN_AIN2 | R/W | 0b | Enable analog input channel 2 in the auto channel sequence mode.<br>0b = AIN2 not enabled in scanning sequence.<br>1b = AIN2 enabled in scanning sequence. |
| 1 | EN_AIN1 | R/W | 0b | Enable analog input channel 1 in the auto channel sequence mode.<br>0b = AIN1 not enabled in scanning sequence.<br>1b = AIN1 enabled in scanning sequence. |
| 0 | EN_AIN0 | R/W | 0b | Enable analog input channel 0 in the auto channel sequence mode.<br>0b = AIN0 not enabled in scanning sequence.<br>1b = AIN0 enabled in scanning sequence. |

### *7.6.4.7 AUTO_SEQ_CFG2 Register (address = 082h) [reset = 00h]*

This register enables sequence loop for auto channel sequence mode.

**Figure 76. AUTO_SEQ_CFG2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | AUTO_REPEAT |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

**Table 39. AUTO_SEQ_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 000 0000b | Reserved bits. Reads return 000 0000b. |
| 0 | AUTO_REPEAT | R/W | 0b | Enables looping the sequence indefinitely in auto channel sequence mode.<br>0b = Sequence will terminate after all enabled channels have been scanned.<br>1b = Sequence will repeat after scanning all enabled channels. |

### *7.6.4.8 Custom Channel Sequencing Mode Registers*

The device features following registers for custom channel sequencing mode, mapped as described in Table 20.

**Table 40. Custom Channel Sequencing Registers**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 088h | CCS_START_INDEX | Start index for custom channel sequencing mode sequence. |
| 089h | CCS_STOP_INDEX | End index for custom channel sequencing mode sequence. |
| 08Ah | CCS_SEQ_LOOP | custom channel sequencing mode loop control. |
| 08Ch | CCS_CHID_INDEX_0 | Channel ID configuration register index 0. |

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**Table 40. Custom Channel Sequencing Registers (continued)**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 08Dh | REPEAT_INDEX_0 | Repeat count register index 0. |
| 08Eh | CCS_CHID_INDEX_1 | Channel ID configuration register index 1. |
| 08Fh | REPEAT_INDEX_1 | Repeat count register index 1. |
| 090h | CCS_CHID_INDEX_2 | Channel ID configuration register index 2. |
| 091h | REPEAT_INDEX_2 | Repeat count register index 2. |
| 092h | CCS_CHID_INDEX_3 | Channel ID configuration register index 3. |
| 093h | REPEAT_INDEX_3 | Repeat count register index 3. |
| 094h | CCS_CHID_INDEX_4 | Channel ID configuration register index 4. |
| 095h | REPEAT_INDEX_4 | Repeat count register index 4. |
| 096h | CCS_CHID_INDEX_5 | Channel ID configuration register index 5. |
| 097h | REPEAT_INDEX_5 | Repeat count register index 5. |
| 098h | CCS_CHID_INDEX_6 | Channel ID configuration register index 6. |
| 099h | REPEAT_INDEX_6 | Repeat count register index 6. |
| 09Ah | CCS_CHID_INDEX_7 | Channel ID configuration register index 7. |
| 09Bh | REPEAT_INDEX_7 | Repeat count register index 7. |
| 09Ch | CCS_CHID_INDEX_8 | Channel ID configuration register index 8. |
| 09Dh | REPEAT_INDEX_8 | Repeat count register index 8. |
| 09Eh | CCS_CHID_INDEX_9 | Channel ID configuration register index 9. |
| 09Fh | REPEAT_INDEX_9 | Repeat count register index 9. |
| 0A0h | CCS_CHID_INDEX_10 | Channel ID configuration register index 10. |
| 0A1h | REPEAT_INDEX_10 | Repeat count register index 10. |
| 0A2h | CCS_CHID_INDEX_11 | Channel ID configuration register index 11. |
| 0A3h | REPEAT_INDEX_11 | Repeat count register index 11. |
| 0A4h | CCS_CHID_INDEX_12 | Channel ID configuration register index 12. |
| 0A5h | REPEAT_INDEX_12 | Repeat count register index 12. |
| 0A6h | CCS_CHID_INDEX_13 | Channel ID configuration register index 13. |
| 0A7h | REPEAT_INDEX_13 | Repeat count register index 13. |
| 0A8h | CCS_CHID_INDEX_14 | Channel ID configuration register index 14. |
| 0A9h | REPEAT_INDEX_14 | Repeat count register index 14. |
| 0AAh | CCS_CHID_INDEX_15 | Channel ID configuration register index 15. |
| 0ABh | REPEAT_INDEX_15 | Repeat count register index 15. |

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#### 7.6.4.8.1 CCS_START_INDEX Register (address = 088h) [reset = 00h]

This register sets the relative sequence index from which the custom channel sequencing mode starts execution.

**Figure 77. CCS_START_INDEX Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | SEQ_START_INDEX[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-0000b | | | |

**Table 41. CCS_START_INDEX Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved bits. Reads return 0000b. |
| 3-0 | SEQ_START_INDEX[3:0] | R/W | 0000b | Relative pointer to the index for start of sequencing in custom channel sequencing mode. |

#### 7.6.4.8.2 CCS_END_INDEX Register (address = 089h) [reset = 00h]

This register sets the relative sequence index where the lookup based sequencing mode stops execution. The value in the CCS_END_INDEX register must not be less than the value in CCS_START_INDEX.

**Figure 78. CCS_END_INDEX Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | SEQ_END_INDEX[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-0000b | | | |

**Table 42. CCS_END_INDEX Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved bits. Reads return 0000b. |
| 3-0 | SEQ_END_INDEX[3:0] | R/W | 0000b | Relative pointer to the index for end of sequence in lookup based sequencing mode. |

#### 7.6.4.8.3 CCS_SEQ_LOOP Register (address = 08Bh) [reset = 00h]

This register controls the looping of sequence in custom channel sequencing mode.

**Figure 79. CCS_SEQ_LOOP Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEQ_LOOP |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

**Table 43. CCS_SEQ_LOOP Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 000 0000b | Reserved bits. Reads return 000 0000b. |
| 0 | SEQ_LOOP | R/W | 0b | Configures the looping of sequence in custom channel sequencing mode.<br>0b = Sequence will end at index location configured in CCS_END_INDEX[3:0].<br>1b = Sequence will resume from CCS_START_INDEX[3:0] after executing CCS_END_INDEX[3:0]. |

#### 7.6.4.8.4 CCS_CHID_INDEX_m Registers (address = 08C, 08E, 090, 092, 094, 096, 098, 09A, 09C, 09E, 0A0, 0A2, 0A4, 0A6, 0A8, and 0AAh) [reset = 00h]

In custom channel sequencing mode, the intended sequence of analog input channels can be programmed in these 16 registers. Refer to REPEAT_INDEX_m for details about repeating a particular channel before switching to the next index.

**Figure 80. CCS_CHID_INDEX_m Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | CHID[2:0] | | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R/W-000b | | |

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**Table 44. CCS_CHID_INDEX_m Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R | 0 0000b | Reserved bits. Reads return 0 0000b. |
| 2-0 | CHID[2:0] | R/W | 000b | Configures the analog input channel associated with the index in custom channel sequencing mode.<br>000b = AIN0<br>001b = AIN1<br>010b = AIN2<br>011b = AIN3<br>100b = AIN4<br>101b = AIN5<br>110b = AIN6<br>111b = AIN7 |

#### 7.6.4.8.5 REPEAT_INDEX_m Registers (address = 08D, 08F, 091, 093, 095, 097, 099, 09B, 09D, 09F, 0A1, 0A3, 0A5, 0A7, 0A9, and 0ABh) [reset = 00h]

In custom channel sequencing mode, the analog input selected in corresponding CCS_CHID_INDEX can be repeated by configuring the respective registers.

**Figure 81. REPEAT_INDEX_m Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REPEAT[7:0] | | | | | | | |
| R/W-0000 0001b | | | | | | | |

**Table 45. REPEAT_INDEX_m Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | REPEAT[7:0] | R/W | 0000 0001b | Configures the number of times the analog input configured in corresponding CCS_CHID_INDEX are repeated. Configuring 0000 0000b in this register will result in error. |

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### 7.6.5 Digital Window Comparator Configuration Registers Map

The device features the following configuration registers for the digital window comparator, mapped as described in Table 46.

**Table 46. Digital Window Comparator Configuration Registers Mapping**

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|
| 02Eh | ALERT_CFG | ALERT enable control for individual analog input channels. |
| 031h and 030h | HI_TRIG_AIN7 | High threshold input for AIN7 digital window comparator. |
| 035h and 034h | HI_TRIG_AIN6 | High threshold input for AIN6 digital window comparator. |
| 039h and 038h | HI_TRIG_AIN5 | High threshold input for AIN5 digital window comparator. |
| 03Dh and 03Ch | HI_TRIG_AIN4 | High threshold input for AIN4 digital window comparator. |
| 041h and 040h | HI_TRIG_AIN3 | High threshold input for AIN3 digital window comparator. |
| 045h and 044h | HI_TRIG_AIN2 | High threshold input for AIN2 digital window comparator. |
| 049h and 048h | HI_TRIG_AIN1 | High threshold input for AIN1 digital window comparator. |
| 04Dh and 04Ch | HI_TRIG_AIN0 | High threshold input for AIN0 digital window comparator. |
| 055h and 054h | LO_TRIG_AIN7 | Low threshold input for AIN7 digital window comparator. |
| 059h and 058h | LO_TRIG_AIN6 | Low threshold input for AIN6 digital window comparator. |
| 05Dh and 05Ch | LO_TRIG_AIN5 | Low threshold input for AIN5 digital window comparator. |
| 061h and 060h | LO_TRIG_AIN4 | Low threshold input for AIN4 digital window comparator. |
| 065h and 064h | LO_TRIG_AIN3 | Low threshold input for AIN3 digital window comparator. |
| 069h and 068h | LO_TRIG_AIN2 | Low threshold input for AIN2 digital window comparator. |
| 06Dh and 06Ch | LO_TRIG_AIN1 | Low threshold input for AIN1 digital window comparator. |
| 071h and 070h | LO_TRIG_AIN0 | Low threshold input for AIN0 digital window comparator. |
| 033h | HYSTERESIS_AIN7 | Threshold hysteresis for AIN7 digital window comparator. |
| 037h | HYSTERESIS_AIN6 | Threshold hysteresis for AIN6 digital window comparator. |
| 03Bh | HYSTERESIS_AIN5 | Threshold hysteresis for AIN5 digital window comparator. |
| 03Fh | HYSTERESIS_AIN4 | Threshold hysteresis for AIN4 digital window comparator. |
| 043h | HYSTERESIS_AIN3 | Threshold hysteresis for AIN3 digital window comparator. |
| 047h | HYSTERESIS_AIN2 | Threshold hysteresis for AIN2 digital window comparator. |
| 04Bh | HYSTERESIS_AIN1 | Threshold hysteresis for AIN1 digital window comparator. |
| 04Fh | HYSTERESIS_AIN0 | Threshold hysteresis for AIN0 digital window comparator. |
| 078h | ALERT_STATUS | Indicates analog input channel-wise ALERT status. |
| 079h | ALERT_HI_STATUS | Indicates analog input channel-wise ALERT resulting from a high threshold. |
| 07Ah | ALERT_LO_STATUS | Indicates analog input channel-wise ALERT resulting from a low threshold. |
| 07Ch | CURR_ALARM_STATUS | Indicates analog input channel-wise ALERT status for the last conversion data. |
| 07Dh | CURR_ALERT_HI_STATUS | Indicates analog input channel-wise ALERT resulting from a high threshold for the last conversion data. |
| 07Eh | CURR_ALERT_LO_STATUS | Indicates analog input channel-wise ALERT resulting from a low threshold for the last conversion data. |

#### *7.6.5.1 ALERT_CFG Register (address = 02Eh) [reset = 00h]*

This register enables/disables the sigital window comparator for individual analog input channels.

**Figure 82. ALERT_CFG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_EN_AIN7 | ALERT_EN_AIN6 | ALERT_EN_AIN5 | ALERT_EN_AIN4 | ALERT_EN_AIN3 | ALERT_EN_AIN2 | ALERT_EN_AIN1 | ALERT_EN_AIN0 |
| R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

**Table 47. ALERT_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALERT_EN_AIN7 | R/W | 0b | Digital window comparator control for AIN7.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |
| 6 | ALERT_EN_AIN6 | R/W | 0b | Digital window comparator control for AIN6.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |
| 5 | ALERT_EN_AIN5 | R/W | 0b | Digital window comparator control for AIN5.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |
| 4 | ALERT_EN_AIN4 | R/W | 0b | Digital window comparator control for AIN4.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |
| 3 | ALERT_EN_AIN3 | R/W | 0b | Digital window comparator control for AIN3.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |
| 2 | ALERT_EN_AIN2 | R/W | 0b | Digital window comparator control for AIN2.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |
| 1 | ALERT_EN_AIN1 | R/W | 0b | Digital window comparator control for AIN1.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |
| 0 | ALERT_EN_AIN0 | R/W | 0b | Digital window comparator control for AIN0.<br>0b = Digital window comparator disabled.<br>1b = Digital window comparator enabled. |

When the digital window comparator is disabled, the bits corresponding to the disabled digital window comparator are not updated in the ALARM_STATUS, ALARM_HI_STATUS, ALARM_LO_STATUS, CURR_ALARM_STATUS, CURR_ALARM_HI_STATUS, and CURR_ALARM_LO_STATUS registers.

### *7.6.5.2 HI_TRIG_AINx[15:0] Register (address = 04Dh to 030h) [reset = 0000h]*

This bank of registers configures high threshold for digital window comparator. For 16-bit ADC data output, the comparator thresholds are 16-bits wide and spread over two 8-bit registers. High threshold can be configured for the analog input channels individually using the registers shown in Table 48.

**Table 48. Register Address Map For HI_TRIG_AINx[15:0](1)**

| ANALOG INPUT | REGISTER ADDRESS FOR HI_TRIG_AINx[15:8] | REGISTER ADDRESS FOR HI_TRIG_AINx[7:0] |
|---|---|---|
| AIN7 | 031h | 030h |
| AIN6 | 035h | 034h |
| AIN5 | 039h | 038h |
| AIN4 | 03Dh | 03Ch |
| AIN3 | 041h | 040h |
| AIN2 | 045h | 044h |
| AIN1 | 049h | 048h |
| AIN0 | 04Dh | 04Ch |

(1) AINx refers to analog inputs channels AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

**Figure 83. MSB Byte Register for HI_TRIG_AINx[15:8]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HI_TRIG[15:8] | | | | | | | |
| R/W-0000 0000b | | | | | | | |

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**Figure 84. LSB Byte Register for HI_TRIG_AINx[7:0]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HI_TRIG[7:0] | | | | | | | |
| R/W-0000 0000b | | | | | | | |

**Table 49. HI_TRIG_AINx[15:0] Registers Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | HI_TRIG[15:0] | R/W | 0000 0000 0000 0000b | High threshold for Digital Window Comparator. |

### *7.6.5.3 LO_TRIG_AINx[15:0] Register (address = 071h to 054h) [reset = 0000h]*

This bank of registers configures low threshold for digital window comparator. For 16-bit ADC data output, the comparator thresholds are 16-bits wide and are spread over 2 registers. Low threshold can be configured for the analog input channels individually using the registers shown in Table 50.

**Table 50. Register Address Map For LO_TRIG_AINx[15:0](1)**

| ANALOG INPUT | REGISTER ADDRESS FOR LO_TRIG_AINx[15:8] | REGISTER ADDRESS FOR LO_TRIG_AINx[7:0] |
|---|---|---|
| AIN7 | 051h | 054h |
| AIN6 | 059h | 058h |
| AIN5 | 05Dh | 05Ch |
| AIN4 | 061h | 060h |
| AIN3 | 065h | 064h |
| AIN2 | 069h | 068h |
| AIN1 | 06Dh | 06Ch |
| AIN0 | 071h | 070h |

(1) AINx refers to analog inputs channels AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

**Figure 85. MSB Byte Register for LO_TRIG_AINx[15:8]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LO_TRIG[15:8] | | | | | | | |
| R/W-0000 0000b | | | | | | | |

**Figure 86. LSB Byte Register for LO_TRIG_AINx[7:0]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LO_TRIG[7:0] | | | | | | | |
| R/W-0000 0000b | | | | | | | |

**Table 51. LO_TRIG_AINx[15:0] Registers Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | LO_TRIG[15:0] | R/W | 0000 0000 0000 0000b | Low threshold for Digital Window Comparator. |

### *7.6.5.4 HYSTERESIS_AINx[7:0] Register (address = 04Fh to 033h) [reset = 00h]*

This bank of registers configures hysteresis around high and low thresholds for digital window comparator. For 16-bit ADC data output, the hysteresis is 6-bit wide.

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**Figure 87. HYSTERESIS_AINx[7:0] Registers**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HYSTERESIS[5:0] | | | | | | 0 | 0 |
| R/W-00 0000b | | | | | | R-0b | R-0b |

**Table 52. HYSTERESIS_AINx[7:0](1) Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | HYSTERESIS[5:0] | R/W | 000 0000b | Low threshold for Digital Window Comparator. |

(1) AINx refers to analog inputs channels AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

### *7.6.5.5 ALERT_STATUS Register (address = 078h) [reset = 00h]*

This register reflects the ALERT status for the analog input channels.

**Figure 88. ALERT_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_AIN7 | ALERT_AIN6 | ALERT_AIN5 | ALERT_AIN4 | ALERT_AIN3 | ALERT_AIN2 | ALERT_AIN1 | ALERT_AIN0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b |

**Table 53. ALERT_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALERT_AIN7 | R | 0b | This bit indicates either high or low threshold for AIN7 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 6 | ALERT_AIN6 | R | 0b | This bit indicates either high or low threshold for AIN6 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 5 | ALERT_AIN5 | R | 0b | This bit indicates either high or low threshold for AIN5 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 4 | ALERT_AIN4 | R | 0b | This bit indicates either high or low threshold for AIN4 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 3 | ALERT_AIN3 | R | 0b | This bit indicates either high or low threshold for AIN3 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 2 | ALERT_AIN2 | R | 0b | This bit indicates either high or low threshold for AIN2 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 1 | ALERT_AIN1 | R | 0b | This bit indicates either high or low threshold for AIN1 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 0 | ALERT_AIN0 | R | 0b | This bit indicates either high or low threshold for AIN0 was exceeded.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |

If the ALERT bit for a particular channel is set in the ALERT_STATUS register, it can be cleared by writing 1b to the corresponding bit in the ALARM_HI_STATUS or ALARM_LO_STATUS registers. If both high and low thresholds were exceeded for a particular analog input channel, corresponding ALERT bit in both ALARM_HI_STATUS and ALARM_LO_STATUS registers must be set to 1b to clear the ALERT.

### *7.6.5.6 ALERT_HI_STATUS Register (address = 079h) [reset = 00h]*

This register reflects the status of ALERT due to high thresholds of the respective analog input channels.

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**Figure 89. ALERT_HI_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_HI_AIN 7 | ALERT_HI_AIN 6 | ALERT_HI_AIN 5 | ALERT_HI_AIN 4 | ALERT_HI_AIN 3 | ALERT_HI_AIN 2 | ALERT_HI_AIN 1 | ALERT_HI_AIN 0 |
| R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

**Table 54. ALERT_HI_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALERT_HI_AIN7 | R/W | 0b | This bit indicates high threshold for AIN7 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |
| 6 | ALERT_HI_AIN6 | R/W | 0b | This bit indicates high threshold for AIN6 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |
| 5 | ALERT_HI_AIN5 | R/W | 0b | This bit indicates high threshold for AIN5 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |
| 4 | ALERT_HI_AIN4 | R/W | 0b | This bit indicates high threshold for AIN4 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |
| 3 | ALERT_HI_AIN3 | R/W | 0b | This bit indicates high threshold for AIN3 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |
| 2 | ALERT_HI_AIN2 | R/W | 0b | This bit indicates high threshold for AIN2 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |
| 1 | ALERT_HI_AIN1 | R/W | 0b | This bit indicates high threshold for AIN1 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |
| 0 | ALERT_HI_AIN0 | R/W | 0b | This bit indicates high threshold for AIN0 was exceeded.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. This bit can be cleared by writing 1b to it. |

### *7.6.5.7 ALERT_LO_STATUS Register (address = 07Ah) [reset = 00h]*

This register reflects the status of ALERT due to low thresholds of the respective analog input channels.

**Figure 90. ALERT_LO_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_LO_AIN7 | ALERT_LO_AIN6 | ALERT_LO_AIN5 | ALERT_LO_AIN4 | ALERT_LO_AIN3 | ALERT_LO_AIN2 | ALERT_LO_AIN1 | ALERT_LO_AIN0 |
| R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

**Table 55. ALERT_LO_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALERT_LO_AIN7 | R/W | 0b | This bit indicates low threshold for AIN7 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |
| 6 | ALERT_LO_AIN6 | R/W | 0b | This bit indicates low threshold for AIN6 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |
| 5 | ALERT_LO_AIN5 | R/W | 0b | This bit indicates low threshold for AIN5 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |
| 4 | ALERT_LO_AIN4 | R/W | 0b | This bit indicates low threshold for AIN4 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |
| 3 | ALERT_LO_AIN3 | R/W | 0b | This bit indicates low threshold for AIN3 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |

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**Table 55. ALERT_LO_STATUS Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2 | ALERT_LO_AIN2 | R/W | 0b | This bit indicates low threshold for AIN2 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |
| 1 | ALERT_LO_AIN1 | R/W | 0b | This bit indicates low threshold for AIN1 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |
| 0 | ALERT_LO_AIN0 | R/W | 0b | This bit indicates low threshold for AIN0 was exceeded.<br>0b = Low threshold not exceeded.<br>1b = Low threshold exceeded. This bit can be cleared by writing 1b to it. |

### *7.6.5.8 CURR_ALERT_STATUS Register (address = 07Ch) [reset = 00h]*

This register reflects the ALERT status for the analog input channels. The bits in this register are updated after every conversion.

**Figure 91. CURR_ALERT_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_AIN7 | ALERT_AIN6 | ALERT_AIN5 | ALERT_AIN4 | ALERT_AIN3 | ALERT_AIN2 | ALERT_AIN1 | ALERT_AIN0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b |

**Table 56. CURR_ALERT_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALERT_AIN7 | R | 0b | This bit indicates either high or low threshold for AIN7 was exceeded by the last converted data from channel AIN7.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 6 | ALERT_AIN6 | R | 0b | This bit indicates either high or low threshold for AIN6 was exceeded by the last converted data from channel AIN6.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 5 | ALERT_AIN5 | R | 0b | This bit indicates either high or low threshold for AIN5 was exceeded by the last converted data from channel AIN5.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 4 | ALERT_AIN4 | R | 0b | This bit indicates either high or low threshold for AIN4 was exceeded by the last converted data from channel AIN4.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 3 | ALERT_AIN3 | R | 0b | This bit indicates either high or low threshold for AIN3 was exceeded by the last converted data from channel AIN3.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 2 | ALERT_AIN2 | R | 0b | This bit indicates either high or low threshold for AIN2 was exceeded by the last converted data from channel AIN2.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 1 | ALERT_AIN1 | R | 0b | This bit indicates either high or low threshold for AIN1 was exceeded by the last converted data from channel AIN1.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |
| 0 | ALERT_AIN0 | R | 0b | This bit indicates either high or low threshold for AIN0 was exceeded by the last converted data from channel AIN0.<br>0b = Both high threshold and low threshold not exceeded.<br>1b = High threshold or low threshold or both have been exceeded. |

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Bits in this register reflect the result of the logical OR of the corresponding channel bits in CURR_ALARM_HI_STATUS and CURR_ALARM_LO_STATUS. The status of individual bits in this register is evaluated after every conversion. The contents of this register can be used to ascertain if the last output data was within the specified high and low thresholds for the respective analog input channels.

### 7.6.5.9 CURR_ALERT_HI_STATUS Register (address = 07Dh) [reset = 00h]

This register reflects the high threshold ALERT status for the analog input channels. The bits in this register are updated after every conversion.

**Figure 92. CURR_ALERT_HI_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_HI_AIN7 | ALERT_HI_AIN6 | ALERT_HI_AIN5 | ALERT_HI_AIN4 | ALERT_HI_AIN3 | ALERT_HI_AIN2 | ALERT_HI_AIN1 | ALERT_HI_AIN0 |
| R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

**Table 57. CURR_ALERT_HI_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALERT_HI_AIN7 | R | 0b | This bit indicates high threshold for AIN7 was exceeded by the last converted data from channel AIN7.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |
| 6 | ALERT_HI_AIN6 | R | 0b | This bit indicates high threshold for AIN6 was exceeded by the last converted data from channel AIN6.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |
| 5 | ALERT_HI_AIN5 | R | 0b | This bit indicates high threshold for AIN5 was exceeded by the last converted data from channel AIN5.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |
| 4 | ALERT_HI_AIN4 | R | 0b | This bit indicates high threshold for AIN4 was exceeded by the last converted data from channel AIN4.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |
| 3 | ALERT_HI_AIN3 | R | 0b | This bit indicates high threshold for AIN3 was exceeded by the last converted data from channel AIN3.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |
| 2 | ALERT_HI_AIN2 | R | 0b | This bit indicates high threshold for AIN2 was exceeded by the last converted data from channel AIN2.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |
| 1 | ALERT_HI_AIN1 | R | 0b | This bit indicates high threshold for AIN1 was exceeded by the last converted data from channel AIN1.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |
| 0 | ALERT_HI_AIN0 | R | 0b | This bit indicates high threshold for AIN0 was exceeded by the last converted data from channel AIN0.<br>0b = High threshold not exceeded.<br>1b = High threshold exceeded. |

The status of individual bits in this register is evaluated after every conversion. The contents of this register can be used to ascertain if the last output data was within the specified high threshold for the respective analog input channels.

### 7.6.5.10 CURR_ALERT_LO_STATUS Register (address = 07Eh) [reset = 00h]

This register reflects the low threshold ALERT status for the analog input channels. The bits in this register are updated after every conversion.

**Figure 93. CURR_ALERT_LO_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_LO_AIN7 | ALERT_LO_AIN6 | ALERT_LO_AIN5 | ALERT_LO_AIN4 | ALERT_LO_AIN3 | ALERT_LO_AIN2 | ALERT_LO_AIN1 | ALERT_LO_AIN0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b |

**Table 58. CURR_ALERT_LO_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALERT_LO_AIN7 | R | 0b | This bit indicates low threshold for AIN7 was exceeded by the last converted data from channel AIN7.<br>0b = High threshold not exceeded.<br>1b = Low threshold exceeded. |
| 6 | ALERT_LO_AIN6 | R | 0b | This bit indicates low threshold for AIN6 was exceeded by the last converted data from channel AIN6.<br>0b = High threshold not exceeded.<br>1b = Low threshold exceeded. |
| 5 | ALERT_LO_AIN5 | R | 0b | This bit indicates low threshold for AIN5 was exceeded by the last converted data from channel AIN5.<br>0b = High threshold not exceeded.<br>1b = Low threshold exceeded. |
| 4 | ALERT_LO_AIN4 | R | 0b | This bit indicates low threshold for AIN4 was exceeded by the last converted data from channel AIN4.<br>0b = High threshold not exceeded.<br>1b = Low threshold exceeded. |
| 3 | ALERT_LO_AIN3 | R | 0b | This bit indicates low threshold for AIN3 was exceeded by the last converted data from channel AIN3.<br>0b = High threshold not exceeded.<br>1b = Low threshold exceeded. |
| 2 | ALERT_LO_AIN2 | R | 0b | This bit indicates low threshold for AIN2 was exceeded by the last converted data from channel AIN2.<br>0b = High threshold not exceeded.<br>1b = Low threshold exceeded. |
| 1 | ALERT_LO_AIN1 | R | 0b | This bit indicates low threshold for AIN1 was exceeded by the last converted data from channel AIN1.<br>0b = High threshold not exceeded.<br>1b = Low threshold exceeded. |
| 0 | ALERT_LO_AIN0 | R | 0b | This bit indicates low threshold for AIN0 was exceeded by the last converted data from channel AIN0.<br>0b = High threshold not exceeded.<br>1b = Low exceeded. |

The status of individual bits in this register is evaluated after every conversion. The contents of this register can be used to ascertain if the last output data was within the specified high threshold for the respective analog input channels.

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Multiplexer Input Connection

Conventional multi-channel ADC solutions internally connect the multiplexer output directly to the switched capacitor input of the ADC. In this case, a wide bandwidth amplifier is required for each channel, whereas the ADS8168 only requires one amplifier for many applications. The ADS8168 solution shown in Figure 94 has lower power, smaller PCB area, and lower cost compared to the comparative solution. Furthermore, from a calibration perspective, the offset error is the same in each channel and is set by the multiplexer output amplifier. The offset error in the conventional solution, on the other hand, is different for each channel. To calibrate the offset error for the conventional solution would require a separate calibration for each channel.

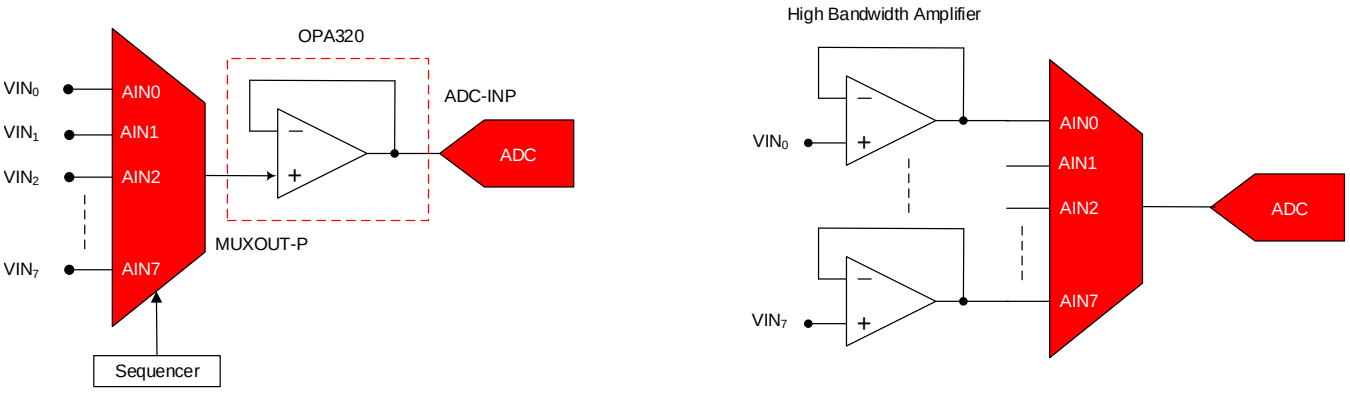



**Figure 94. Small Size and Low Power 8-Channel DAQ System Using the ADS8168**

When connecting the sensor directly to the input of the ADS8168, the maximum switching speed of the multiplexer is limited by multiplexer ON-resistance and parasitic capacitance. Figure 95 shows the source resistance ($R_{S0}$, $R_{S1}$…), multiplexer impedance ($R_{MUX}$), multiplexer capacitance ($C_{MUX}$), op amp input capacitance ($C_{OPA}$), and the stray PCB capacitance at the output of the multiplexer ($C_{STRAY}$). In this example, the total at the output capacitance is the combination of the multiplexer output capacitance, the op amp input capacitance and the stray capacitance ($C_{MUX}$ + $C_{OPA}$ + $C_{STRAY}$) = 15 pF. When switching to a channel, this capacitance needs to be charged to the sensor output voltage via the source resistance and the multiplexer resistance ($R_{S0}$ + $R_{MUX}$).

Equation 2 can be used to estimate the number of time constants required for N-bits of settling. For this example, to achieve 16-bit settling, 11.09 time constants are required. Thus, for channel 0 the required settling time is 167-ns, as computed in Equation 3 and Equation 4.

$$N_{TC} = \ln(2^{16}) = 11.09 \quad (2)$$

$$\text{Settling time required} = (R_{S0} + R_{MUX}) \times (C_{MUX} + C_{OPA} + C_{STRAY}) \times N_{TC} \quad (3)$$

$$\text{Settling time required} = (1k\Omega) \times (15pF) \times 11.09 = 167ns \quad (4)$$

ADVANCE INFORMATION

## Application Information (continued)

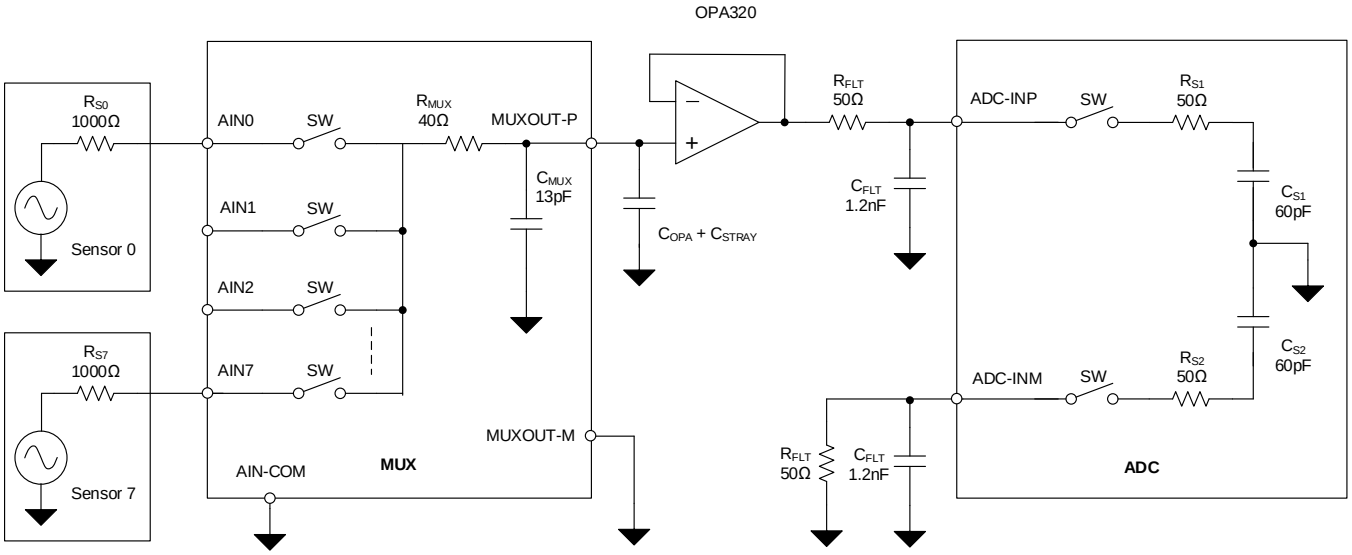



**Figure 95. Direct Sensor Interface With ADS8168 in an 8-Channel, Single-Ended Configuration**

When operating at 1-MSPS in either manual mode, auto channel sequence mode, or custom channel sequencing mode, 900-ns settling time is available at the analog inputs of the multiplexer as shown in Early Switching for Direct Sensor Interface. Using Equation 4, the maximum sensor output impedance for direct connection is 5.4-kΩ.

In some applications, such as temperature sensing, the sensor output impedance can be greater than 10-kΩ. When scanning the multiplexer channels at high throughput, the relatively higher driving impedance results in settling error. In such cases, the multiplexer inputs can be driven using an amplifier as shown in Figure 96. The multiplexer outputs can be connected to ADC inputs directly. For best distortion performance, an amplifier can be used between multiplexer and ADC as described in Selecting ADC Input Buffer.

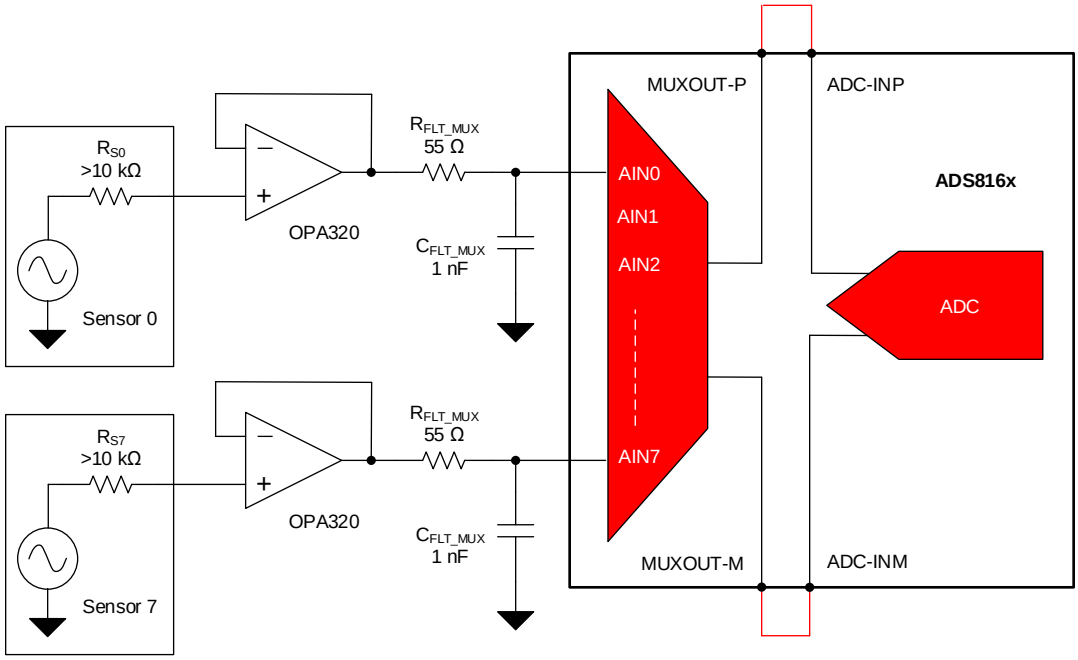



**Figure 96. High Output Impedance Sensor Interface**

ADVANCE INFORMATION

## Application Information (continued)

### 8.1.2 Selecting ADC Input Buffer

Figure 97 shows the external amplifier, charge bucket filter, and sample-and-hold circuit at the ADC input for the ADS816. To understand the design procedure for selecting the amplifier and RC filter, it is helpful to have a short background on the conversion process. The conversion process is broken up into two phases: the acquisition phase and the conversion phase. During the acquisition phase the switches SW are closed, and the input signal is stored on the sample and hold capacitors, $C_{S1}$ and $C_{S2}$. After the acquisition phase, the switches will open and the voltage stored on the capacitors is converted to digital code by the SAR algorithm. This conversion process will deplete the charge on the sample and hold capacitors.

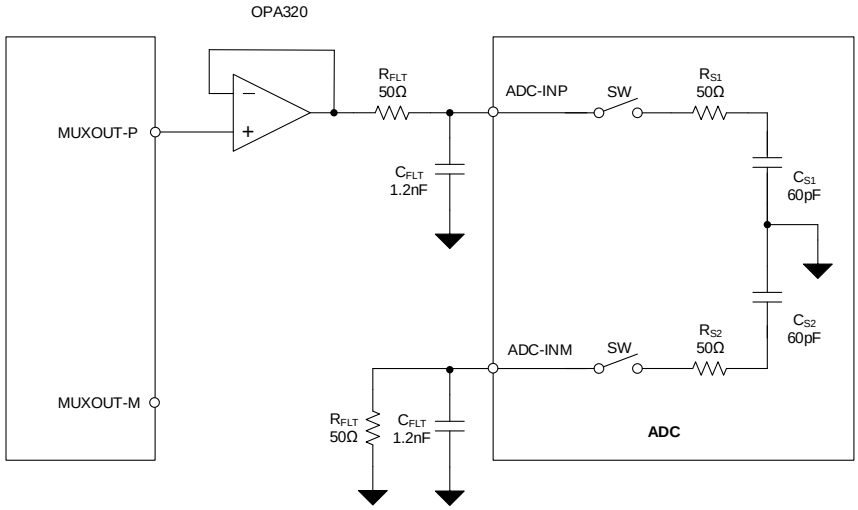



**Figure 97. Driving ADC Inputs (ADC-INP and ADC-INM)**

During subsequent acquisition cycles, the sample and hold capacitor will have to be charged to ADC input voltage which may make step changes in value as each input may be from a different multiplexer channel. For example, if AIN0 is connected to 4 V and AIN1 is connected to 0.5 V, the sample and hold will have to charge to 4-V for the first acquisition cycle and 0.5 V for the second acquisition cycle. When running at high throughput, the acquisition time will be small and a wide bandwidth amplifier is required for proper settling at ADC inputs (minimum acquisition time for ADS8168 is $t_{ACQ}$ = 330 ns). The RC filter ($R_{FLT}$ and $C_{FLT}$) is designed to provide a reservoir of charge that will help charge the internal sample and hold capacitor rapidly at the start of the acquisition period. For this reason, the RC filter is sometimes called a “charge bucket” or “charge kickback” filter. In this section we will provide a method for determining the required amplifier bandwidth and the values of the RC charge bucket filter.

A summary of the equations and an example calculation is provided to determine the amplifier bandwidth and RC charge bucket circuit for the ADS8168 assuming minimum ADC acquisition time. Equation 8 finds the amplifier time constant and Equation 9 uses this to computer the amplifiers required unity gain bandwidth.

$$C_{SH} = 60pF, t_{ACQ} = 330ns, N = 16bits, V_{REF} = 4.096V \quad (5)$$

$$LSB = \frac{V_{REF}}{2^N} = \frac{4.096V}{2^{16}} = 62.5\mu V \quad (6)$$

$$\tau_C = \frac{-t_{ACQ}}{\ln\left(\frac{0.5 \times LSB}{100mV}\right)} = \frac{-330ns}{\ln\left(\frac{0.5 \times (62.5\mu V)}{100mV}\right)} = 40.9ns \quad (7)$$

$$\tau_{AMP} = \frac{\tau_C}{\sqrt{17}} = \frac{40.9ns}{\sqrt{17}} = 9.917ns \quad (8)$$

$$UGBW = \frac{1}{2\pi \times \tau_{AMP}} = \frac{1}{2\pi \times (9.917ns)} = 16MHz \quad (9)$$

ADVANCE INFORMATION

## Application Information (continued)

The value of $C_{FLT}$ is computed in Equation 10 by taking twenty times the internal sample and hold capacitance. The factor of twenty is a rule of thumb that is intended to minimize the droop in voltage on the charge bucket capacitor, $C_{FLT}$, after the start of the acquisition period. The filter resistor, $R_{FLT}$, is computed in Equation 11 using the op amp time constant and $C_{FLT}$. Note that these equations model the system as a first order system, and in reality the system is a higher order. Consequently, the values may need to be adjusted to optimize performance. This optimization and more details on the math behind the component selection are covered in ADC Precision Labs.

$$C_{FLT} = 20 \times C_{FLT} = 20 \times (60pF) = 1.2nF \quad (10)$$

$$R_{FLT} = \frac{4 \times \tau_{AMP}}{C_{FLT}} = \frac{4 \times (9.917ns)}{1.2nF} = 33.05\Omega \quad (11)$$

## 8.2 Typical Applications

### 8.2.1 1-MSPS DAQ Circuit With Lowest Distortion and Noise Performance

An 8-channel and 1-MSPS solution with minimum external components is shown in Figure 98. This solution significantly reduces solution size and power by not requiring amplifiers on every analog input.

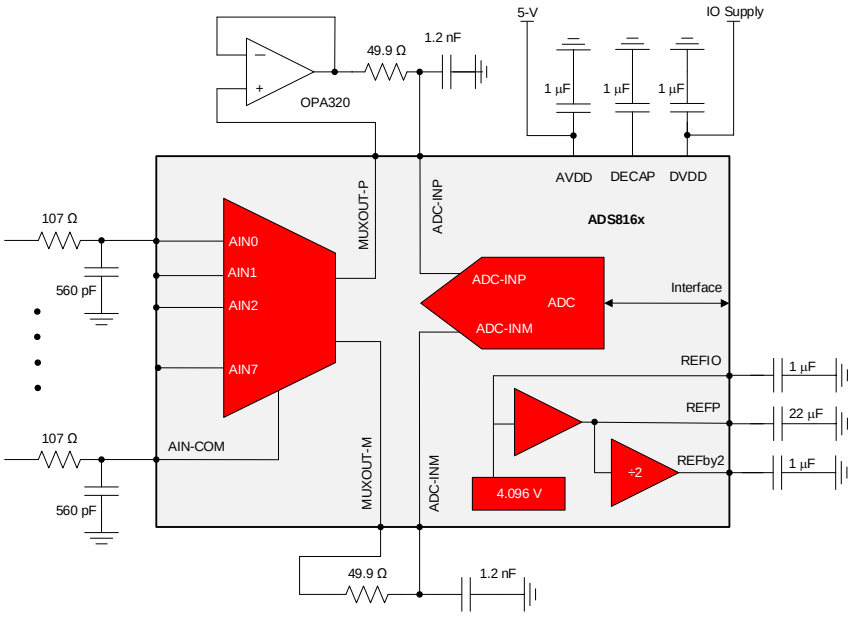



**Figure 98. 1-MSPS DAQ Circuit With Lowest Distortion and Noise Performance**

#### *8.2.1.1 Design Requirements*

For this example, the design parameters are listed in Table 59.

**Table 59. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| SNR | ≥ 92-dB |
| THD | ≤ -108-dB |
| Throughput | 1-MSPS |
| Input signal frequency | ≤100-kSPS |

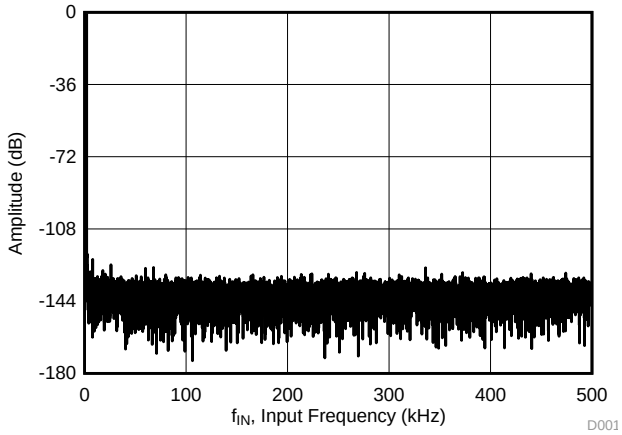
ADVANCE INFORMATION

#### 8.2.1.2 Detailed Design Procedure

The general design procedure below can be used for any ADS8168 application circuit. The final design for this example is shown in Example Schematic.

- All ADS8168 applications require the supply and reference decoupling as given in the *Example Schematic* and *Layout* sections.
- Select the buffer amplifier and associated charge bucket filter between the multiplexer output and ADC input using the method described in the Selecting ADC Input Buffer. The values given in this section meet the maximum throughput and input signal frequency design requirements given. A lower bandwidth solution could be used in cases where lower power is required.
- Select an input amplifier for rapid settling when the multiplexer switches channels. This selection is covered in the Multiplexer Input Connection. The OPA320 buffer and associated RC filter shown in Figure 96 meet these requirements.

#### 8.2.1.3 Application Curve




$f_{IN}$ = 2 kHz, 92-dB SNR, –109-dB THD

**Figure 99. FFT Plot: ADS8168**

### 8.2.2 8-Channel Photodiode Detector With Smallest Size and Lowest Number of Components

The circuit in Figure 100 shows an 8-channel photodiode detector using the ADS8168. In this example, one common amplifier is used for eight photodiodes. A detailed description of the transimpedance amplifier is given in TI Precision Designs.

ADVANCE INFORMATION

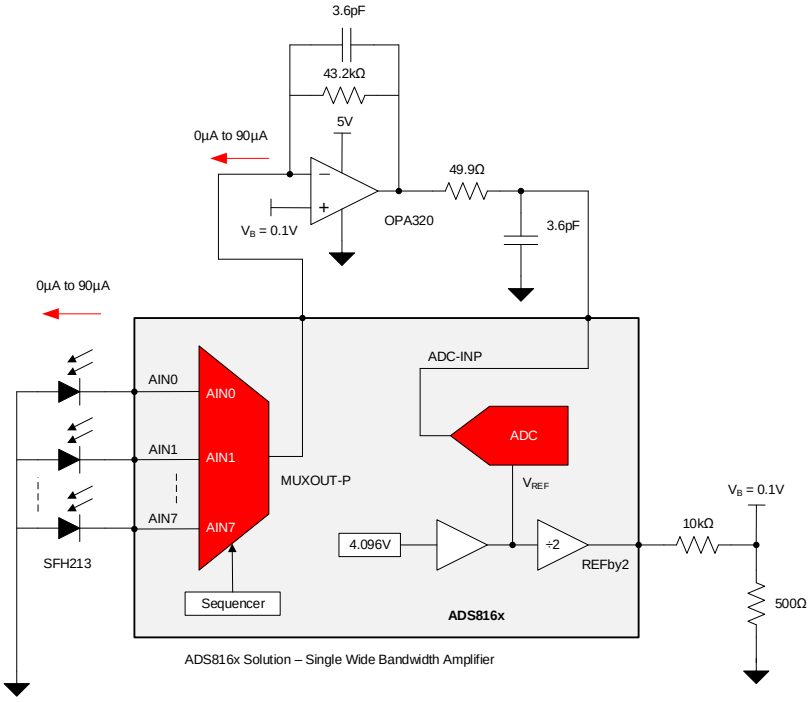



**Figure 100. Small Size, 8-channel Photo Detector**

### 8.2.2.1 Design Requirements

The objective of this design is to achieve:

- Smallest solution size.
- Transimpedance output of 0.1-V to 4-V for a 0-µA to 90-µA input with a bandwidth of 1-MHz.
- The voltage divider is designed to provide a minimum amplifier output of 0.1-V when the photodiode current is zero (dark current). This prevents the amplifier from saturating to the negative rail.

### 8.2.2.2 Detailed Design Procedure

In Figure 100, the photodiodes are connected to the multiplexer input in photovoltaic mode. Depending on the application requirements, either photovoltaic mode or photoconductive mode can be used. The multiplexer in the ADS8168 is used as a current multiplexer in this example. One common amplifier for all photodiodes reduces cost, complexity, PCB area, and power consumption. It also simplifies system calibration as the gain and offset error is the same for all channels. Finally, the low leakage current of the multiplexer is ideal for photodiode applications

OPA320 is used as a transimpedance amplifier that can also drive the ADC inputs. In order to set the output voltage of OPA320 to 0.1-V in dark conditions, an equivalent bias voltage ($V_B$) is applied at the non-inverting terminal. This bias voltage is derived using a resistive voltage divider on REFby2 output (2.048V), as shown in Equation 12.

$$V_B = (V_{REFby2} V) \times \left( \frac{500\Omega}{10k\Omega + 500\Omega} \right) = 97.5mV \quad (12)$$

The feedback resistor for the transimpedance amplifier can be selected by designing for 4-V output for a 90-µA input, as shown in Equation 13.

$$R_F = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{I_{IN\_MAX}} = \frac{4V - 0.1V}{90\mu A} = 43.3k\Omega \quad (13)$$

Equation 14 computed the value of feedback capacitance to limit the bandwidth of transimpedance circuit to 1-MHz.

ADVANCE INFORMATION

$$C_F = \frac{1}{2\pi \times f_C \times R_F} = \frac{1}{2\pi \times (1\text{MHz}) \times (43.3\text{k}\Omega)} = 3.6\text{pF} \quad (14)$$

Transimpedance amplifiers can have potential stability concerns. Stability is a function of the feedback capacitance, the capacitance on the inverting input of the amplifier, and the amplifier gain bandwidth. In this case the capacitance on the inverting amplifier input ($C_{IN}$) includes, Equation 15, the photodiode junction capacitance ($C_J$), the multiplexer capacitance ($C_{MUX}$), the trace capacitance, and the op amp input differential ($C_D$) and common-mode ($C_{CM2}$) capacitances. Minimum gain bandwidth of the amplifier for stability given CIN can be computed by Equation 17. The minimum required gain bandwidth is 10.9MHz and the gain bandwidth for the OPA320 is 20MHz, so the stability test passes.

$$C_{IN} = C_J + C_D + C_{CM2} + C_{MUX} \quad (15)$$

$$C_{IN} = 11\text{pF} + 5\text{pF} + 4\text{pF} + 15\text{pF} = 35\text{pF} \quad (16)$$

$$F_{GBW} > \frac{C_{IN} + C_F}{2\pi \times R_F \times (C_F)^2} \quad (17)$$

$$F_{GBW} > \frac{35\text{pF} + 3.6\text{pF}}{2\pi \times 43.3\text{k}\Omega \times (3.6\text{pF})^2} = 10.9\text{MHz} \quad (18)$$

### 8.2.3 1-MSPS DAQ Circuit for Factory Automation

The circuit in Figure 8 shows an example of how the ADS8168 can be used for a factory automation application.

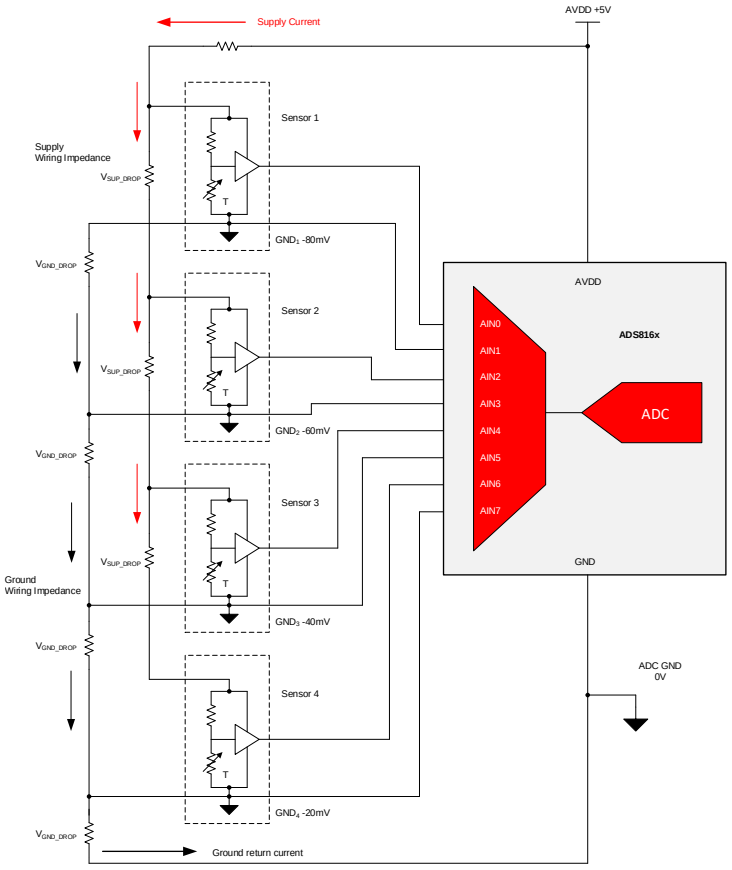



**Figure 101. Remote Ground Sense With the ADS8168 in Factory Automation**

#### *8.2.3.1 Design Requirements*

The goal of this design to sense outputs from four sensors, each sensor being at different ground potentials.

#### 8.2.3.2 Detailed Design Procedure

In Figure 101, the sensors are connected over long leads to the supply, ground, and ADC inputs. Voltage drop due to ground wiring impedance will cause the ground connections to be at different potentials for each sensor. The ADS8168 can be configured into four single-ended pairs with remote ground sense as described in Multiplexer Configurations. In this input configuration, the error in ground potential is sensed and accounted for in the measurement.

The ADC negative input can sense ground voltages of ±100-mV. The ADC has digital window comparators that can be programed to set an alarm if the sensor output is out of range. Many industrial applications require isolation. When scanning all the channels at 1Msps, the serial clock rate can be as low as 16-MHz. This clock rate is suitable for most isolators. Using a common amplifier to drive the ADC input simplifies calibration as all channels have a common error.

## 9 Power Supply Recommendations

The ADS8168 has two separate power supplies: AVDD and DVDD. The internal reference, reference buffer, multiplexer and the internal LDO operate on AVDD. The ADC core operates on the LDO output (available on the DECAP pin). DVDD is used for the setting the logic levels on digital interface. AVDD and DVDD can be independently set to any value within their permissible ranges. During normal operation, if voltage on AVDD supply drops below AVDD minimum specification, it is recommended to ramp AVDD supply down to ≤ 0.7-V before power-up. Also, during power-up, AVDD must monotonously rise to desired operating voltage above minimum AVDD specification.

When using internal reference, set AVDD so that:

$$4.5\text{-V} \le \text{AVDD} \le 5.5\text{-V} \quad (19)$$

The AVDD supply voltage value defines the permissible range for the external reference voltage $V_{REF}$ on REFIO pin as:

$$2.5\text{-V} \le V_{REF} \le (\text{AVDD} - 0.3)\ \text{V} \quad (20)$$

In other words, to use the external reference voltage of $V_{REF}$, set AVDD so that:

$$3\text{-V} \le \text{AVDD} \le (\text{AVDD} + 0.3)\ \text{V} \quad (21)$$

Place minimum 1-µF decoupling capacitor between the RVDD and GND pins, and between the DVDD and GND pins, as shown in Figure 102. Use minimum 1-µF decoupling capacitor between the DECAP pins and the GND pin.

There are no specific requirements with regard to the power-supply sequencing of the device. However, issue a reset after the supplies are powered and are stable to ensure the device is properly configured.

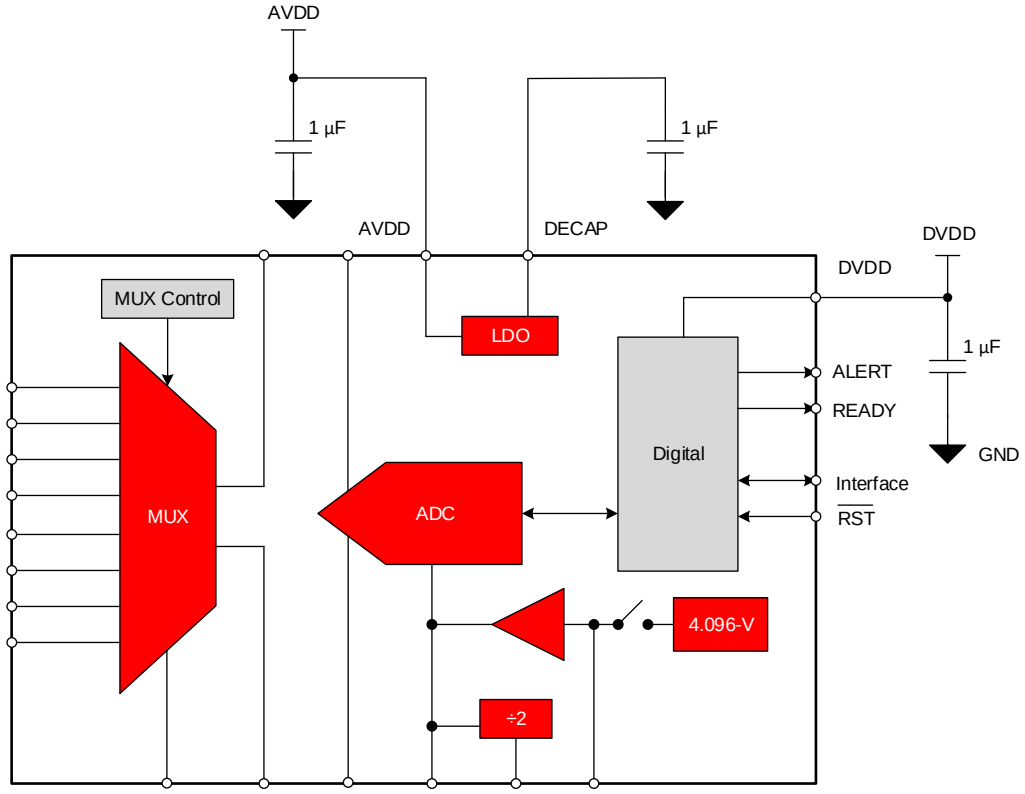



**Figure 102. Power-Supply Decoupling**

ADVANCE INFORMATION

# 10 Layout

## 10.1 Layout Guidelines

This section provides some layout guidelines for achieving optimum performance with the ADS8168.

### 10.1.1 Analog Signal Path

As illustrated in Figure 103, the analog input signals are routed in opposite directions to the digital connections. The reference decoupling components are kept away from the switching digital signals. This arrangement prevents noise generated by digital switching activity from coupling to sensitive analog signals.

### 10.1.2 Grounding and PCB Stack-Up

Low inductance grounding is critical for achieving optimum performance. Place all critical components of the signal chain on the same PCB layer as the ADS816x.

For lowest inductance grounding, connect the GND pins of the ADS816x (pins 1, 21, and 31) and reference ground REFM (pin 4) directly to the device thermal pad. Connect the device thermal pad to PCB ground using four vias, as shown in Figure 103.

### 10.1.3 Decoupling of Power Supplies

Use wide traces or a dedicated power supply plane to minimize trace inductance. Place 1-µF, X7R grade, ceramic decoupling capacitors in close proximity on AVDD (pin 32), the DECAP (pin 2), DVDD (pin 30), and REFby2 (pin 7). Avoid placing vias between any supply pin and the respective decoupling capacitor.

### 10.1.4 Reference Decoupling

When using the internal reference, as discussed in External Reference, the REFIO (pin 3) should have a 1-µF, X7R-grade, ceramic capacitor with at least 10-V rating. This capacitor must be placed close to the REFIO pin, as illustrated in Figure 103. In cases where external reference is used, refer to the reference datasheet for filtering capacitor requirements.

### 10.1.5 Reference Buffer Decoupling

Dynamic currents are present at the REFP and REFM pins during the conversion phase, and excellent decoupling is required to achieve optimum performance. Place a 22-µF, X7R-grade, ceramic capacitor with at least 10-V rating between the REFP and the REFM pins, as illustrated in Figure 103. Select 0603- or 0805-size capacitors to keep equivalent series inductance (ESL) low. Connect the REFM pins to the decoupling capacitor before a ground via.

### 10.1.6 Multiplexer Input Decoupling

Minimizing channel-to-channel parasitic capacitance will reduce the cross-talk induced on the PCB. This can be achieved by increasing the spacing between the analog traces to multiplexer input.

In Figure 103, each multiplexer input has a RC filter. Use C0G- or NPO-type capacitors in the RC filter. The purpose of this filter is to aid in settling when switching between multiplexer channels. When not switching the multiplexer, as discussed in Figure 39 and Figure 40, the RC filter may be omitted.

### 10.1.7 ADC Input Decoupling

Dynamic currents are also present at the ADC analog inputs of the ADS816x (pins 18 and 19). Use C0G- or NPO-type capacitors to decouple these inputs. With these type of capacitors, capacitance stays almost constant over the full input voltage range. Lower-quality capacitors (such as X5R and X7R) have large capacitance changes over the full input-voltage range that may cause degradation in the performance of the device.

In Figure 103, each multiplexer input has a RC filter. The purpose of this filter is to aid in settling when switching between multiplexer channels. When not switching the multiplexer, as discussed in Figure 39 and Figure 40, the RC filter may be omitted.

ADVANCE INFORMATION

## 10.2 Layout Example

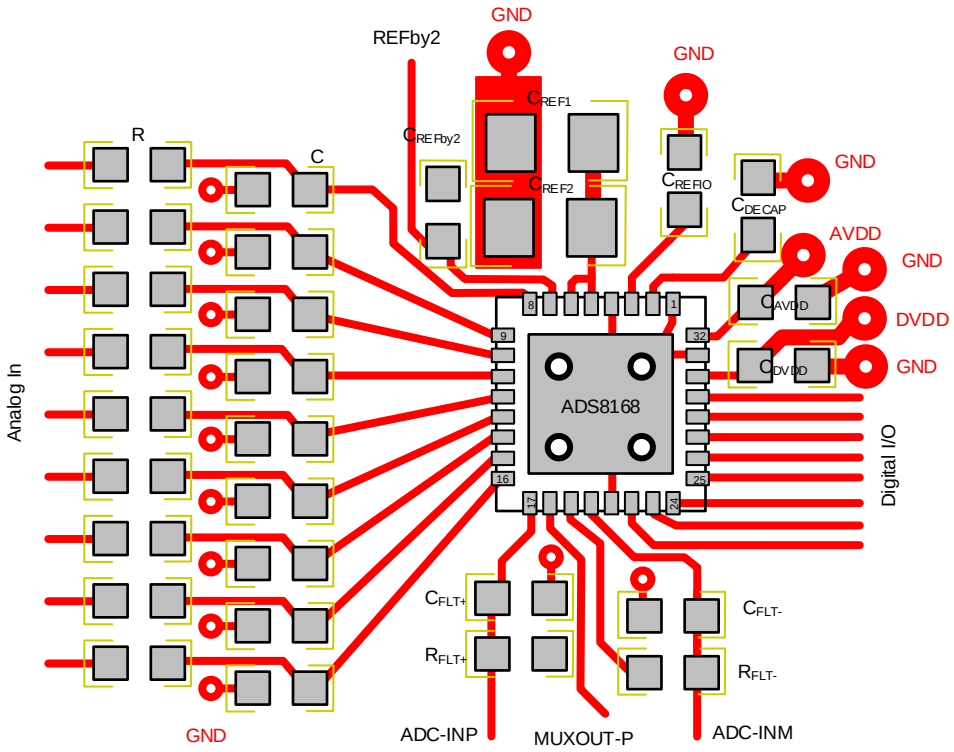



**Figure 103. Recommended Layout**

ADVANCE INFORMATION

## Layout Example (continued)

### 10.2.1 Example Schematic

The schematic for Layout Example is shown in Figure 104.

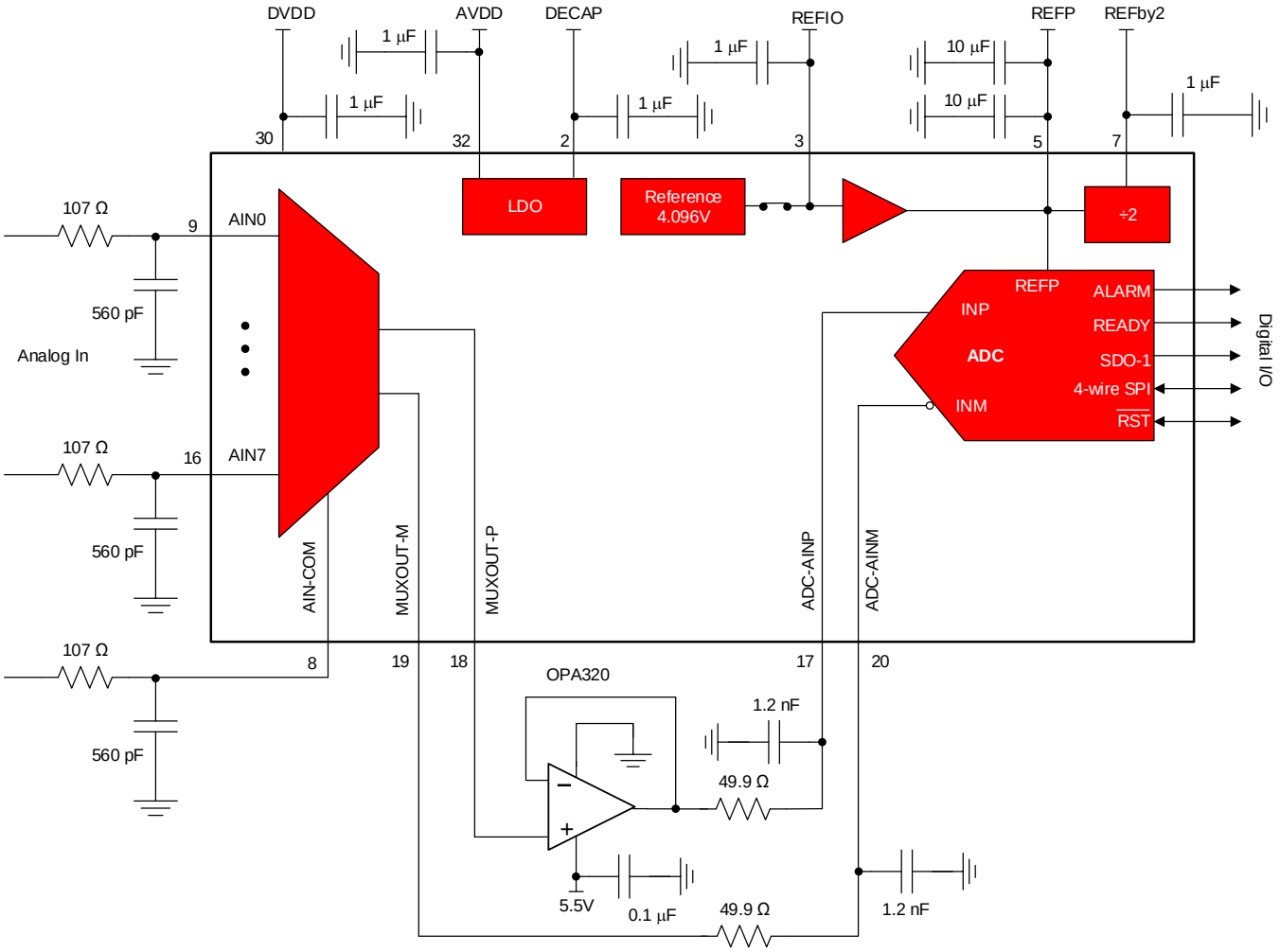



**Figure 104. Example Schematic Used in the Recommended Layout**

ADVANCE INFORMATION

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

- *16-Bit 1-MSPS Data Acquisition Reference Design for Single-Ended Multiplexed Applications*
- *OPAx625 High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers Data Sheet*
- *THS4551 Low Noise, Precision, 150MHz, Fully Differential Amplifier*

## 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 60. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| ADS8166 | Click here | Click here | Click here | Click here | Click here |
| ADS8168 | Click here | Click here | Click here | Click here | Click here |

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

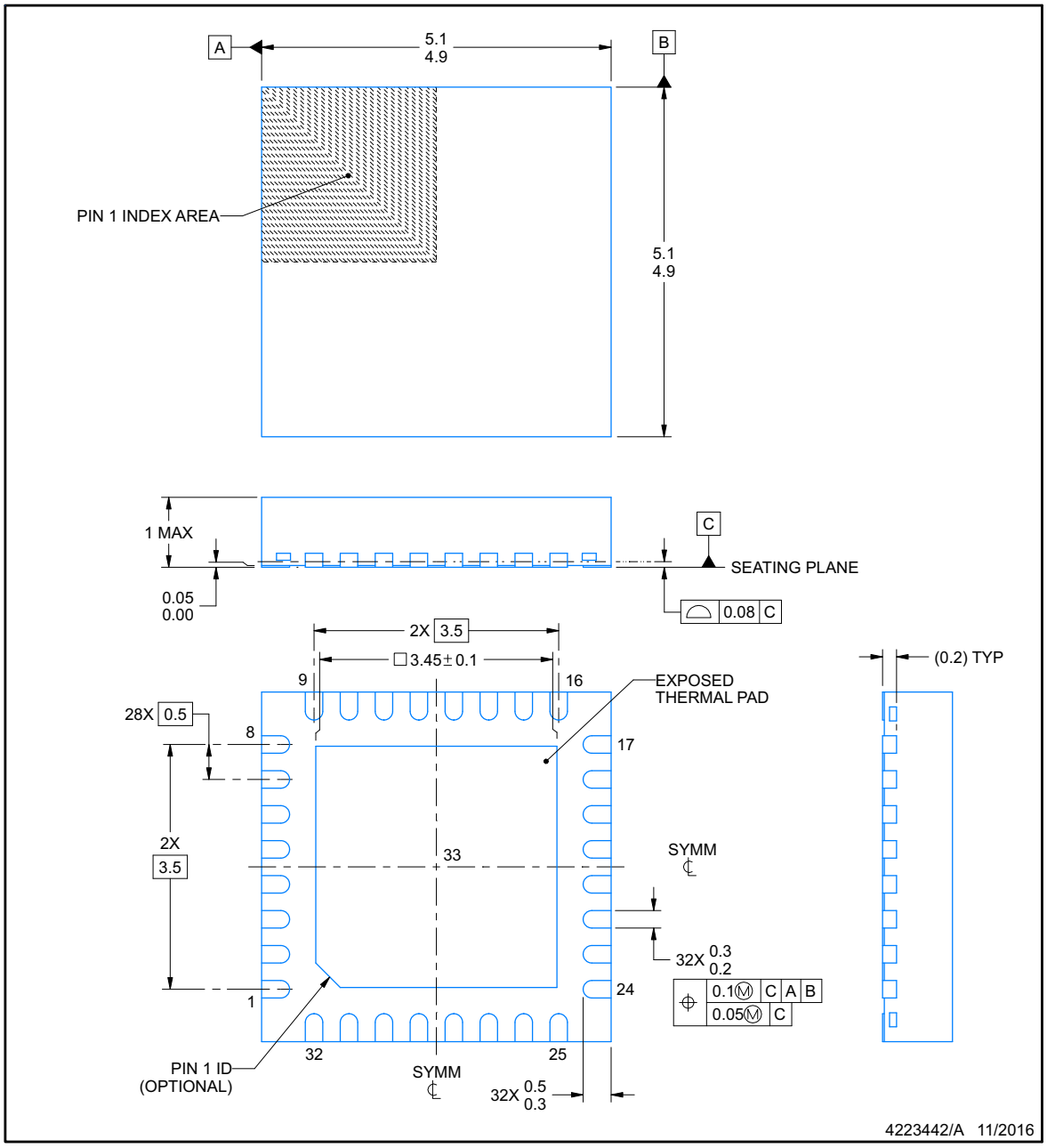
ADVANCE INFORMATION

# RHB0032E

## PACKAGE OUTLINE

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



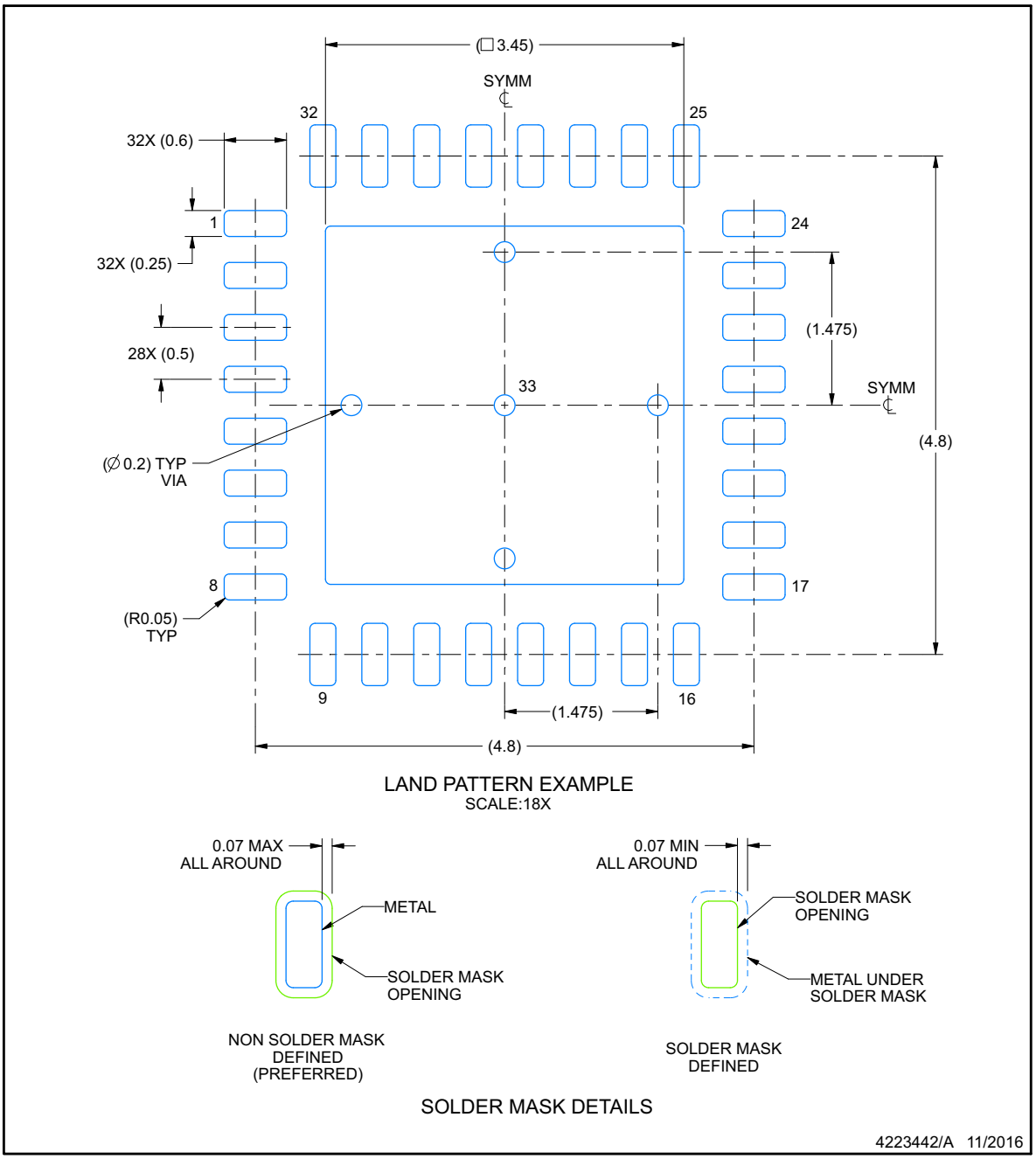

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**RHB0032E** — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

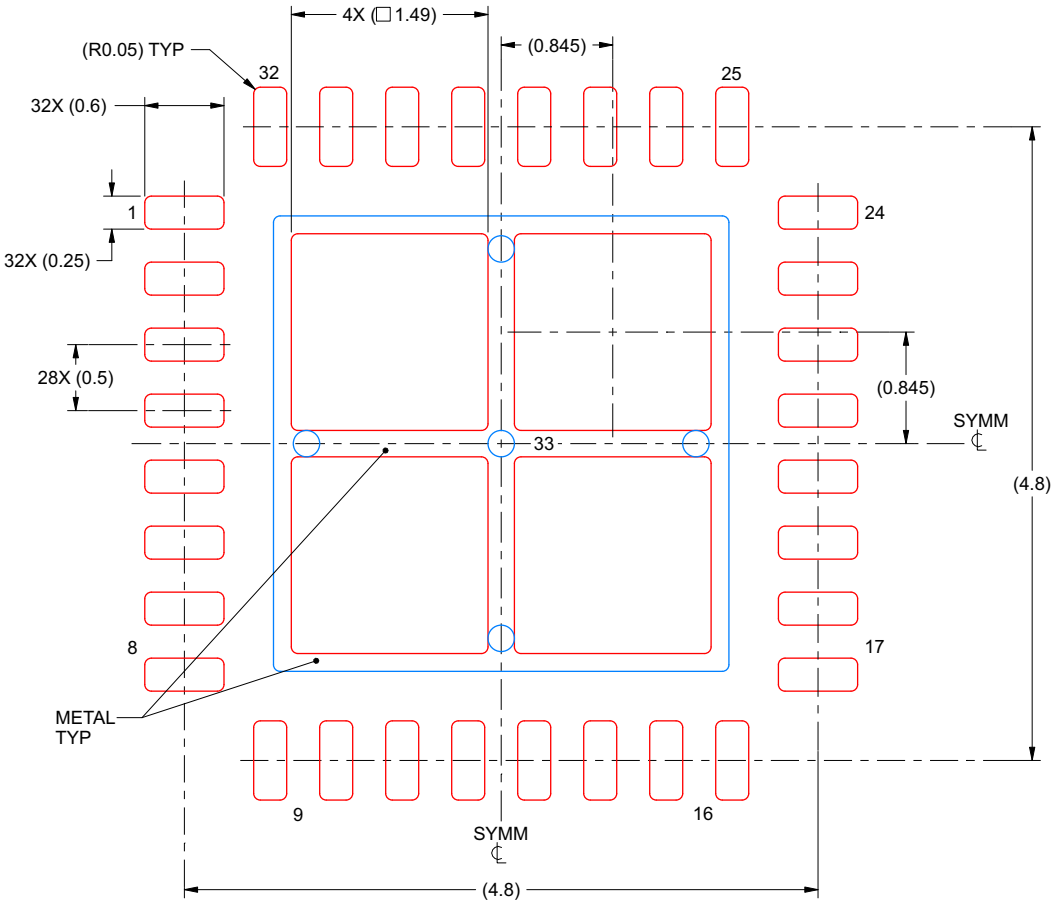
ADVANCE INFORMATION

ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

**RHB0032E** — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8166IRHBR | PREVIEW | VQFN | RHB | 32 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ADS8166IRHBT | PREVIEW | VQFN | RHB | 32 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| ADS8168IRHBR | PREVIEW | VQFN | RHB | 32 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ADS8168IRHBT | PREVIEW | VQFN | RHB | 32 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| XADS8166IRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| XADS8168IRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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