DDR Termination Regulator TJ2995

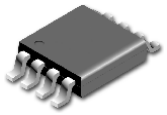
FEATURES

- Low Output Voltage Offset
- Works with +5V, +3.3V, and 2.5V Rails
- Source and Sink Current
- Low External Component Count
- No External Resistors Required
- Linear Topology
- Available in SOP8, SOP8-PP Package
- Low Cost and Easy to Use

APPLICATION

- DDR-I and DDR-II Termination Voltage
- SSTL-2 and SSTL-3 Termination

SOP8 / SOP8-PP PKG



ORDERING INFORMATION

Device (Marking)	Package
TJ2995D	SOP8
TJ2995DP	SOP8-PP

DESCRIPSION

The TJ2995 linear regulator is designed to meet the JEDEC SSTL-2 and SSTL-3 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transient. This device can deliver 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. With an independent V_{SENSE} pin, the TJ2995 can provide superior load regulation. The TJ2995 provides a V_{REF} output as the reference for the chipset and DDR DIMMS. The TJ2995 can easily provide the accurate V_{TT} and V_{REF} voltages without external resistors that PCB areas can be reduced. The quiescent current is low to meet the low power consumption applications.

Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage to GND	PV_{IN} AV_{IN} V_{DDQ}	-0.3 -0.3 -0.3	6.0 6.0 6.0	V
Lead Temperature (Soldering, 10 sec)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	-65	150	℃
Operating Junction Temperature Range	T_{JOPR}	-40	125	℃

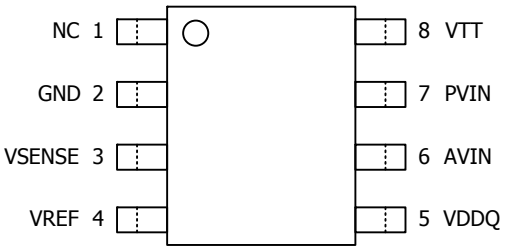
Recommended Operation Range

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
AV_{IN} to GND	AV_{IN}	2.3	5.5	V
PV_{IN} to GND	PV_{IN}	0	AV_{IN}	V

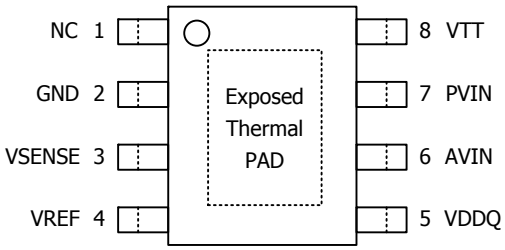
Ordering Information

Package	Order No.	Description	Package Marking	Supplied As
SOP8	TJ2995D	DDR Termination Regulator	TJ2995	Reel
SOP8-PP	TJ2995DP	DDR Termination Regulator	TJ2995	Reel

PIN CONFIGURATION



SOP8

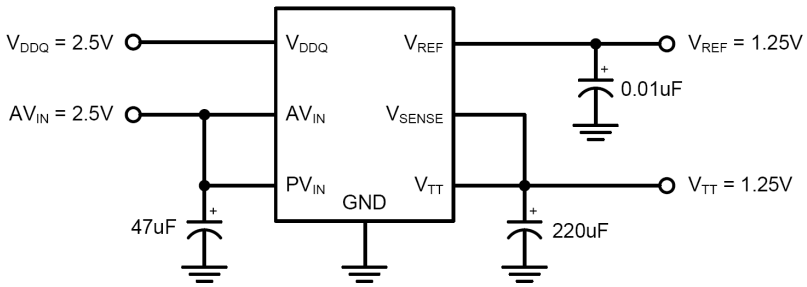


SOP8-PP

PIN DESCRIPTION

Pin No.	Pin Name	Pin Function
1	NC	No Internal Connection
2	GND	Ground
3	VSENSE	Feedback Pin for Regulating V_{TT}
4	VREF	Buffered Internal Reference Voltage of $V_{DDQ}/2$
5	VDDQ	Input for Internal Reference Equal to $V_{DDQ}/2$
6	AVIN	Analog Input Pin
7	PVIN	Power Input Pin
8	VTT	Output Voltage for Connection to Termination Resistors
	Exposed Thermal PAD	Exposed Thermal Connection. Connect to Ground. (SOP8-PP Only)

TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS (1)

Specifications with standard typeface are for T_J = 25°. Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V.(1), (4)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{REF} Voltage	V_{REF}	V_{DDQ} = 2.3V V_{DDQ} = 2.5V V_{DDQ} = 2.7V	1.11 1.21 1.31	1.15 1.25 1.35	1.19 1.29 1.39	V
V_{TT} Output Voltage	V_{TT}	I_{OUT} = 0 A V_{DDQ} = 2.3V V_{DDQ} = 2.5V V_{DDQ} = 2.7V I_{OUT} = ± 1.5 A V_{DDQ} = 2.3V V_{DDQ} = 2.5V V_{DDQ} = 2.7V	 1.11 1.21 1.31 1.11 1.21 1.31	 1.15 1.25 1.35 1.15 1.25 1.35	 1.19 1.29 1.39 1.19 1.29 1.39	V
V_{TT} Output Voltage Offset (2)	V_{OSVTT}	I_{OUT} = 0 A I_{OUT} = +1.5 A I_{OUT} = -1.5 A	-40 -40 -40	0 0 0	40 40 40	mV
Quiescent Current (3)	I_Q	I_{OUT} = 0A	-	250	2000	uA
V_{DDQ} Input Impedance	Z_{VDDQ}		-	100	-	kΩ
V_{SENSE} Input Current	I_{SENSE}			-	0.1	uA
Thermal Shutdown (5)	T_{SD}		-	165	-	℃

Note 1. Stresses listed as the absolute maximum ratings may cause permanent damage to the device. These are for stress ratings. Functional operating of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibly to affect device reliability.

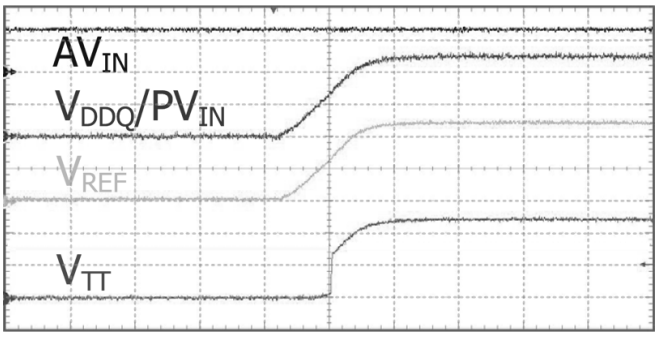
Note 2: V_{TT} offset is the voltage measurement defined as V_{TT} subtracted from V_{REF}.

Note 3: Quiescent current defined as the current flow into AVIN.

Note 4: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation.

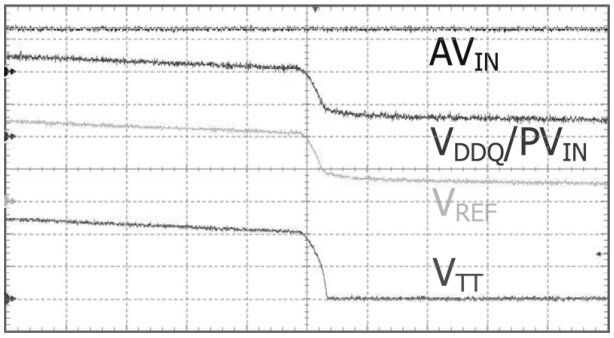
Note 5. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

TYPICAL OPERATING CHARACTERISTICS



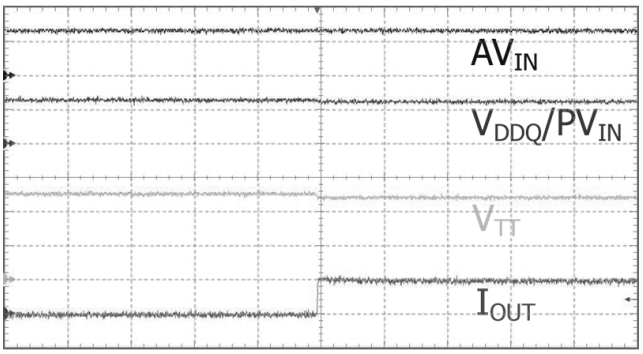
AVIN = 2.0V/Div, VDDQ/PVIN = 1.0V/div, VREF = 500mV/div, VTT = 500mV/div, Time = 10ms/div

Start Up



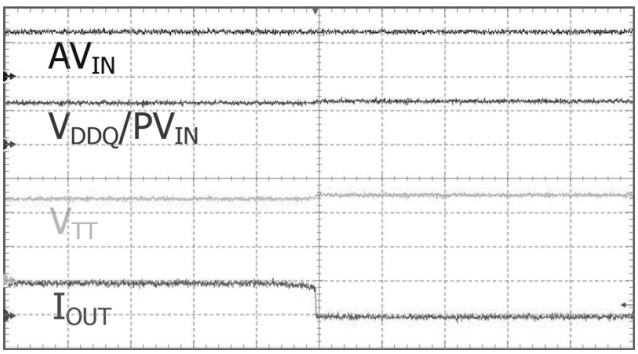
AVIN = 2.0V/Div, VDDQ/PVIN = 1.0V/div, VREF = 500mV/div, VTT = 500mV/div, Time = 10ms/div

Shut Down



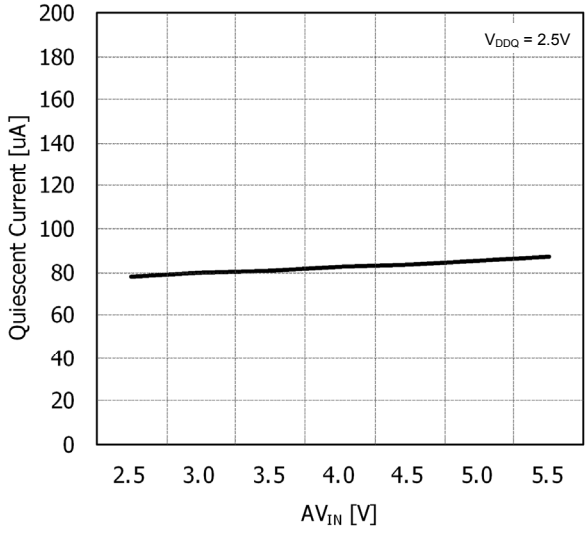
AVIN = 2.0V/Div, VDDQ/PVIN = 2.0V/div, VTT = 100mV/div, IOUT = 1A/div, Time = 10ms/div

Load (0A → 1A)



AVIN = 2.0V/Div, VDDQ/PVIN = 2.0V/div, VTT = 100mV/div, IOUT = 1A/div, Time = 10ms/div

Load (1A → 0A)



AV_{IN} vs. Quiescent Current

DESCRIPTION

The TJ2995 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2 and SSTL-3. The TJ2995 is capable of sinking and sourcing current at the output V_{TT}, regulating the voltage to equal V_{DDQ} / 2. A buffered reference voltage that also tracks V_{DDQ} / 2 is generated on the V_{REF} pin for providing a global reference to the DDR-SDRAM and Northbridge Chipset. V_{TT} is designed to track the V_{REF} voltage with a tight tolerance over the entire current range while preventing shoot through on the output stage.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR RAM. The most common form of termination is Class II single parallel termination. This involves using one RS series resistor from the chipset to the memory and one RT termination resistor. This implementation can be seen below in Figure 1.

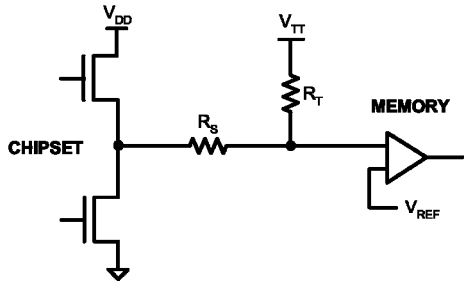


FIGURE 1. SSTL-Termination Scheme

PIN DESCRIPTION

AV_{IN} AND PV_{IN}

AV_{IN} and PV_{IN} are the input supply pins for the TJ2995. AV_{IN} is used to supply all the internal control circuitry for the two op-amps and the output stage of V_{REF}. PV_{IN} is used exclusively to provide the rail voltage for the output stage on the power operational amplifier used to create V_{TT}. For SSTL-2 applications AV_{IN} and PV_{IN} pins should be connected directly and tied to the 2.5V rail for optimal performance. This eliminates the need for bypassing the two supply pins separately.

V_{DDQ}

V_{DDQ} is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This guarantees that V_{TT} will track V_{DDQ} / 2 precisely. The optimal implementation of V_{DDQ} is as a remote sense. This can be achieved by connecting V_{DDQ} directly to the 2.5V rail at the DIMM instead of AV_{IN} and PV_{IN}. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications V_{DDQ} will be a 2.5V signal, which will create a 1.25V termination voltage at V_{TT} (See Electrical Characteristics Table for exact values of V_{TT} over temperature).

V_{SENSE}

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the TJ2995, then the long trace will cause a significant IR drop, resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used, then the V_{SENSE} pin must still be connected to V_{TT}.

V_{REF}

V_{REF} provides the buffered output of the internal reference voltage V_{DDQ} / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from V_{REF}. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 μF to 0.01 μF is recommended. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to V_{DDQ} / 2. The TJ2995 is designed to handle peak transient currents of up to ± 3A with a fast transient response. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the TJ2995 is designed to handle large transient output currents it is not capable of handling these for long durations, under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used (please refer to the Thermal Dissipation section).

THERMAL DISSIPATION

Since the TJ2995 is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise, T_{Rmax} can be calculated given the maximum ambient temperature, T_{Amax} of the application and the maximum allowable junction temperature, T_{Jmax}.

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

From this equation, the maximum allowable power dissipation, P_{Dmax} of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA}$$

The maximum allowable value for junction-to-ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D = (T_{Jmax} - T_{Amax}) / P_D$$

The θ_{JA} of the TJ2995 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the θ_{JA} of the SOP8 is 165°C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 152°C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard.

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the θ_{JA} further than the nominal values. Additional improvements in lowering the θ_{JA} can also be achieved with a constant airflow across the package.

Optimizing the θ_{JA} and placing the TJ2995 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at V_{TT}, either sinking or sourcing, and quiescent current at AV_{IN} and V_{DDQ}. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$$

Where, $P_{AVIN} = I_{AVIN} \times V_{AVIN}$

$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$

To calculate the maximum power dissipation at V_{TT} both conditions at V_{TT} need to be examined, sinking and sourcing current. Although only one equation will add into the total, V_{TT} cannot source and sink current simultaneously.

$P_{VTT} = V_{VTT} \times I_{LOAD}$ (Sinking) or $P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD}$ (Sourcing)

The power dissipation of the TJ2995 can also be calculated during the shutdown state. During this condition the output V_{TT} will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AV_{IN} and the constant impedance that is seen at the V_{DDQ} pin.

$$P_D = P_{AVIN} + P_{VDDQ} ,$$

Where, $P_{AVIN} = I_{AVIN} \times V_{AVIN}$

$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$

TYPICAL APPLICATION INFORMATION

The typical application circuit used for SSTL-2 termination schemes with DDR-SDRAM can be seen in Figure 2.

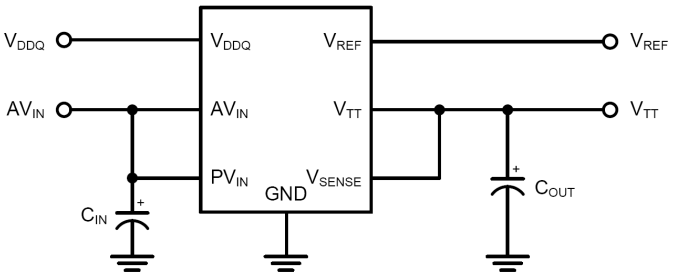


FIGURE 2. SSTL-2 Implementation

For SSTL-3 and other applications, it may be desirable to change internal reference voltage scaling from the V_{DDQ} / 2. An external resistor in series with the V_{DDQ} pin can be used to lower the reference voltage. Internally two 50 kΩ resistors set the output V_{TT} to be equal to V_{DDQ} / 2. The addition of a 11.1 kΩ external resistor will change the internal reference voltage causing the two outputs to track V_{DDQ} * 0.45. An implementation of this circuit can be seen in Figure 3.

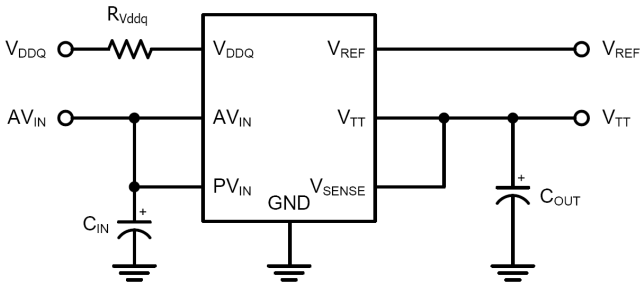


FIGURE 3. SSTL-3 Implementation

Another application that is sometimes required is to increase the V_{TT} output voltage from the scaling factor of V_{DDQ} * 0.5. This can be accomplished independently of V_{REF} by using a resistor divider network between V_{TT}, V_{SENSE} and Ground. An example of this circuit can be seen in Figure 4.

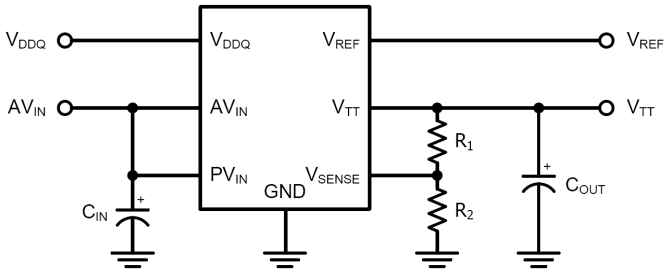


FIGURE 4. Increased VTT from the Scaling Factor

PCB LAYOUT CONSIDERATIONS

1. AV_{IN} and PV_{IN} should be tied together for optimal performance. A local bypass capacitor should be placed as close as possible to the PV_{IN} pin.
2. GND should be connected to a ground plane with multiple vias for improved thermal performance.
3. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
4. V_{DDQ} can be connected remotely to the V_{DDQ} rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
5. V_{REF} should be bypassed with a 0.01 µF or 0.1 µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the V_{REF} pin.