PL613-01

1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC

Features

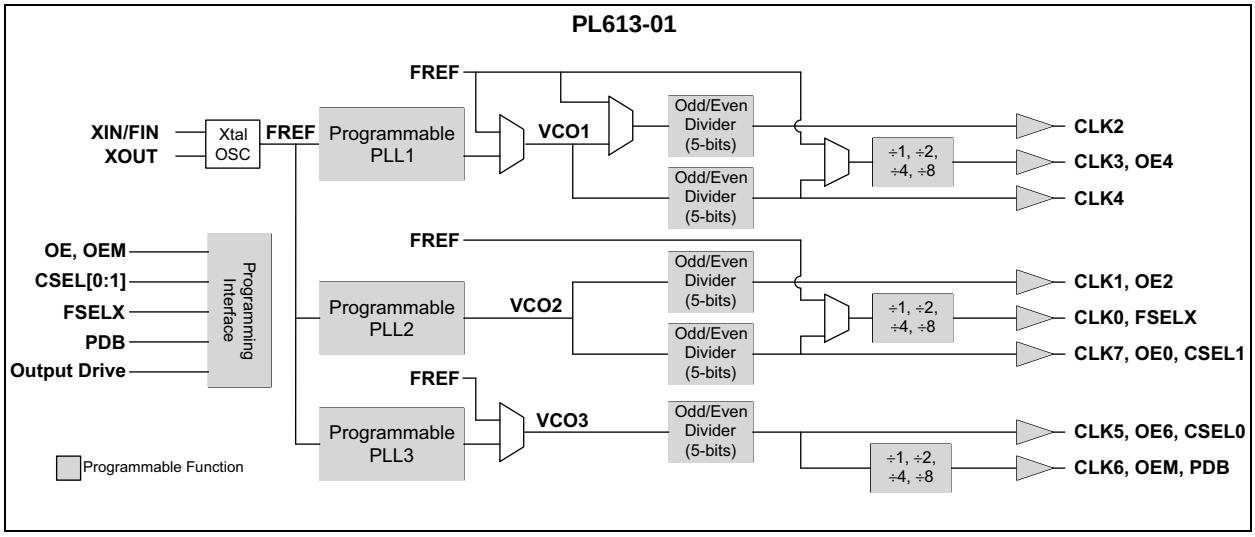
- Designed for PCB Space Savings with Three Low-Power Programmable PLLs and up to 8 Clock Outputs
- Low Power Consumption
  - 10 µA Typical When PDB is Activated
- Output Frequency:
  - ≤110 MHz at 1.8V Operation
  - ≤166 MHz at 2.5V Operation
  - ≤200 MHz at 3.3V Operation
- Input Frequency:
  - Fundamental Crystal: 10 MHz to 40 MHz
  - Reference Input: 10 MHz to 200 MHz
- Programmable I/O Pins Can be Configured as Output Enable (OE), Configuration Switching (CSEL), Frequency Switching (FSELX), Power Down (PDB) Inputs, or Clock Outputs
- Disabled Outputs Programmable as HiZ or Active Low
- Four Distinct Configurations Selectable with CSEL[0:1]
- Single 1.8V, 2.5V, or 3.3V ±10% Power Supply
- Temperature range: 0°C to 70°C, –40°C to +85°C
- Available in 3 mm x 3 mm QFN or TSSOP Packages

General Description

The PL613-01 is an advanced triple PLL design based on Microchip's PicoPLL™, the world's smallest programmable clock, technology. This advanced technology allows the eight output PL613-01 to fit in to a small 3 mm x 3 mm QFN or TSSOP package for high performance, low-power, low-cost applications. Besides its small form factor and 8 outputs that can reduce overall system costs, the PL613-01 offers superior phase noise, jitter and power consumption performance.

The power down feature of PL613-01, when activated, allows the IC to consume less than 10 µA of power, while its CSEL[0:1] allows switching between up to four pre-programmed configurations. The FSELX, on the other hand, allows frequency switching of two outputs (CLK1 and CLK2) on a single clock pin (CLK2).

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage Range (V_{DD}) ..... –0.5V to +4.6V
Input Voltage Range (V_{IN}) ..... –0.5V to V_{DD} + 0.5V
Output Voltage Range (V_{OUT}) ..... –0.5V to V_{DD} + 0.5V
Data Retention at +85°C ..... 10 Years

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: AC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Crystal Input Frequency	X_{IN}	10	—	40	MHz	Fundamental Crystal
Input Frequency	F_{IN}	10	—	200	MHz	at V_{DD} = 3.3V, ±10%
		10	—	166	MHz	at V_{DD} = 2.5V, ±10%
		10	—	110	MHz	at V_{DD} = 1.8V, ±10%
Input Signal Amplitude	—	0.8	—	V_{DD}	V_{PP}	Internally AC-Coupled
Output Frequency	—	1	—	200	MHz	at V_{DD} = 3.3V, ±10% (High Drive)
		1	—	166	MHz	at V_{DD} = 2.5V, ±10% (High Drive)
		1	—	110	MHz	at V_{DD} = 1.8V, ±10% (High Drive)
Settling Time	—	—	—	2	ms	At power-up (V_{DD} ≥ 90% of operating V_{DD})
Output Enable Time	—	—	—	500	ns	OE function; T_A = 25°C, 15 pF load. Add one clock period to this measurement for a usable clock output.
		—	—	2	ms	PDB function; T_A = 25°C, 15 pF load.
V_{DD} Sensitivity	—	–2	—	2	ppm	Frequency vs. V_{DD}, ±10%
Output Rise Time	—	—	1.2	1.7	ns	15 pF load, 10/90% V_{DD}, High Drive, 3.3V
Output Fall Time	—	—	1.2	1.7	ns	15 pF load, 10/90% V_{DD}, High Drive, 3.3V
Duty Cycle	—	45	50	55	%	PLL-driven output, @ V_{DD}/2, 15 pF load, High Drive, over entire frequency range
Period Jitter (Note 1) (10,000 Samples)	—	—	300	—	ps	Configuration-dependent, with capacitive decoupling between V_{DD} and GND

Note 1: Jitter performance depends on the programming parameters.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current (V_{DD} = 3.3V)	I_{DD}	—	17	23	mA	All 8 outputs @ 20 MHz No load
Supply Current (V_{DD} = 2.5V)	I_{DD}	—	13.5	18	mA	All 8 outputs @ 20 MHz No load
Supply Current (V_{DD} = 1.8V)	I_{DD}	—	9.5	13	mA	All 8 outputs @ 20 MHz No load
Supply Current	I_{DD}	—	10	—	µA	When PDB = 0
Operating Voltage	V_{DD}	2.97	3.3	3.63	V	Configured for 3.3V Operation
		2.25	2.5	2.75	V	Configured for 2.5V Operation
		1.62	1.8	1.98	V	Configured for 1.8V Operation
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = +4 mA, Standard Drive, 3.3V

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OL} = –4 mA, Standard Drive, 3.3V
Output Current, Low Drive	I_{OLD}	4	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V
Output Current, Standard Drive	I_{OSD}	8	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V
Output Current, High Drive	I_{OHD}	16	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V

TABLE 1-3: CRYSTAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units
Fundamental Crystal Resonator Frequency	F_{XIN}	10	—	40	MHz
Crystal Loading Rating	$C_{L(XTAL)}$	—	15	—	pF
Operating Drive Level	—	—	0.1	2	mW
Metal Can Crystal, Shunt Capacitance	C0	—	—	5.5	pF
Metal Can Crystal, ESR Max.	ESR	—	—	40	Ω
Small SMD Crystal, Shunt Capacitance	C0	—	—	2.5	pF
Small SMD Crystal, ESR Max.	ESR	—	—	60	Ω

TEMPERATURE SPECIFICATIONS (Note 1)

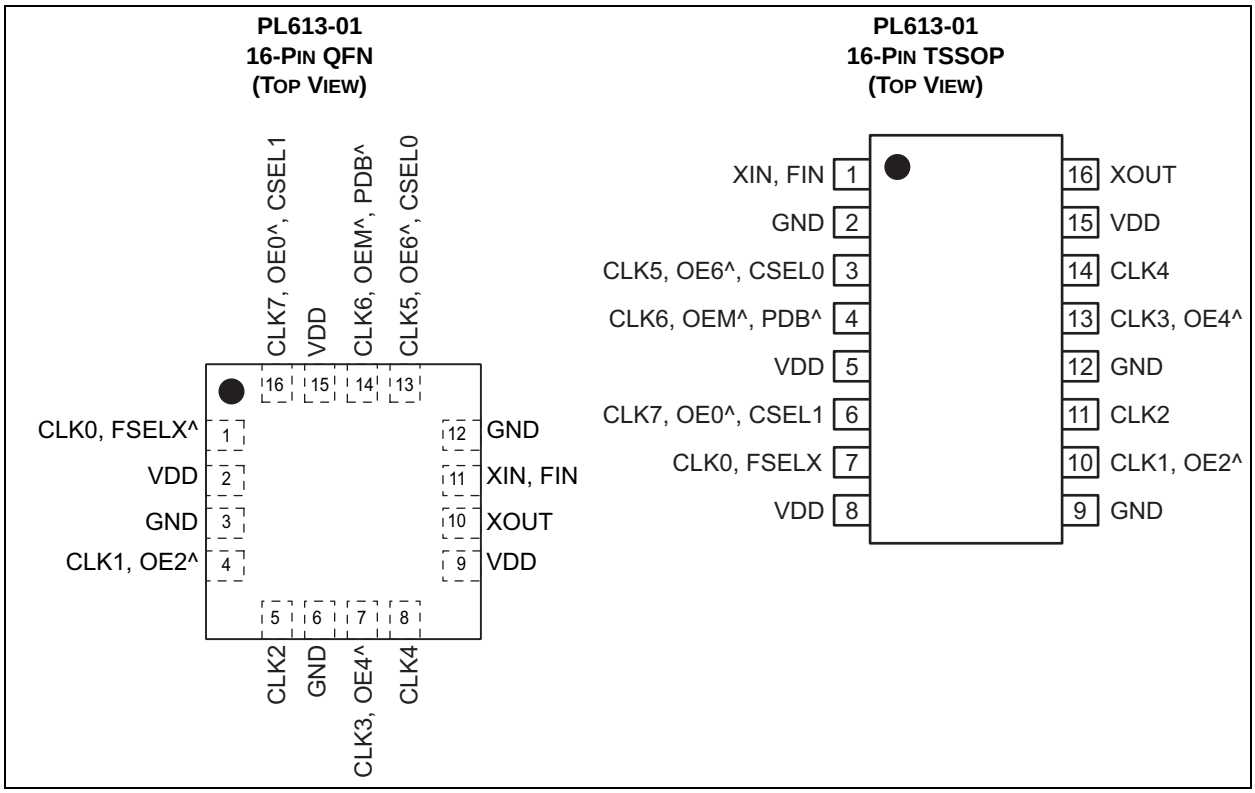
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Soldering Temperature	—	—	—	+260	°C	—
Ambient Operating Temperature Range	T_A	–40	—	+85	°C	—

Note 1: Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

Package Types



Note 1: ^ denotes internal pull-up.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number QFN-16	Pin Number TSSOP-16	Pin Name	Pin Type (Note 1)	Description
1	7	CLK0, FSELX	B	Programmable clock (CLK0) output or CLK2 frequency switching (FSELX) input.
3, 6, 12	2, 9, 12	GND	P	Ground connection.
2, 9, 15	5, 8, 15	VDD	P	V_{DD} connection.
4	10	CLK1, OE2	B	Programmable clock (CLK1) output or Output Enable (OE) input for CLK2.
5	11	CLK2	O	Programmable clock (CLK2) output.
7	13	CLK3, OE4	B	Programmable clock (CLK3) output or Output Enable (OE) input for CLK4.
8	14	CLK4	O	Programmable clock (CLK4) output.
10	16	XOUT	O	Crystal output pin. Do not connect when using FIN.
11	1	XIN, FIN	I	Crystal or reference clock input.
13	3	CLK5, OE6, CSEL0	B	Programmable clock (CLK5) output or Output Enable (OE) input for CLK6 or configuration switching input.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number QFN-16	Pin Number TSSOP-16	Pin Name	Pin Type (Note 1)	Description
14	4	CLK6, OEM, PDB	B	Programmable clock (CLK6) output or Output Enable master (OEM) all clock outputs or power down mode (PDB) input.
16	6	CLK7, OE0, CSEL1	B	Programmable clock (CLK7) output or Output Enable (OE) input for CLK0 or configuration switching input.

Note 1: All bidirectional buffers (I/Os) incorporate an internal 60 kΩ pull-up resistor when used as an input, except when PDB mode is used. In configurations that use PDB, the PDB pin will have a 10 MΩ pull-up resistor.

TABLE 2-2: KEY PROGRAMMING PARAMETERS

CLK[0:7] Output Frequency	Output Drive Strength	Programmable Input/Output
CLK[0,3,6]: F_{VCOx} / (P*(1,2,4,8)), F_{REF}, or F_{REF} / (P*(1,2,4,8)) **CLK[1,4,7]:** F_{VCOx} / P **CLK[2,5]:** F_{VCOx} / P, F_{REF}, or F_{REF} / P Where $F_{VCOx} = F_{REF} * M / R$ M = 11 bit R = 8 bit P = 5 bit (odd/even divider)	Each output has three optional drive strengths to choose from: • Low: 4 mA • Standard: 8 mA (default) • High: 16 mA	Most pins are multi-function I/Os. In addition to CLK, they can be configured to perform as the following: • OE[0,2,4,6]: Output Enable for Individual I/Os. • OEM: Master OE Controlling All Outputs. • CSEL[0:1]: Device Configuration Switching. • FSELX: CLK2 Frequency Switching. • PDB: Power Down. • CLK[0:8]: Output. • HiZ or Active-Low Disabled State.

3.0 FUNCTIONAL DESCRIPTION

The PL613-01 is a highly featured, very flexible, advanced triple-PLL design for high performance, low-power applications. The device accepts a low-cost fundamental crystal input of 10 MHz to 40 MHz or a reference clock input of 10 MHz to 200 MHz and is capable of producing eight distinct output frequencies up to 200 MHz. All three PLLs are fully programmable, with a total of five, 5-bit post-VCO, odd/even 'P-counter' dividers with an additional 1, 2, 4, or 8 'Post P-counter' dividers that easily generate the most demanding frequencies. The outputs can be programmed to deliver the generated frequencies from the PLLs or the reference input. Each bidirectional feature pin (I/O) on the PL613-01 incorporates a 60 kΩ pull-up resistor and can be configured to perform various functions. Usage of various design features of these products is mentioned in the following paragraphs.

3.1 PLL Programming

The three PLLs in PL613-01 are fully programmable. Each PLL is equipped with an 8-bit input frequency divider (R-Counter) and an 11-bit VCO frequency feedback loop (M-Counter) divider. The three PLL outputs are transferred to five 5-bit post-VCO, odd/even dividers (P-Counter), as shown in the Block Diagram. In addition, there are three optional (÷1, ÷2, ÷4, or ÷8) post P-Counter dividers that can further divide the VCO frequency. In general, the PLL output frequency is determined by the following formula:

EQUATION 3-1:

$$F_{OUT} = (F_{REF} \times M)/(R \times P)$$

For output calculations, please note that 'P' includes the P-Counter bits plus the additional optional dividers (÷1, ÷2, ÷4, or ÷8), if used.

3.2 CLKx (Clock Outputs)

There are a maximum of eight outputs available on the PL613-01. Clock output frequencies can be configured as follows:

- CLK[0,3,6]
  - F_{VCOx} / (P*(1, 2, 4, 8))
  - F_{REF} (Crystal or Reference Clock frequency)
  - F_{REF} / (P*(1,2,4,8))
- CLK[1, 7]
  - F_{VCOx} / P
- CLK[2, 4, 5]
  - F_{VCOx} / P
  - F_{REF}
  - F_{REF} / P

Each output can be programmed with a 4 mA, 8 mA, or 16 mA drive strength. The maximum output frequency is 200 MHz at 3.3V, 166 MHz at 2.5V, or 110 MHz at 1.8V.

3.3 OE (Output Enable)

Four pins can be configured as OE inputs for controlling individual clock outputs, as show in the table below.

OEx	Controls Output on CLK#
OE0	CLK0
OE2	CLK2
OE4	CLK4
OE6	CLK6

Typical enable time is <500 ns plus one clock period.

The OE feature can be programmed to allow the output to float (HiZ) or to operate in active-low mode. The programming control for individual OEs is show below.

OE Pin	OE Type (Programmable)	Osc	PLL	Output
0	0 (default)	On	On	HiZ
	1	On	On	Active 0
1	Normal Operation (default)			

3.4 OEM (Master Output Enable)

One pin can be configured to be a single Master OE (OEM) input pin that controls all the outputs of the PL613-01. In addition, the state of the disabled outputs can be programmed to float (HiZ) or to operate in active-low mode. The OEM function operates on the following logic:

OE Pin	OE Type (Programmable)	Osc	PLL	Output
0	0 (default)	On	On	HiZ
	1	On	On	Active 0
1	Normal Operation (default)			

Typical enable time is <500 ns plus one clock period.

3.5 PDB (Power Down Control)

When activated, PDB disables all the PLLs, the oscillator circuitry, counters, and all other active circuitry. PDB activation disables all outputs and the IC consumes <10 µA of power. The PDB input incorporates a 10 MΩ pull-up resistor for normal operation.

The PDB feature can be programmed to allow the output to float (HiZ) or to operate in active-low mode. The logic for PDB is shown in the following table:

PDB Pin	PDB Type (Programmable)	Osc	PLL	Output
0	0 (default)	Off	Off	HiZ
	1	Off	Off	Active 0
1	Normal Operation (default)			

Typical enable time from power down in <2 ms.

3.6 CSEL (On-the-Fly Configuration Switching)

The PL613-01 can be programmed to allow switching between four different configurations, allowing for changes in the output frequencies. Many applications (i.e. video/audio) can use the same design footprint, but allow for configuration switching, adhering to various standards. CSEL0 and CSEL1 are used in the switching selection. These pins incorporate a 60 kΩ pull-up resistor for normal operation. The logic for configuration switching of the programmed parts is shown below:

CSEL1	CSEL0	Programmed Configuration
0	0	0
0	1	1
1	0	2
1	1	3 (default)

Typical enable time is <500 µs.

3.7 FSELX (On-the-Fly Output Frequency Switching Between Two Output Frequencies)

The PL613-01 is equipped with the FSELX feature to allow frequency switching between two frequencies on one of the output pins. Frequencies assigned to CLK1 and CLK2 can be switched when FSELX is activated on CLK2 output. The logic for FSELX is shown below:

FSELX	CLK2 Output
0	Frequency 2
1 (default)	Frequency 1

Typical enable time is <10 ns plus one clock period.

4.0 LAYOUT RECOMMENDATIONS

The following guidelines are designed to help create a performance-optimized PCB design.

4.1 Signal Integrity and Termination Considerations

- Keep traces short.
- Trace = Inductor. With capacitive loads, this creates ringing.
- Long trace = long transmission line. Without proper termination, this causes reflections that look like ringing.
- Design long traces (greater than one inch) as striplines or microstrips with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

4.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply.
- Multiple V_{DD} pins should be decoupled separately for best performance.
- The addition of resistors in series with V_{DD} can help prevent noise from other board sources.
  - Traditionally, ferrite beads are used for this purpose, but with the PL613-01 the results are better when using resistors.

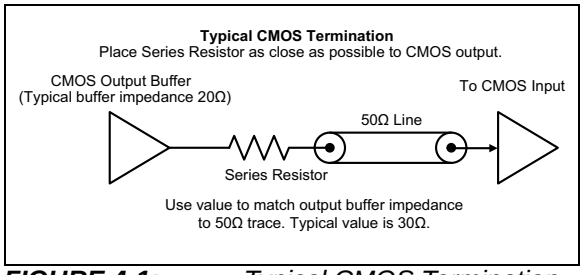


FIGURE 4-1: *Typical CMOS Termination.*

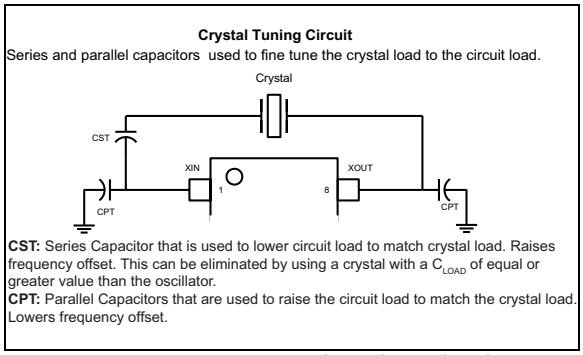


FIGURE 4-2: *Crystal Tuning Circuit.*

4.3 Layout Example

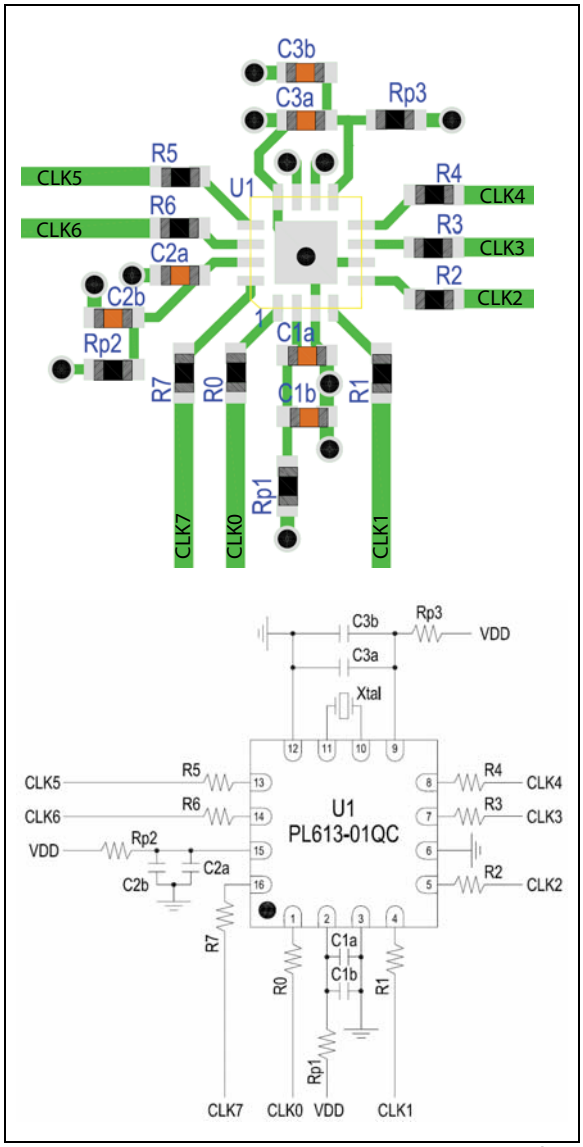


FIGURE 4-3: *PL613-01 Layout Example.*

U1 = PL613-01 in QFN-16L. In this example, all eight outputs are used.

C1a, C2a, C3a = 0.1 µF and C1b, C2b, C3b = 1 µF for power supply decoupling. The vias connected to the capacitors go to the ground plane inside the PCB.

Rp1, Rp2, Rp3 = 10Ω for power supply filtering. The power supply filter is a first order low pass filter with –3 dB at 30 kHz. It is important that the frequencies of the loop bandwidth of the PLLs are filtered properly. The loop bandwidth of the PLLs is in the range of 100 kHz to 1 MHz depending upon the programmed configuration. The vias connected to Rp1, Rp2, and Rp3 go to the V_{DD} plane inside the PCB.

R0 ~ R7 = 30Ω for matching CLK0 ~ CLK7 outputs to the PCB trace impedance. Place the resistors as close as possible to the IC pins and design the traces to the

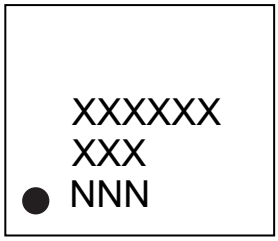
target clock inputs as transmission lines (microstrip or stripline) for the best signal integrity and the lowest EMI.

When using ferrite beads instead of Rp1, Rp2, or Rp3, make sure the resonance frequency of the bead with the decoupling capacitors is below 50 kHz so as not to interfere with the PLL loop bandwidth. This requirement is difficult to fulfill, so it is recommended to use the resistors Rp1, Rp2, and Rp3 for power supply filtering.

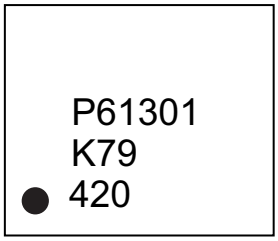
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

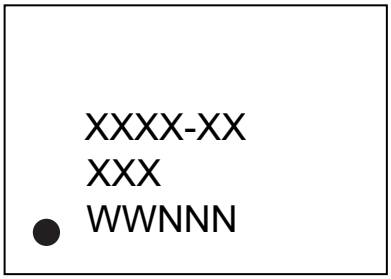
16-Pin QFN*



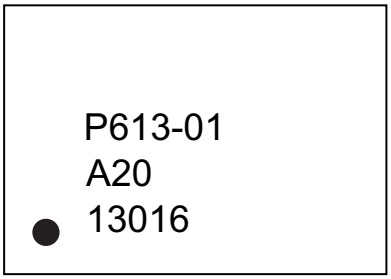
Example



16-Pin TSSOP*



Example

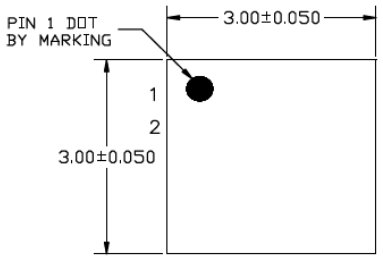


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

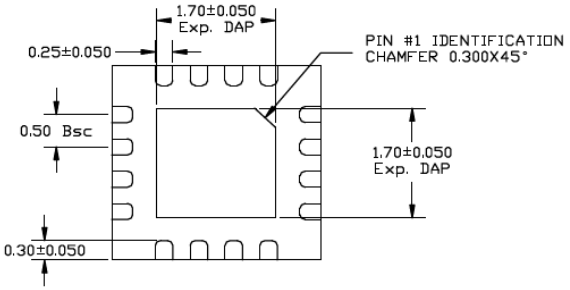
16-Lead QFN Package Outline and Recommended Land Pattern

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

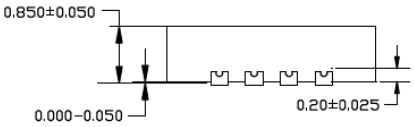
DRAWING #	QFN33-16LD-PL-3	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



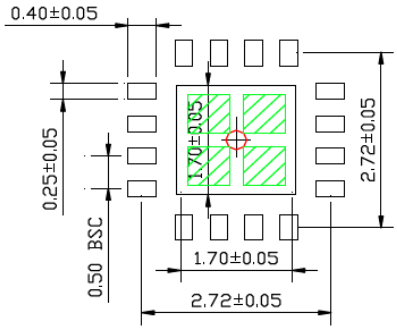
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

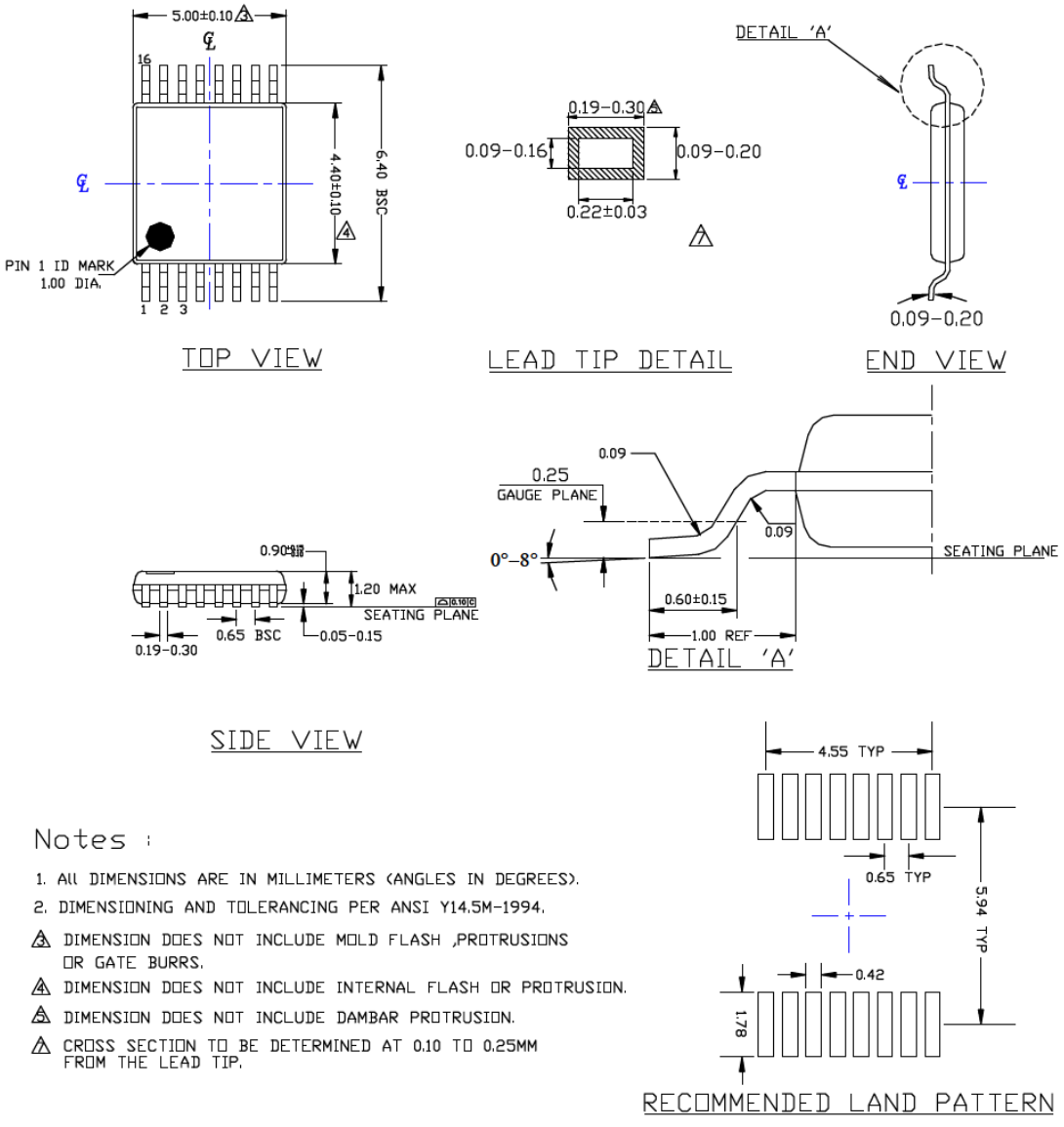
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

16-Lead TSSOP Package Outline and Recommended Land Pattern

TITLE
16 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOP-16LD-PL-1	UNIT	MM



Notes :

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH ,PROTRUSIONS OR GATE BURRS.
4. DIMENSION DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
6. CROSS SECTION TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Converted Micrel document PL613-01 to Microchip data sheet DS20005650A.
- Minor text changes throughout.
- Discontinued SSOP package offering.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	—	XXX	X	X	—	XX
Device		ID Code	Package	Temperature		Media Type

Device:	PL613-01:	1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC
ID Code:	XXX =	Unique 3-digit code assigned at programming time
Package:	O =	16-Lead TSSOP
	Q =	16-Lead QFN
Temperature:	C =	0°C to +70°C (Commercial)
	I =	–40°C to +85°C (Industrial)
Media Type:	blank=	Tube
	TR =	Tape & Reel

Examples:

a) PL613-01-XXXOC: 1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead TSSOP, Commercial Temperature Range, Tube

b) PL613-01-XXXOI-TR: 1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead TSSOP, Industrial Temperature Range, Tape & Reel

c) PL613-01-XXXQC-TR: 1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead QFN, Commercial Temperature Range, Tape & Reel

d) PL613-01-XXXQI: 1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead QFN, Industrial Temperature Range, Tube

e) PL613-01-XXXOC-TR: 1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead TSSOP, Commercial Temperature Range, Tape & Reel

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-1038-6

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

06/23/16