National Semiconductor

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LMX2364
2.6 GHz PLLatinum Fractional RF Frequency Synthesizer with 850 MHz Integer IF Frequency Synthesizer

General Description

The LMX2364 integrates a high performance 2.6 GHz fractional frequency synthesizer with a 850 MHz low power Integer-N frequency synthesizer. Designed for use in a local oscillator subsystem of a radio transceiver, the LMX2364 generates very stable, low noise control signals for UHF and VHF voltage controlled oscillators. It is fabricated using National's high performance BiCMOS process.

The RF Synthesizer supports both fractional and integer modes. The N counter contains a selectable, quadruple modulus prescaler and can support fractional denominators from 1 to 128. A flexible, 4 level programmable charge pump supplies output current magnitudes ranging from 1 mA to 16 mA. Only a single word write is required to power up and tune the synthesizer to a new frequency.

High performance FastLock™ technology makes the LMX2364 an excellent choice for applications requiring aggressive lock time while maintaining excellent phase noise and spurious performance. The combination of the improved FastLock circuitry, the enhanced fractional compensation engine, and the programmable charge pump architecture gives the designer maximum freedom to optimize the performance of the synthesizer for the target application. Integrated timeout counters greatly simplify the programming aspects of FastLock. These timeout counters reduce the demands on the microcontroller by automatically disengaging FastLock after a perscribed number of reference cycles of the phase detector.

The IF synthesizer includes a fixed 8/9 dual modulus prescaler, a two level programmable charge pump, and dedicated FastLock circuitry with an integrated timeout counter.

The LMX2364 offers many performance enhancements over the LMX2354. Improvements in the fractional compensation make the spurs on the LMX2364 approximately 6 dB better in a typical application. The higher and more flexible fractional modulus combined with the higher charge pump currents result in phase noise improvements on the order of 10 dB. The cycle slip reduction circuitry of the LMX2364 is both easy to use and effective in reducing cycle slipping and allows one to use very high phase detector frequencies without degrading lock times.

Serial data is transferred to the device via a three-wire interface (DATA, LE, CLK). The low voltage logic interface allows direct connection to 1.8 Volt and 3.0 Volt devices. Supply voltages from 2.7V to 5.5V are supported. Independent charge pump supplies for each synthesizer allows the designer to optimize the bias level for the selected VCO. The LMX2364 consumes 5.0 mA (typical) of current in integer mode and 7.2 mA (typical) in fractional mode. The LMX2364 is available in a 24 Pin Ultra Thin CSP package and 24 Pin TSSOP Package.

Features

- RF Synthesizer supports both Fractional and Integer Operating Modes
- Pin Compatible upgrade for LMX2354
- 2.7V to 5.5V operation
- Pin and programmable power down
- Fractional N divider supports fractional denominators ranging from 1 through 128
- Supports Integer Mode Operation
- Programmable charge pump current levels
  RF: 4 level, 1 – 16 mA
  IF: 2 level, 100/800 uA
- FastLock Technology with integrated timeout counters
- Digital filtered & analog lock detect output
- FastLock Glitch Reduction Technology
- Enhanced Low Noise Fractional Compensation Engine
- Low voltage programming interface allows direct connection to 1.8V logic

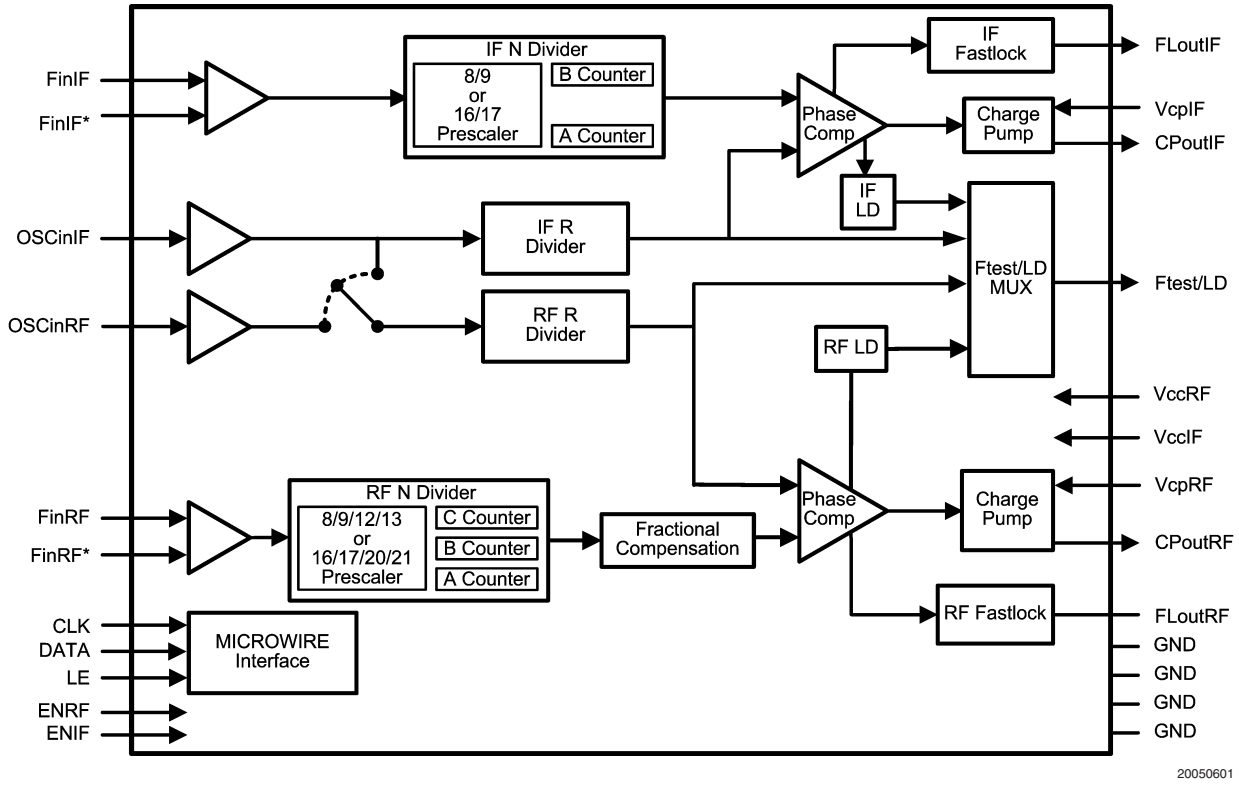
Applications

- Digital Cellular
- GPRS
- IS-136
- GAIT
- PDC
- EDGE
- CDMA
- Zero blind slot TDMA systems
- Cable TV Tuners (CATV)

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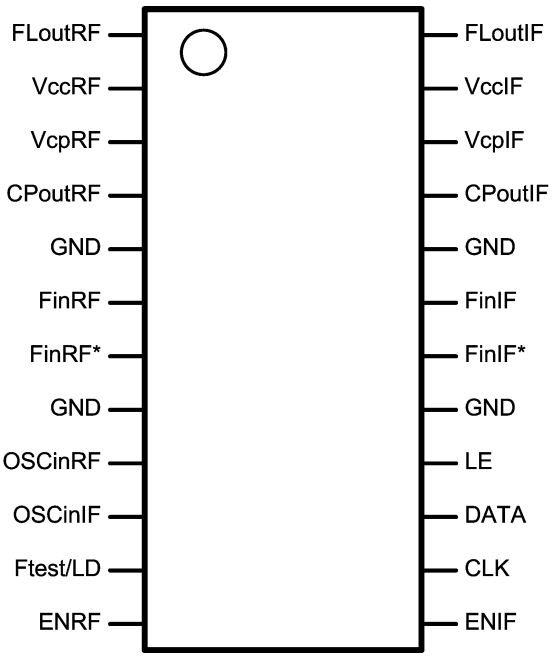
Functional Block Diagram



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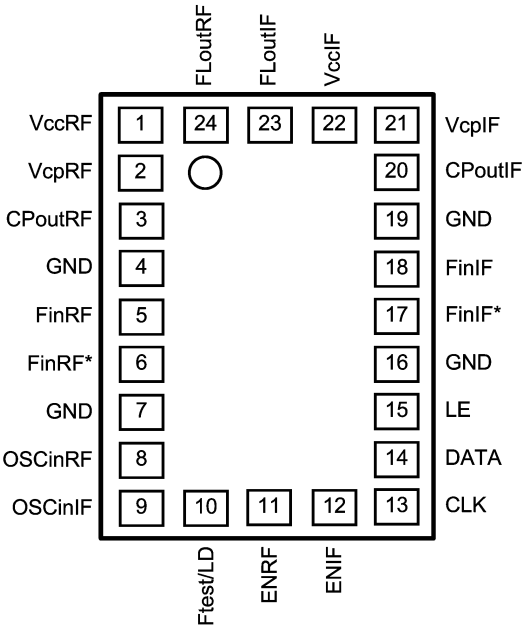
Connection Diagrams

24-Pin TSSOP (TM) Package



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Ultra Thin 24-Pin CSP (SLE) Package



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Pin Descriptions

Pin Number		Pin	Description
TSSOP	SLE		
2	1	VccRF	RF PLL power supply voltage input. Must be equal to V_{VccIF}. May range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
3	2	VcpRF	Power supply for RF charge pump. Must be ≥ V_{VccRF} and V_{VccIF}.
4	3	CPoutRF	RF charge pump output.
5	4	GND	Ground for RF PLL digital circuitry.
6	5	FinRF	RF prescaler input. Small signal input from the VCO.
7	6	FinRF*	RF prescaler complementary input. For single-ended operation, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
8	7	GND	Ground for RF PLL analog circuitry.
9	8	OSCinRF	RF R counter input. Has a $V_{CC}/2$ input threshold when configured as an input and can be driven from an external CMOS or TTL logic gate.
10	9	OSCinIF	Oscillator input which can be configured to drive both the IF and RF R counter inputs or only the IF R counter depending on the state of the OSC programming bit.
11	10	Ftest/LD	Programmable multiplexed output pin. Can function as general purpose CMOS TRI-STATE® I/O, analog lock detect output, digital filtered lock detect output, or N & R divider output.
12	11	ENRF	RF PLL Enable. Powers down RF N and R counters, prescaler, and TRI-STATE charge pump output when LOW, regardless of the state RF_PD bit. Bringing ENRF high powers up RF PLL depending on the state of RF_PD control bit.
13	12	ENIF	IF PLL Enable. Powers down IF N and R counters, prescaler, and will TRI-STATE the charge pump output when LOW, regardless of the state IF_PD bit. Bringing ENIF high powers up IF PLL depending on the state of IF_PD control bit.
14	13	CLK	High impedance CMOS Clock input. Data for the control registers is clocked into the 24-bit shift register on the rising edge.
15	14	DATA	Binary serial data input. Data entered MSB first. The last three bits are the control bits. High impedance CMOS input.
16	15	LE	Latch enable. High impedance CMOS input. Data stored in the shift register is loaded into one of the 7 internal latches when LE goes HIGH.
17	16	GND	Ground for IF analog circuitry.
18	17	FinIF*	IF prescaler complementary input. For single-ended operation, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground.
19	18	FinIF	IF prescaler input. Small signal input from the VCO.
20	19	GND	Ground for IF digital circuitry.
21	20	CPoutIF	IF charge pump output.
22	21	VcpIF	Power supply for IF charge pump. Must be ≥ V_{VccRF} and V_{VccIF}.
23	22	VccIF	IF power supply voltage input. Must be equal to V_{VccRF}. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
24	23	FLoutIF	IF FastLock Output. Also functions as Programmable TRI-STATE CMOS output.
1	24	FLoutRF	RF FastLock Output. Also functions as Programmable TRI-STATE CMOS output.

Absolute Maximum Ratings (Notes 1, 2)

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Power Supply Voltage	V_{Vcc}	−0.3		6.5	V
	V_{Vcp}	−0.3		6.5	V
Voltage on any pin with GND = 0V	V_{CC}	−0.3		V_{CC} + 0.3	V
Storage Temperature Range	T_s	−65		+150	˚C
Lead Temperature (Solder 4 sec.)	T_L			+260	˚C

Recommended Operating Conditions

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Power Supply Voltage	V_{VccRF}	2.7		5.5	V
	V_{VccIF}	V_{VccRF}		V_{VccRF}	V
	V_{VcpRF}	V_{VccRF}		5.5	V
	V_{VcpIF}	V_{CCIF}		5.5	V
Operating Temperature	T_A	−40		+85	˚C

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: This Device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.

Electrical Characteristics (V_{Vcc} = V_{Vcp} = 3.0V; −40˚C ≤ T_A ≤ +85˚C except as specified)

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
I_{CC} PARAMETERS						
I_{CC}RF	Power Supply Current, RF Synthesizer, Integer Mode	V_{ENIF}=V_{CLK}=V_{DATA}=V_{LE} = LOW V_{ENRFV}= HIGH FE = 0		5.0	6.3	mA
	Power Supply Current, RF Synthesizer, Fractional Mode	V_{ENIF}=$V_{CLK,}$=V_{DATA}=V_{LE}=0 V V_{ENRF}=HIGH FE = 1		7.2	8.0	mA
I_{CC}IF	Power Supply Current, IF Synthesizer	V_{ENRF}=V_{CLK}=V_{DATA}=V_{LE}=LOW V_{ENIF}=HIGH		2.4	3.2	mA
I_{CC}IF PD	Power Down Current	V_{ENRF}=V_{ENIF}= LOW V_{CLK}=V_{DATA}=V_{LE}= LOW		5.0	20	µA
RF SYNTHESIZER PARAMETERS						
f_{FinRF}	Operating Frequency	Prescaler = 8/9/12/13	500		1200	MHz
		Prescaler = 16/17/20/21	1200		2600	MHz
N	Continuous N Divider Range, Fractional Mode	Prescaler = 8/9/12/13	40		4095	
		Prescaler = 16/17/20/21	80		8191	
	Continuous N Divider Range, Integer Mode	Prescaler = 8/9/12/13	40		266,239	
		Prescaler = 16/17/20/21	80		532,479	
R	R Divider Range, Fractional Mode		1		511	
	R Divider Range, Integer Mode (Note 3)		1		64,897	
f_{COMP}	Phase Detector Frequency				15	MHz
p_{FinRF}	RF Input Sensitivity	V_{CC} = 3.0V	−15		0	dBm
		V_{CC} = 5.0V	−10		0	dBm

Electrical Characteristics (V_{Vcc} = V_{Vcp} = 3.0V; −40˚C ≤ T_A ≤ +85˚C except as specified) (Continued)

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
RF SYNTHESIZER PARAMETERS						
$I_{CPoutRF}$SRCE	RF Charge Pump Source Current	RF_CP=0 $V_{CPoutRF}$ = V_{VcpRF} /2		1		mA
		RF_CP=1 $V_{CPoutRF}$ = V_{VcpRF} /2		4		mA
		RF_CP=2 $V_{CPoutRF}$ = V_{VcpRF} /2		8		mA
		RF_CP=3 $V_{CPoutRF}$ = V_{VcpRF} /2		16		mA
$I_{CPoutRF}$SINK	RF Charge Pump Sink Current	RF_CP=0 $V_{CPoutRF}$ = V_{VcpRF} /2		−1		mA
		RF_CP=1 $V_{CPoutRF}$ = V_{VcpRF} /2		−4		mA
		RF_CP=2 $V_{CPoutRF}$ = V_{VcpRF} /2		−8		mA
		RF_CP=3 $V_{CPoutRF}$ = V_{VcpRF} /2		−16		mA
$I_{CPoutRF}$TRI	RF Charge Pump TRI-STATE Current	0.5 ≤ $V_{CPoutRF}$ ≤ V_{VcpRF} −0.5	−10.0		10.0	nA
$I_{CPoutRF}$%MIS	RF CP Sink vs. CP Source Mismatch	$V_{CPoutRF}$ = V_{VcpRF} /2 T_A = 25˚C		3.5		%
$I_{CPoutRF}$%V	RF CP Current vs. CP Voltage	0.5 ≤ $V_{CPoutRF}$ ≤ V_{VcpRF} −0.5 T_A = 25˚C RF_CP=0, 1, or 2		5	10	%
$I_{CPoutRF}$%TEMP	RF CP Current vs. Temperature	$VP_{CPoutRF}$ = V_{VcpRF} /2		8	10	%
IF SYNTHESIZER PARAMETERS						
f_{FinIF}	Operating Frequency		50		850	MHz
N IF	Continuous N Divider Range		56		262,143	
R IF	R Divider Range		3		32,767	
f_{COMP}	Phase Detector Frequency				10	MHz
p_{FinIF}	IF Input Sensitivity	2.7 ≤ V_{Vcc} ≤ 5.5V	−10		0	dBm
$I_{CPoutIF}$SRCE	IF Charge Pump Source Current	IF_CP = 0 $V_{CPoutIF}$ = V_{VcpIF} /2		100		µA
		IF_CP = 1 $V_{CPoutIF}$ = V_{VcpIF} /2		800		µA
$I_{CPoutIF}$SINK	IF Charge Pump Sink Current	IF_CP = 0 $V_{CPoutIF}$ = V_{VcpIF} /2		−100		µA
		IF_CP = 1 $V_{CPoutIF}$ = V_{VcpIF} /2		−800		µA
I_{CPout}TRI	IF Charge Pump TRI-STATE Current	0.5 ≤ V_{CPout} ≤ V_{VcpIF} −0.5	−2.0		2.0	nA
$I_{CPoutIF}$%MIS	IF CP Sink vs. CP Source Mismatch	$V_{CPoutIF}$ = V_{VcpIF} /2 T_A = 25˚C		5		%
$I_{CPoutIF}$%V	IF CP Current vs. CP Voltage	0.5 ≤ $V_{CPoutIF}$ ≤ V_{VcpIF} −0.5 T_A = 25˚C		5	10	%
$I_{CPoutIF}$%TEMP	IF CP Current vs. Temperature	$V_{CPoutIF}$ = V_{VcpIF} /2		8		%

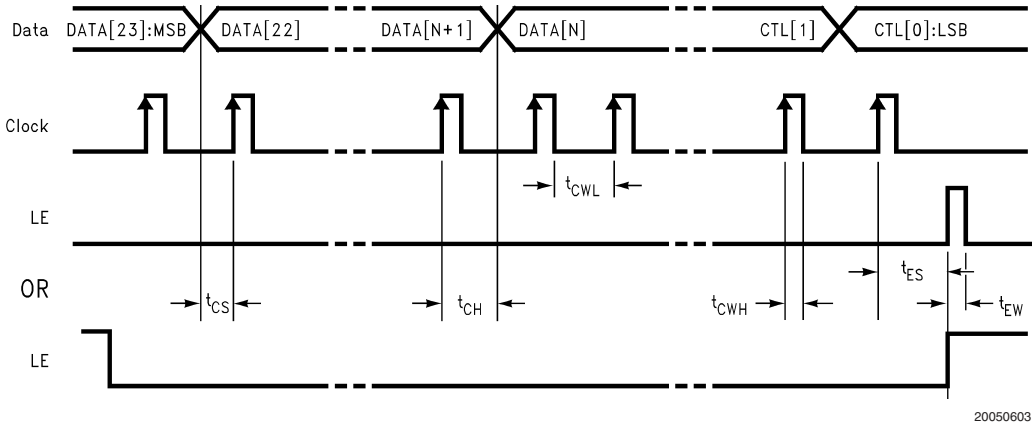
Electrical Characteristics (V_{Vcc} = V_{Vcp} = 3.0V; −40˚C ≤ T_A ≤ +85˚C except as specified) (Continued)

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
OSCILLATOR PARAMETERS						
f_{OSC}	Oscillator Operating Frequency		2		110	MHz
v_{OSC}	Oscillator Sensitivity	OSCinRF, OSCinIF	0.5		V_{Vcc}	V
I_{OSC}	Oscillator Input Current	V_{OSC} = V_{Vcc}			100	µA
		V_{OSC} = 0V	−100			µA
DIGITAL INTERFACE (DATA, CLK, LE, ENIF, ENRF, Ftest/LD, FLoutRF, FLoutIF)						
V_{IH}	High-Level Input Voltage	2.7 ≤ V_{Vcc} ≤ 3.2	1.6			V
		3.2< V_{Vcc} ≤ 5.5	2			V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	V_{IH} = V_{CC}	−1.0		1.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0	−1.0		1.0	µA
V_{OH}	High-Level Output Voltage	I_{OH} = −500 µA	V_{CC} −0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 500 µA			0.4	V
MICROWIRE INTERFACE TIMING						
T_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
T_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
T_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
T_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
T_{ES}	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
T_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns
PHASE NOISE						
L_{F1Hz}(f) RF	RF Synthesizer's Normalized Phase Noise Contribution, Fractional Mode (Note 4)	RF_OM = 1 (Fractional Mode) f = 3 KHz TCXO Reference Source RF_CP = 1 (4 mA) V_{ENIF} = LOW		−208		dBc/Hz
	RF Synthesizer's Normalized Phase Noise Contribution, Integer Mode (Note 4)	RF_OM = 0 (Integer Mode) f = 3 KHz TCXO Reference Source RF_CP = 2 (4 mA) V_{ENIF} = LOW		−215		dBc/Hz
L_{F1Hz}(f) IF	IF Synthesizer's Normalized Phase Noise Contribution (Note 4)	f = 3 KHz TCXO Reference Source IF_CP = 1 (800 mA) V_{ENRF} = LOW		−212		dBc/Hz

Note 3: Some reference divider ratios between the minimum and maximum are not realizable. See the section on R divider programming for more details.

Note 4: Normalized Phase Noise Contribution is defined as: $L_{F1Hz}(f) = L(f) - 20 \cdot \log(N) - 10\log(f_{COMP})$ where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth. The offset frequency, f, must be chosen sufficiently smaller than the PLL's loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source.

Serial Data Input Timing



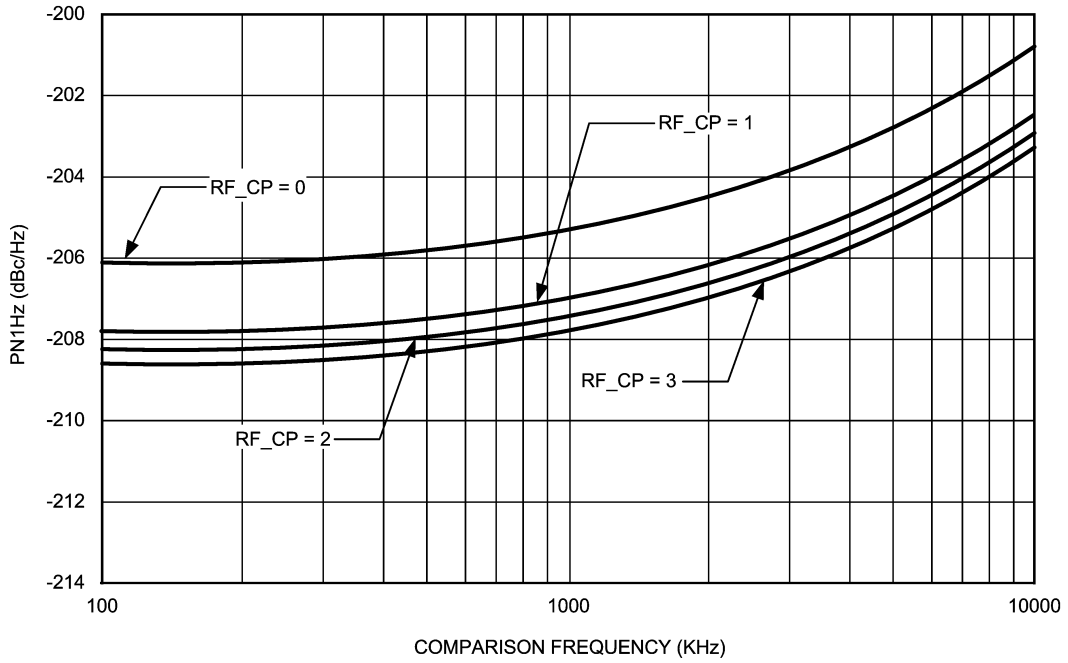
Note: Data is shifted MSB first into the MICROWIRE shift register on the rising edge of the Clock signal. When a rising edge is seen on the LE pulse, these values are actually loaded into the PLL target registers.

Since the data is clocked in on the rising edge of the LE pulse, the programming time of one register can be eliminated by sending the Data and Clock signals in advance and delaying the LE pulse until it is desired that the values are to be loaded.

Note: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC}=2.7V and 2.6V @ V_{CC} = 3.3V.

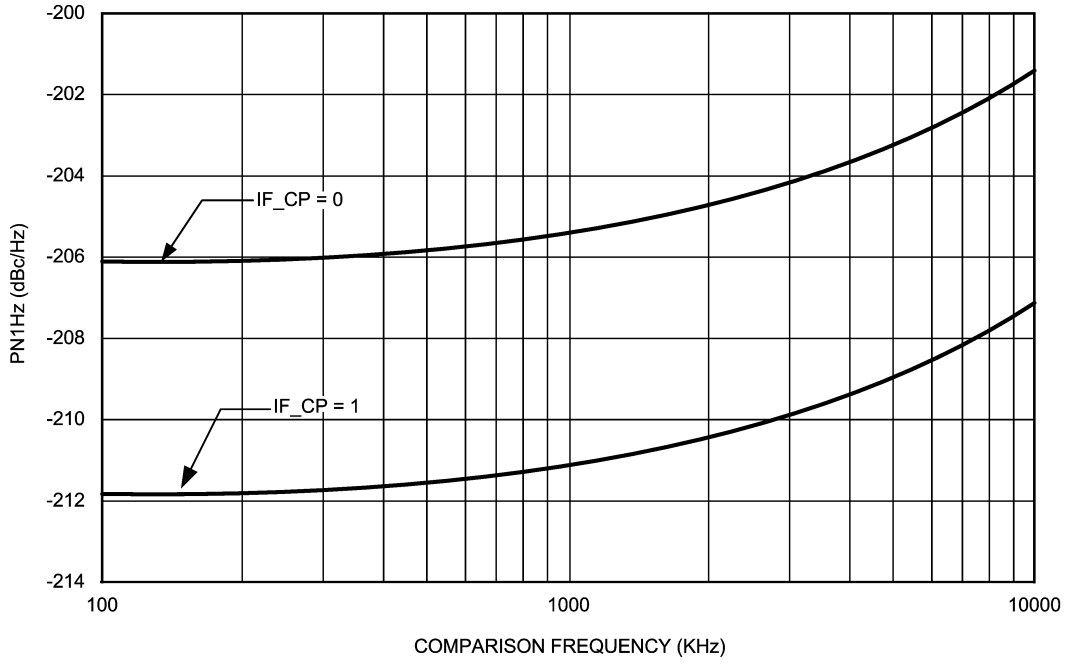
Typical Performance Characteristics

RF PLL 1 Hz Normalized Phase Noise (Fractional Mode)



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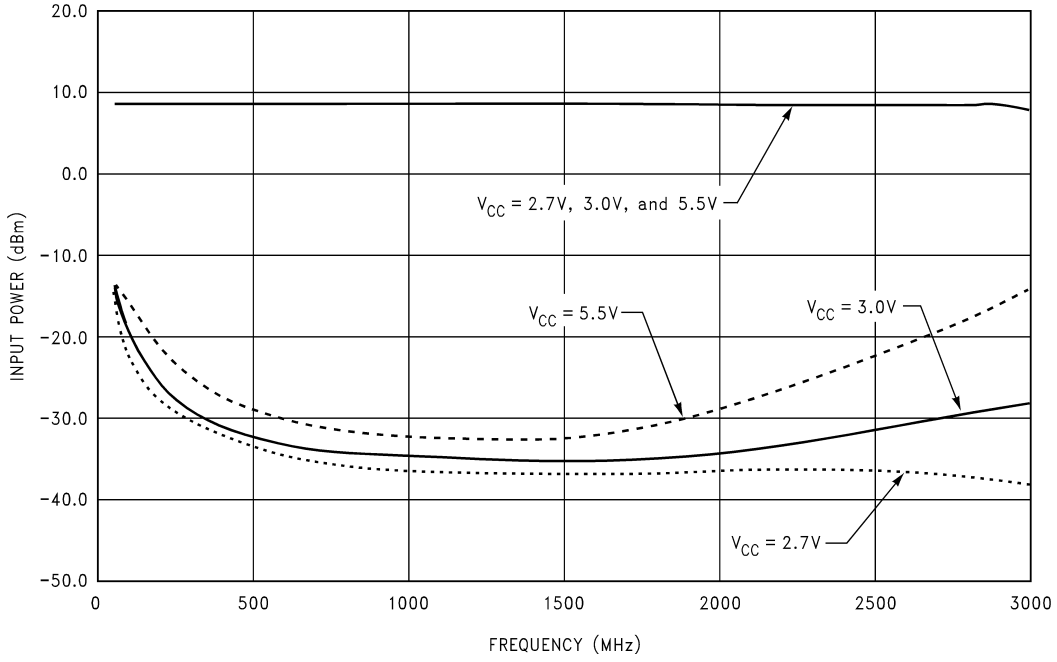
IF PLL 1 Hz Normalized Phase Noise



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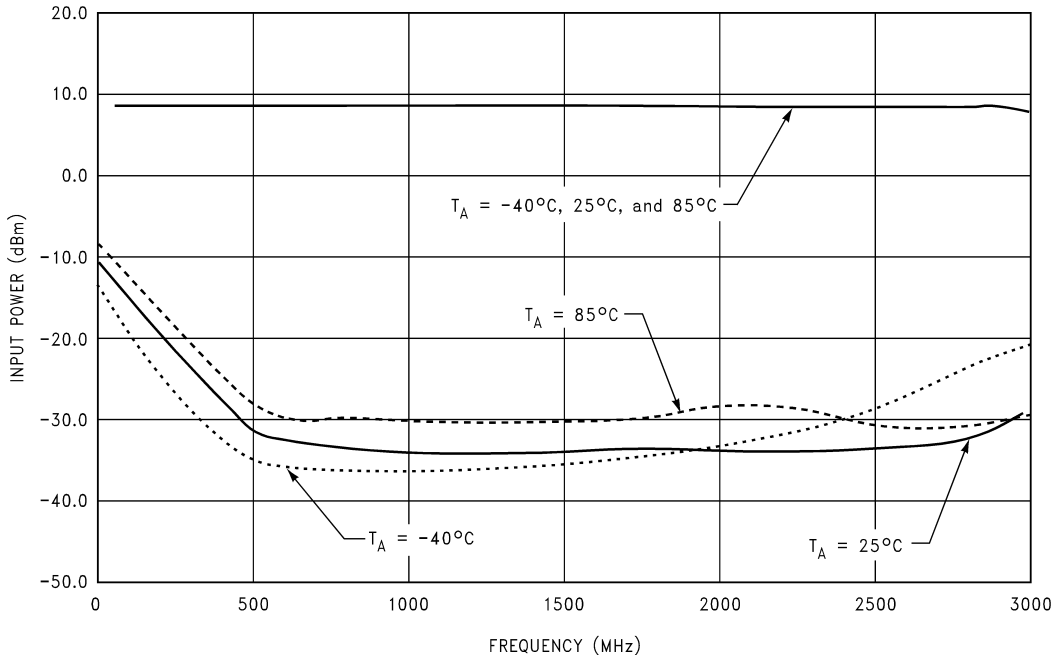
Typical Performance Characteristics (Continued)

RF N Counter Sensitivity
T_A = 25˚C



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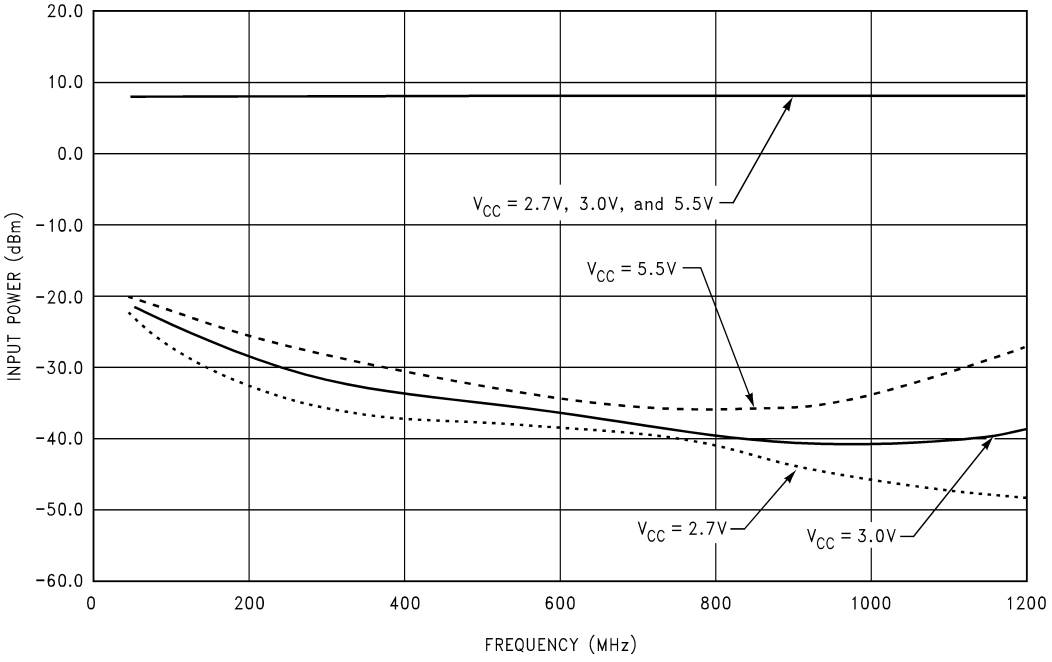
RF N Counter Sensitivity
Vcc = 3.0V



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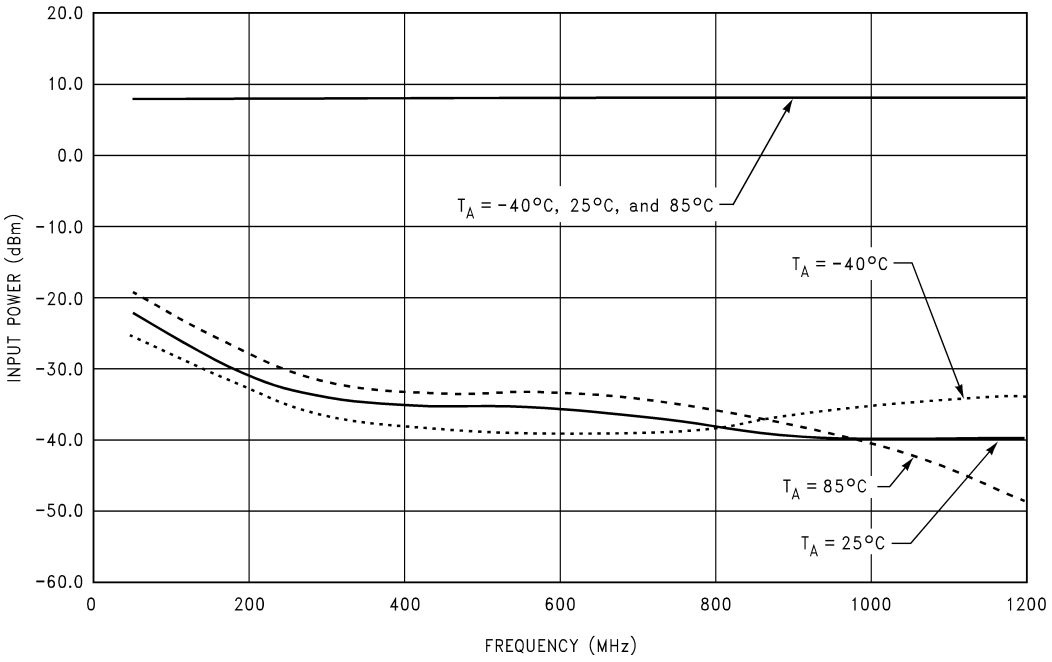
Typical Performance Characteristics (Continued)

IF N Counter Sensitivity
T_A = 25˚C



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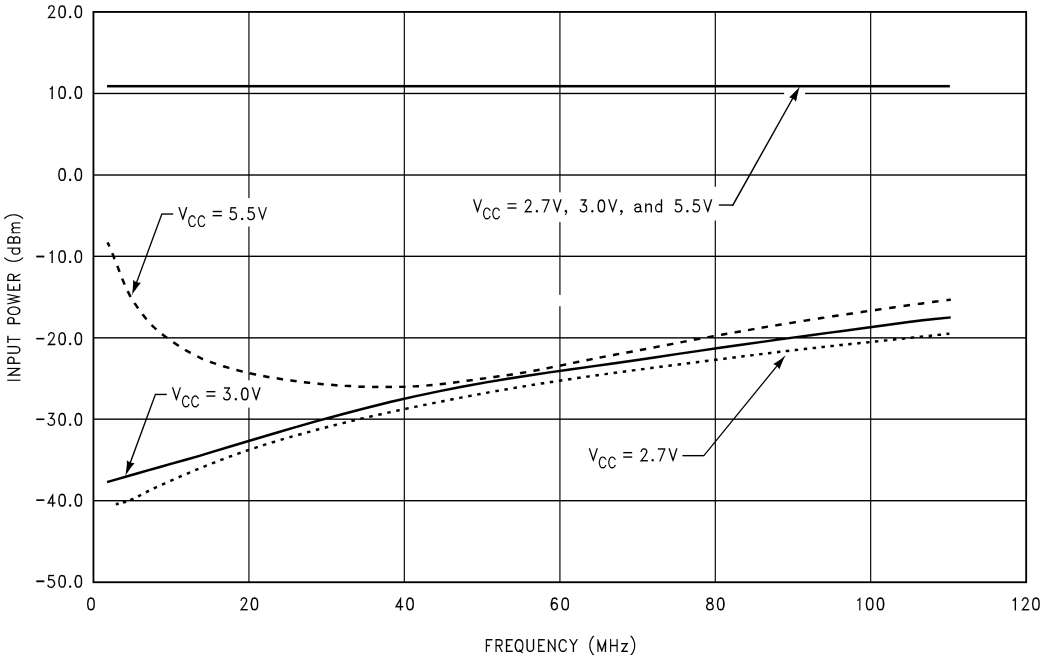
IF N Counter Sensitivity
Vcc = 3.0V



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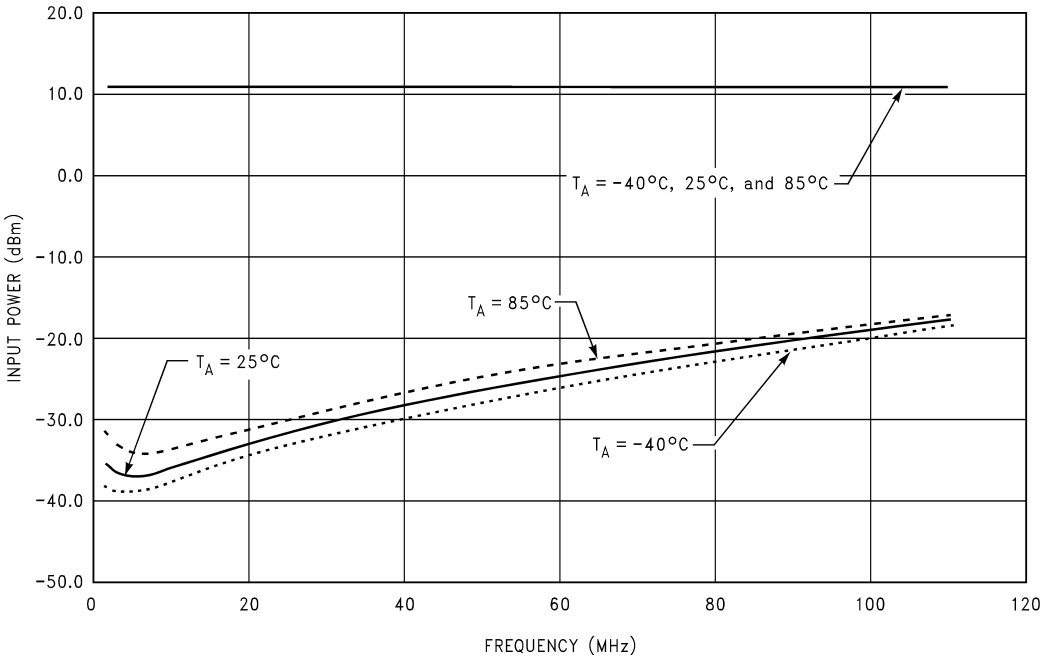
Typical Performance Characteristics (Continued)

OSCinRF Counter Sensitivity
T_A = 25˚C



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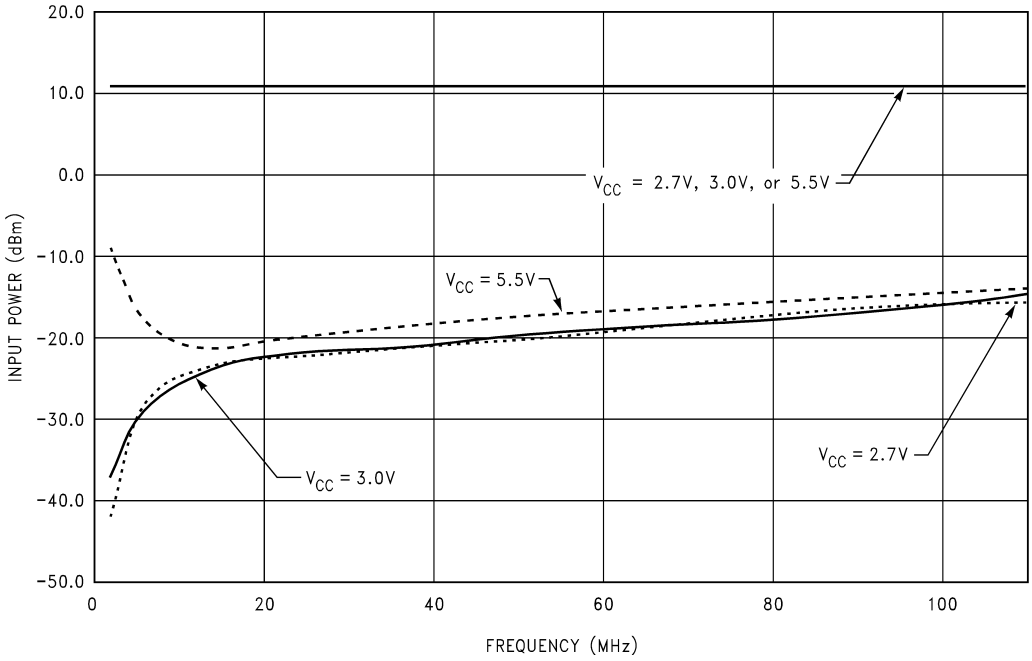
OSCinRF Counter Sensitivity
Vcc = 3.0V



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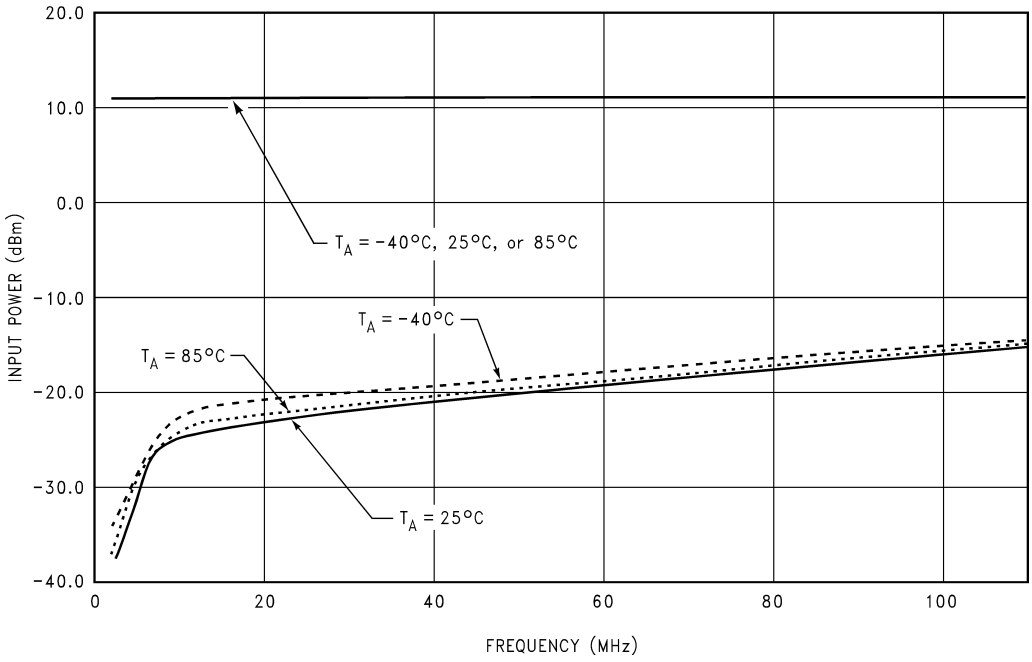
Typical Performance Characteristics (Continued)

OSCinIF Counter Sensitivity
T_A = 25˚C



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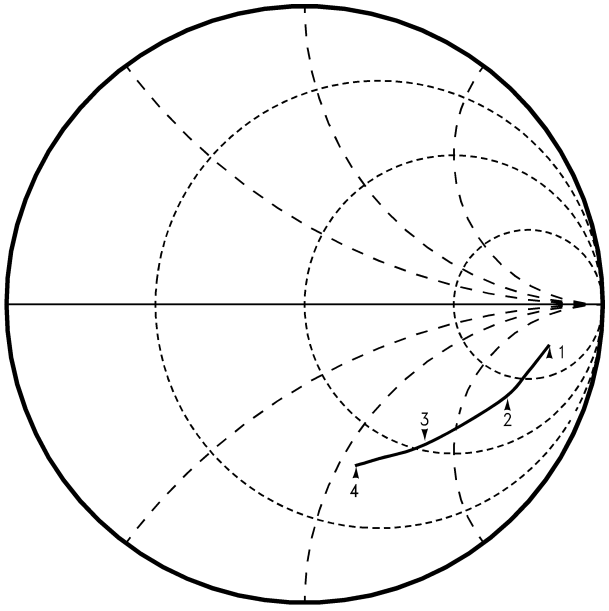
OSCinIF Counter Sensitivity
Vcc = 3.0V



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Input Impedance: FinRF Pin

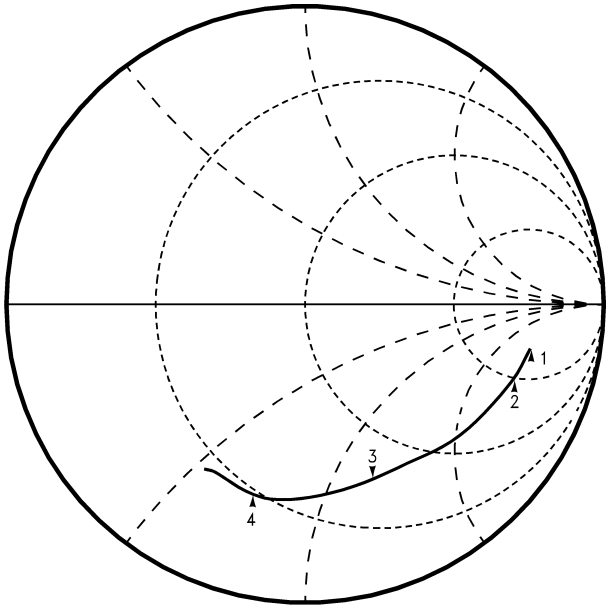
CSP Package



Marker 1 = 500 MHz
Marker 2 = 1 GHz
Marker 3 = 2 GHz
Marker 4 = 3 GHz

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TSSOP Package



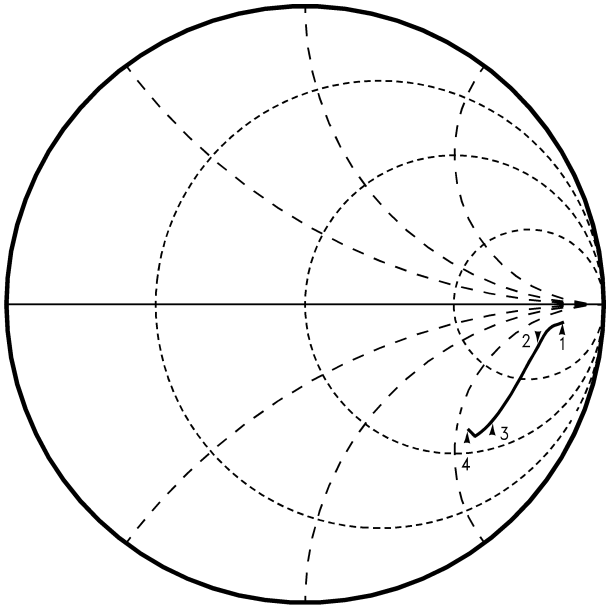
Marker 1 = 500 MHz
Marker 2 = 1 GHz
Marker 3 = 2 GHz
Marker 4 = 3 GHz

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FinRF Input Impedance (Ohms)				
Frequency (MHz)	CSP Package		TSSOP Package	
	Real	Imaginary	Real	Imaginary
500	195	-234	278	-215
750	128	-183	213	-196
1000	98	-152	151	-173
1250	77	-125	96	-133
1500	67	-106	63	-99
1750	59	-92	44	-82
2000	53	-81	35	-62
2250	46	-80	26	-53
2500	43	-67	21	-46
2750	41	-61	17	-36
3000	38	-58	15	-26

Input Impedance: FinIF Pin

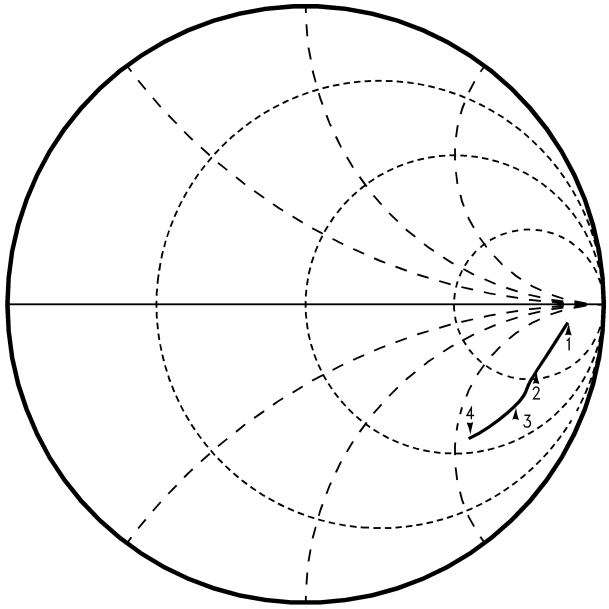
CSP Package



Marker 1 = 110 MHz
Marker 2 = 500 MHz
Marker 3 = 900 MHz
Marker 4 = 1.5 GHz

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TSSOP Package



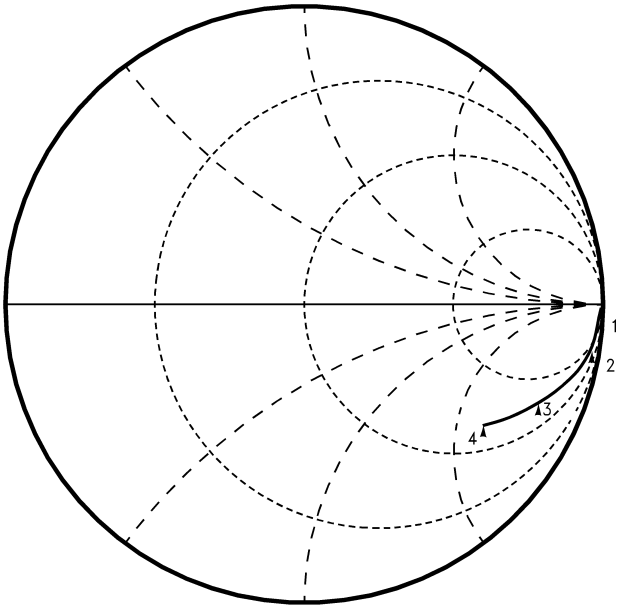
Marker 1 = 50 MHz
Marker 2 = 500 MHz
Marker 3 = 900 MHz
Marker 4 = 1.2 GHz

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FinIF Input Impedance (ohms)				
Frequency (MHz)	CSP Package		TSSOP Package	
	Real	Imaginary	Real	Imaginary
100	504	-279	505	-222
200	374	-280	414	-205
300	283	-270	349	-198
400	222	-250	295	-194
500	179	-230	243	-190
600	150	-209	190	-183
700	129	-193	141	-168
800	112	-176	110	-151
900	99	-163	86	-138
1000	98	-151	72	-125
1100	82	-140	65	-118
1200	76	-131	64	-116

Input Impedance: OSCinIF Pin

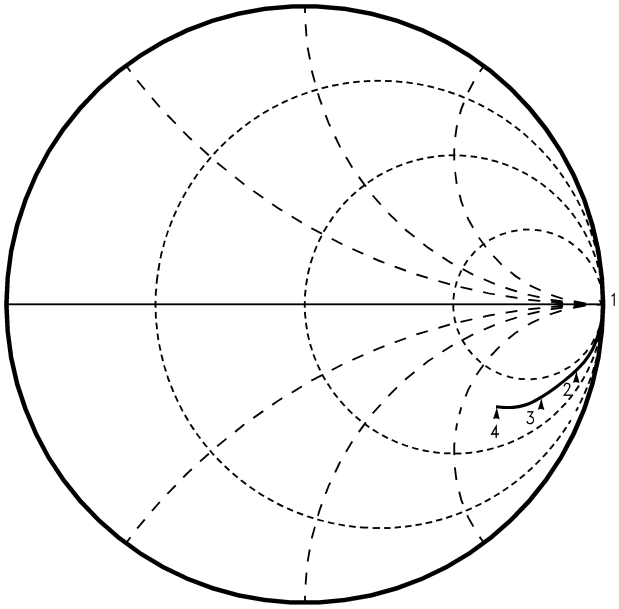
CSP Package



Marker 1 = 10 MHz
Marker 2 = 50 MHz
Marker 3 = 100 MHz
Marker 4 = 200 MHz

20050655

TSSOP Package



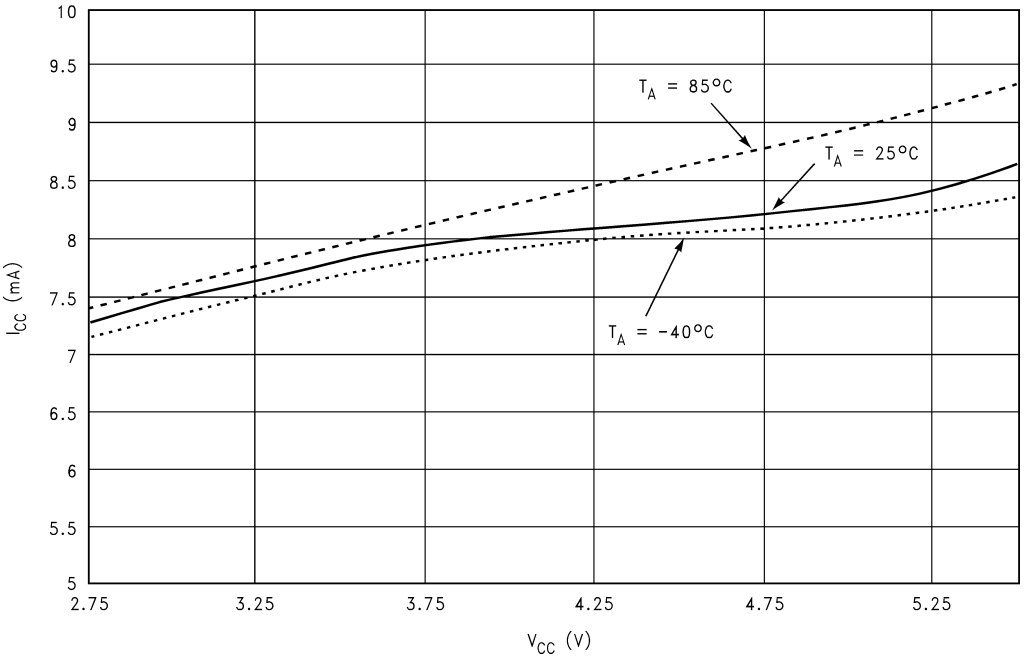
Marker 1 = 10 MHz
Marker 2 = 50 MHz
Marker 3 = 100 MHz
Marker 4 = 200 MHz

20050658

OSCinIF Input Impedance (ohms)								
Frequency (MHz)	CSP Package				TSSOP Package			
	Powered Up		Powered Down		Powered Up		Powered Down	
	Real	Imaginary	Real	Imaginary	Real	Imaginary	Real	Imaginary
10	338	-2741	143	-3239	326	-2100	147	-2400
25	130	-1098	92	-1281	112	-909	84	-1100
50	97	-552	81	-645	86	-463	75	-538
75	89	-366	77	-428	81	-320	71	-372
100	84	-276	75	-322	81	-247	72	-284
110	83	-251	75	-292	82	-230	76	-261

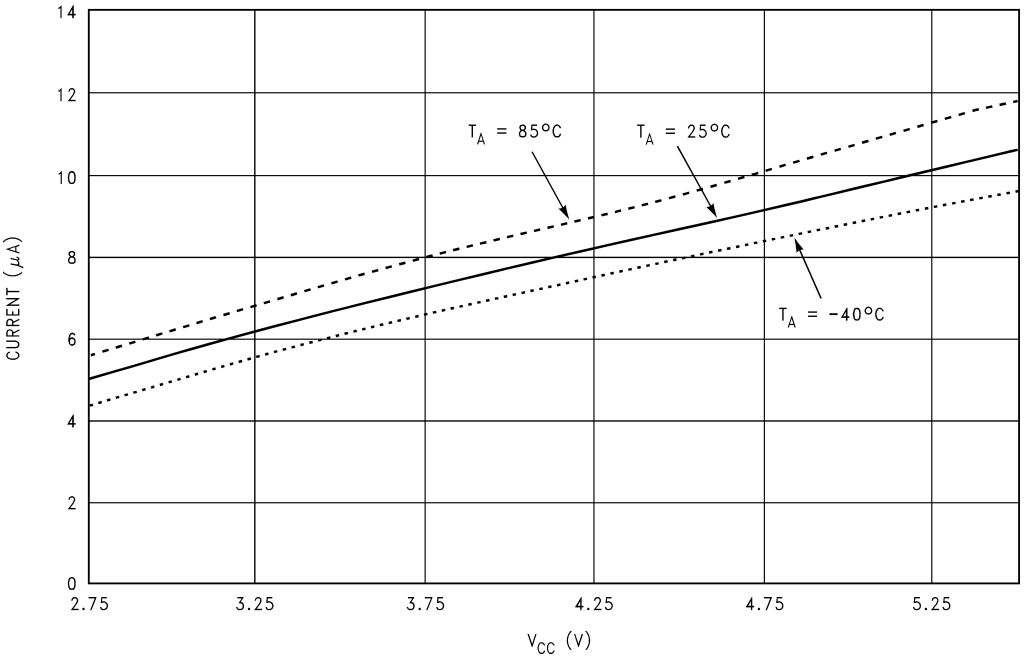
Typical Performance Characteristics

Total Current Consumption
RF_OM=1



20050660

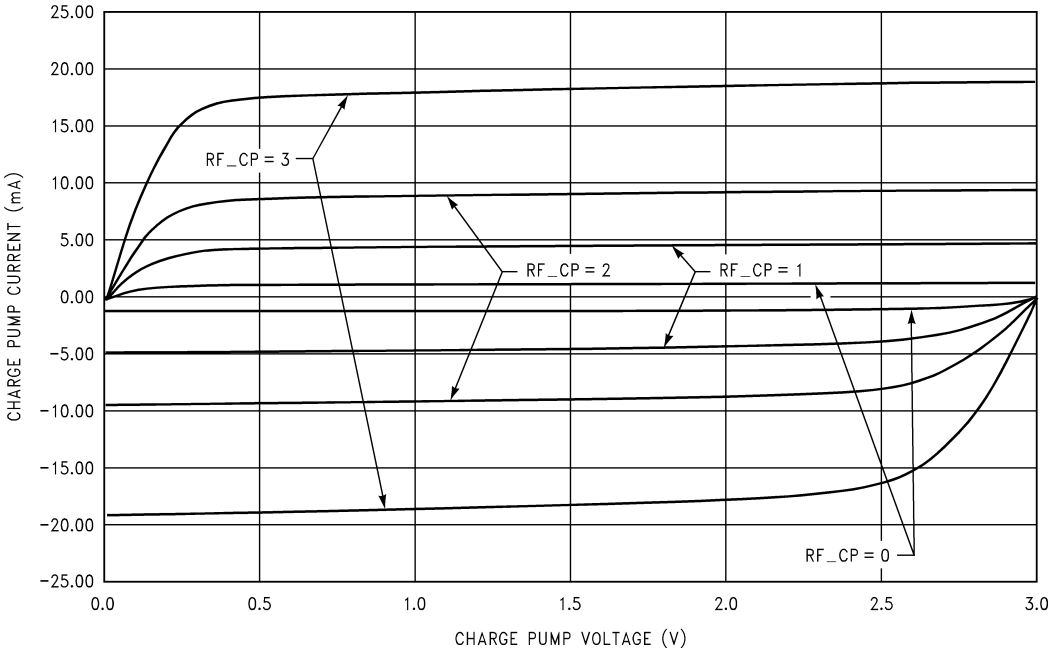
Powerdown Current
V_{ENRF} = V_{ENIF} = 0V



20050661

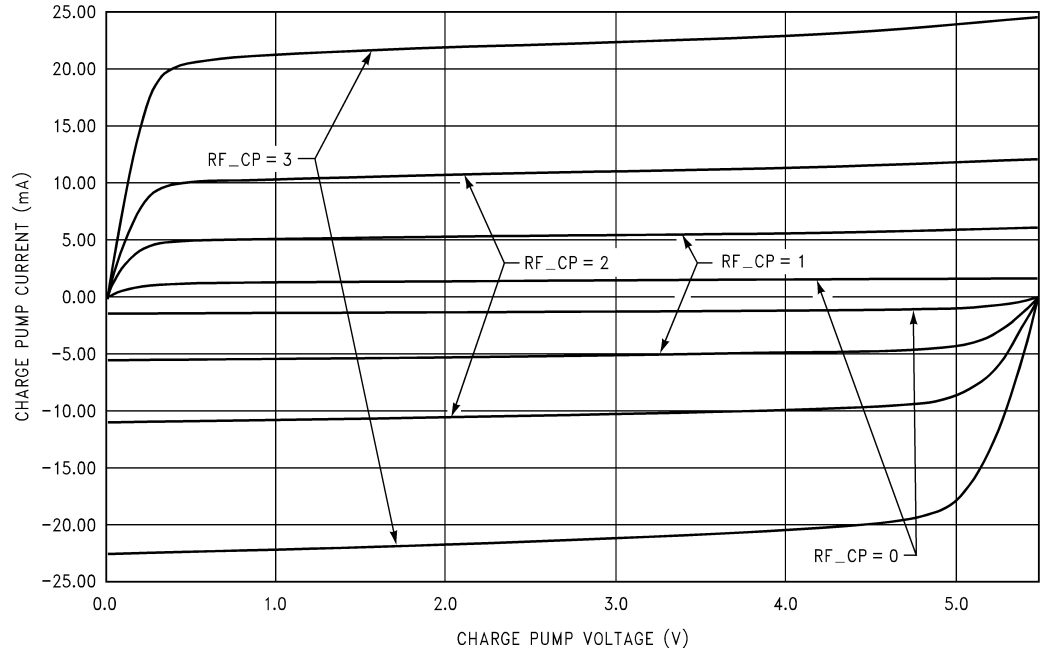
Typical Performance Characteristics (Continued)

RF Charge Pump Current
V_{VcpRF} = 3.0V



20050667

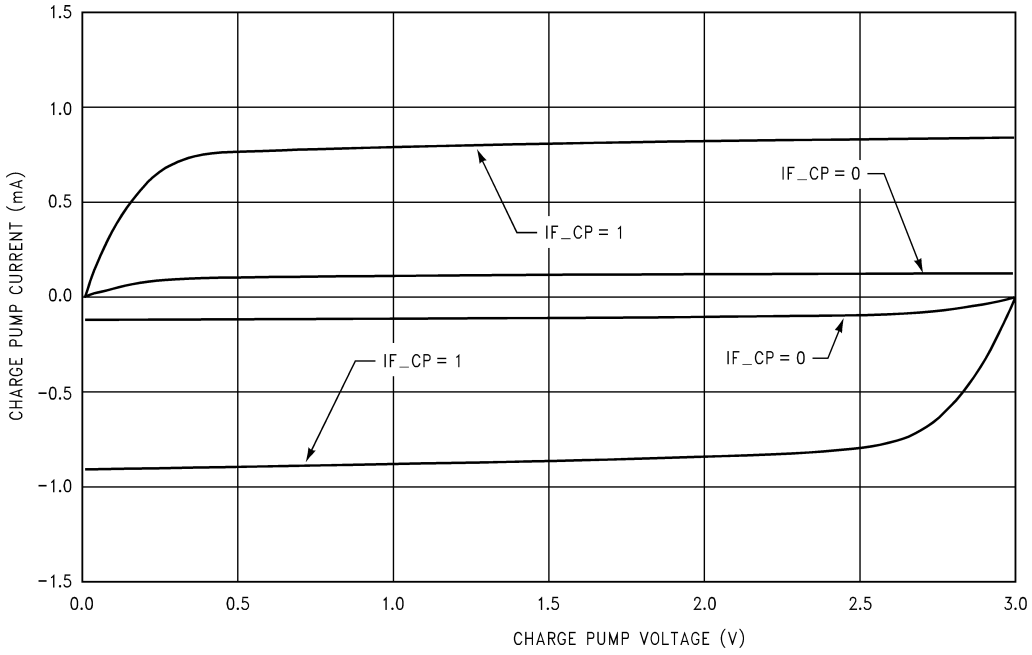
RF Charge Pump Current
V_{VcpRF} = 5.0V



20050668

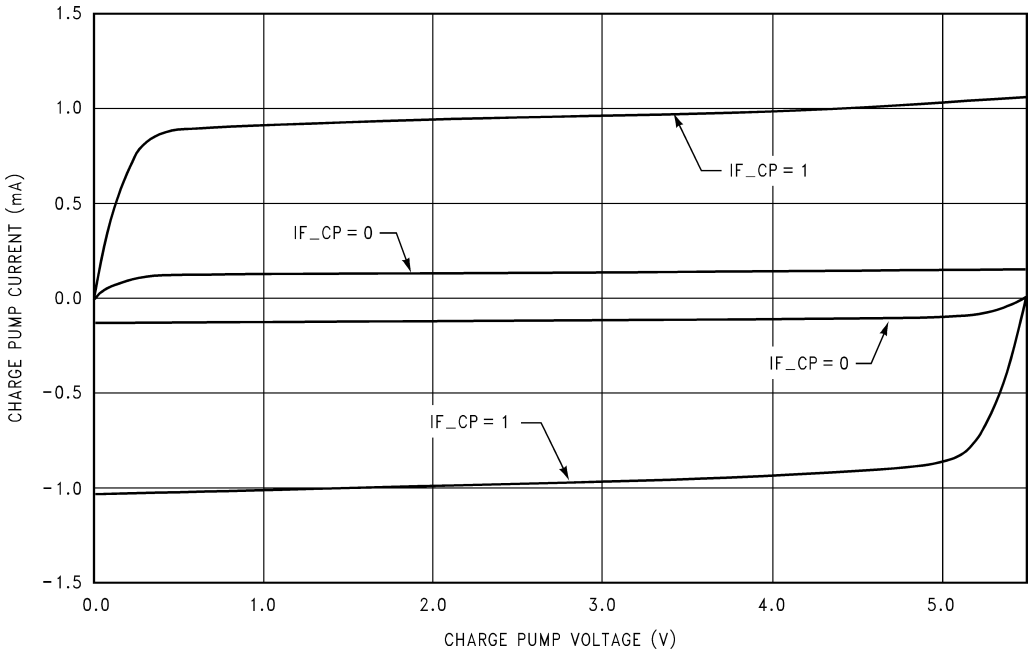
Typical Performance Characteristics (Continued)

IF Charge Pump Current
V_{VcpIF} = 3.0V



20050665

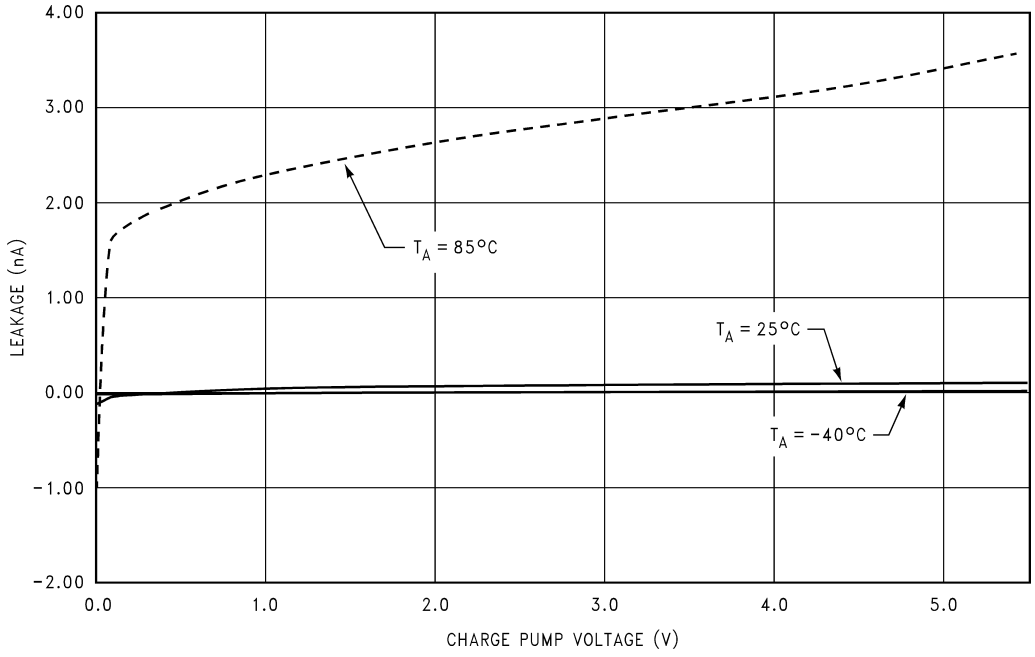
IF Charge Pump Current
V_{VcpIF} = 5.0V



20050666

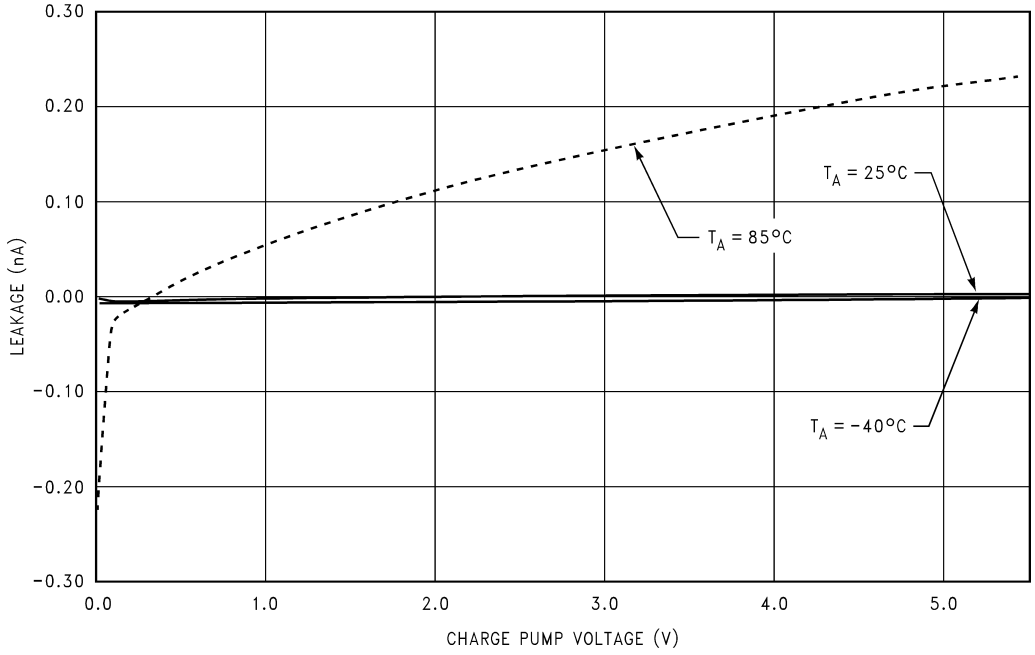
Typical Performance Characteristics (Continued)

Charge Pump Leakage
RF PLL



20050664

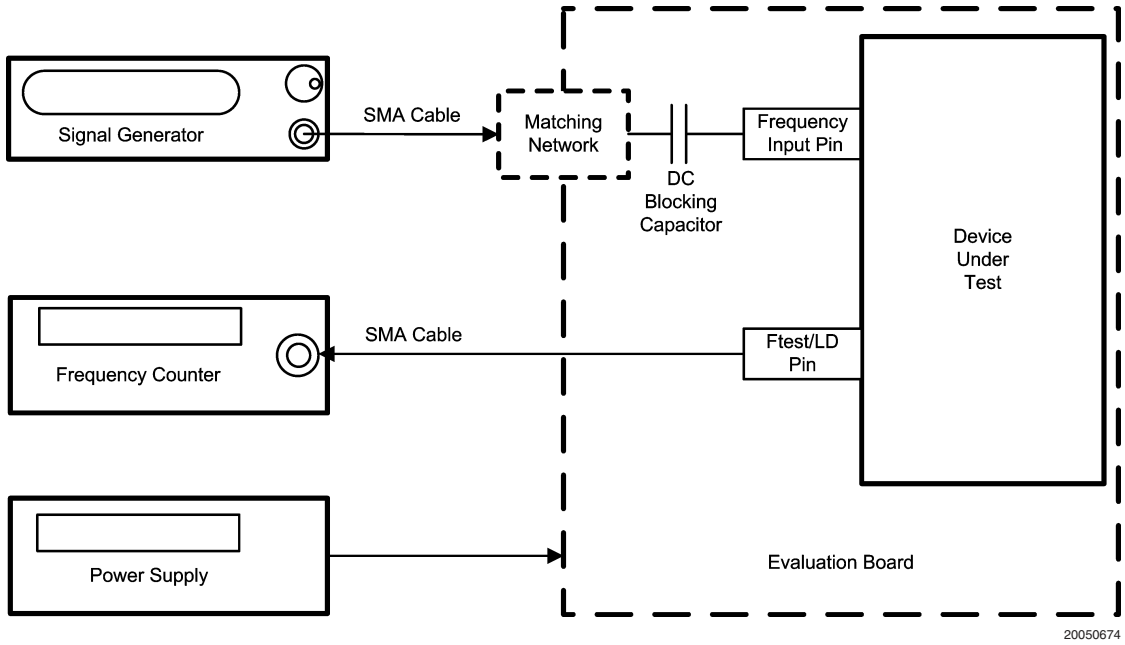
Charge Pump Leakage
IF PLL



20050663

Test Setup Procedures

Sensitivity



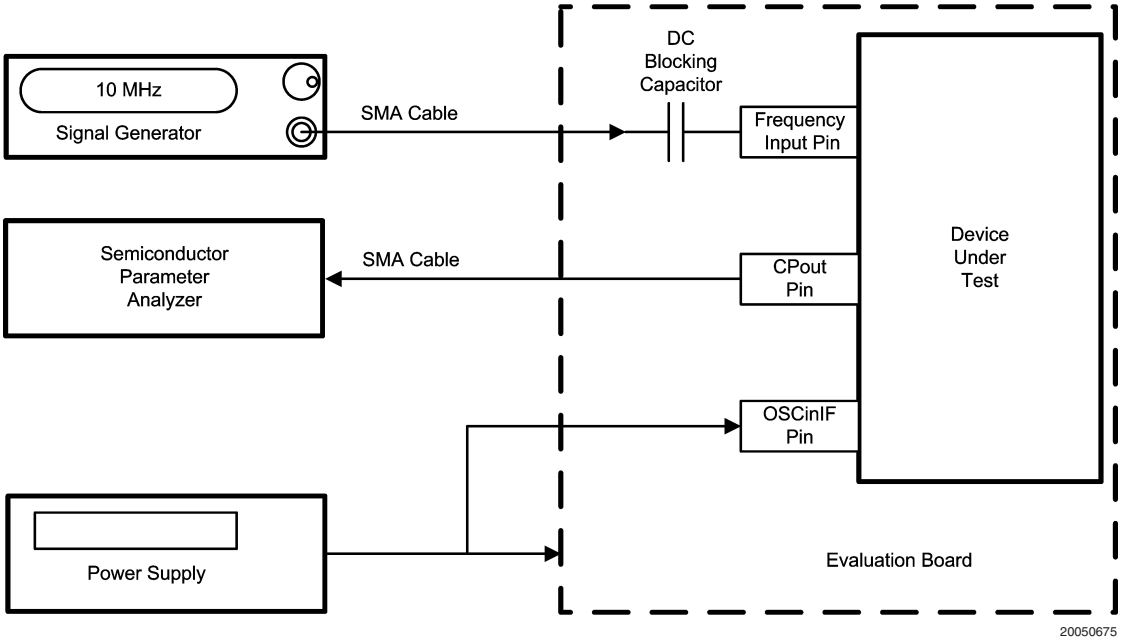
Frequency Input Pin	DC Blocking Capacitor	Corresponding Counter	Default Counter Value	MUX Value
OSCinIF	1 nF	IF_R/RF_R	5000	9 (IF R/2)
FinIF	100 pF	IF_N	5000	10 (IF N/2)
OSCinRF	1 nF	RF_R	50	11 (RF R/2)
FinRF	100 pF	RF_N	50	12 (RF N/2)

Sensitivity is defined as the power level limits beyond which the output of the counter being tested is off by 1 Hz or more of its expected value. It is typically measured over frequency, voltage, and temperature. In order to test sensitivity, the MUX[3:0] word is programmed to the appropriate value. The counter value isthen programmed to a fixed value and a frequency counter is set to monitor the frequency of this pin. The expected frequency at the Ftest/LD pin should be the signal generator frequency divided by twice the corresponding counter value. The factor of two comes in because the LMX2364 has a flip-flop which divides this frequency by two to make the duty cycle 50% in order to make it easier to read with the frequency counter. The frequency counter input impedance should be set to high impedance.

In order to perform the measurement, the temperature, frequency, and voltage is set to a fixed value and the power level of the signal is varied. Note that the power level at the part is assumed to be 4 dB less than the signal generator power level. This accounts for 1 dB for cable losses and 3 dB for the pad. The power level range where the frequency is correct at the Ftest/LD pin to within 1 Hz accuracy is recorded for the sensitivity limits. The temperature, frequency, and voltage can be varied in order to produce a family of sensitivity curves. Since this is an open-loop test, the charge pump is set to TRI-STATE and the unused side of the PLL (RF or IF) is powered down when not being tested.

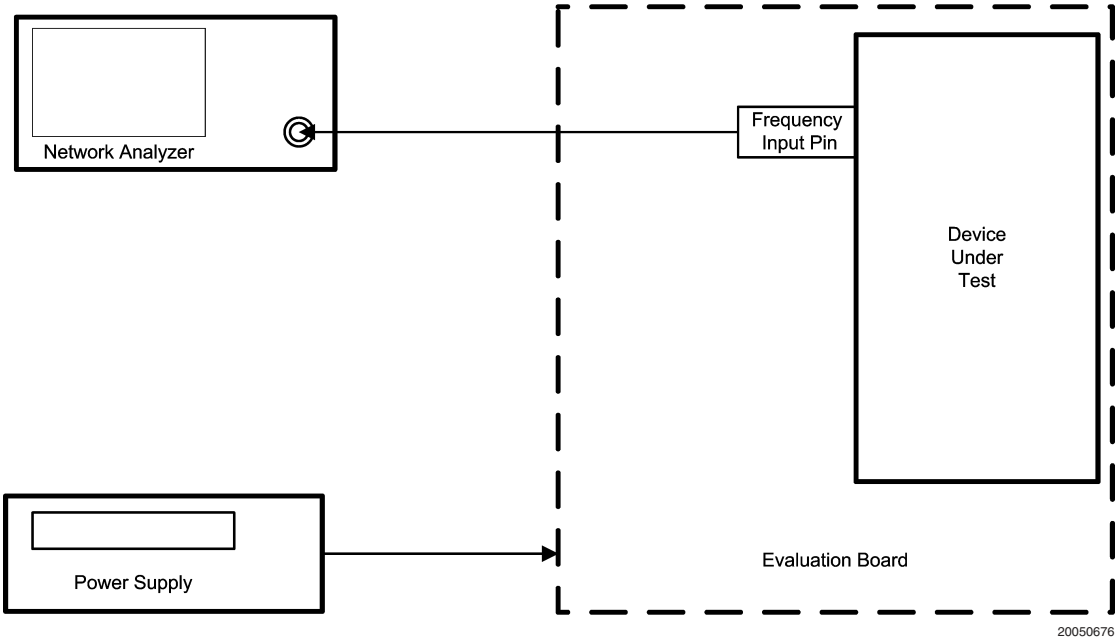
For this part, there are actually four frequency input pins, although there is only one frequency test pin (Ftest/LD). The conditions specific to each pin are show above.

Charge Pump Currents



The above block diagram shows the test procedure for testing the RF and IF charge pumps. These tests include absolute current level, mismatch, and leakage. In order to measure the charge pump currents, a signal is applied to the high frequency input pins. The reason for this is to guarantee that the phase detector gets enough transitions in order to be able to change states. If no signal is applied, it is possible that the charge pump current reading will be low due to the fact that the duty cycle is not 100%. The OSCinIF Pin is tied to the supply. The charge pump currents can be measured by simply programming the phase detector to the necessary polarity. For instance, in order to measure the RF charge pump current, a 10 MHz signal is applied to the FinRF pin. The source current can be measured by setting the RF PLL phase detector to a positive polarity, and the sink current can be measured by setting the phase detector to a negative polarity. The IF PLL currents can be measured in a similar way. Note that the magnitude of the RF and IF PLL charge pump currents are also controlled by the RF_CP and IF_CP bits. Once the charge pump currents are known, the mismatch can be calculated as well. In order to measure leakage currents, the charge pump current is set to a TRI-STATE mode by enabling the counter reset bits. This is RF_RST for the RF PLL and IF_RST for the IF PLL.

Input Impedance



The above block diagram shows the test procedure measuring the input impedance for the LMX2364. This applies to the FinRF, FinIF, OSCinRF, and OSCinIF pins. The input impedance of the CSP and the TSSOP package should always be assumed to be different, until proven otherwise. The basic test procedure is to calibrate the network analyzer, ensure that the part is powered up, and then measure the input impedance.

The network analyzer can be calibrated by using either calibration standards or by soldering resistors directly to the evaluation board. An open can be implemented by putting no resistor, a short can be implemented by using a 0 ohm resistor, and a short can be implemented by using two 100 ohm resistors in parallel. Note that no DC blocking capacitor is used for this test procedure. This is done with the PLL removed from the PCB. This requires the use of a clamp down fixture that may not always be generally available. If no clamp down fixture is available, then this procedure can be done by calibrating up to the point where the DC blocking capacitor usually is, and then adding a 0 ohm resistor back for the actual measurement.

Once that the network analyzer is calibrated, it is necessary to ensure that the PLL is powered up. This can be done by toggling the power down bits (RF_PD and IF_PD) and observing that the current consumption indeed increases when the bit is disabled. Sometimes it may be necessary to apply a signal to the OSCinIF pin in order to program the part. If this is necessary, disconnect the signal once it is established that the part is powered up.

It is useful to know the input impedance of the PLL for the purposes of debugging RF problems and designing matching networks. Another use of knowing this parameter is make the trace width on the PCB such that the input impedance of this trace matches the real part of the input impedance of the PLL frequency of operation. In general, it is good practice to keep trace lengths short and make designs that are relatively resistant to variations in the input impedance of the PLL.

Functional Description

1.0 GENERAL

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2364, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, charge pump, and programmable frequency dividers. These dividers are the reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R counter to obtain a frequency in order to establish the comparison frequency. This comparison frequency, f_{COMP}, is input to the phase detector, which compares this signal to another signal, f_N, the feedback signal. f_N is the result of dividing the VCO frequency down by way of the N counter and fractional circuitry. The phase/frequency detector's charge pump outputs a current into the loop filter, which is then converted into the VCO's control voltage. The phase/frequency comparator's function is to adjust the voltage presented to the VCO until the feedback signal's frequency (and phase) match that of the reference signal. When this 'phase-locked' condition exists, the VCO's frequency will be N+F times that of the comparison frequency, where N is the integer component of the divide ratio and F is the fractional component. Fractional synthesis allows the phase detector frequency to be increased while maintaining the same frequency step size for channel selection. The division value N is thereby reduced giving a lower phase noise referred to the phase detector input, and the comparison frequency is increased allowing faster switching times.

1.1 OPERATING MODES

The LMX2364 RF PLL is a capable of operating as both a Fractional N synthesizer and an Integer N synthesizer. Operating in Fractional mode is likely to yield the best phase noise, but Integer mode often yields the lowest spur levels. The operating mode is determined by the RF_OM[1:0] word. It is possible to cause this PLL to behave as an integer PLL in fractional mode by setting the fractional numerator, RF_FN, to zero and disabling the fractional compensation that is controlled by the FE bit. However, by actually setting the part to Integer mode allows the range of the counters to be extended.

1.2 POWER DOWN

The LMX2364 can be powered down via the two software bits and the two enable pins. The RF PLL is only powered up when the ENRF pin is high and the RF_PD bit (R4[23]) is low. In a similar manner, the IF PLL is powered up only when the ENIF pin is high and the IF_PD bit (R1[23]) is low.

1.3 OSCILLATOR

The OSCinRF and OSCinIFpins are used to drive the R dividers for the RF and IF PLLs. In the case that the OSC Bit (R6[7]) is set to 0, the RF R counter is driven by the OSCinRF pin and the IF R counter is driven independently of this by the OSCinIF pin. In the case that both R counters are to be driven with the same frequency, this bit needs to be set to one. This PLL does not support the use of a crystal in any mode.

Programming Description

2.0 INPUT DATA REGISTER

The 24-bit input data register is loaded through the MICROWIRE Interface. The input data register is used to program the control registers. The data format of the 24-bit data register is shown below. The control bits (CTL[2:0]) decode the internal register address and the data bits (DATA[21:0]) are used to program various control words for the synthesizer. On the rising edge of LE, data stored in the input date register is loaded into one of the 8 appropriate latches (selected by control bits). Data is shifted in MSB first

MSB		LSB
DATA [21:0]		CTL[2:0]
23	3	2 0

2.1 REGISTER LOCATION TRUTH TABLE

The control bits CTL[2:0] decode the internal register address. The table below shows how the control bits are mapped to the target control register.

CTL[2:0]	Target Control Register
0	R0
1	R1
2	R2
3	R3
4	R4
5	R5
6	R6
7	This address is invalid.

2.2 CONTROL REGISTER CONTENT MAP

The control register content map describes how the bits within each control register are allocated to specific control functions. The bits that are marked “0” should be programmed as such to insure proper device operation. It is important to note that some control words are dual mapped and take one a different control function depending on the operating mode of the device.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R0	0	0	0	IF_RST	IF_CP	IF_CPP	IF_R[14:0]															0	0	0
R1	IF_PD	0	0	0	IF_N[16:0]																	0	0	1
R2	0	0	0	0	0	0	0	IF_TOC[13:0]														0	1	0
R3	RF_RST	RF_P	RF_CPP	RF_CP[1:0]			RF_R[8:0]								RF_FD[6:0]							0	1	1
R4	RF_PD	RF_N[12:0]													RF_FN[6:0]							1	0	0
R5	0	RF_CSR[1:0]		RF_OM[1:0]		RF_CPF[1:0]		RF_TOC[13:0]														1	0	1
R6	0	0	0	0	0	0	0	FE	0	0	0	0	0	0	0	PD_M	OSC	MUX[3:0]				1	1	0

Programming Description (Continued)

2.3 R0 REGISTER

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R0	0	0	0	IF_RST	IF_CP	IF_CPP	IF_R[14:0]															0	0	0

2.3.1 IF_R[14:0] — R Divider Ratio, IF Synthesizer

The R0 control word is used to configure the 15 Bit R Divider for the IF Synthesizer. Divide ratios ranging from 3 to 32,767 are supported.

	IF_R[14:0]														
Divide Ratio	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32,767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.3.2 IF_CPP — Charge Pump Polarity, IF Synthesizer

This bit controls the polarity of phase detector for the IF synthesizer. It should be set to “1” when the IF VCO has positive tuning gain, and “0” when the tuning gain is negative.

2.3.3 IF_CP — Charge Pump Gain, IF Synthesizer

This bit controls the charge pump gain for the IF Synthesizer. Set this bit to 0 for low gain mode (100 uA) and a 1 for high gain mode (800 uA). When FastLock mode is enabled, the charge pump gain is controlled by the FastLock circuit.

2.3.4 IF_RST — Counter Reset, IF Synthesizer

The IF Counter Reset enable bit when activated (IF_RST = 1) allows the reset of both the IF N and R dividers and sets the IF charge pump to a TRI-STATE condition®. Upon powering up, the N counter resumes counting in "close" alignment with the R counter. The maximum error is one prescaler cycle.

Programming Description (Continued)

2.4 R1 REGISTER

This register is used to configure the N divider for the IF synthesizer. A single word write to this register is all that is required to power up and tune the synthesizer to the desired frequency.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R1	IF_PD	0	0	0	IF_N[16:0]																	0	0	1

2.4.1 IF_N[16:0] — N Divider Ratio,IF Synthesizer

The IF_N[16:0] word is used to setup up the N Divider Ratio for the IF synthesizer. The IF N counter is actually a combination of an IF A counter, IF B counter, and an IF 8/9 prescaler. The relationship between IF_N, IF_B, and IF_A is shown below.

$$IF_N = 8 \times IF_B + IF_A$$

Although the IF_N counter value can created by programming the IF_B and IF_A values, it is easier to simply convert the IF N counter value into binary and program the entire IF_N[16:0] word in this manner. The fact that the IF N counter has a prescaler is what puts restrictions on IF_N values less than 56.

	IF_N[16:0]																	
	IF_B[13:0]														IF_A[2:0]			
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0-23	Divide ratios of less than 24 are not allowed.																	
24-55	Legal divide ratios in this range are: 24-27, 32-36, 40-45, and 48-54.																	
56	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	
57	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	
131071	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

2.4.2 IF_PD — Power Down, IF Synthesizer

Activation of the IF Synthesizer power down bit results in the disabling of the respective N divider and de-biasing of its respective Fin inputs (to a high impedance state). The respective R divider functionality also becomes disabled when the power down bit is activated. The OSCinIF pin reverts to a high impedance state when both RF and IF power down bits are asserted. Power down forces the respective charge pump and phase comparator logic to a TRI-STATE condition. The MICROWIRE control register remains active and capable of loading and latching in data during all of the power down modes.

Both synchronous and asynchronous power down modes are supported. The power down mode bit R6[8] is used to select between synchronous and asynchronous power down. The MICROWIRE control register remains active and capable of loading and latching in data in either power down mode.

Synchronous Power Down Mode: The IF synthesizer can be synchronously powered down by first setting the power down mode bit HIGH (R6[8] = 1) and then asserting its power down bit (R1[23] = 1). The power down function is gated by the charge pump. Once the power down bit is loaded, the part will go into power down mode upon the completion of a charge pump pulse event.

Asynchronous Power Down Mode: The IF synthesizer can be asynchronously powered down by first setting the power down mode bit LOW (R6[8] = 0) and then asserting its power down bit (R1[23]] = 1). The power down function is NOT gated by the charge pump. Once the power down bit is loaded, the part will go into power down mode immediately

Programming Description (Continued)

2.5 R2 REGISTER

The R2 Register is used to setup the FastLock circuitry for the IF synthesizer.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R2	0	0	0	0	0	0	0	IF_TOC[13:0]														0	1	0

2.5.1 IF_TOC[13:0] — FastLock Timeout Counter, IF Synthesizer

The IF_TOC[13:0] word controls the operation of the IF FastLock circuitry as well as the function of the FLoutIF output pin. When IF_TOC is set to a value between 0 and 3, the IF timeout counter is disabled and the FLoutIF pin operates as a general purpose I/O pin. When IF_TOC is set to a value between 4 and 16383, the IF FastLock mode is enabled and FLoutIF is utilized as the IF FastLock output pin. The value programmed into IF_TOC represents the number of phase comparison cycles that the IF synthesizer will spend in the FastLock state.

IF_TOC[13:0]	FastLock Mode	FastLock Period [CP Events]	FLoutIF Pin Functionality
0	Disabled	N/A	High Impedance
1	Disabled	N/A	Logic LOW State
2	Manual	N/A	Logic LOW State. Force IF Charge Pump to 800 µA
3	Disabled	3	Logic HIGH State
4	Enabled	4	FastLock
…	Enabled	…	FastLock
16,383	Enabled	16383	FastLock

Programming Description (Continued)

2.6 R3 REGISTER

The R3 register is used to setup the RF R Divider ratio as well as several other control functions related to the RF synthesizer.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R3	RF_RST	RF_P	RF_CPP	RF_CP[1:0]		RF_R[8:0]									RF_FD[6:0]							0	1	1

2.6.1 RF_FD[6:0] — Fractional Denominator, RF Synthesizer

In Fractional Mode, RF_FD[6:0] is used to specify the fractional denominator of the fractional part of the N counter value. Note that in this mode, values below 32 are not supported. If a fractional denominator between 2 and 32 is desired, the same N counter value can be achieved by multiplying the fractional numerator and denominator by some constant factor. For instance, 1/16 can be expressed as 5/80.

In integer mode, the value represented by this bit multiplies both the RF_N and RF_R counter values. If both of these counter sizes are sufficiently large, it is recommended to set this bit to one. If the counter sizes are too small, this bit can be used to extend the counter range.

RF_FD[6:0]	RF_FD Value	
	Integer Mode	Fractional Mode
	[RF_OM = 0]	RF_OM = 1
0	128	128
1	1	Not Supported (Use Integer Mode Instead)
…	…	Not Supported (Use a higher value)
32	32	32
33	33	33
34	34	34
…	…	…
127	127	127

Value	Fractional Mode (RF_OM=1)	Integer Mode (RF_OM=0)
R Divider Value	RF_R	RF_R x RF_FD
Complete N Divider Value	RF_N x RF_FN/RF_FD	RF_N x RF_FD + RF_FN

See R divider programming (section 2.6.2) and N divider programming (Section 2.7.2) for more detailed programming information.

2.6.2 RF_R[8:0] — R Divider Ratio, RF Synthesizer

RF_R[8:0] is used to specify an integer value from 1 to 511 that is used in calculating the R divider ratio for the RF synthesizer. In the case that the PLL is operating in fractional mode, the R counter value is simply the value represented by RF_R. However, in integer mode, the R counter value is calculated by multiplying RF_R by the fractional denominator value.

R (Integer Mode) = RF_R x RF_FD

Since RF_R can take on integer values between 1 – 511 and RF_FD can take on integer values between 1 – 128, this value can range from 1 - 65408, although prime values between 512 and 65,408 can not be realized.

RF_R[8:0]	RF_R Value
0	Not Supported
1	1
…	…
511	511

Programming Description (Continued)

2.6.3 RF_CP[1:0] — Charge Pump Gain, RF Synthesizer

The RF_CP word is used to control the charge pump gain for the RF synthesizer. Four different CP gains are supported ranging from 1 to 16 mA. Note that when RF FastLock mode is enabled and the synthesizer is operating in the FastLock state, the charge pump gain is controlled by the RF_CPF[1:0] control word. Higher charge pump currents yield slightly better phase noise, but lead to larger loop filter capacitors and slightly higher current consumption in cases where the comparison frequency is very high.

RF_CP[1:0]	Charge Pump Current
0	1 mA
1	4 mA
2	8 mA
3	16 mA

2.6.4 RF_CPP — Phase Detector Polarity, RF Synthesizer

This bit controls the polarity of phase detector for the RF synthesizer. It should be set to one when the chosen RF VCO has positive tuning gain, and zero when the tuning gain is negative.

2.6.5 RF_P — Prescaler, RF Synthesizer

The RF synthesizer utilizes a selectable quadruple modulus prescaler. RF_P selects between the 8/9/12/13 prescaler and the 16/17/20/21 prescaler as described in the table below.

RF_P[1:0]	Selected Prescaler
0	8 (8/9/12/13)
1	16 (16/17/20/21)

2.6.6 RF_RST — Counter Reset, RF Synthesizer

The RF Counter Reset enable bit when activated (RF_RST = 1) allows the reset of both the RF N and RF R dividers. Upon powering up, the N counter resumes counting in "close" alignment with the R counter. The maximum error is one prescaler cycle.

Programming Description (Continued)

2.7 R4 REGISTER

This register is used to setup the N divider for the RF Synthesizer. A single word write to this register is all that is required to power up and tune the RF synthesizer to the desired frequency.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R4	RF_ PD	RF_N[12:0]													RF_FN[6:0]							1	0	0

2.7.1 RF_FN — Fractional Numerator, RF Synthesizer

In the case that the PLL is operating in fractional mode (RF_OM=1), RF_FN[6:0] specifies the fractional numerator of the complete N counter value of the RF PLL. In the case that the PLL is operating in integer mode (RF_OM=0), RF_FN adds to the total value of the N counter.

Operating Mode	RF N Divider Value Calculation
Fractional Mode (RF_OM=1)	RF_N +RF_FN/RF_FD
Integer Mode (RF_OM=0)	RF_N x RF_FD + RF_FN

2.7.2 RF_N[12:0] — N Divider Ratio, RF Synthesizer

RF_N[12:0] specifies an integer value that is used in calculating the N divider ratio for the RF synthesizer. In the case the part is operating in fractional mode, it value is the N divider ratio. In the case the part is operating in integer mode, this number is used in conjunction with the RF_FD and RF_FN values to calculate the N divider value. The range of values supported is dependant on the selected prescaler. When the 8/9/12/13 prescaler is selected, RF_N value can range from 40 to 4095. When the 16/17/20/21 prescaler is selected, the RF_N value can range from 80 to 8191. The following tables describe how to program a specific value of RF_N for a given prescaler.

The RF_N value is actually created using a prescaler, C counter, B counter, and an A counter. If RF_P = 16, then the RF_N[12:0] word is just the binary representation of the desired value. If RF_P = 8, then the case is similiar, except that the third LSB is disregarded in all calculations. The relationship between RF_N, RF_P, RF_A, RF_B, and RF_C is shown below.

$$RF_N = RF_P \times RF_C + 4 \times RF_B + RF_A$$

RF_N[12:0] Programming with RF_P = 16

	RF_N[12:0]												
	12	11	10	9	8	7	6	5	4	3	2	1	0
	RF_C[8:0]									RF_B [1:0]		RF_A[1:0]	
0–47	Values from 0–47 are not allowed.												
48–79	Some of these N values are allowed, others are illegal divide ratios and not allowed. Legal Divide Ratios in Fractional Mode: 48–49, 52–53, 64–66, 68–70, 72–74, 76–78 Legal Divide Ratios in Integer Mode: All these values are legal in integer mode.												
80	0	0	0	0	0	0	1	0	1	0	0	0	0
81	0	0	0	0	0	0	1	0	1	0	0	0	1
…													
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

RF_N[12:0] Programming with RF_P = 8

	RF_N[12:0]												
	12	11	10	9	8	7	6	5	4	3	2	1	0
	RF_C[8:0]									RF_B[1:0]		RF_A[1:0]	
0–23	Values from 0–23 are not allowed.												
24–39	Some of these N values are allowed, others are illegal divide ratios and not allowed. Legal Divide Ratios in Fractional Mode: 24–25, 28–29, 32–34, 36–38 Legal Divide Ratios in Integer Mode: All these values are legal in integer mode.												
40	0	0	0	0	0	0	0	1	1	X	0	0	0
41	0	0	0	0	0	0	0	1	1	X	0	0	1
…													
4095	1	1	1	1	1	1	1	1	1	X	1	1	1

Programming Description (Continued)

2.7.3 RF_PD — RF Synthesizer Power Down

Activation of the RF Synthesizer power down bit results in the disabling of the respective N divider and de-biasing of its respective Fin inputs (to a high impedance state). The respective R divider functionality also becomes disabled when the power down bit is activated. The OSCinRF pin reverts to a high impedance state when both RF and IF power down bits are asserted. Power down forces the respective charge pump and phase comparator logic to a TRI-STATE condition. The MICROWIRE control register remains active and capable of loading and latching in data during all of the power down modes.

Both synchronous and asynchronous power down modes are available with the LMX2364 in order to adapt to different types of applications. The power down mode bit R6[8] is used to select between synchronous and asynchronous power down. The MICROWIRE control register remains active and capable of loading and latching in data in either power down mode.

Synchronous Power down Mode: The RF synthesizer can be synchronously powered down by first setting the power down mode bit HIGH (R6[8] = 1) and then asserting its power down bit (R4[23] = 1). The power down function is gated by the charge pump. Once the power down bit is loaded, the part will go into power down mode upon the completion of a charge pump pulse event.

Asynchronous Power down Mode: The RF synthesizer can be asynchronously powered down by first setting the power down mode bit LOW (R6[8] = 0) and then asserting its power down bit (R4[23]] = 1). The power down function is NOT gated by the charge pump. Once the power down bit is loaded, the part will go into power down mode immediately

Programming Description (Continued)

2.8 R5 REGISTER

The R5 Register is used to setup and control the FastLock circuitry for the RF synthesizer.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R5	0	RF_CSR[1:0]		RF_OM[1:0]		RF_CPF[1:0]		RF_TOC[13:0]														1	0	1

2.8.1 RF_TOC[13:0] — FastLock Timeout Counter, RF Synthesizer

The RF_TOC[13:0] word controls the operation of the RF FastLock circuitry as well as the function of the FLoutRF output pin. When RF_TOC is set to a value between 0 and 3, the RF timeout counter is disabled and the FLoutRF pin operates as a general purpose I/O pin. When RF_TOC is set to a value between 4 and 16383, the RF FastLock mode is enabled and FLoutRF is utilized as the RF FastLock output pin. The value programmed into RF_TOC represents the number of phase comparison cycles that the RF synthesizer will spend in the FastLock state.

RF_TOC[13:0]	FastLock Mode	FastLock Period [CP Events]	FLoutRF Pin Functionality
0	Disabled	N/A	High Impedance
1	Disabled	N/A	Logic LOW State
2	Manual	N/A	Logic LOW State. Force RF Change Pump to 16 mA
3	Disabled	3	Logic HIGH State
4	Enabled	4	FastLock
…	Enabled	…	FastLock
16,383	Enabled	16383	FastLock

2.8.2 RF_CPF[1:0] — FastLock Charge Pump Gain, RF Synthesizer

The RF_CPF[1:0] word is used to control the charge pump gain for the RF synthesizer when FastLock is enabled and engaged. Four different CP gains are supported ranging from 1 to 16 mA. Note that when RF FastLock mode is disengaged or disabled the charge pump gain is controlled by RF_CP[1:0].

RF_CPF[1:0]	Charge Pump Current
0	1 mA
1	4 mA
2	8 mA
3	16 mA

2.8.3 RF_OM[1:0] — RF Synthesizer Operating Mode

RF_OM[1:0] controls the operating mode of the RF synthesizer. The various operating modes are described below:

RF Synthesizer Operating Mode Descriptions

RF_OM	FE<R6[16]>	Operating Mode	Operating Mode Description
0	0	Integer	RF synthesizer always operates as an Integer N PLL
1	1	Fractional	RF synthesizer always operates as a Fractional N PLL
2	X	Reserved	Do Not use this mode
3	X	Reserved	Do Not use this mode.

Note that the Fractional Enable Bit, FE (R6[16]) needs to be set appropriately. Enabling the fractional compensation in Integer mode always degrades performance. It is generally recommended to enable it in fractional mode, although there may be some rare exceptions that it may be set to 0.

2.8.4 RF_CSR[1:0] — Cycle Slip Reduction Control, RF Synthesizer

RF_CSR[1:0] controls the operation of the cycle slip reduction circuitry. This circuit can be used eliminate the occurrence of phase detector cycle slips when operating in Fractional Mode (RF_OM = 1). When operating in integer mode,the cycle slip reduction circuitry should be disabled by setting RF_CSR = 0.

RF_CSR	CSR State	Sample Rate Reduction Factor
0	Disabled	N/A
1	Enabled	1/2
2	Enabled	1/4
3	Enabled	1/8

Programming Description (Continued)

2.9 R6 REGISTER

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0]																					C2	C1	C0
R6	0	0	0	0	0	0	0	FE	0	0	0	0	0	0	0	PD_M	OSC	MUX[3:0]				1	1	0

2.9.1 MUX[3:0] — Coltrol Word for the Ftest/LD Pin

The MUX[3:0] control word is used to determine the function of the Ftest/LD output pin. The pin can be setup as a general-purpose CMOS TRI-STATE I/O pin, a digital filtered lock detect pin, an analog lock detect pin (push-pull or open drain output), or used to view the output of the various R & N dividers.

MUX[3:0]				Ftest/LD Output Pin Function	Output Type
0	0	0	0	Disabled	High Impedance
0	0	0	1	General Purpose I/O. Logic HIGH Output	Push-Pull
0	0	1	0	General Purpose I/O. Logic LOW Output	Push-Pull
0	0	1	1	RF & IF Analog Lock Detect (Width of narrow low pulses determines lock)	Open-Drain
0	1	0	0	RF Analog Lock Detect (Width of narrow low pulses determines lock)	Open-Drain
0	1	0	1	IF Analog Lock Detect (Width of narrow low pulses determines lock)	Open-Drain
0	1	1	0	RF & IF Digital Lock Detect (High = Lock)	Push-Pull
0	1	1	1	RF Digital Lock Detect (High = Lock)	Push-Pull
1	0	0	0	IF Digital Lock Detect (High = Lock)	Push-Pull
1	0	0	1	RF & IF Analog Lock Detect (Width of narrow low pulses determines lock)	Push-Pull
1	0	1	0	RF Analog Lock Detect (Width of narrow low pulses determines lock)	Push-Pull
1	0	1	1	IF Analog Lock Detect (Width of narrow low pulses determines lock)	Push-Pull
1	1	0	0	IF R Divider/2 (Output is divided by 2 to simplify testing)	Push-Pull
1	1	0	1	IF N Divider/2 (Output is divided by 2 to simplify testing)	Push-Pull
1	1	1	0	RF R Divider/2 (Output is divided by 2 to simplify testing)	Push-Pull
1	1	1	1	RF N Divider/2 (Output is divided by 2 to simplify testing)	Push-Pull

2.9.2 OSC — Single Resonator Mode

The OSC bit selects whether the oscillator input pins OSCinIF and OSCinRF drive the IF and RF R dividers separately or by a common input signal path. When OSC is set to 0, the OSCinIF pin drives the IF R divider while the OSCinRF pin drives the RF R divider. When the OSC bit is set to “1” the OSCinIF pin drives both the RF R and IF R counters. Note that setting the OSC mode to “1” does not allow the use of a crystal. This part does not include the inverter for use in construction of a crystal oscillator.

2.9.3 PD_M — Power Down Mode

This bit determines if a power down event for either synthesizer will be handled synchronously or asynchronously with respect to a charge pump event. Synchronous powerdown means that the PLL does not power down until the charge pump turns off. Asynchronous powerdown means that the PLL powers down, regardless of the charge pump state. When set to one, synchronous mode is enabled. When set to 0, asynchronous mode is enabled. The setting of this bit applies to both the RF & IF synthesizers.

2.9.4 FE — Fractional Compensation Enable

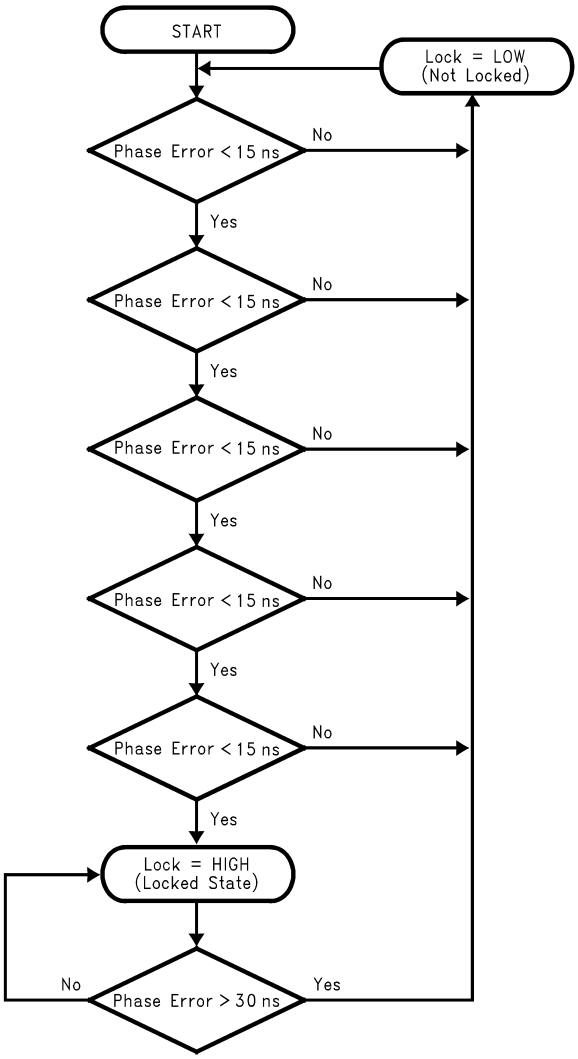
For integer mode (RF_OM = 0) mode, this bit should always be set to 0. For fractional mode (RF_OM = 1), this bit should be set to 1 for the best fractional spurs. However, there may be applications using fractional mode where it would be beneficial to set this bit to 0. Disabling this bit will drastically degrade the fractional spurs, but will also result in a small improvement in phase noise, which may be practical for some applications.

FE	Fractional Compensation Circuitry	Integer Mode	Fractional Mode	
			Approximate Spur Improvement	Approximate Phase Noise Degradation
0	Disabled	Default State	0 dB	0 dB
1	Enabled	Illegal State	20 dB	7 dB

Supplemental Information

3.0 USE OF THE DIGITAL LOCK DETECT FUNCTION

The Lock Detect Digital Filter compares the difference between the phase of the inputs of the phase detector to a RC generated delay of approximately 15nS. To enter the locked state (Lock = HIGH) the phase error must be less than the 15nS RC delay for 5 consecutive reference cycles. Once in lock (Lock = HIGH), the RC delay is changed to approximately 30nS. To exit the locked state (Lock = LOW), the phase error must become greater than the 30nS RC delay. When the PLL is in the power down mode, Lock is forced LOW. A flow chart of the digital filter is shown below.



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Supplemental Information (Continued)

3.1 PCB LAYOUT CONSIDERATIONS

Power Supply Pins: For these pins, it is recommended that these be filtered by taking a series 18 ohm resistor and then placing two capacitors shunt to ground, thus creating a lowpass filter. Although theoretically, it makes sense to make these capacitors as large as possible, the ESR (Equivalent Series Resistance) is greater for larger capacitors. It is therefore recommended to provide two capacitors of very different sizes for the best filtering. 0.1 uF and 100 pF are typical values. The charge pump supply pins in particular are vulnerable to power supply noise.

High Frequency Input Pins, FinRF and FinIF: The signal path from the VCO to the PLL is sensitive to matching and layout, therefore creating unique challenges fro board layout. It is generally recommended that the VCO output go through a resistive pad and then through a DC blocking capacitor before it gets to these high frequency input pins. If the trace length is sufficiently short (< 1/10th of a wavelength), then the pad may not be necessary, however, a series resistor of about 39 ohms is still recommended to isolate the PLL from the VCO. The DC blocking capacitor should be chosen at least to be 100 pF. It may turn out that the frequency in this trace is above the self-resonant frequency of the capacitor, but since the input impedance of the PLL tends to be capacitive, it actually be a benefit to exceed the self-resonant frequency. The pad and the DC blocking capacitor should be placed as close to the PLL as possible

Complimentary High Frequency Pins, FinRF* and FinIF*: These outputs may be used to drive the PLL differentially, but it is very common to drive the PLL in a single ended fashion. These capacitors should be chosen such that the impedance, including the ESR of the capacitor, is as close to an AC short as possible at the operating frequency of the PLL. 100 pF is a typical value.

3.2 FASTLOCK AND CYCLE SLIP REDUCTION CIRCUITRY OPERATION

The LMX2364 has enhanced features for FastLock operation. When the PLL is switching frequencies, the charge pump current and comparison frequencies may be adjusted. The purpose of increasing the charge pump current is to increase the loop bandwidth. The purpose of reducing the comparison frequency is to combat cycle slipping. If these two parameters are not changed by the same ratio, then it is necessary to switch in a resistor in order to keep the loop filter optimized. Furthermore, it may be difficult in this case to keep loop filters of higher than second order well optimized during FastLock in these cases. The timeout counter controls how long the change in charge pump current and/or comparison frequency is active. One also needs to realize that there is a frequency glitch that is caused when any sort of FastLock or Cycle Slip Reduction is disengaged. This frequency glitch is application specific. In this case the table below shows all the possible permutations for using the FastLock and cycle slip reduction circuitry.

	Keep Comparison Frequency the Same	**Decrease Comparison Frequency (RF Side Only)**
Increase Charge Pump Current	Classical Fastlock This mode allows the loop bandwidth to be increased during FastLock and then switched back to normal after FastLock is disengaged.	CSR/Fastlock Combination This is the recommended way to use CSR. If the charge pump gain is used to balance the change in loop gain due to the lower comparision frequency, no fastlock resistor is necessary.
Keep Charge Pump Current the Same	Operation Without Fastlock This mode is essentially not using fastlock at all.	CSR Only In general, this mode is not recommended, but it may be practical in some rare situations.
Decrease Charge Pump Current	Illegal Mode This mode degrades performance and should never be used.	

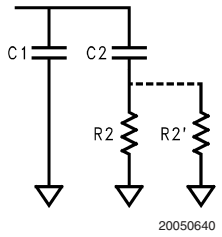
Note: If the charge pump current and cycle slip reduction circuitry are engaged in the same proportion, then it is not necessary to switch in a FastLock resistor and the loop filter will be optimized for both normal mode and FastLocking mode. For third and fourth order filters which have problems with cycle slipping, this may prove to be the optimal choice of settings.

Supplemental Information (Continued)

3.3 DETERMINING THE THEORETICAL LOCK TIME IMPROVEMENT AND FASTLOCK RESISTOR, R2

The loop bandwidth multiplier, K, is necessary in order to determine the theoretical impact of FastLock/CSR on the loop bandwidth and also which resistor should be switched in parallel with the loop filter resistor R2. K = K_Kphi x K_Fcomp where K is the loop gain multiplier K_Kphi and K_Fcomp are the ratio of the FastLock currents and comparison frequencies to their steady state conditions. Note that this should always be greater than or equal to one. K_Fcomp is the ratio of the FastLock comparison frequency to the steady state comparison frequency. If this ratio is less than one, this implies that the CSR is being used.

When K is greater than one, is necessary to switch a FastLock resistor, R2', in parallel with R2 in order to keep the loop filter optimized and maintain the same phase margin. After the PLL has achieved a frequency that is sufficiently close to the desired frequency, the resistor R2' is disengaged and the charge pump current is and comparison frequency are returned to normal. Of special concern is the glitch that is caused when the resistor R2' is disengaged. This glitch can take up a significant portion of the lock time. The LMX2364 has enhanced switching circuitry to minimize this glitch and therefore improve the lock time.



The change in loop bandwidth is dependent upon the loop gain multiplier, K. The theoretical improvement in lock time is given below, but the actual improvement will be less than this due to the glitch that is caused by disengaging FastLock. The theoretical improvement is given to show an upper bound on what improvement is possible with FastLock. In the case that K < 1, this implies the CSR is being engaged and that the theoretical lock time will be degraded. However, since this mode reduces or eliminates cycle slipping, the actual lock time may be better in cases where the loop bandwidth is small relative to the comparison frequency. Realize that the theoretical lock time multiplier does not account for the FastLock/CSR disengagement glitch, which is most severe for larger values of K.

Loop Gain Multiplier, K	FastLock Loop Bandwidth/Steady State Loop	R2' Value	Theoretical Lock Time Multiplier
1:8*	0.35	open	x 2.828
1:4*	0.50	open	x 2.000
1:2*	0.71	open	x 1.414
1:1	1.00	open	x 1.000
2:1	1.41	R2/0.41	x 0.707
4:1	2.00	R2	x 0.500
8:1	2.83	R2/1.83	x 0.354
16:1	4.00	R2/3.00	x 0.250
K:1	$\sqrt{K}$	$\frac{R2}{\sqrt{K}-1}$	$1/\sqrt{K}$

* These modes of operation are generally not recommended

3.4 USING FASTLOCK AND CSR TO AVOID CYCLE SLIPPING

In the case that the comparison frequency is very large (ie. 70 x) of the loop bandwidth, cycle slipping may occur when an instantaneous phase error is presented to the phase detector. This can be reduced by increasing the loop bandwidth during frequency aquisition, decreasing the comparison frequency during frequency acquisition, or some combination of the these. If increasing the loop bandwidth during frequency acquisition is not sufficient to reduce cycle slipping, the LMX2364 also has a routine to decrease the comparison frequency.

Supplemental Information (Continued)

3.5 RF PLL FASTLOCK REFERENCE TABLE

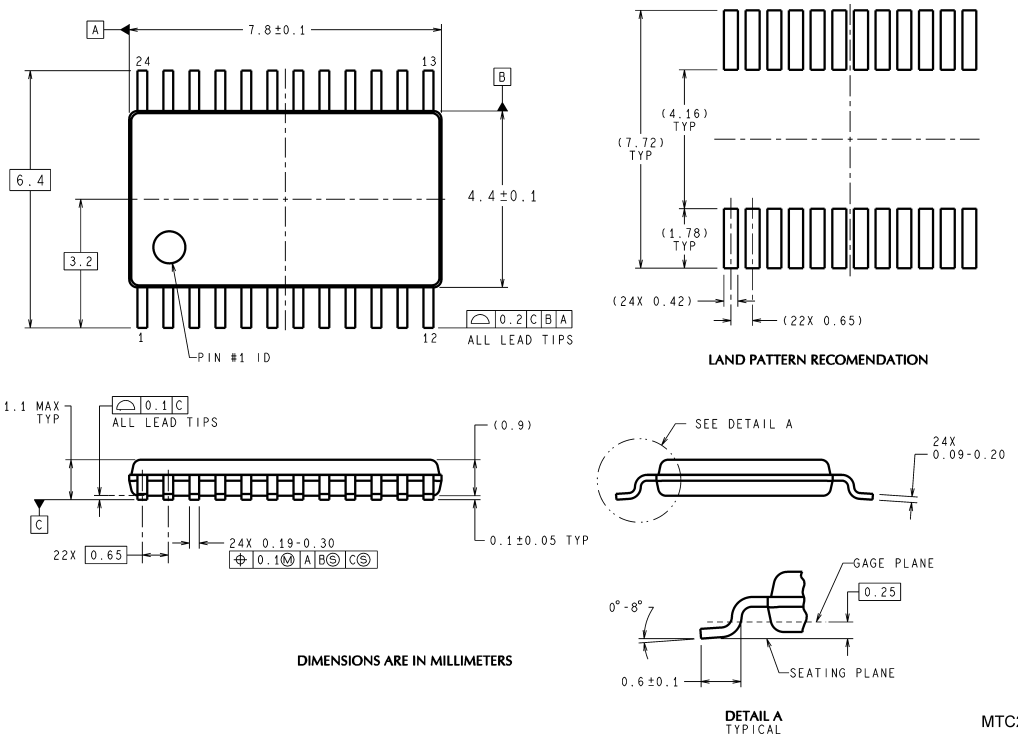
The table below shows most of the trade offs involved in choosing a steady-state charge pump current (RF_CP), the FastLock charge pump current (RF_CPF[1:0]), and the Cycle Slip Reduction Factor CSR.

Parameter	Advantages to Choosing Smaller	Advantages to Choosing Larger
RF_CP	1. Allows capacitors in loop filter to be smaller values making it easier to find physically smaller components and components with better dielectric properties. 2. Allows a larger loop bandwidth multiplier for FastLock, or a higher cycle slip reduction factor.	Phase noise, especially within the loop bandwidth of the system will be slightly worse for lower charge pump currents. If the charge pump gain is at least 4 mA, most of the phase noise benefit will be realized.
RF_CPF	The only reason not to always choose this to 16 mA is to make it such that no FastLock resistor is required for FastLock. For 3rd and 4th order filters, it is not possible to keep the filter perfectly optimized by simply switching in a resistor for FastLock.	This allows the maximum possible benefit for FastLock.
RF_CSR	Do not choose this any larger than necessary to eliminate cycle slipping. Keeping this small allows a larger loop bandwidth multiplier for FastLock.	This will eliminate cycle slips better.

3.6 CAPACITOR DIELECTRIC CONSIDERATIONS

The LMX2364 has a high fractional modulus and high charge pump gain for the lowest possible phase noise. One consideration is that the reduced N value and higher charge pump may cause the capacitors in the loop filter to become larger in value. For larger capacitor values, it is common to have a trade-off between capacitor dielectric quality and physical size. Using film capacitors or NP0/CG0 capacitors yields the best possible lock times, where as using X7R or Z5R capacitors can increase lock time by 0 – 500%. In general, designs with higher comparison frequencies tend to be less succeptible to degradations in lock time due to capacitor dielectric effects. Capacitor dielectrics have very little impact on phase noise or spurs. Although the use of lesser quality dielectric capacitors may be unavoidable in many circumstances, allowing a larger footprint for the loop filter capacitors, using a lower charge pump current, and reducing the fractional modulus are all ways to reduce capacitor values.

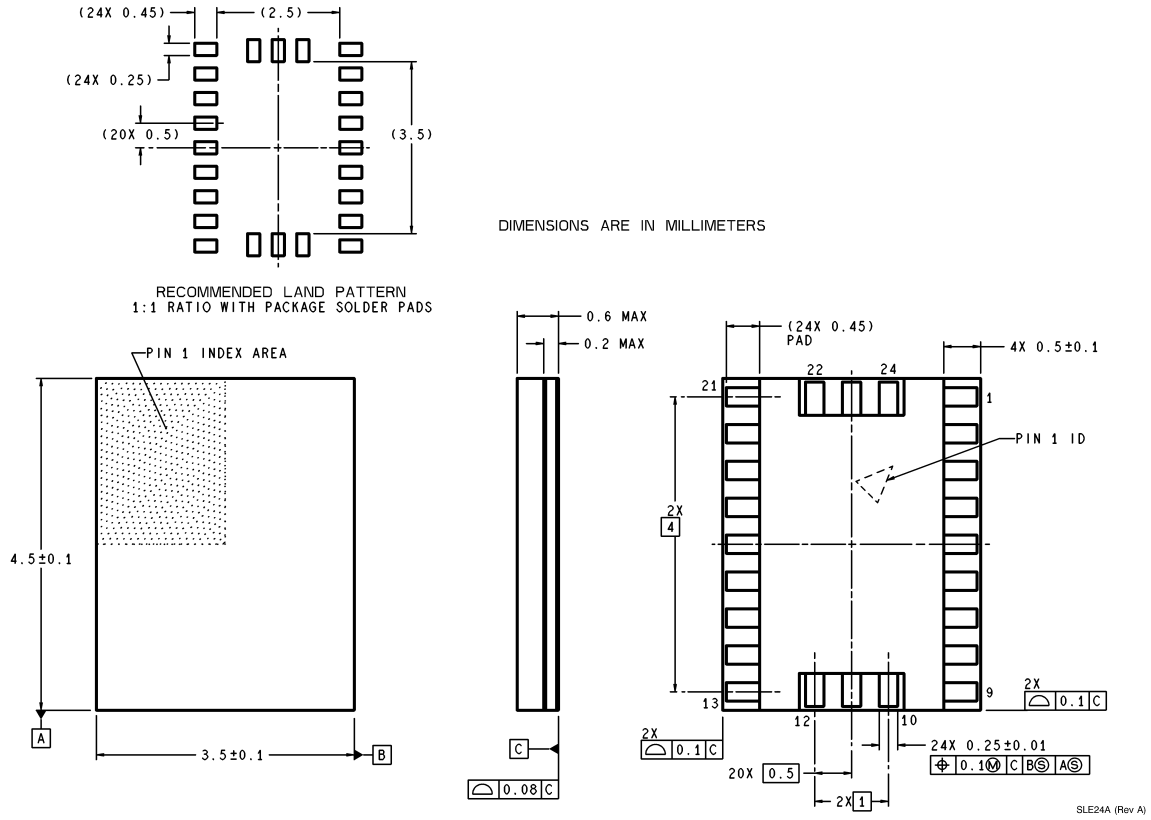
Physical Dimensions inches (millimeters) unless otherwise noted



MTC24 (Rev E)

Thin Shrink Small Outline (TSSOP) Package
Order Number LMX2364TM (Rail)
Order Number LMX2364TMX (Tape and Reel)
NS Package Number MTC24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Ultra Thin Chip Scale Package (SLE)
For Tape and Reel (2500 Units per Reel)
Order Number LMX2364SLEX
NS Package Number SLE24A

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