

PC87435 Enhanced IPMI Baseboard Management Controller

General Description

The National Semiconductor® PC87435 is a highly-integrated Enhanced IPMI Baseboard Management Controller (BMC), or satellite management controller, with an embedded RISC core and advanced functions. It is targeted for a wide range of host-independent controlled platforms such as servers and desktops.

The PC87435 incorporates National's CompactRISC® CR16B core (a high-performance 16-bit RISC processor), on-chip flash and RAM memories, system support functions, Low Pin Count (LPC) host interface and a Bus Interface Unit (BIU) that directly interfaces with optional expansion memory and I/O devices.

System support functions include: two SMBus® channels; high-accuracy analog-to-digital (ADC) for system control, system health monitoring and analog controls, USART for ICMB extension, Watchdog and other timers; interrupt control and general-purpose I/O (GPIO).

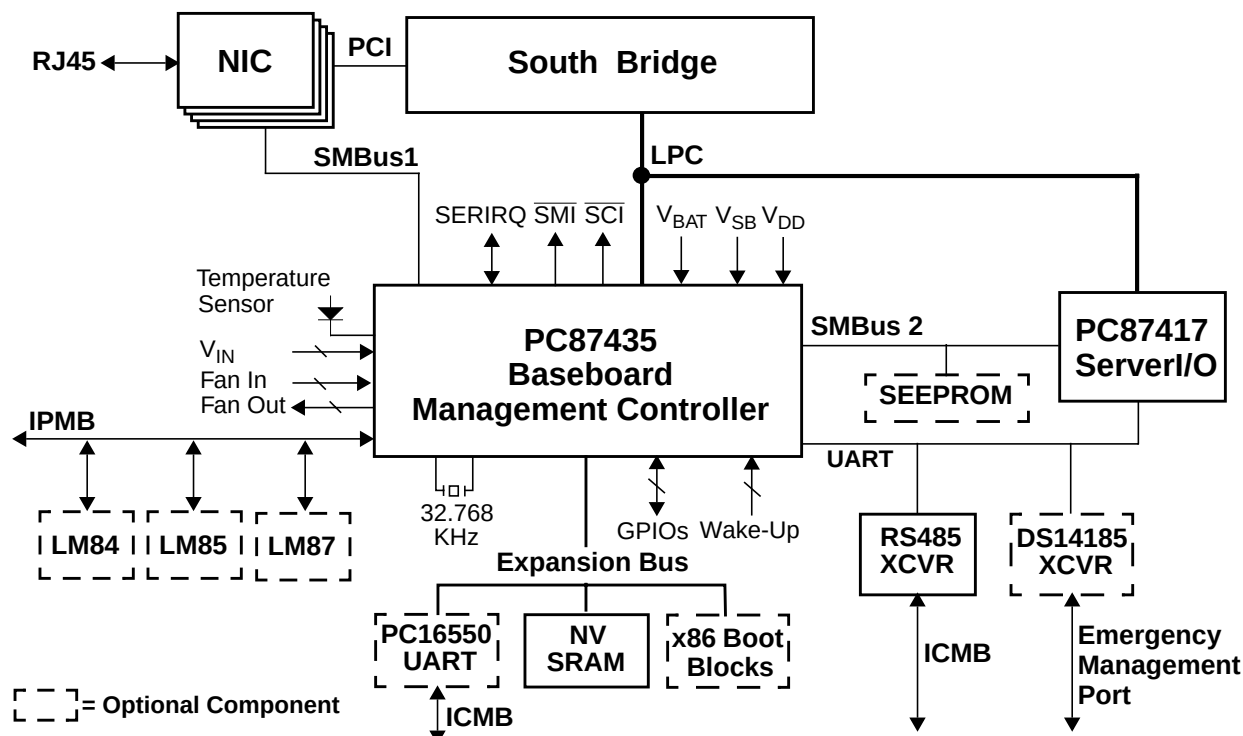
The PC87435 interfaces with the host via an LPC bus that provides three interface channels, with peripherals and IPMI devices via two independent SMBuses and with additional memory and I/O ports via a private expansion bus.

The PC87435, like all members of National's AdvancedI/O family, is PC01 and ACPI compliant.

Outstanding Features

- Intelligent Platform Management Interface (IPMI)-optimized BMC
- 16-bit RISC core, with 2 Mbyte linear address space and running at up to 20 MHz
- On-chip flash and RAM
- Host interface, based on Intel's *LPC Interface Specification Revision 1.0*, September 29th, 1997
- Two SMBus interface modules (each module can be master and slave)
- USART for ICMB interface extension
- System timers, PWM and ADC channels
- 84/108 GPIO ports with a variety of wake-up events
- Random Number Generator for IPMI v1.5 authentication
- Integrated RTC
- Low current consumption
- JTAG-based debugger interface

System Connection Diagram



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Features

- Supports *Intelligent Platform Management Interface (IPMI) Specification v1.5*, February 21, 2001
- Supports Microsoft® *Advanced Power Management (APM) Specifications Revision 1.2*, February 1996

Embedded Controller Features

- Processing Unit
 - CompactRISC CR16B 16-bit embedded RISC processor core
 - 2 Mbytes of linear address space
- Internal Memory
 - 128 Kbytes of on-chip flash memory
 - Field upgradable by host, CR16B, parallel programmer interface or JTAG
 - Boot block for CR16B
 - Memory contents protection
 - 4096 bytes of on-chip RAM
- Expansion Memory (Optional in 176-pin packages)
 - Three address zones for static devices, with configurable wait states and 8- or 16-bit-wide bus
 - Up to 1 Mbyte of additional code and data
 - Supports host-controlled code download and on-board flash update
 - Memory access protection
- Host Interface Channels
 - Three KCS host interface channels
 - IRQ, SMI and SCI (PWUREQ) generation
- Multi-Input Wake-Up (MIWU)
 - Supports up to 32 wake-up or interrupt inputs
 - Special input for system On/Off switch
 - Generates wake-up event to PMC (Power Management Control) module
 - Generates interrupts to ICU module
 - Provides user-selectable trigger conditions
- Interrupt Control Unit (ICU)
 - 31 maskable vector interrupt sources
 - 26 general-purpose external interrupt inputs through MIWU
 - Enable and pending indication for each interrupt
 - Non-maskable interrupt input
- Authentication Function Support
 - Random Number Generator (RNG)
 - Full Random using temperature, voltage and system noise.
- General-Purpose I/O (GPIO)
 - 84/108 port pins in 128/176 packages, respectively
 - I/O pins individually configured as input or output with optional pull-up resistors
 - 27 external wake-up events
 - Low-cost external GPIO expansion
- Two SMBus Interface modules.
 - Each module:
 - Is master and slave
 - Detects up to three simultaneous slave addresses
 - Supports polling and interrupt controlled operation
 - Generates a wake-up signal on detection of a Start Condition while in Idle mode
 - Has optional internal pull-up on SDA and SCL pins
- Two 16-bit Multi-Function Timer (MFT16) modules.
 - Each module:
 - Contains two 16-bit timers
 - Supports Pulse Width Modulation (PWM), Capture and Counter modes
- Universal Synchronous/Asynchronous Receiver-transmitter (USART)
 - A full-duplex USART channel
 - Programmable baud rate
 - Synchronous mode with either internal or external clock
 - 7-, 8- or 9-bit protocols
 - Data transfer via Interrupt, polling
 - Data double buffering with DMA support
- Pulse Width Modulation (PWM) Module
 - Eight outputs
 - 8-bit resolution
 - Common input clock prescaler
- Timer and WATCHDOG
 - 16-bit periodic interrupt timer with 30 μ s resolution and 5-bit prescaler for embedded controller tick and periodic wake-up tasks
 - 8-bit WATCHDOG timer
- Hardware Monitoring (by ADC)
 - 14 inputs, with 10-bit resolution
 - Controlled by embedded controller
 - System Voltage Measurement
 - Up to eight external measurement points
 - Four internal measurement points
 - Diode-Based Temperature Measurement
 - Software-controlled fault detection
 - Hardware-monitored over-temperature detection
 - Production time calibration using flash parameters
- Development Support Features
 - Interface to debugger via JTAG pins
 - ISE/ADB mode (DEV mode)
 - On-board Debug mode
 - Flash programming via JTAG
- CR16B Access to Host Controlled Functions
 - Enabled when host inactive

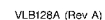
Features (Continued)

Host Controlled Function Features

- LPC System Interface
 - Synchronous cycles, up to 33 MHz bus clock
 - Serial IRQ
 - I/O and Memory read and write cycles
 - LPC and FWH read cycles
- Base Address (BADDR) strap to determine the base address of the configuration Index-Data register pair PC01 and ACPI Compliant
 - PnP Configuration Register structure
 - Flexible resource allocation for all logical devices
 - Relocatable base address
 - 15 IRQ routing options
 - Generates SCI ($\overline{\text{PWUREQ}}$) for ACPI systems
- Shared Memory and Protection
 - Bridges LPC access to internal and expansion memory
 - CR16B controlled, LPC access protection
 - FWH transaction support
- Real-Time Clock (RTC)
- System Wake-Up Control (SWC)
 - Wake-up on detection on:
 - Software controlled off events
 - Optional routing of power-up request to IRQ, $\overline{\text{SMI}}$ and SCI ($\overline{\text{PWUREQ}}$) lines

Clocking, Supply and Package Information

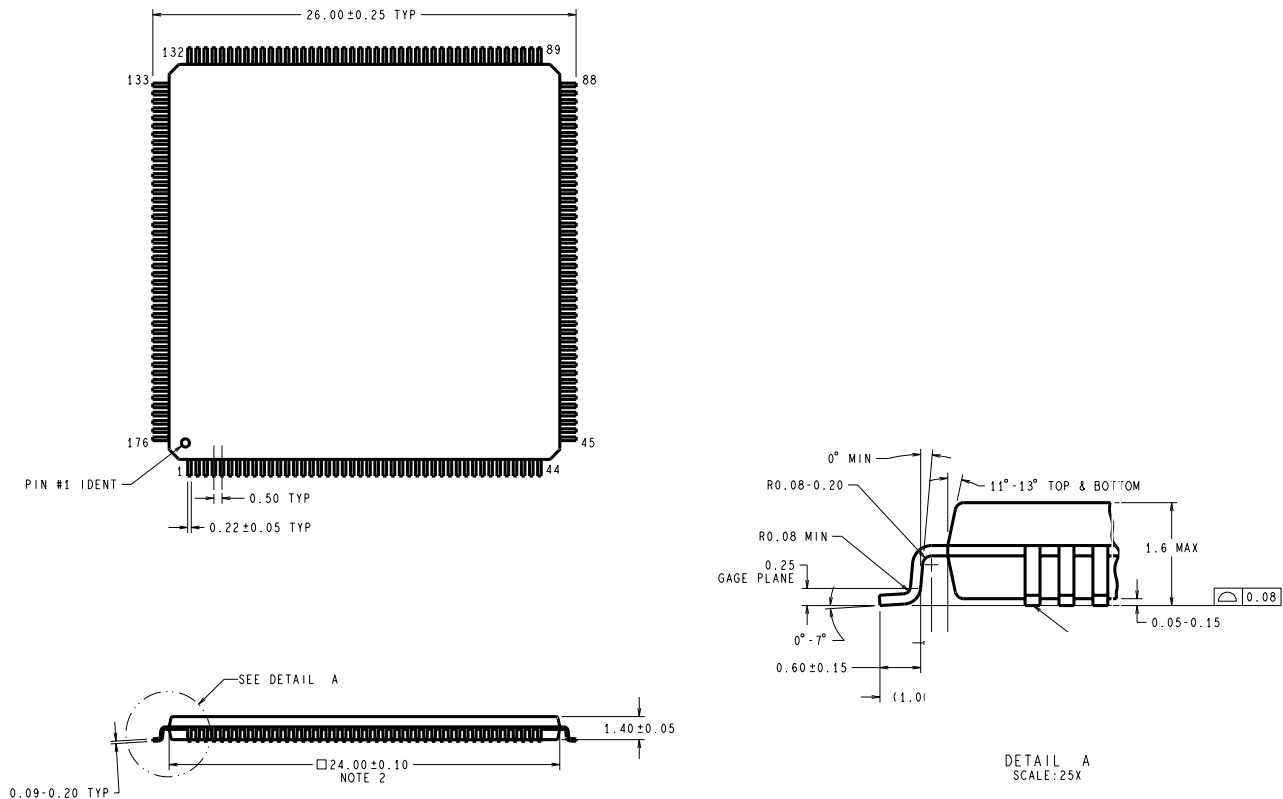
- Strap Input Controlled Operating Modes
 - TRI-STATE[™] of all the pins
 - Development (ISE/ADB)
 - On-board development
 - Programming Environment
- Clocks
 - Single 32.768 KHz crystal oscillator
 - On-chip high frequency clock generator
 - CPU clock 4-20 MHz
 - Software-controlled frequency generation
 - Based on the 32.768 KHz input
 - 32.768 KHz clock output
 - CPU clock output
- Power Management Control (PMC)
 - Separate 3.3V supply for the CPU and its peripherals (V_{CC}), Analog (AV_{CC}) and for the other functions (V_{DD})
 - All pins are 5V tolerant and back-drive protected (except the LPC bus pins)
 - Backup battery input for RTC, and wake-up configuration
 - Reduced power consumption capability
 - Automatic wake-up on system events
- Package options
 - 176-pin LQFP package for Expansion Memory use and development
 - 128-pin LQFP package for a minimal BMC



Revision 1.01

Physical Dimensions (Continued)

All dimensions are in millimeters



NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)
THICKNESS ON COPPER.
2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
3. REFERENCE JEDEC REGISTRATION MO-136, VARIATION BV,
DATED 10/93.

176-Low Profile Plastic Quad Flatpack (LQFP)
Order Number PC87435-VPC
NS Package Number VPC176

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