Offline Switching Regulator

FEATURES

- ±1% Line and Load Regulation with No Optocoupler
- Switch Frequency Up to 200kHz
- Internal 2A Switch and Current Sense (LT1103)
- Internal 1A Totem-Pole Driver (LT1105)
- Start-Up Mode Draws Only 200µA
- Fully Protected Against Overloads
- Overvoltage Lockout of Main Supply
- Protected Against Underdrive or Overdrive to FET
- Operates in Continuous or Discontinuous Mode
- Ideal for Flyback and Forward Topologies
- Isolated Flyback Mode Has Fully Floating Outputs

APPLICATIONS

- Up to 250W Isolated Mains Converter
- Up to 50W Isolated Telecom Converter
- Fully Isolated Multiple Outputs
- Distributed Power Conversion Networks

DESCRIPTION

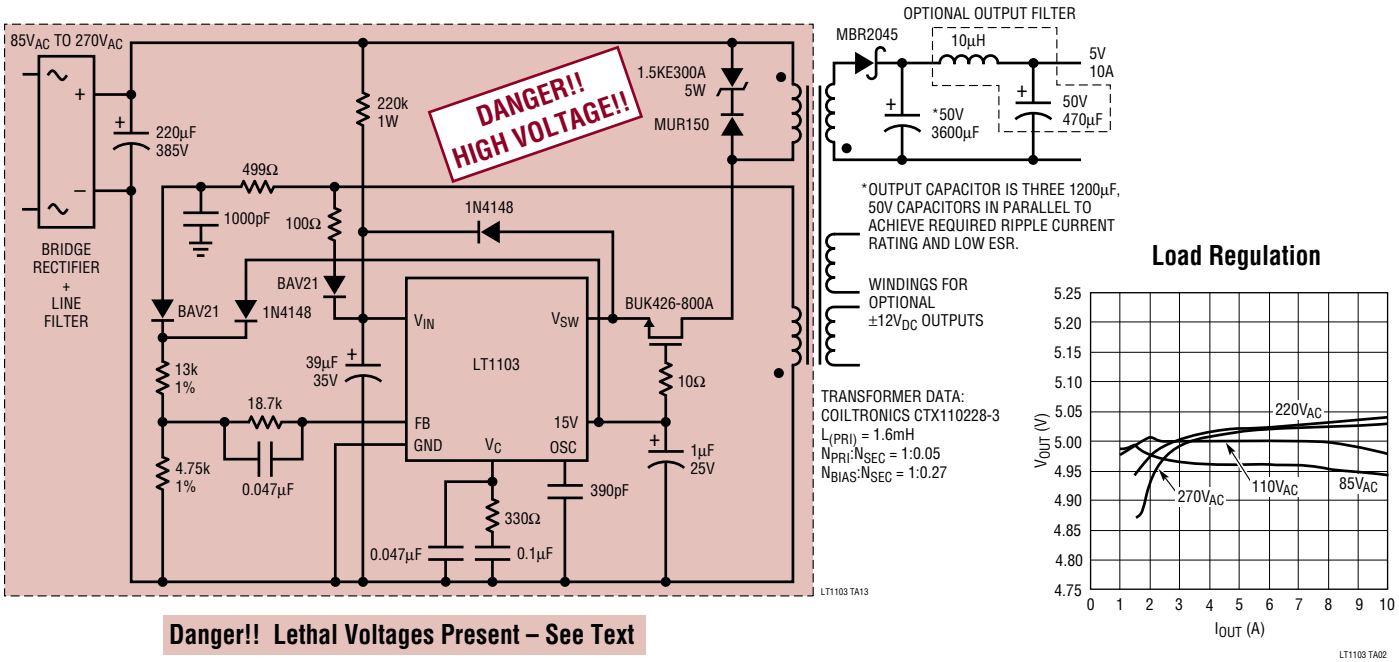
The LT®1103 Offline Switching Regulator is designed for high input voltage applications using an external FET switch whose source is driven by the open collector output of the LT1103. The LT1103 is optimized for 15W to 100W applications. For higher power applications or additional switch current flexibility, the LT1105 is available and its totem pole output drives the gate of an external FET. Unique design of the LT1103/LT1105 eliminates the need for an optocoupler while still providing ±1% load and line regulation in a magnetic flux-sensed converter. This significantly simplifies the design of offline power supplies and reduces the number of components which must cross the isolation barrier to one, the transformer.

The LT1103/LT1105 current mode switching techniques are well suited to transformer isolated flyback and forward topologies while providing ease of frequency compensation with a minimum of external components. Low external part count for a typical application combines with a

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TYPICAL APPLICATION

Fully Isolated Flyback 100kHz 50W Converter with Load Regulation Compensation



Danger!! Lethal Voltages Present – See Text

Load Regulation

DESCRIPTION

200kHz maximum switching frequency to achieve high power density. Performance at switching frequencies above 100kHz may be degraded due to internal timing constraints associated with fully isolated flyback mode.

Included are the oscillator, control, and protection circuitry such as current limit and overvoltage lockout. Switch frequency and maximum duty cycle are adjustable. Bootstrap circuitry draws 200μA for start-up of isolated topologies. A 5V reference as well as a 15V gate bias are available to power external primary-side circuitry. No external current sense resistor is necessary with LT1103 because it is integrated with the high current switch. The LT1105 brings out the input to the current limit amplifier and requires the use of an external sense resistor.

The LT1103/LT1105 have unique features not found on other offline switching regulators. Adaptive antisat switch drive allows wide ranging load currents while maintaining high efficiency. The external FET is protected from insufficient or excessive gate drive voltage with a drive detection circuit. An externally activated shutdown mode reduces total supply current to less than 200μA, typical for standby operation. Fully isolated and regulated outputs can be generated in the optional isolated flyback mode without the need for optocouplers or other isolated feedback paths.

WARNING!

DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN OFFLINE CIRCUITS!

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF OFFLINE CIRCUITS. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THESE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. REPEAT: OFFLINE CIRCUITS CONTAIN DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

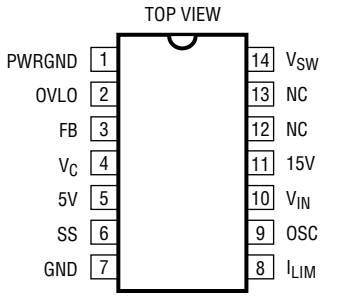
ALL TESTING PERFORMED ON AN OFFLINE CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE OFFLINE CIRCUIT'S INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF OFFLINE CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN THE CIRCUIT INPUT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} 30V
V_{SW} Output Voltage (LT1103) 50V
V_{SW} Output Current (200ns)(LT1105) ..... ±1.5A
V_C, FB, OSC, SS 6V
I_{LIM} (LT1105) 3V
0VLO Input Current 1mA
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Maximum Operating Ambient Temperature Range
LT1103C ..... 0°C to 70°C
LT1105C ..... 0°C to 70°C
Maximum Operating Junction Temperature Range
LT1103C ..... 0°C to 100°C
LT1105C ..... 0°C to 100°C
LT1105I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

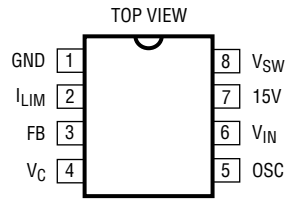
PACKAGE/ORDER INFORMATION



N PACKAGE
14-LEAD PDIP
PINS 1 AND 7 MUST BE TIED TOGETHER
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

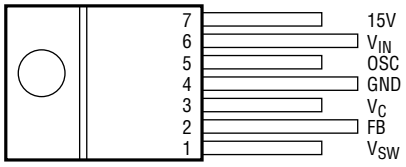
LT1105CN
LT1105IN



N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1105CN8
LT1105IN8



T7 PACKAGE
7-LEAD TO-220
CASE IS CONNECTED TO GROUND. LEADS ARE FORMED
T_{JMAX} = 100°C, θ_{JA} = 50°C/W

ORDER PART NUMBER

LT1103CT7

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	8V < V_{IN} < 30V, After Device Has Started	●	10	20	30	mA
I_{START}	Start-Up Current	V_{IN} < V_{IN} Start Threshold	●		200	400	µA
		Industrial Grade	●			450	µA
	V_{IN} Start Threshold		●	14.5	16.0	17.5	V
	V_{IN} Shutdown Threshold	Note: Switching Stops When V_{SW} < 10V (LT1103) Note: Switching Stops When V_{GATE} < 10V (LT1105)	●	5.0	7.0	8.0	V
V_{REF}	5V Reference Voltage		●	4.80	4.95	5.20	V
	V_{REF} Line Regulation	10V < V_{IN} < 30V	●		0.025	0.1	%/V
	V_{REF} Load Regulation	0mA < I_L < 20mA	●		0.025	0.05	%/mA
	V_{REF} Short-Circuit Current	Commercial Grade	●	25	60	110	mA
		Industrial Grade	●	20		120	mA
	15V Short-Circuit Current	Commercial Grade	●	30		130	mA
		Industrial Grade	●	25		140	mA
V_{GATE}	15V Gate Bias Reference	17 < V_{IN} < 30V, 0mA < I_L < 30mA	●	13.8	15.0	16.2	V
	15V Dropout Voltage	V_{IN} = 15V, I_L = 30mA	●		2.0	2.5	V
	15V Short-Circuit Current		●	30	70	130	mA
SF	Oscillator Scaling Factor	FB = 4V, V_C = Open, Measured at V_{SW}, I_{SW} = 25mA,		36	40	44	Hz • µF
		OVLO = 5V, f_{OSC} = SF/C_{OSC}, 40kHz < f_{OSC} < 200kHz	●	32	40	48	Hz • µF
	Oscillator Valley Voltage				2.0		V
	Oscillator Peak Voltage				4.5		V

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS		MIN	TYP	MAX	UNIT
DC	Preset Max Switch Duty Cycle (LT1103)	FB = 4V, V_C = Open, f_{OSC} = 40kHz, I_{SW} = 25mA, Note: Maximum Duty Cycle Can Be Altered at OSC Pin	●	58	65	72	%
	Preset Max Switch Duty Cycle (LT1105)	FB = 4V, V_C = Open, f_{OSC} = 40kHz, I_{SW} = 25mA, Note: Maximum Duty Cycle Can Be Altered at OSC Pin	●	56	63	70	%
		Industrial Grade	●	55		75	%
	OVLO Threshold	Overvoltage Lockout Threshold at Which Switching is Inhibited	●	2.3	2.5	2.7	V
		Industrial Grade	●	2.2		2.8	V
	OVLO Input Bias Current	OVLO = 2V, Measured Out of Pin (Note 2)	●		1.0	3.0	µA
V_{FB}	FB Threshold Voltage	$I(V_C)$ = 0mA		4.425	4.50	4.575	V
			●	4.400	4.50	4.600	V
	FB Input Bias Current	FB = V_{FB} (Note 3)	●	5	10	20	µA
		Industrial Grade	●	4		22	µA
	Change in FB Input Bias Current with Change in V_C	FB = V_{FB}, V_C = 1V to 4V (Note 3)		8	11	13	µA/V
			●	7	11	14	µA/V
		Industrial Grade	●	6		15	µA/V
	FB Threshold Line Regulation	10V < V_{IN} < 30V	●		0.025	0.10	%/V
gm	Error Amp Transconductance	$\Delta I(V_C)$ = ±50µA		9000	12000	17500	µmho
			●	6000	12000	20000	µmho
		Industrial Grade	●	5000		24000	µmho
A_V	Error Amp Voltage Gain	1V < V_C < 3V	●	500	1250		V/V
		Industrial Grade	●	450			V/V
	V_C Switching Threshold	Switch Duty Cycle = 0%	●	0.85	1.25	1.4	V
	Shutdown Threshold Voltage		●	50	150	250	mV
		Industrial Grade	●	50		300	mV
	Error Amp Source Current		●	150	275		µA
	Error Amp Sink Current		●	1.5	3	4.5	mA
		Industrial Grade	●	0.7		4.5	mA
	Error Amp Clamp Voltage	FB = 4.75V	●	0.3	0.7	0.9	V
		FB = 4.0V	●	4.2	4.4	4.6	V
	Soft-Start Charging Current	SS = 0V	●	25	40	60	µA
		Industrial Grade	●	20		75	µA
	Soft-Start Reset Current	V_{IN} = 6V, SS = 0.3V	●	1	2		mA
	Output Switch Leakage (LT1103)	V_{SW} = 45V	●			500	µA
		V_{SW} = 15V	●			200	µA
BV	Switch Breakdown Voltage (LT1103)	I_{SW} = 5mA	●	50	70		V
	V_{SW} Current Limit (LT1103)	Duty Cycle = 25% (Note 4)	●	2.0	2.5	3.0	A
	Output Switch On Resistance (LT1103)		●		0.4	0.75	Ω
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	I_Q Increase During Switch On Time (LT1103)	I_{SW} = 0.5A to 1.5A	●		30	50	mA/A
	Switch Output High Level (LT1105)	I_{SW} = 200mA, V_{GATE} = 15V	●	13.00	13.5		V
		I_{SW} = 750mA, V_{GATE} = 15V	●	12.50	13.2		V
	Switch Output High Level Industrial Grade	I_{SW} = 200mA, V_{GATE} = 15V	●	12.75			V
		I_{SW} = 750mA, V_{GATE} = 15V	●	12.25			V

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS		MIN	TYP	MAX	UNIT
	Switch Output Low Level (LT1105)	I_{SW} = 200mA I_{SW} = 750mA	● ●		0.25 0.75	0.50 1.50	V V
	Rise Time (LT1105)	C_L = 1000pF			50		ns
	Fall Time (LT1105)	C_L = 1000pF			20		ns
	I_{LIM} Threshold Voltage (LT1105)	Duty Cycle = 25% (Note 5)	●	300	375	450	mV
	Low Switch Drive Lockout Threshold	Measured at V_{SW} (LT1103) Measured at 15V Gate Bias Reference (LT1105)	●	9.0	9.5	10.5	V
	High Switch Drive Lockout Threshold	Measured at V_{SW} (LT1103) Measured at 15V Gate Bias Reference (LT1105)	●	17.0	18.5	20.0	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The OVLO pin is clamped with a 5.5V Zener and can sink a maximum input current of 1mA.

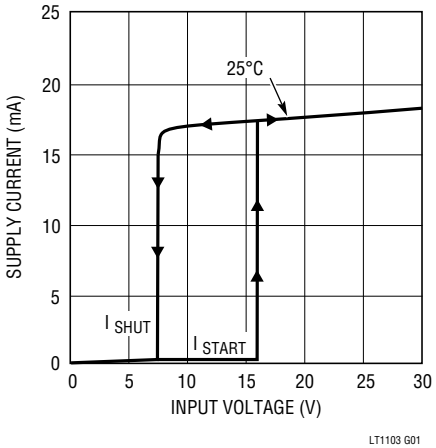
Note 3: FB input bias current changes as a function of the V_C pin voltage. Rate of change of FB input bias current is 11µA/V of change on V_C. By including a resistor in series with the FB pin, load regulation can be set to zero.

Note 4: Current limit on V_{SW} is constant for DC < 35% and decreases for DC > 35% due to internal slope compensation circuity. The LT1103 switch current limit is given by I_{LIM} = 1.76 (1.536 – DC) above 35% duty cycle.

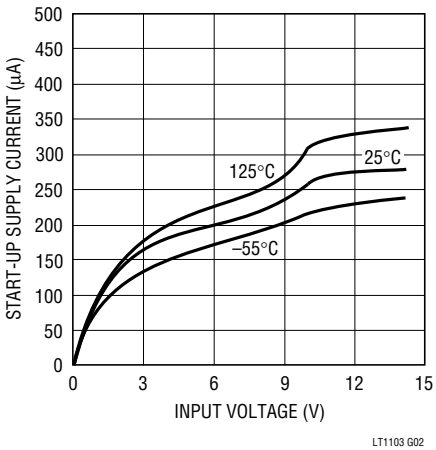
Note 5: The current limit threshold voltage is constant for DC < 35% and decreases for DC > 35% due to internal slope compensation circuitry. The LT1105 switch current limit threshold voltage is given by V_{LIM} = 0.225 (1.7 – DC) above 35% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

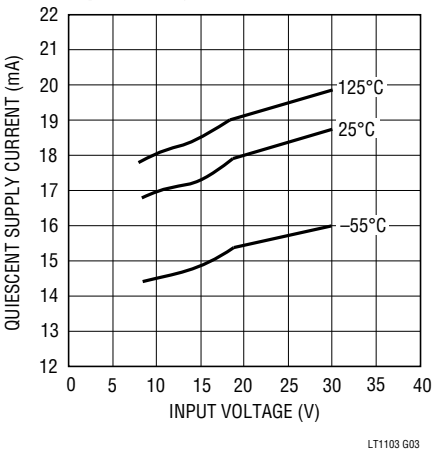
Supply Current vs Input Voltage



Start-Up Supply Current vs Input Voltage

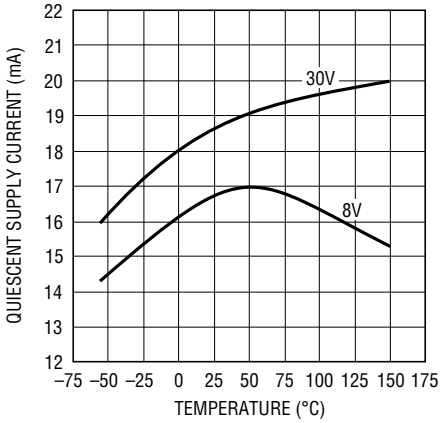


Quiescent Supply Current vs Input Voltage



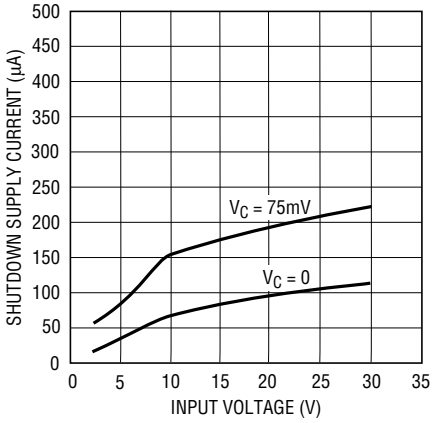
TYPICAL PERFORMANCE CHARACTERISTICS

Quiescent Supply Current vs Temperature



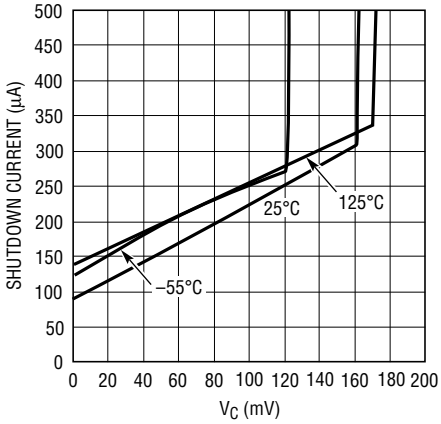
LT1103 G04

Shutdown Supply Current vs Input Voltage



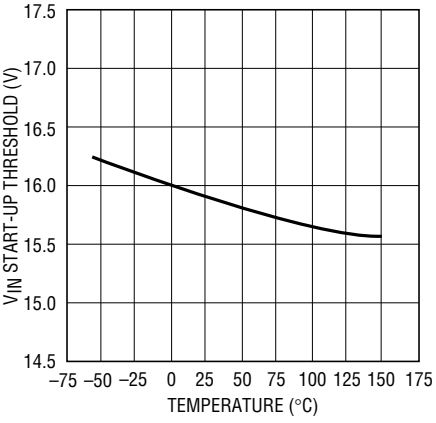
LT1103 G05

Shutdown Supply Current vs V_C Voltage



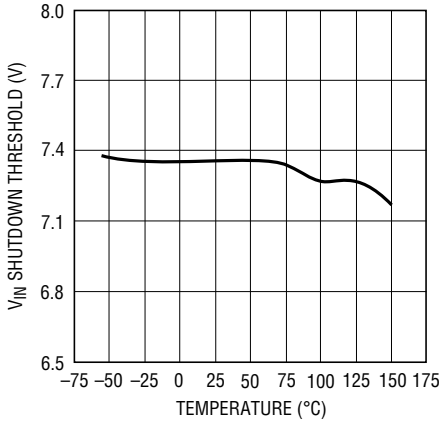
LT1103 G06

V_{IN} Start-Up Threshold vs Temperature



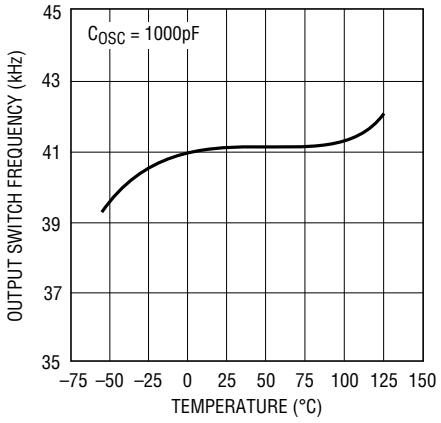
LT1103 G07

V_{IN} Shutdown Threshold vs Temperature



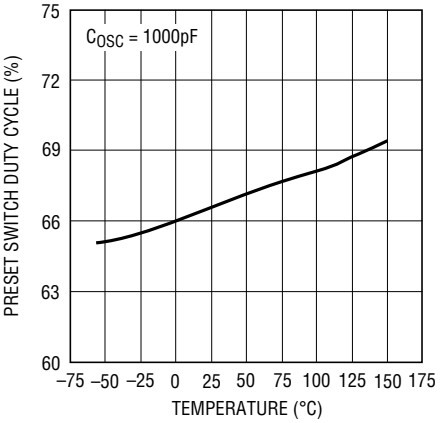
LT1103 G08

Output Switch Frequency vs Temperature



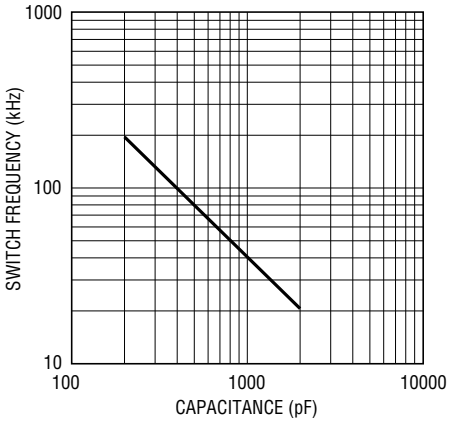
LT1103 G09

Preset Switch Maximum Duty Cycle vs Temperature



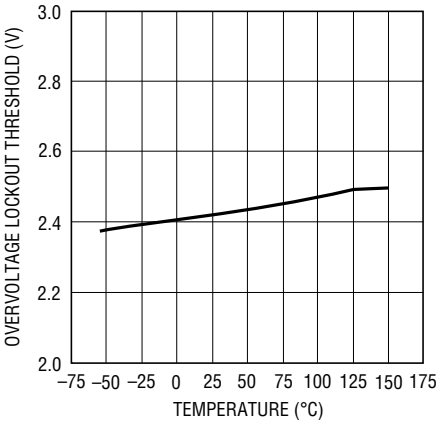
LT1103 G10

Switch Oscillator Frequency vs Capacitance



LT1103 G11

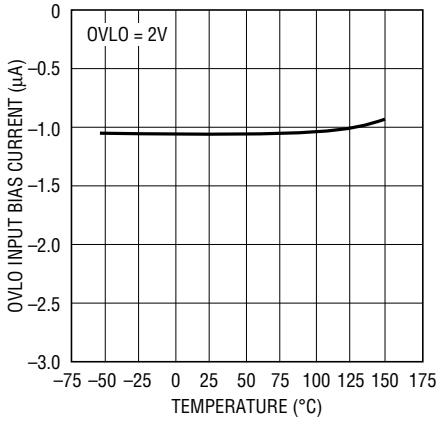
Overvoltage Lockout Threshold vs Temperature



LT1103 G12

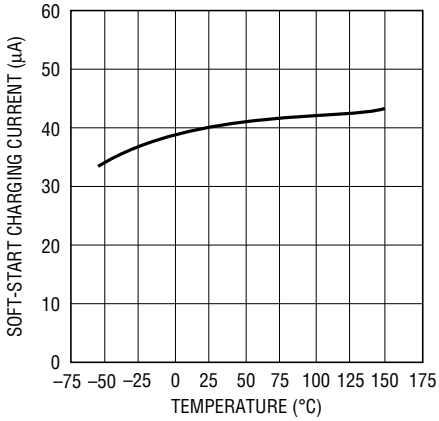
TYPICAL PERFORMANCE CHARACTERISTICS

OVLO Input Bias Current vs Temperature



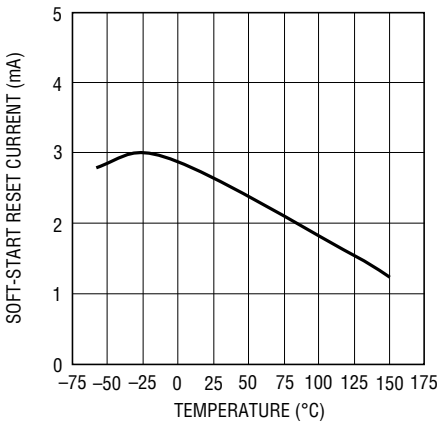
LT1103 G13

Soft-Start Charging Current vs Temperature



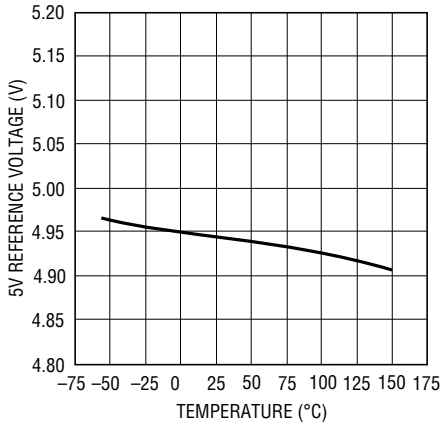
LT1103 G14

Soft-Start Reset Current vs Temperature



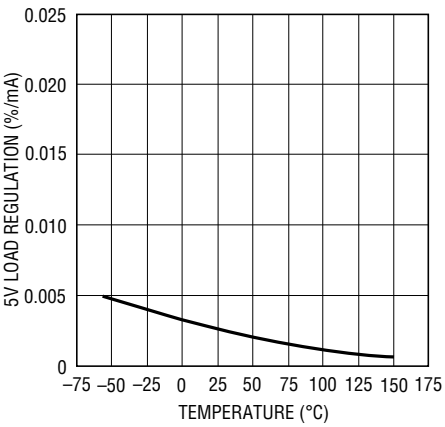
LT1103 G15

5V Reference Voltage vs Temperature



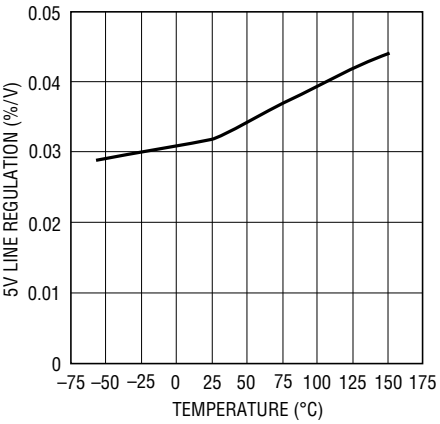
LT1103 G16

5V Load Regulation vs Temperature



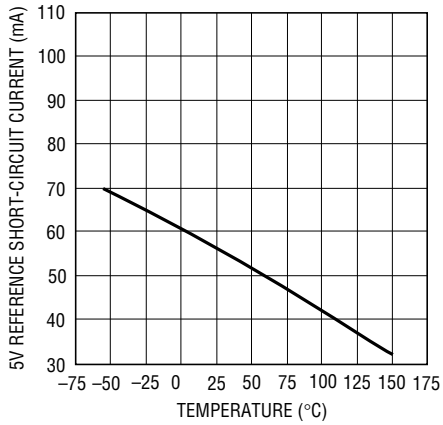
LT1103 G17

5V Line Regulation vs Temperature



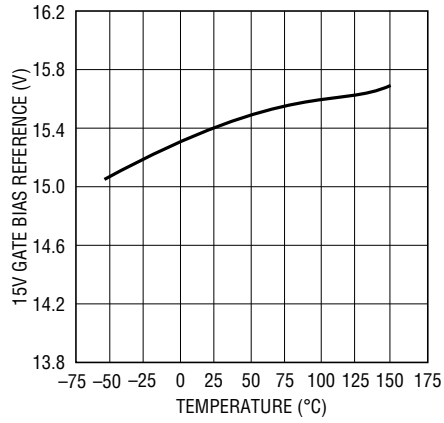
LT1103 G18

5V Reference Short-Circuit Current vs Temperature



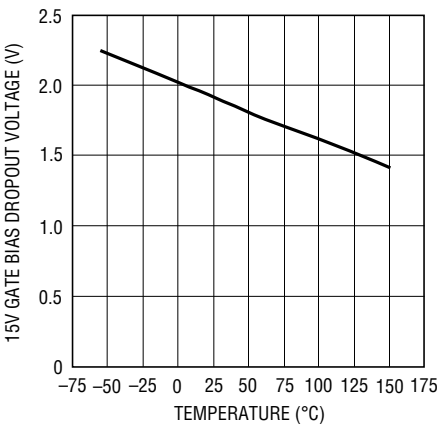
LT1103 G19

15V Gate Bias Reference vs Temperature



LT1103 G20

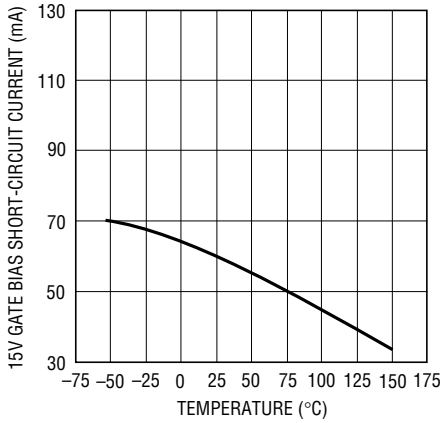
15V Gate Bias Dropout Voltage vs Temperature



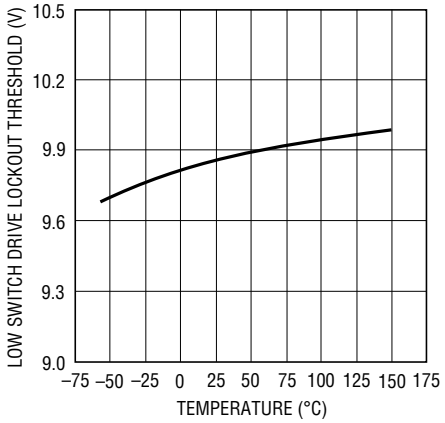
LT1103 G21

TYPICAL PERFORMANCE CHARACTERISTICS

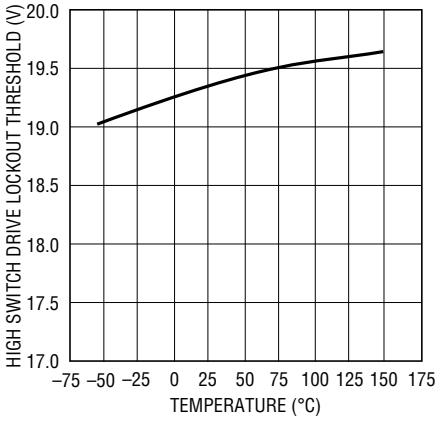
15V Gate Bias Short-Circuit Current vs Temperature



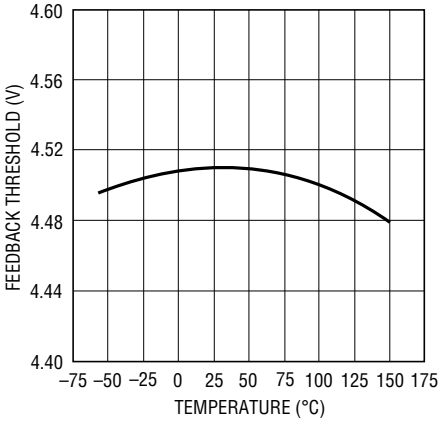
Low Switch Drive Lockout Threshold vs Temperature



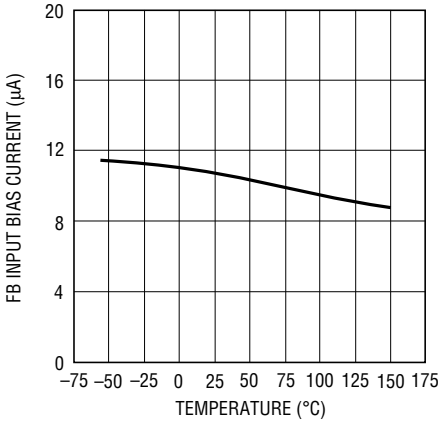
High Switch Drive Lockout Threshold vs Temperature



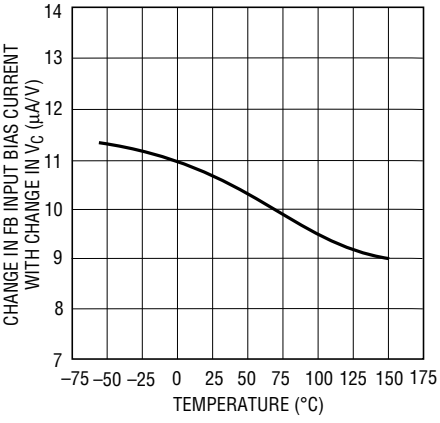
Feedback Threshold vs Temperature



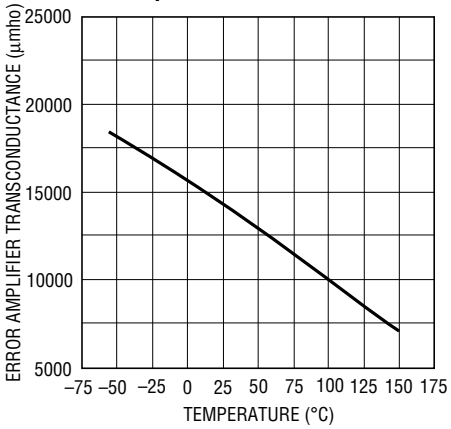
FB Input Bias Current vs Temperature (V_C = 1V)



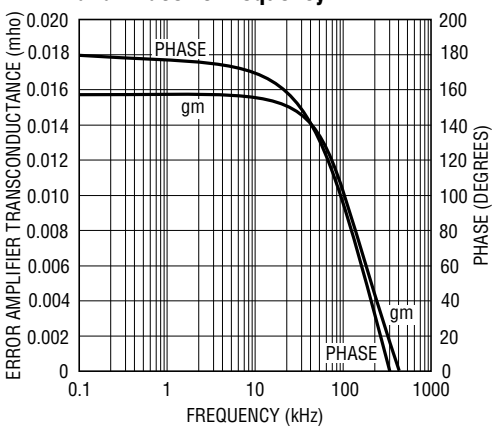
Change in FB Input Bias Current with Change in V_C vs Temperature (V_C = 1V to 4V)



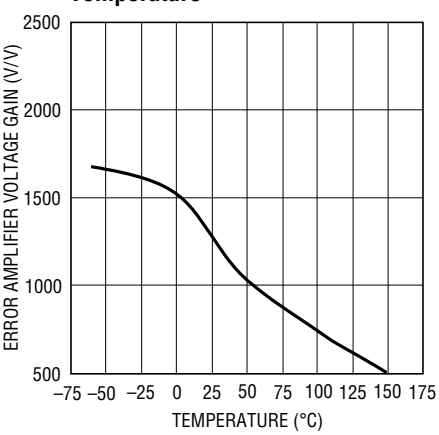
Error Amplifier Transconductance vs Temperature



Error Amplifier Transconductance and Phase vs Frequency

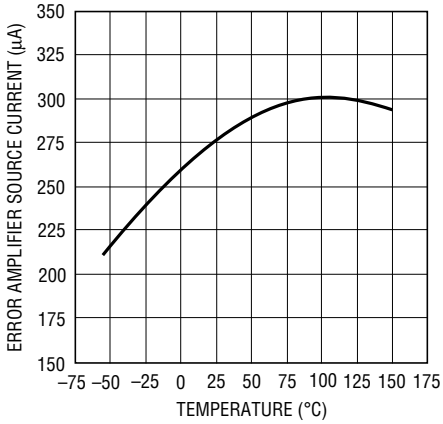


Error Amplifier Voltage Gain vs Temperature



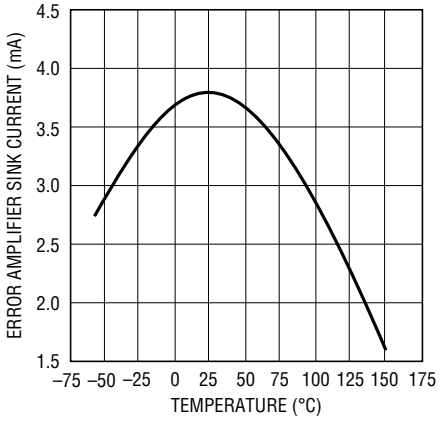
TYPICAL PERFORMANCE CHARACTERISTICS

Error Amplifier Source Current vs Temperature



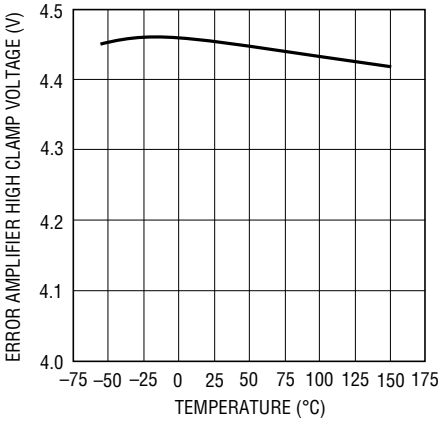
LT1103 G31

Error Amplifier Sink Current vs Temperature



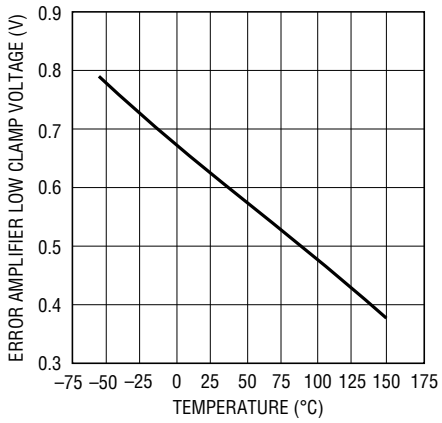
LT1103 G32

Error Amplifier High Clamp Voltage vs Temperature (FB = 4V)



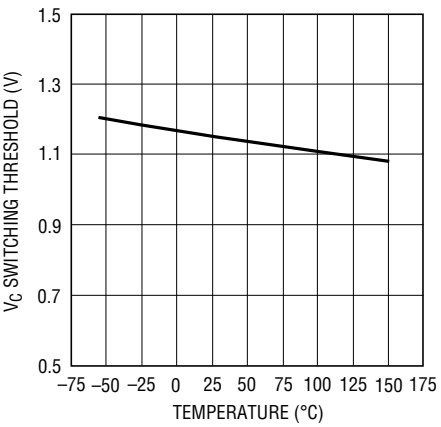
LT1103 G33

Error Amplifier Low Clamp Voltage vs Temperature (FB = 4.75V)



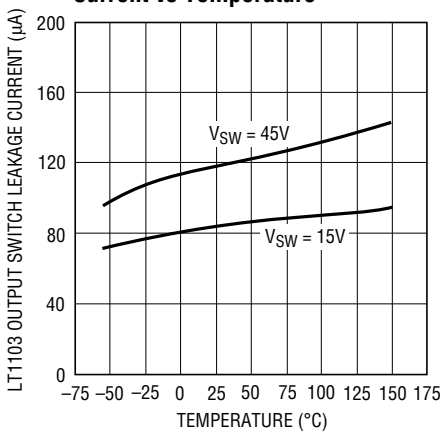
LT1103 G34

V_C Switching Threshold Voltage vs Temperature



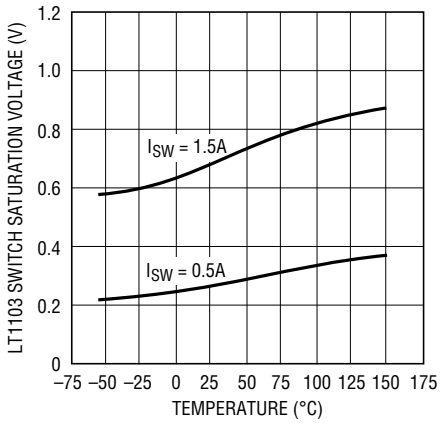
LT1103 G35

LT1103 Output Switch Leakage Current vs Temperature



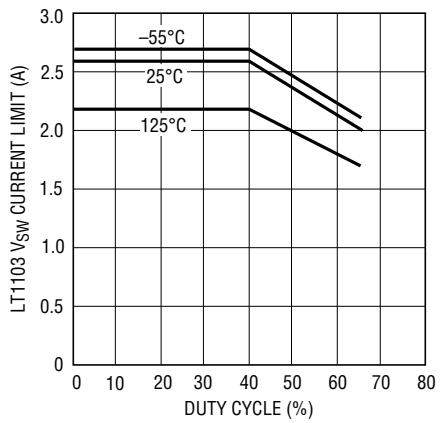
LT1103 G36

LT1103 Switch Saturation Voltage vs Temperature



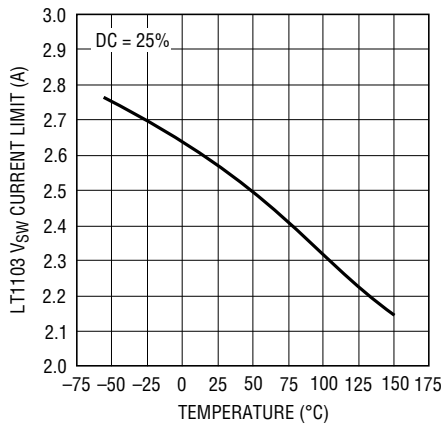
LT1103 G38

LT1103 V_{SW} Current Limit vs Duty Cycle



LT1103 G39

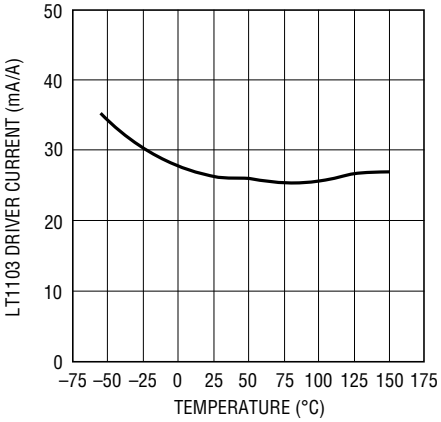
LT1103 V_{SW} Current Limit vs Temperature



LT1103 G40

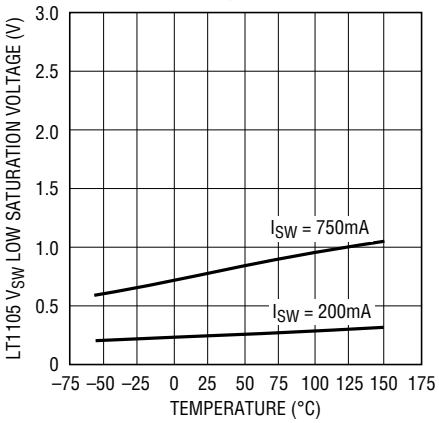
TYPICAL PERFORMANCE CHARACTERISTICS

LT1103 Driver Current vs Temperature



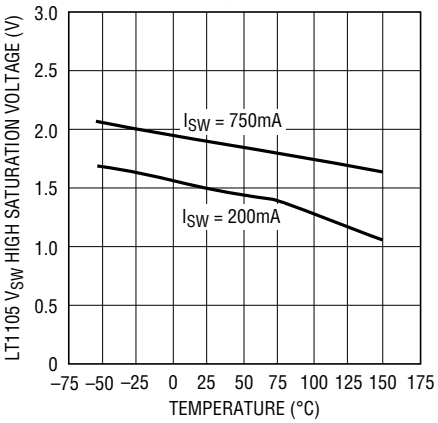
LT1103 G41

LT1105 V_{SW} Low Saturation Voltage vs Temperature



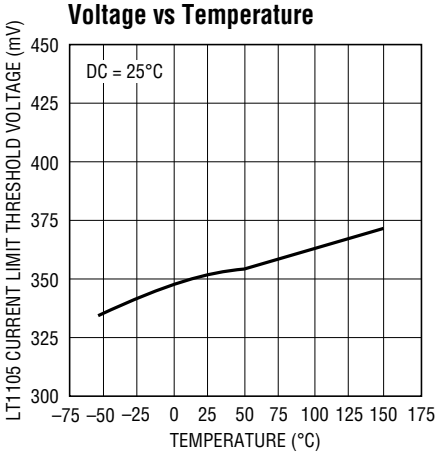
LT1103 G42

LT1105 V_{SW} High Saturation Voltage vs Temperature



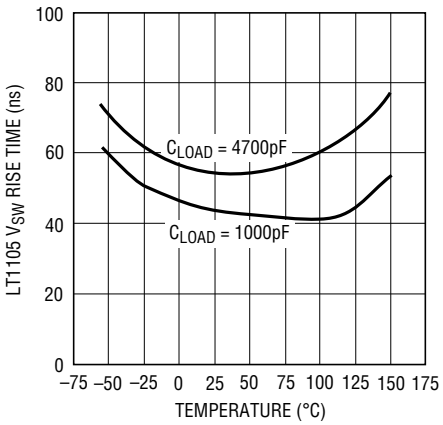
LT1103 G43

LT1105 Current Limit Threshold Voltage vs Temperature



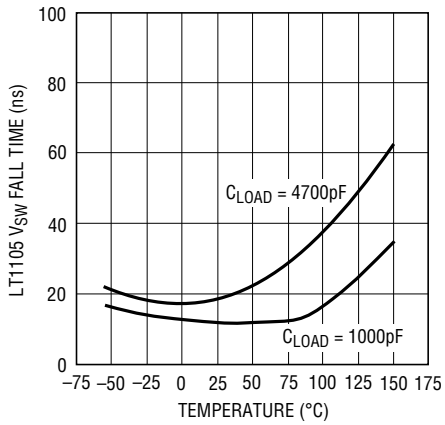
LT1103 G46

LT1105 V_{SW} Rise Time vs Temperature



LT1103 G44

LT1105 V_{SW} Fall Time vs Temperature



LT1103 G45

PIN FUNCTIONS

LT1103

FB: The Feedback pin is the inverting input to the sampling error amplifier. The noninverting input is tied to a 4.5V reference. The FB pin is used for output voltage sensing. The input bias current is a function of the control pin V_C voltage and can be used for load regulation compensation by including a resistor in series with the FB pin. The sampling error amplifier has a typical g_m of 0.012 mhos and the output of the sampling error amplifier has asymmetrical slew rate to reduce overshoot during start-up conditions or following the release of an output overload.

V_C: The V_C control pin is used for frequency compensation, current limiting and shutdown. It is the high impedance output of the sampling error amplifier and the input of the current limit comparator.

GND: The Ground pin acts as both the negative sense point for the internal sampling error amplifier feedback signal and as the high current path for the 2A switch. Also, the case of the 7-lead TO-220 is connected to ground. Proper connections to ground for signal paths and high current paths must be made in order to insure good load regulation.

OSC: The Oscillator pin sets the operating frequency of the regulator with one external capacitor to ground. Maximum duty cycle can also be adjusted by using an external resistor to alter the charge/discharge ratio.

V_{IN}: The Input Supply pin is designed to operate with voltages of 12V to 30V. The supply current is typically 200μA up to the start-up threshold of 16V. Normal operating supply current is fairly flat at 18mA down to the shutdown threshold of 7V. Switching is inhibited for V_{IN} less than 12V due to the gate drive detection circuit.

15V: A 15V reference is used to bias the gate of an external power FET. The voltage temperature coefficient is typically 3mV/°C and the output can source 30mA. Typical dropout voltage is 1.5V for V_{IN} less than 17V and 30mA of load current.

V_{SW}: The Switch Output pin is the collector of the internal NPN power switch. This pin has a typical ON resistance of 0.4Ω and a minimum breakdown voltage of 50V. This pin also ties to the FET gate drive detection circuit.

LT1105

All functions on the LT1105 are equivalent to the LT1103 with the exception of the V_{SW} pin and the I_{LIM} pin and the availability of the OVLO, 5V, and SS functions.

OVLO: The Overvoltage Lockout pin inhibits switching when the pin is pulled above its threshold voltage of 2.5V. OVLO is implemented with a resistor divider network from the rectified DC line and is used to protect the external FET from an overvoltage condition in the off state. This function is only available on the 14-lead PDIP.

5V: A 5V reference is available to power primary-side circuitry. The temperature coefficient is typically 50ppm/°C and the output can source 25mA. This function is only available on the 14-lead PDIP.

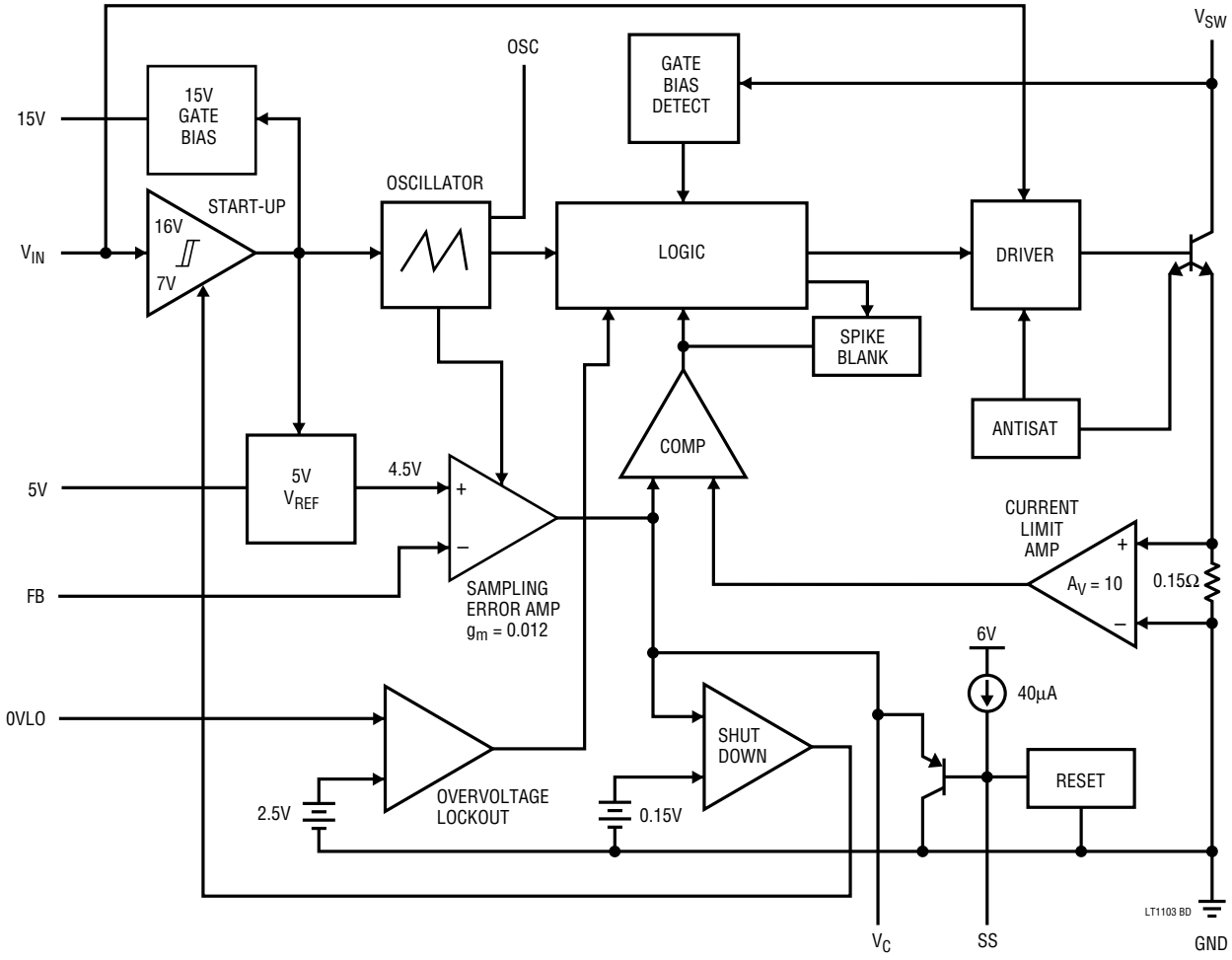
SS: The Soft-Start pin is used to either program start-up time with a capacitor to ground or to set external current limit with a resistor divider. The SS pin has a 40μA pull-up current and is reset to 0V by a 1mA pull-down current during start-up and shutdown. This function is only available on the 14-lead PDIP.

V_{SW}: The Switch Output pin is the output of a 1A NPN totem-pole stage. The V_{SW} pin turns the external FET on by pulling its gate high. Break-Before-Make action of 200ns on each switch edge is built in to eliminate cross conduction currents.

I_{LIM}: The I_{LIM} pin is the input to the current limit amplifier and requires the use of a noninductive, power sense resistor from I_{LIM} to ground to set current limit. The typical current limit threshold voltage is 350mV. The typical input bias current is 100μA out of the pin.

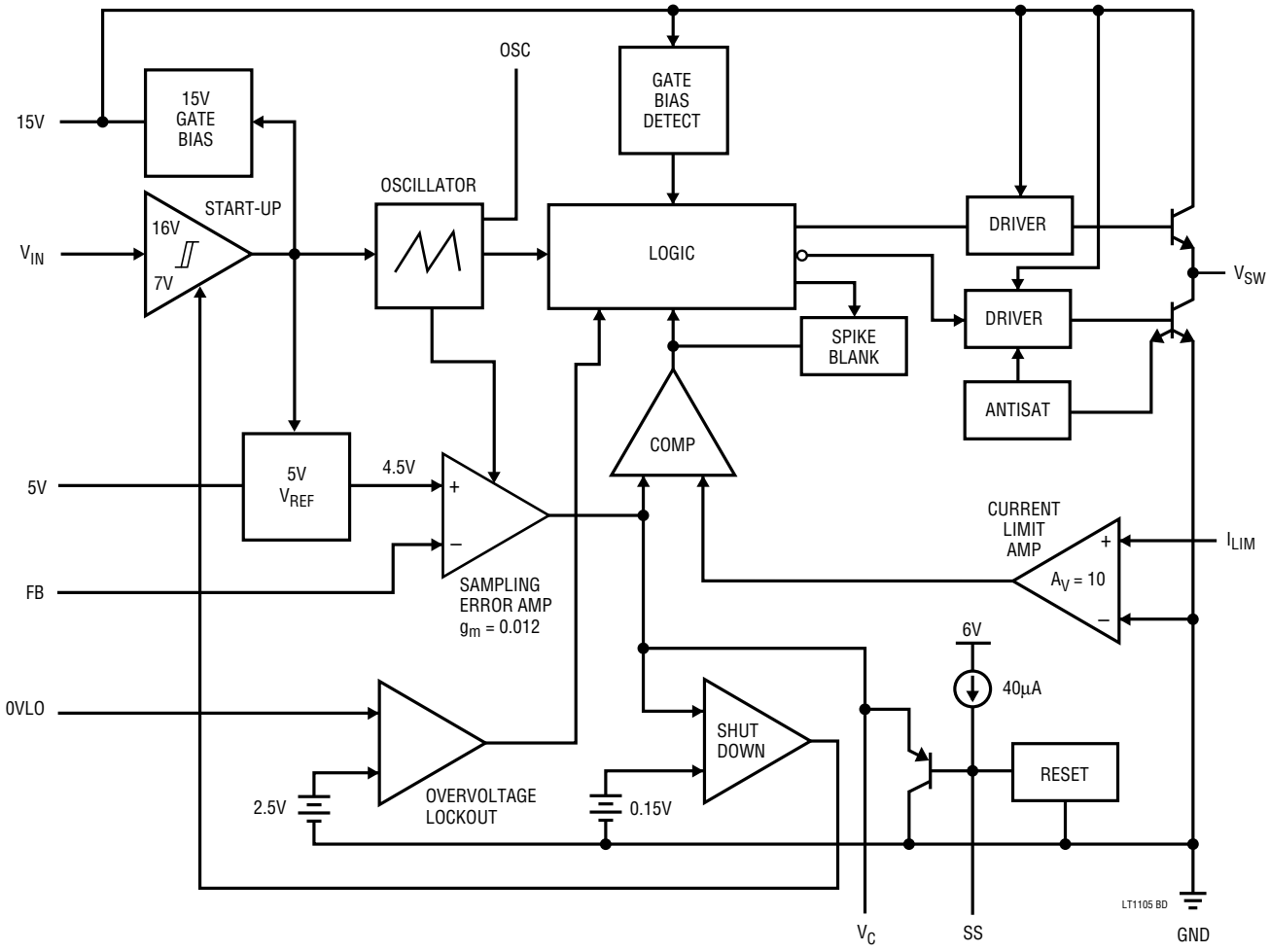
BLOCK DIAGRAMS

LT1103



BLOCK DIAGRAMS

LT1105



OPERATION

LT1103

The LT1103 is a current mode switcher. Switch duty cycle is controlled by switch current rather than directly by the output voltage. Referring to the block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid frequencies in the transformer. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

A start-up loop with hysteresis allows the IC supply voltage to be bootstrapped from an extra primary side winding on the power transformer. From 0V to 16V on V_{IN}, the LT1103 is in a prestart mode and total input current is typically 200μA. Above 16V, up to 30V, the 6V regulator that biases the internal circuitry and the externally available 15V regulator is turned on. The internal circuitry remains biased on until V_{IN} drops below 7V and the part returns to the prestart mode. Output switching stops when the V_{SW} drive is less than 10V corresponding to V_{IN} of about 12V.

The oscillator provides the basic clock for all internal timing. Frequency is adjustable to 200kHz with one external capacitor from OSC to ground. The oscillator turns on the output switch via the logic and driver circuitry. Adaptive antisat circuitry detects the onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

The LT1103 is designed to drive the source of an external power FET in common gate configuration. The 15V regulator biases the gate to guarantee the FET is on when the switch is on. Special drive detection circuitry senses the gate bias voltage and prevents the output switch from turning on if the gate voltage is less than 10V or greater than 20V, the industry standards for power MOSFET operation.

The switch current is sensed internally and amplified to trip the comparator and turn off the switch according to the V_C pin control voltage. A blanking circuit suppresses the output of the current limit comparator for 500ns at the beginning of each switch cycle. This prevents false tripping of the comparator due to current spikes caused by external parasitic capacitance and diode stored charge.

The 4.5V Zener-based reference biases the positive input of the sampling error amplifier. The negative input (FB) is used for output voltage sensing. The sampling error amplifier allows the LT1103 to operate in fully isolated flyback mode by regulating from the flyback voltage of the bootstrap winding. The leakage inductance spike at the leading edge of the flyback waveform is ignored with a blanking circuit. The flyback waveform is directly proportional to the output voltage in a transformer-coupled flyback topology. Output voltages are fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings.

The error signal developed at the comparator input is brought out externally. This V_C pin has three functions including frequency compensation, current limit adjustment and total regulator shutdown. During normal operation, this pin sits at a voltage between 1.2V (low output current) and 4.4V (high output current). The error amplifier is a current output (g_m) type, so this voltage can be externally clamped for adjusting current limit. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1103 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown and places the LT1103 in a prestart mode.

LT1105

The LT1105 is a current mode switcher. Switch duty cycle is controlled by switch current rather than directly by output voltage. Referring to the block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level.

OPERATION

Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the transformer. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

A start-up loop with hysteresis allows the IC supply voltage to be bootstrapped from an extra primary side winding on the power transformer. From 0V to 16V on V_{IN}, the LT1105 is in prestart mode and total input current is typically 200μA. Above 16V, up to 30V, the 6V regulator that biases the internal circuitry and the externally available 5V and 15V regulators are turned on. The internal circuitry remains biased on until V_{IN} drops below 7V and the part returns to prestart mode. Output switching stops when the 15V gate bias reference is less than 10V corresponding to V_{IN} of about 12V.

The oscillator provides the basic clock for all internal timing. Frequency is adjustable to 200kHz with one external capacitor from OSC to ground. The oscillator turns on the output switch via the logic and driver circuitry.

The LT1105 is designed to drive the gate of an external power FET in common source configuration. The drivers and the 1A maximum totem-pole output stage are biased from the 15V gate bias reference. Special drive detection circuity senses the gate bias reference voltage and prevents the output switch from turning on if this voltage is less than 10V or greater than 20V. Break-Before-Make action of 200ns is built into each switch edge to eliminate cross conduction currents.

Switch current is sensed externally through a precision, power resistor. This allows for greater flexibility in switch current and output power than allowed by the LT1103. The voltage across the sense resistor is fed into the I_{LIM} pin and amplified to trip the comparator and turn off the switch according to the V_C pin control voltage. A blanking circuit suppresses the output of the current limit comparator for 500ns at the beginning of each switch cycle. This prevents false tripping of the comparator due to current spikes caused by external parasitic capacitance and diode stored charge.

A 4.5V Zener-based reference biases the positive input of the sampling error amplifier. The negative input (FB) is used for output voltage sensing. The sampling error amplifier allows the LT1105 to operate in fully isolated flyback mode by regulating the flyback voltage of the bootstrap winding. The leakage inductance spike at the leading edge of the flyback waveform is ignored with a blanking circuit. The flyback waveform is directly proportional to the output voltage in the transformer coupled flyback topology. Output voltages are fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings.

The error signal developed at the comparator input is brought out externally. The V_C pin has three functions including frequency compensation, current limit adjustment and total regulator shutdown. During normal operation, this pin sits at a voltage between 1.2V (low output current) and 4.4V (high output current). The error amplifier is a current output (g_m) type, so this voltage can be externally clamped for adjusting current limit. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1105 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown and places the LT1105 in prestart mode.

The SS pin implements soft-start with one external capacitor to ground. The internal pull-up current and clamp transistor limit the voltage at V_C to one diode drop above the voltage at the SS pin, thereby controlling the rate of rise of switch current in the regulator. The SS pin is reset to 0V when the LT1105 is in prestart mode.

A final protection feature includes overvoltage lockout monitoring of the main supply voltage on the OVLO pin. If the OVLO pin is greater than 2.5V, the output switch is prevented from turning on. This function can be disabled by grounding the OVLO pin.

APPLICATIONS INFORMATION

Bootstrap Start

It is inefficient as well as impractical to power a switching regulator control IC from the rectified DC input as this voltage is several hundred volts. Self-biased switching regulator topologies take advantage of a lower voltage auxiliary winding on the power transformer or inductor to power the regulator, but require a start-up cycle to begin regulation.

Start-up circuitry with hysteresis built into the LT1103/LT1105 allows the input voltage to increase from 0V to 16V before the regulator tries to start. During this time the start-up current of the switching regulator is typically 200μA and all internal voltage regulators are off. The low quiescent current allows the input voltage to be trickled up with only 500μA of current from the rectified DC line voltage, thereby minimizing power dissipation in the start-up resistor. At 16V, the internal voltage regulators are turned on and switching begins. If enough power feeds back through the auxiliary winding to keep the input voltage to the switching regulator above 12V, then switching continues and a bootstrap start is accomplished. If the input voltage drops below 12V, then the FET drive detection circuit locks out switching. The input voltage continues to fall as the V_{IN} bypass capacitor is discharged by the normal quiescent current of the LT1103/LT1105. Once the input voltage falls below 7V, the internal voltage regulators are turned off and the switching regulator returns to the low start-up current state. A continuous "burp start" mode indicates a fault condition or an incomplete power loop.

The trickle current required to bootstrap the regulator input voltage is typically generated with a resistor from the rectified DC input voltage. When combined with the regulator input bypass capacitor, the start-up resistor creates a ramp whose slope governs the turn-on time of the regulator as well as the period of the "burp start" mode. The design trade-offs are power dissipated in the trickle resistor, the turn-on time of the regulator, and the hold-up time of the regulator input bypass capacitor. The value of the start-up resistor is set by the minimum rectified DC input voltage to guarantee sufficient start-up current. The recommended minimum trickle current is 500μA. The power rating of the start-up resistor is set by the maximum rectified DC input voltage. A final consideration for the start-up resistor is to insure that the maximum voltage rating of the resistor is not exceeded. Typical carbon film resistors have a voltage rating of 250V. The most reliable and economical solution for the start-up resistor is generally provided by placing several 0.25W resistors in series.

The LT1103/LT1105 is designed to operate with supply pin voltages up to 30V. However, the auxiliary bias winding should be designed for a typical output voltage of 17V to minimize IC power dissipation and efficiency loss. Allowances must also be made for cross regulation of the bias voltage due to variations in the rectified DC line voltage and output load current.

Soft-Start

Soft-start refers to the controlled increase of switch current from a start-up or shutdown state. This allows the power supply to come up to voltage in a controlled manner and charge the output capacitor without activating current limit. In general, soft-start is not required on the LT1105 due to the design of the sampling error amplifier g_m stage which generates asymmetrical slew capability on the V_C pin.

This feature exhibits itself as a typical 3mA sink current capability on the V_C pin whereas source current is only 275μA. The low g_m of the error amplifier allows small-valued compensation capacitors to be used on V_C. This allows the sink current to slew the compensation capacitor quickly. Therefore, overshoot of the output voltage on start-up sequences and recovery from overload or short-circuit conditions is prevented. However, if a longer start-up period is required, the soft-start function can be used.

Soft-start is implemented with an internal 40μA pull-up and a transistor clamp on the V_C pin so that a single external capacitor from SS ground can define the linear ramp function. The voltage at V_C is limited to one V_{BE} above the soft-start pin (SS). The time to maximum switch current is defined as the capacitance on SS multiplied by the active range in volts of the V_C pin divided by the pull-up current:

$$T = \frac{C \bullet (3.2V)}{40\mu A}$$

APPLICATIONS INFORMATION

SS is reset to 0V whenever V_{IN} is less than 7V (prestart mode) or when shutdown is activated by pulling V_C below 0.15V. The SS pin has a guaranteed reset sink current of 1mA when either the regulator supply voltage V_{IN} falls below 7V or the regulator is placed in shutdown.

Shutdown

The LT1103/LT1105 can be put in a low quiescent current shutdown mode by pulling V_C below 150mV. In the shutdown mode the internal voltage regulators are turned off, SS is reset to 0V and the part draws less than 200μA. To initiate shutdown, about 400μA must be pulled out of V_C until the internal voltage regulators turn off. Then, less than 50μA pull-down current is required to maintain shutdown. The shutdown function has about 60mV of hysteresis on the V_C pin before the part returns to normal operation. Soft-start, if used, controls the recovery from shutdown.

5V Reference

A 5V reference output is available for the user's convenience to power primary-side circuitry or to generate a clamp voltage for switch current limiting. The output will source 25mA and the voltage temperature coefficient is typically 50ppm/°C. If bypassing of the 5V reference is required, a 0.1μF is recommended. Values of capacitance greater than 1μF may be susceptible to ringing due to decreased phase margin. In such cases, the capacitive load can be isolated from the reference output with a small series resistor at the expense of load regulation performance.

Overvoltage Lockout

The switching supply and primarily the external power MOSFET can be protected from an extreme surge of the input line voltage with the overvoltage lockout feature implemented on the OVLO pin. If the voltage on OVLO rises above its typical threshold voltage of 2.5V, output switching is inhibited. This feature can be implemented with a resistive divider off of the rectified DC input voltage. This feature is only available on the LT1105 in the 14-lead PDIP and must be tied to ground if left unused.

Ground (LT1103)

The ground pin of the LT1103 is important because it acts as the negative sense point for the internal error amplifier feedback signal, the negative sense point for the current limit amplifier, and as the high current path for the 2A switch. The tab of the 7-lead TO-220 is internally connected to GND (Pin 4).

To avoid degradation of load regulation, the feedback resistor divider string and the reference side of the bias winding should be directly connected to the ground pin on the package. These ground connections should not be mixed with high current carrying ground return paths. The length of the switch current ground path should be as short as possible to the input supply bypass capacitor and low resistance for best performance. The case of the LT1103 package is desirable to use as the high current ground return path as this is a lower resistive and inductive path than that of the actual package pin and will help minimize voltage spikes associated with the high dI/dt switch current.

Avoiding long wire runs to the ground pin minimizes load regulation effects and inductive voltages created by the high dI/dt switch current. Ground plane techniques should also be used and will help keep EMI to a minimum. Grounding techniques are illustrated in the Typical Applications section.

Ground (LT1105)

The ground pin of the LT1105 is important because it acts as the negative sense point for the internal error amplifier feedback signal and as the negative sense point for the current limit amplifier. The LT1105 8-pin PDIP has Pin 1 as its ground. The LT1105 14-pin PDIP has Pin 1 and Pin 7 as grounds and must be tied together for proper operation.

To avoid degradation of load regulation, the feedback resistor divider should be directly connected to the package ground pin. These ground connections should not be mixed with high current carrying ground return paths. The length of the switch current ground path should be as short as possible to the input supply bypass capacitor and

APPLICATIONS INFORMATION

low resistance for best performance. This will help minimize voltage spikes associated with the high dI/dt switch current.

Avoiding long wire runs to the ground pin minimizes load regulation effects and inductive voltages created by the high dI/dt switch current. Ground plane techniques should also be used and will help keep EMI to a minimum. Grounding techniques are illustrated in the Typical Applications section.

Oscillator

The oscillator of the LT1103/LT1105 is a linear ramp type powered from the internal 6V bias line. The charging currents and voltage thresholds are generated internally so that only one external capacitor is required to set the frequency. The 150μA pull-up current, which is on all the time, sets the preset maximum on-time of the switch and the 450μA pull-down current which is turned on and off, sets the dead time. The threshold voltages are typically 2V and 4.5V, so for a 400pF capacitor the ramp-up time of the voltage on the OSC pin is 6.67μs and the ramp-down time is 3.3μs, resulting in an operating frequency of 100kHz. Although the oscillator, as well as the rest of the switching regulator, will function at higher frequencies, 200kHz is the practical upper limit that will allow control range for line and load regulation. The lowest operating frequency is limited by the sampling error amplifier to about 10kHz.

The frequency temperature coefficient is typically –80ppm/°C with a good low T.C. capacitor. This means that with a low temperature coefficient capacitor, the temperature coefficient of the currents and the temperature coefficient of the thresholds sum to –80ppm/°C over the commercial temperature range. Bowing in the temperature coefficient of the currents affects the frequency about ±3% at the extremes of the military temperature range. The capacitor type chosen will have a direct effect on the frequency tempco.

Maximum duty cycle is set internally by the pull-up and pull-down currents, independent of frequency. It can be adjusted externally by modifying the fixed pull-up current with an additional resistor. In practice, one resistor from the OSC pin to the 5V reference or to ground does the job. Note that the capacitor value must change to maintain the same frequency. For example, a 24k resistor from 5V to OSC and a 440pF capacitor from OSC to ground will yield 100kHz with 50% maximum duty cycle. A 56k resistor and a 280pF capacitor from OSC to ground will yield 100 kHz with 80% maximum duty cycle.

The oscillator can be synchronized to an external clock by coupling a sync pulse into the OSC pin. The width of this pulse should be a minimum of 500ns. The oscillator can only be synchronized up in frequency and the synchronizing frequency must be greater than the maximum possible unsynchronized frequency (for the chosen oscillator capacitor value). The amplitude of the sync pulse must be chosen so that the sum of the oscillator voltage amplitude plus the sync pulse amplitude does not exceed the 6V bias reference. Otherwise, the oscillator pull-up current source will saturate and erroneous operation will result. If the LT1103/LT1105 is positioned on the primary side of the transformer and the external clock on the isolated secondary output side, the sync signal must be coupled into the OSC pin using a pulse transformer. The pulse transformer must meet all safety/isolation requirements as it also crosses the isolation boundary. An example of externally synchronizing the oscillator is shown in the Typical Applications section.

Gate Biasing (LT1103)

The LT1103 is designed to drive an external power MOSFET in the common gate or cascode connection with the V_{SW} pin. The advantage is that the switch current can be sensed internally, eliminating a low value, power sense resistor. The gate needs to be biased at a voltage high enough to guarantee that the FET is saturated when the open-collector source drive is on. This means 10V as specified in FET data sheets, plus 1V for the typical switch saturation voltage, plus a couple of volts for temperature variations and processing tolerances. This leads to 15V for a practical gate bias voltage.

Power MOSFETs are well suited to switching power supplies because their high speed switching characteristics promote high switching efficiency. To achieve high switching speed,

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A special circuit in the LT1103 senses the voltage at V_{SW} prior to turning on the switch. V_{SW} is tied to the source of the FET and should represent the bias voltage on the gate when the switch is off. When the switch first turns off, the drain flies back until it is clamped by a snubber network. The source also flies high due to parasitic capacitive coupling on the FET and parasitic inductance of the leads. An extra diode from the source to the gate or V_{IN} will provide insurance against fault conditions that might otherwise damage the FET. The diode clamps the source to one diode drop above the gate or V_{IN}, thereby limiting the gate source reverse bias. Once the energy in the leakage inductance spike is dissipated and the primary is being regulated to its flyback voltage, the diode shuts off. The source is then floating and its voltage will be close to the gate voltage. If the sensed voltage on V_{SW} is less than 10V or greater than 20V, the circuit prevents the switch from turning on. This protects the FET from dissipating high power in a nonsaturated state or from excessive gate-source voltage. The oscillator continues to run and the net effect is to skip switching cycles until the gate bias voltage is corrected. One consequence of the gate bias detection circuit is that the start-up window is 6V if the gate is biased from V_{IN} and to 4V if the gate is biased from the 15V output. This influences the size of the bypass capacitor on V_{IN}.

V_{SW} Output (LT1103)

The V_{SW} pin of the LT1103 is the collector of an internal NPN power switch. This NPN has a typical on resistance of 0.4Ω and a typical breakdown voltage (BV_{CBO}) of 75V. Fast switching times and high efficiency are obtained by using a special driver loop which automatically adapts base drive current to the minimum required to keep the switch in a quasisaturated state. The key element in the loop is an extra emitter on the output power transistor as seen in the block diagram. This emitter carries no current when the NPN output transistor collector is high (unsaturated). In this condition, the driver circuit can deliver very high base drive to the switch for fast turn-on. When the switch saturates, the extra emitter acts as a collector of an NPN operating in inverted mode and pulls base current away from the driver. This linear feedback loop serves itself to keep the switch just at the edge of saturation. Very low switch current results in nearly zero driver current and high switch currents automatically increase driver current as necessary. The ratio of switch current to driver current is approximately 30:1. This ratio is determined by the sizing of the extra emitter and the value of the current source feeding the driver circuitry. The quasisaturation state of the switch permits rapid turn-off without the need for reverse base emitter voltage drive.

Gate Biasing (LT1105)

The LT1105 is designed to drive an external power MOSFET in the common source configuration with the totem-pole output V_{SW} pin. The advantage is added switch current flexibility (limited only by the choice of external power FET) and higher output power applications than allowed by LT1103. An external, noninductive, power sense resistor must be used in series with the source of the FET to detect switch current and must be tied to the input of the current limit amplifier. The gate needs to be biased at a voltage high enough to guarantee that the FET is saturated when the totem-pole gate drive is on. This means 10V as specified in FET data sheets, plus the totem-pole high side saturation voltage plus a couple of volts for temperature variations and processing tolerances. This leads to 15V for a practical gate bias voltage.

Power MOSFETs are well suited to switching power supplies because their high speed switching characteristics promote high switching efficiency. To achieve high switching speed, the gate capacitance must be charged and discharged quickly with high peak currents. In particular, the turn-off current can be as high as the peak switch current. The switching speed is controlled by the impedance seen by the gate capacitance. Practically speaking, zero impedance is not desirable because of the high frequency noise spikes introduced to the system. The gate bias supply which drives the totem-pole output stage should be bypassed with a 1μF low ESR capacitor to ground. This capacitor supplies the energy to charge the gate capacitance during gate drive turn-on. The power MOSFET should have a 5Ω resistor or larger in series with its gate from the V_{SW} pin to define the source impedance.

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The LT1105 provides a 15V regulated output intended for driving the totem-pole output stage. It will source 30mA into a capacitive load with no stability problems. The output voltage temperature coefficient is 3mV/°C. If V_{IN} drops below 17V, the 15V output follows about 2.0V below V_{IN} until the part shuts down. If the 15V output is pulled above 17.5V, it will sink 5mA.

A special circuit in the LT1105 senses the voltage at the 15V regulated output prior to turning on the switch. The 15V regulator drives the totem-pole output stage and the V_{SW} pin will pull the gate of the FET very close to the value of the 15V output when V_{SW} turns on. Therefore, the 15V output represents what the gate bias voltage on the FET will be when the FET is turned on. If the sensed voltage on the 15V output is less than 10V or greater than 20V, the circuit prevents the switch from turning on. This protects the FET from dissipating high power in a nonsaturated state or from excessive gate-source voltage. The oscillator continues to run and the net effect is to skip switching cycles until the gate bias voltage is corrected. One consequence of the gate bias detection circuit is that the start-up window is 4V. This influences the size of the bypass capacitor on V_{IN}.

V_{SW} Output (LT1105)

The V_{SW} pin of the LT1105 is the output of a 1A totem-pole driver stage. This output stage turns an external power MOSFET on by pulling its gate high. Break-Before-Make action of 200ns is built into each switch edge to eliminate cross-conduction currents. Fast switching times and high efficiency are obtained by using a low loss output stage and a special driver loop which automatically adapts base drive current to the totem-pole low side drive. The key element in the loop is an extra emitter on the output pull-down transistor as seen in the block diagram. This emitter carries no current when the low side transistor collector is high (unsaturated). In this condition, the driver can deliver very high base drive to the output transistor for fast turn-off. When the low side transistor saturates, the extra emitter acts as a collector of an NPN operating in inverted mode and pulls base current away from the driver. This linear feedback loop serves itself to keep the switch just at the edge of saturation. This results in nearly zero driver current. The quasisaturation state of the low side switch permits rapid turn-on of the external FET when V_{SW} pulls high.

Fully Isolated Flyback Mode

A unique sampling error amplifier included in the control loop of the LT1103/LT1105 eliminates the need for an optoisolator while providing ±1% line and load regulation in a magnetic flux-sensed flyback converter. In this mode, the flyback voltage on the primary during "switch off" time is sensed and regulated. It is difficult to derive a feedback signal directly from the primary flyback voltage as this voltage is typically several hundred volts. A dedicated winding is not required because the bias winding for the regulator lends itself to flux-sensing. Flux-sensing made practical simplifies the design of off line power supplies by minimizing the total number of external components and reduces the components which must cross the isolation barrier to one, the transformer. This inherently implies greater safety and reliability. The transformer must be optimized for coupling between the bias winding and the secondary output winding(s) while maintaining the required isolation and minimizing the parasitic leakage inductances.

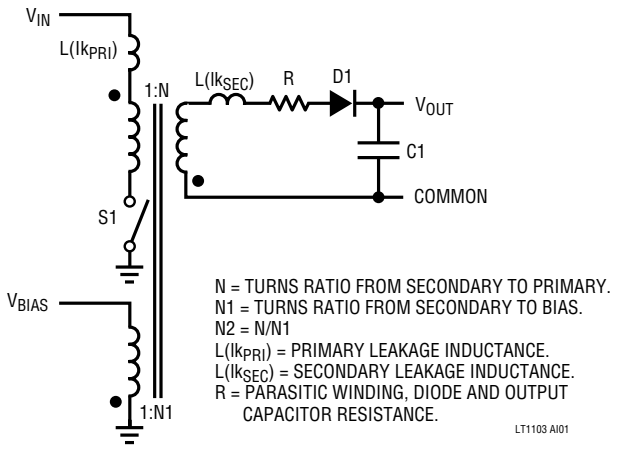
Although magnetic flux-sensing has been used in the past, the technique has exhibited poor output voltage regulation due to the parasitics present in a transformer coupled design. Transformers which provide the safety and isolation as required by various international safety/regulatory agencies also provide the poorest output voltage regulation. Solutions to these parasitic elements have been achieved with the novel sampling error amplifier of the LT1103/LT1105. A brief review of flyback converter operation and the problems which create a poorly regulated output will provide insight on how the sampling error amplifier of the LT1103/LT1105 addresses the regulation issue of magnetic flux sensed converters.

The following figure shows a simplified diagram of a flyback converter using magnetic flux sensing. The major parasitic elements present in the transformer coupled design are indicated. The relationships between the primary

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voltage, the secondary voltage, the bias voltage and the winding currents are indicated in the figures found on the following page for both continuous and discontinuous modes of operation.

Simplified Flyback Converter



When the switch "turns on," the primary winding sees the input voltage and the secondary and bias windings go to negative voltages as a function of the turns ratio. Current builds in the primary winding as the transformer stores energy. When the switch "turns off," the voltage across the switch flies back to a clamp level as defined by a snubber network until the energy in the leakage inductance of the primary dissipates. Leakage inductance is one of the main parasitic elements in a flux-sensed converter and is modeled as an inductor in series with the primary and secondary of the transformer. These parasitic inductances contribute to changes in the bias winding voltage and thus the output voltage with increasing load current.

The energy stored in the transformer transfers through the secondary and bias windings during "switch off" time. Ideally, the voltage across the bias winding is set by the DC output voltage, the forward voltage of the output diode, and the turns ratio of the transformer after the energy in the leakage inductance spike of the primary is dissipated.

This relationship holds until the energy in the transformer drops to zero (discontinuous mode) or the switch turns on again (continuous mode). Either case results in the voltage across the secondary and bias windings decreasing to zero or changing polarity. Therefore, the voltage on the bias winding is only valid as a representation of the output voltage while the secondary is delivering current.

Although the bias winding flyback voltage is a representation of the output voltage, its voltage is not constant. For a brief period following the leakage inductance spike, the bias winding flyback voltage decreases due to nonlinearities and parasitics present in the transformer. Following this nonlinear behavior is a period where the bias winding flyback voltage decreases linearly. This behavior is easily explained. Current flow in the secondary decreases linearly at a rate determined by the voltage across the secondary and the inductance of the secondary. The parasitic secondary leakage inductance appears as an impedance in series with the secondary winding. In addition, parasitic resistances exist in the secondary winding, the output diode and the output capacitor. These impedances can be combined to form a lumped sum equivalent and which cause a voltage drop as secondary current flows. This voltage drop is coupled from the secondary to the bias winding flyback voltage and becomes more significant as the output is loaded more heavily. This voltage drop is largest at the beginning of "switch off" time and smallest just prior to either all transformer energy being depleted or the switch turning on again.

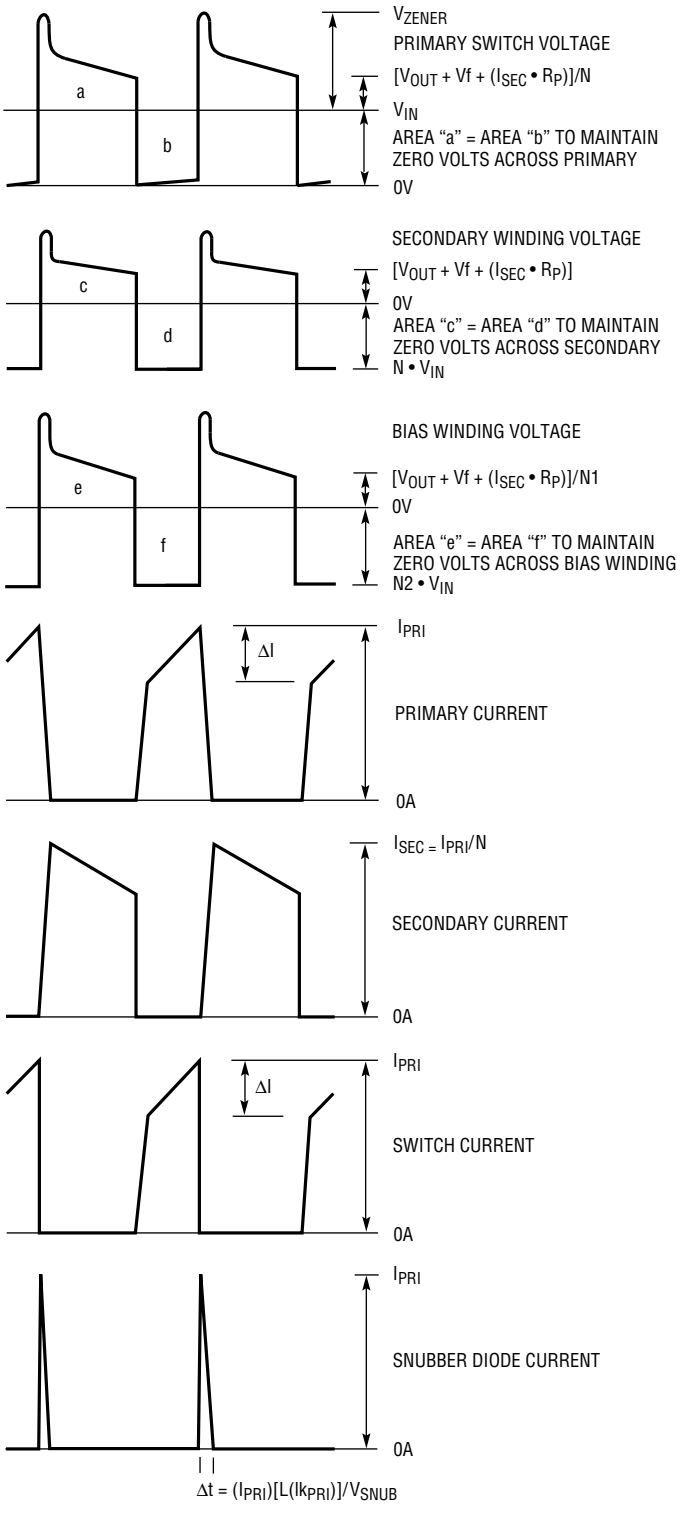
The best representation of the output voltage is just prior to either all transformer energy being used up and the bias winding voltage collapsing to zero or just prior to the switch turning on again and the bias winding going negative. This point in time also represents the smallest forward voltage for the output diode. It is possible to redefine the relationship between the secondary winding voltage and the bias winding voltage as:

$$V_{BIAS} = \frac{\left(V_{OUT} + Vf + I \bullet R_P\right)}{N1}$$

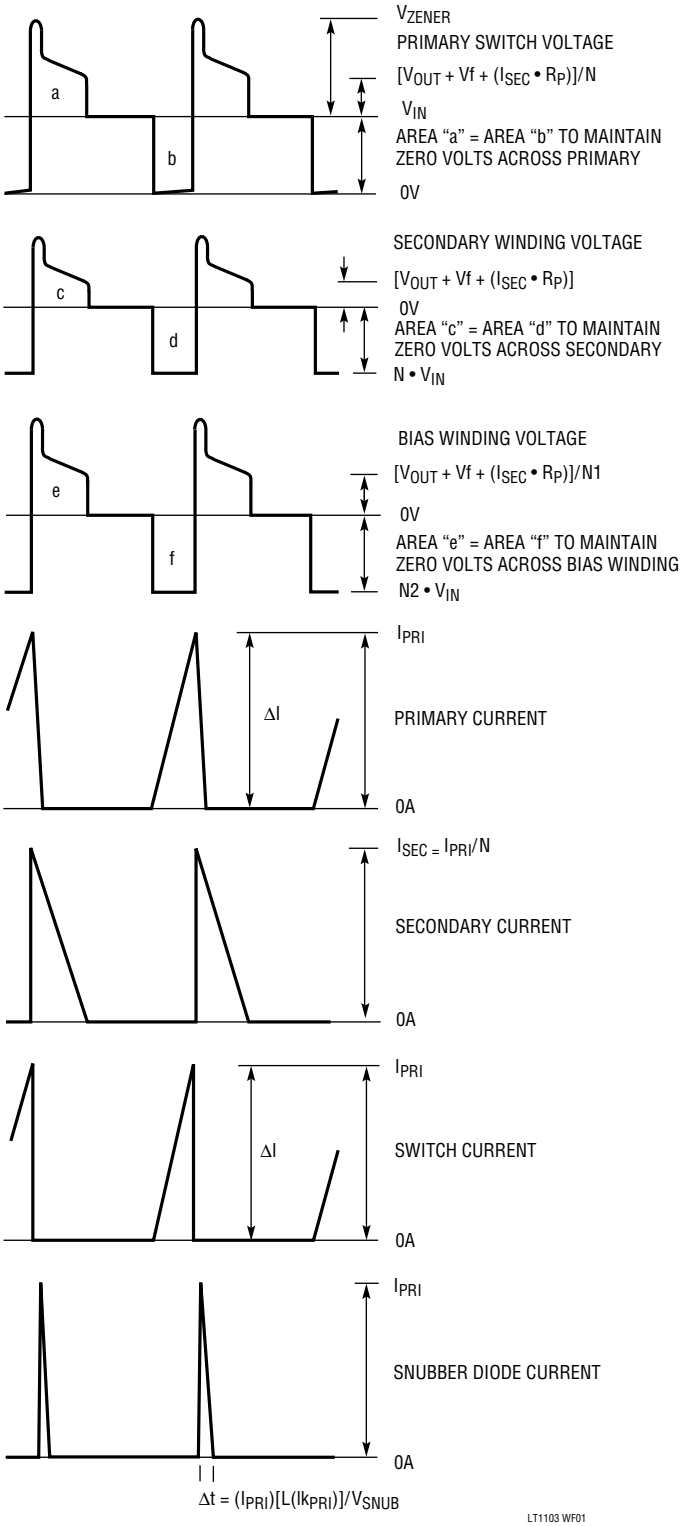
where Vf is the forward voltage of the output diode, I is the current flowing in the secondary, R_P is the lumped sum equivalent secondary parasitic impedance and N1 is the transformer turns ratio from the secondary to the bias winding. It is apparent that even though the above point in

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Flyback Waveform for Continuous Mode Operation



Flyback Waveform for Discontinuous Mode Operation



LT1103 WF01

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time is the most accurate representation of the output voltage, the answer given by the bias winding voltage is still off from the "true" answer by the amount $I \bullet R_P/N1$.

The sampling error amplifier of the LT1103/LT1105 provides solutions to the errors associated with the bias winding flyback voltage. The error amplifier is comprised of a leakage inductance spike blanking circuit, a slew rate limited tracking amplifier, a level detector, a sample-and-hold, an output g_m stage and load regulation compensation circuitry. This all seems complicated at first glance, but its operation is straightforward and transparent to the user of the IC. When viewed from a system or block level, the sampling error amplifier behaves like a simple transconductance amplifier. Here's how it works.

The sampling error amplifier takes advantage of the fact that the voltage across the bias winding during at least a portion of switch off time is proportional to the DC output voltage of the secondary winding. The feedback network used to sense the bias winding voltage is no longer comprised of a traditional peak detector in conjunction with a resistor divider network. The feedback network consists of a diode in series with the bias winding feeding the resistor divider network directly. The resultant error signal is then fed into the input of the error amplifier. The purpose of the diode in series with the bias winding is now not to peak detect, but to prevent the FB pin (input of the error amplifier) from being pulled negative and forward biasing the substrate of the IC when the bias winding changes polarity with "switch turn-on."

The primary winding leakage inductance spike effects are first eliminated with an internal blanking circuit in the LT1103/LT1105 which suppresses the input of the FB pin for 1.5µs at the start of "switch off" time. This prevents the primary leakage inductance spike from being propagated through the error amplifier and affecting the regulated output voltage.

With the effects of the leakage inductance spike eliminated, the effects of decreasing bias winding flyback voltage can be addressed. With the traditional diode/capacitor peak detector circuitry eliminated from the feedback network, the tracking amplifier of the LT1103/LT1105 follows the flyback waveform as it changes with time and amplifies the difference between the flyback signal and the internal 4.5V reference. Tracking is maintained until the point in time where the bias winding voltage collapses as a result of all transformer energy being depleted (discontinuous mode) or the switch turning on again (continuous mode). The level detector circuit senses the fact that the bias winding flyback voltage is no longer a representation of the output voltage and activates an internal peak detector. This effectively saves the most accurate representation of the output voltage which is then buffered to the second stage of the error amplifier.

The second stage of the error amplifier consists of a sample-and-hold. When the switch turns on, the sample-and-hold samples the buffered error voltage for 1µs and then holds for the remainder of the switch cycle. This held voltage is then processed by the output g_m stage and converted into a control signal at the output of the error amplifier, the V_C pin.

The final adjustment in regulation is provided by the load regulation compensation circuitry. As stated earlier, output regulation degrades with increasing load current (output power). The effect is traced to secondary leakage inductance and parasitic secondary winding, diode and output capacitor resistances. Even though the tracking amplifier has obtained the most accurate representation of the output voltage, its answer is still flawed by the amount of the voltage drop across the secondary parasitic lumped sum equivalent impedance which is coupled to the bias winding voltage. This error increases with increasing load current. Therefore, a technique for sensing load current conditions has been added to the LT1103/LT1105. The switch current is proportional to the load current by the turns ratio of the transformer. A small current proportional to switch current is generated in the LT1103/LT1105 and fed back to the FB pin. This allows the input bias current of the sampling error amplifier to be a function of load current. A resistor in series with the FB pin generates a linear increase in the effective reference voltage with increasing load current. This translates to a linear increase in output voltage with increasing load current. By adjusting the value of the series resistor, the slope of the load

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compensation can be set to cancel the effects of these parasitic voltage drops. The feature can be ignored by eliminating the series resistor and lowering the equivalent divider impedance to swamp out the effects of the input bias current.

Frequency Compensation

In order to prevent a regulator loop using the LT1103/LT1105 from oscillating, frequency compensation is required. Although the architecture of the LT1103/LT1105 is simple enough to lend itself to a mathematical approach to frequency compensation, the added complication of input/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage and load current variations all suggest a more practical empirical approach. Many hours spent on breadboards have shown that the simplest way to optimize the frequency compensation of the LT1103/LT1105 is to use transient response techniques and an "RC" box to quickly iterate toward the final compensation network. Additional information on this technique of frequency compensation can be found in Linear Technology's Application Note 19.

In general, frequency compensation is accomplished with an RC series network on the V_C pin. The error amplifier has a g_m (voltage "in" to current "out") of ≈ 12000 μmhos. Voltage gain is determined by multiplying g_m times the total equivalent error amplifier output loading, consisting of the error amplifier output impedance in parallel with the series RC external frequency compensation network. At DC, the external RC can be ignored. The output impedance of the error amplifier is typically 100kΩ resulting in a voltage gain of ≈ 1200V/V. At frequencies just above DC, the voltage gain is determined by the external compensation, R_C and C_C. The gain at mid frequencies is given by:

$$A_V = \frac{g_m}{2\pi \bullet f \bullet C_C}$$

The gain at high frequencies is given by:

$$A_V = g_m \bullet R_C$$

Phase shift from the FB pin to the V_C pin is 90° at mid frequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. Thus, this RC series network forms a pole-zero pair. The pole is set by the high impedance output of the error amplifier and the value of C_C on the V_C pin. The zero is formed by the value of C_C and the value of R_C in series with C_C on the V_C pin. The RC series network will have capacitor values in the range of 0.1μF to 1.0μF and series resistor values in the range of 100Ω to 1000Ω.

It is noted that the RC network on the V_C pin forms the main compensation network for the regulator loop. However, if the load regulation compensation feature is used as explained in the section on fully-isolated flyback mode, additional frequency compensation components are required. The load regulation compensation feature involves the use of local positive feedback from the V_C pin to the FB pin. Thus, it is possible to add enough load regulation compensation to make the loop oscillate. In order to prevent oscillation, it is necessary to roll off this local positive feedback at high frequencies. This is accomplished by placing a capacitor in parallel with the compensation resistor which is in series with the FB pin. A value for this capacitor in the range of 0.01μF to 0.1μF is recommended. The time constant associated with this RC combination will be longer than that associated with the loop bandwidth. Thus, transient response will be affected in that settling time will be increased. However, this is typically not as important as controlling the absolute under or overshoot amplitude of the system in response to load current changes which could cause deleterious system operation.

Switching Regulator Topologies

Two basic switching regulator topologies are pertinent to the LT1103/LT1105, the flyback and forward converter. The flyback converter employs a transformer to convert one voltage to either a higher or lower output voltage. V_{OUT} in *continuous mode* is defined as:

$$V_{OUT} = V_{IN} \bullet N \bullet \frac{DC}{(1-DC)}$$

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where N is the transformer turns ratio of secondary to primary and DC is the duty cycle. This formula can be rewritten in terms of duty cycle as:

$$DC = \frac{V_{OUT}}{\left(V_{OUT} + N \bullet V_{IN}\right)}$$

It is important to define the full range of input voltage, the range of output loading conditions and the regulation requirements for a design. Duty cycle should be calculated for both minimum and maximum input voltage.

In many applications, N can vary over a wide range without degrading performance. If maximum output power is desired, N can be optimized:

$$N_{(OPT)} = \frac{V_{OUT} + Vf}{\left(V_M - V_{IN(MAX)} - V_{SNUB}\right)}$$

where

Vf = Forward voltage of the output diode
V_M = Maximum switch voltage
V_{SNUB} = Snubber clamp level – primary flyback voltage.

In the isolated flyback mode, the LT1103/LT1105 sense and regulate the transformer primary voltage V_{PRI} during "switch off" time. The secondary output voltage will be regulated if V_{PRI} is regulated. V_{PRI} is related to V_{OUT} by:

$$V_{PRI} = \frac{\left(V_{OUT} + Vf\right)}{N}$$

This allows duty cycle for an isolated flyback converter to be rewritten as:

$$DC = \text{Duty Cycle} = \frac{V_{PRI}}{\left(V_{PRI} + V_{IN}\right)}$$

An important transformer parameter to be determined is the primary inductance L_{PRI}. The value of this inductance is a trade-off between core size, regulation requirements, leakage inductance effects and magnetizing current ΔI. Magnetizing current is the difference between the primary current at the start of "switch on" time and the current at the end of "switch on" time. If maximum output power is needed, a reasonable starting value is found by assigning ΔI a value of 20% of the peak switch current (2A for the LT1103 and set by the external FET rating used with the LT1105). With this design approach, L_{PRI} is defined as:

$$L_{PRI} = \frac{V_{IN}}{(\Delta I)(f)\left(1 + \frac{V_{IN}}{V_{PRI}}\right)}$$

If maximum output power is not required, then ΔI can be increased which results in lower primary inductance and smaller magnetics. Maximum output power with an isolated flyback converter is defined by the primary flyback voltage and the peak allowed switch current and is limited to:

$$P_{OUT(MAX)} = \frac{\left(V_{PRI}\right)}{\left(V_{PRI} + V_{IN}\right)}\left[V_{IN}\left(I_P - \frac{\Delta I}{2}\right) - (Ip)^2 R\right]E$$

where

R = Total "switch" on resistance
I_P = Maximum switch current
E = Overall efficiency ≈ 75%

Peak primary current is used to determine core size for the transformer and is found from:

$$I_{PRI} = \frac{\left(V_{OUT}\right)\left(I_{OUT}\right)\left(V_{PRI} + V_{IN}\right)}{E\left(V_{PRI}\right)\left(V_{IN}\right)} + \frac{\Delta I}{2}$$

A second consideration on primary inductance is the transition point from continuous mode to discontinuous mode. At light loads, the flyback pulse across the primary will drop to zero before the end of "switch off" time. The load current at which this starts to occur can be calculated from:

$$I_{OUT(TRANSITION)} = \frac{\left(V_{PRI} \bullet V_{IN}\right)^2}{\left(V_{PRI} + V_{IN}\right)^2\left(2V_{OUT}\right)\left(f\right)\left(L_{PRI}\right)}$$

The forward converter as shown below is another transformer-based topology that converts one voltage to either a higher or a lower voltage.

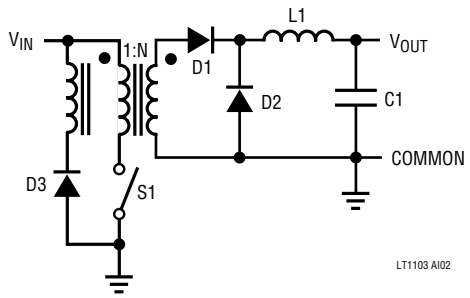
APPLICATIONS INFORMATION

V_{OUT} in *continuous mode* is defined as:

$$V_{OUT} = V_{IN} \bullet N \bullet DC$$

The secondary voltage charges up L1 through D1 when S1 is on. When S1 is off, energy in L1 is transferred through free-wheeling diode D2 to C1. The extra transformer winding and diode D3 are needed in a single switch forward converter to define the switch voltage when S1 is off. This "reset" winding limits the maximum duty cycle allowed for the switch. This topology trades off reduced transformer size for increased complexity and parts count. A separate isolated feedback path is required for full isolation from input to output because voltages on the primary are no longer related to the DC output voltage during switch off time.

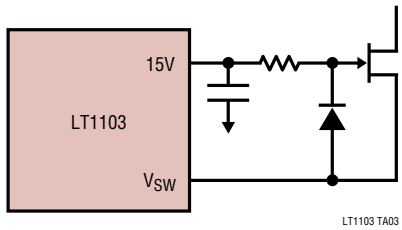
Simplified Forward Converter



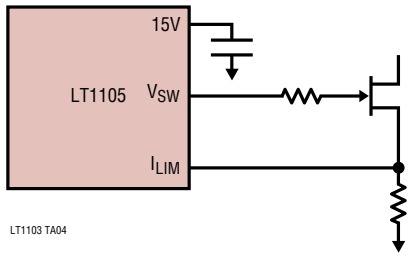
The isolated feedback path can take several forms. A second transformer in a modulator/demodulator scheme provides the isolation, but with significant complexity. An optoisolator can be substituted for the transformer with a savings in volume to be traded off with component variations and possible aging problems with the optoisolator transfer function. Finally, an extra winding closely coupled to the output inductor L1 can sense the flux in this element and give a representation of the output voltage when S1 is off.

TYPICAL APPLICATIONS

LT1103 FET Connection

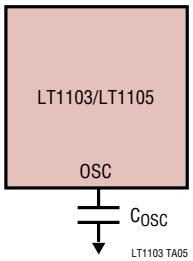


LT1105 FET Connection



TYPICAL APPLICATIONS

Setting Oscillator Frequency

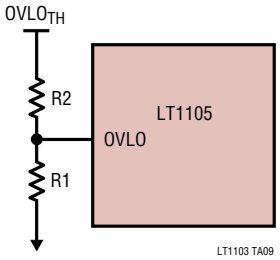


CHOOSE $20kHz \le f_{OSC} \le 200kHz$

$$C_{OSC} = \frac{SF}{f_{OSC}} = \frac{I}{(\Delta V)(f_{OSC})} = \frac{100\mu A}{(2.5V)(f_{OSC})}$$

$DC \cong 0.66 \Rightarrow 66\%$

Setting Overvoltage Lockout

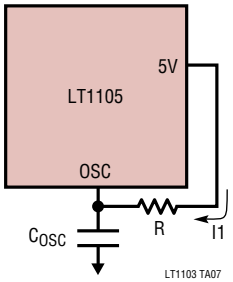


CHOOSE $OVLO_{TH}$

LET $R1 = 5k$

$$R2 = \left(\frac{OVLO_{TH}}{2.5V} - 1\right) R1$$

Decreasing Oscillator Maximum Duty Cycle



CHOOSE $0 \le DC \le 0.66$

SOLVE FOR $X \Rightarrow X = \frac{(6 - 9DC)}{2}$

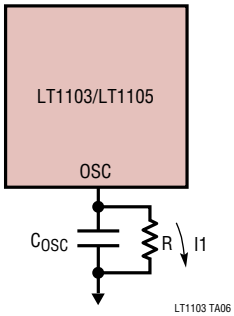
$0 \le X \le 3$

$\Rightarrow I1 = X \bullet I = X \bullet 100\mu A$

$$\Rightarrow R = \frac{1.75V}{I1}$$

$$C_{OSC} = \frac{100\mu A}{(2.5V)(f_{OSC})} \bullet \left[1 + \frac{(3X - 2X^2)}{9}\right]$$

Increasing Oscillator Maximum Duty Cycle



CHOOSE $0.66 \le DC \le 1.0$

SOLVE FOR $X \Rightarrow X = \frac{(9DC - 6)}{2}$

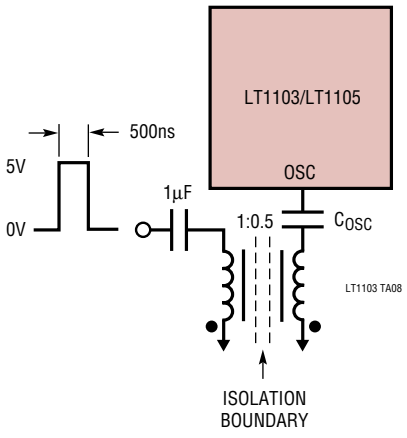
$0 \le X \le 1.5$

$\Rightarrow I1 = X \bullet I = X \bullet 100\mu A$

$$\Rightarrow R = \frac{3.25V}{I1}$$

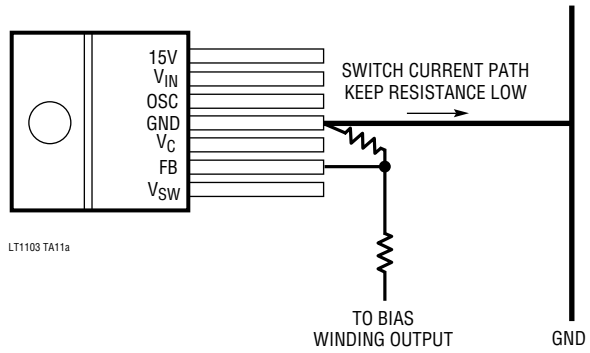
$$C_{OSC} = \frac{100\mu A}{(2.5V)(f_{OSC})} \bullet \left[1 - \frac{(3X + 2X^2)}{9}\right]$$

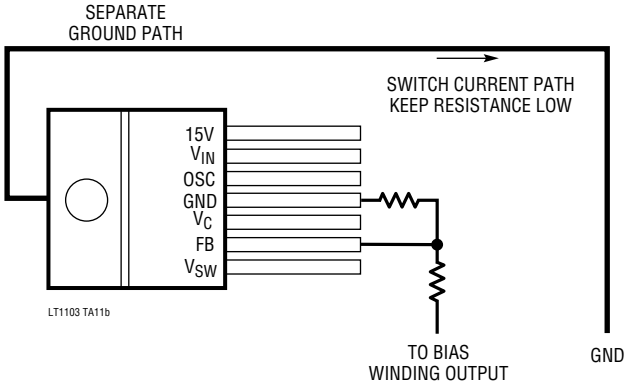
Synchronizing Oscillator Frequency to an External Clock



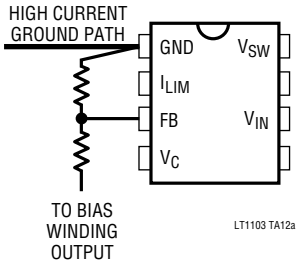
TYPICAL APPLICATIONS

LT1103 Ground Connections





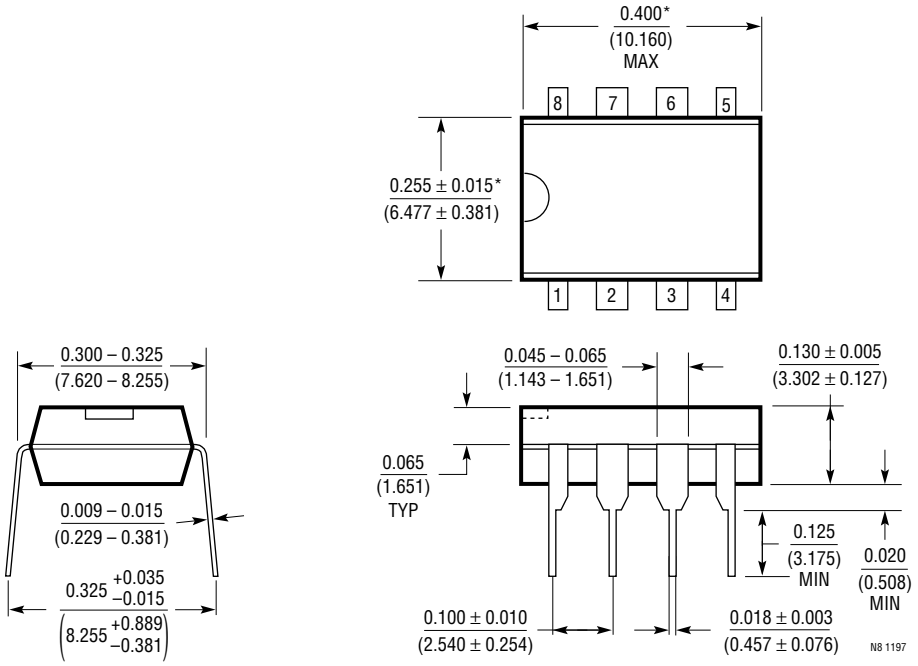
LT1105 Ground Connections



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

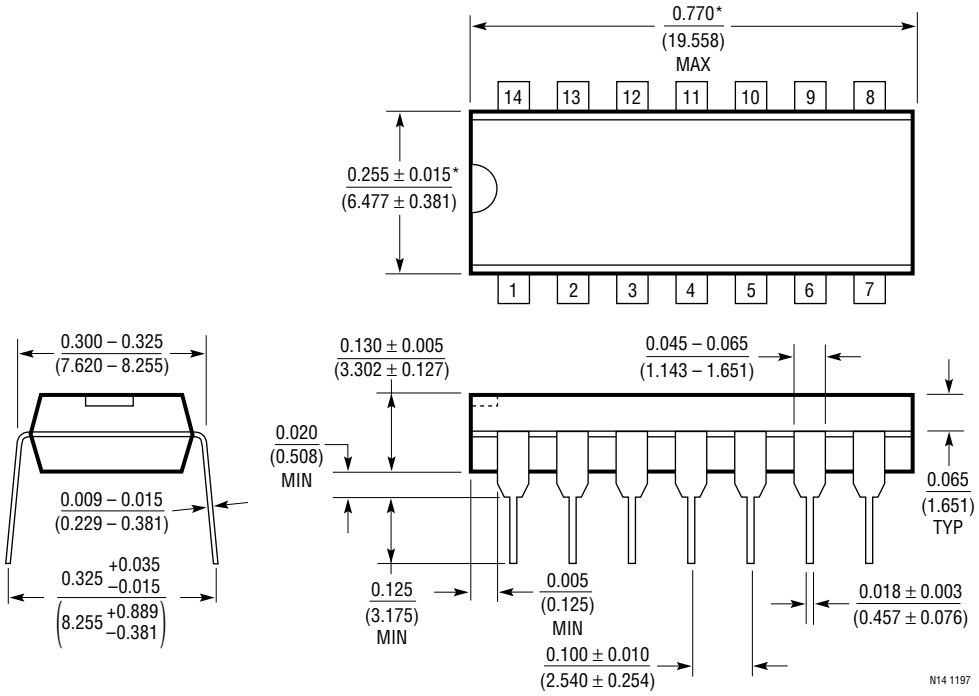


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

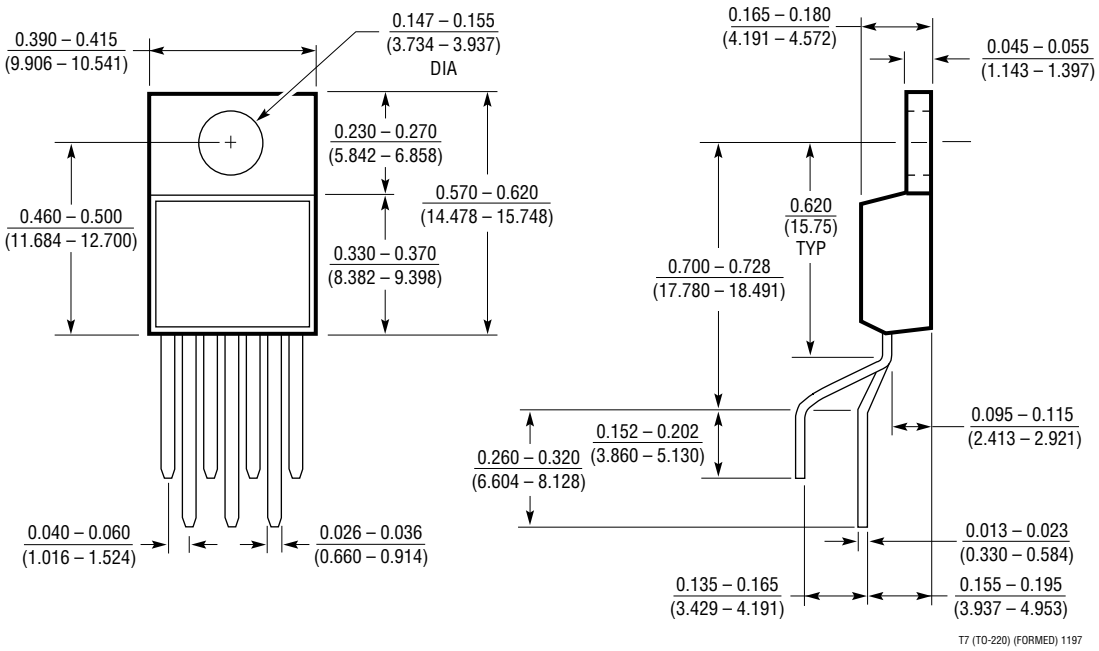


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

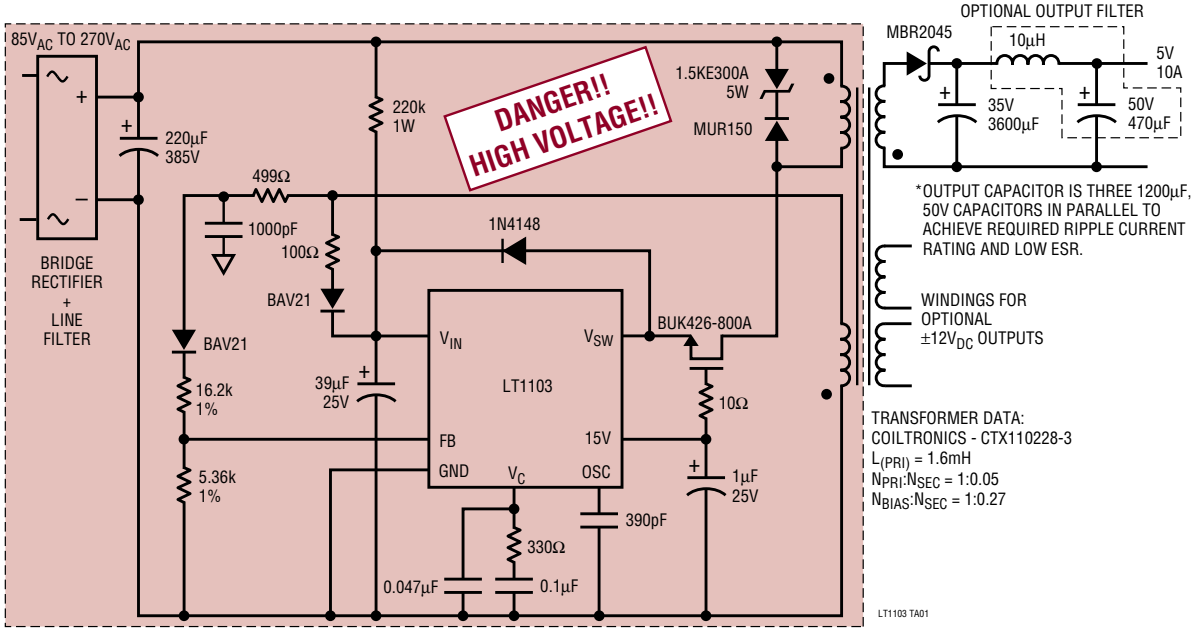
T7 Package
7-Lead Plastic TO-220 (Standard)
(LTC DWG # 05-08-1422)



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

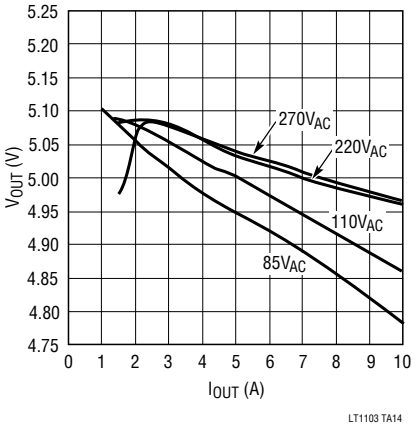
TYPICAL APPLICATION

Minimum Parts Count Fully-Isolated Flyback 100kHz 50W Converter



Danger!! Lethal Voltages Present – See Text

Load Regulation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1241	High Speed Current Mode Pulse Width Modulators	Up to 500kHz Operation
LT1246	Off-Line Current Mode PWM	1MHz Operation
LT1248	Power Factor Controller	Programmable Frequency, 16-Pin SO
LT1249	Power Factor Controller	100kHz, SO-8
LT1508	Power Factor and PWM Controller	Voltage Mode
LT1509	Power Factor and PWM Controller	Current Mode

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