150mA, Ultra-Low Quiescent Current, I_Q 1μA Low-Dropout Linear Regulator

FEATURES

- **Low I_Q: 1μA**
- **150mA, Low-Dropout Regulator**
- **Low-Dropout at +25°C, 130mV at 150mA**
- **Low-Dropout at +85°C, 175mV at 150mA**
- **3% Accuracy Over Load/Line/Temperature**
- **Available in Fixed Voltage Options (2.5V, 2.7V, and 2.8V) Using Innovative Factory EEPROM Programming**
- **Stable with a 1.0μF Ceramic Capacitor**
- **Thermal Shutdown and Overcurrent Protection**
- **CMOS Logic Level-Compatible Enable Pin**
- **Available in DDC (TSOT23-5) or DRV (2mm x 2mm SON-6) Packages**

APPLICATIONS

- **TI MSP430 Attach Applications**
- **Power Rails with Programming Mode**
- **Wireless Handsets, Smartphones, PDAs, MP3 Players, and Other Battery-Operated Handheld Products**

DESCRIPTION

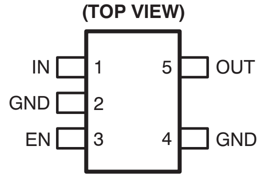
The TPS782 family of low-dropout regulators (LDOs) offers the benefits of ultra-low power (I_Q = 1μA), and miniaturized packaging (2×2 SON).

This LDO is designed specifically for battery-powered applications where ultra-low quiescent current is a critical parameter. The TPS782, with ultra-low I_Q (1μA), is ideal for microprocessors, memory cards, and smoke detectors.

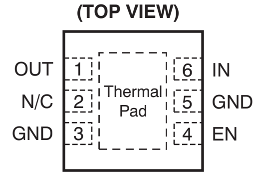
The ultra-low power and miniaturized packaging allow designers to customize power consumption for specific applications. Consult with your local factory representative for exact voltage options and ordering information; minimum order quantities may apply.

The TPS782 family is designed to be compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This LDO is stable with any output capacitor greater than 1.0μF. Therefore, this device requires minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS782 series also features thermal shutdown and current limit to protect the device during fault conditions. All packages have an operating temperature range of T_J = –40°C to +125°C. For high-performance applications that require a dual-level voltage option, consider the TPS780 series, with an I_Q of 500nA and dynamic voltage scaling.

TPS782xxDDC
TSOT23-5
(TOP VIEW)



TPS782xxDRV
2mm x 2mm SON-6
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

PRODUCT	V_{OUT}
TPS782***xxyyyz***	**XX** is the nominal output voltage **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Additional output voltage combinations are available on a quick-turn basis using innovative, factory EEPROM programming. Minimum-order quantities apply; contact your sales representative for details and availability

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

PARAMETER		TPS782xx	UNIT
Input voltage range, V_{IN}		–0.3 to +6.0	V
Enable		–0.3 to V_{IN} + 0.3V	V
Output voltage range, V_{OUT}		–0.3 to V_{IN} + 0.3V	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See the Dissipation Ratings table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–40 to +125	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	DRV	20°C/W	65°C/W	15.4mW/°C	1540mW	845mW	615mW
High-K(1)	DDC	90°C/W	200°C/W	5.0mW/°C	500mW	275mW	200mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

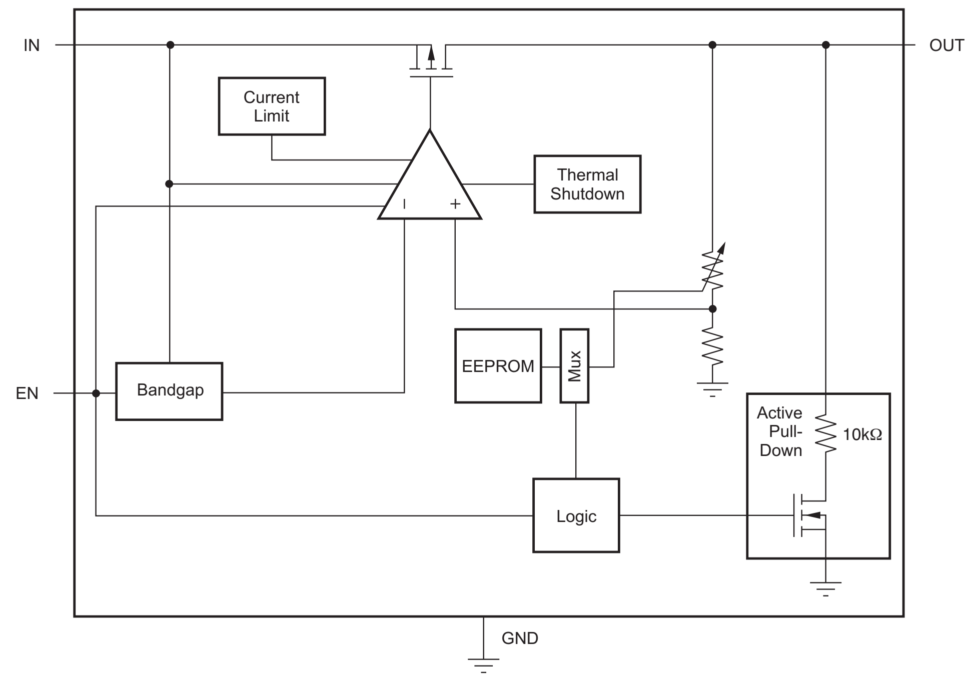
ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(NOM)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, $V_{EN} = V_{IN}$, C_{OUT} = 1.0µF, fixed V_{OUT} test conditions, unless otherwise noted. Typical values at T_J = +25°C.

				TPS782xx			
PARAMETER			**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
V_{IN}	Input voltage range			2.2		5.5	V
V_{OUT}	DC output accuracy	Nominal	T_J = +25°C	–2	±1	+2	%
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 150mA	–3.0	±2.0	+3.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 5mA		±1.0		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0mA ≤ I_{OUT} ≤ 150mA		±2.0		%
V_{DO}	Dropout voltage(1)		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 150mA		130	250	mV
V_N	Output noise voltage		BW = 100Hz to 100kHz, V_{IN} = 2.2V, V_{OUT} = 1.2V, I_{OUT} = 1mA		86		μV_{RMS}
I_{CL}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(NOM)}$	150	230	400	mA
I_{GND}	Ground pin current		I_{OUT} = 0mA		1.0	1.3	µA
			I_{OUT} = 150mA		8		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, 2.2V ≤ V_{IN} < 5.5V, T_J = –40°C to +100°C		18	130	nA
I_{EN}	EN pin current		V_{EN} = 5.5V			40	nA
PSRR	Power-supply rejection ratio		V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 150mA; f = 10Hz		40		dB
			f = 100Hz		20		dB
			f = 1kHz		15		dB
t_{STR}	Startup time(2)		C_{OUT} = 1.0µF, V_{OUT} = 10% $V_{OUT(NOM)}$ to V_{OUT} = 90% $V_{OUT(NOM)}$		500		µs
t_{SHDN}	Shutdown time(3)		I_{OUT} = 150mA, C_{OUT} = 1.0µF, V_{OUT} = 2.8V, V_{OUT} = 90% $V_{OUT(NOM)}$ to V_{OUT} = 10% $V_{OUT(NOM)}$		500(4)		µs
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		+160		°C
			Reset, temperature decreasing		+140		°C
T_J	Operating junction temperature			–40		+125	°C

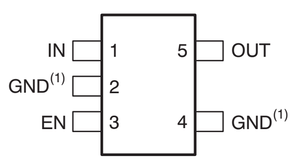
(1) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ ≤ 2.3V because minimum V_{IN} = 2.2V.
(2) Time from V_{EN} = 1.2V to V_{OUT} = 90% ($V_{OUT(NOM)}$).
(3) Time from V_{EN} = 0.4V to V_{OUT} = 10% ($V_{OUT(NOM)}$).
(4) See *Shutdown* in the *Application Information* section for more details.

FUNCTIONAL BLOCK DIAGRAM

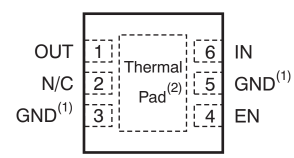


PIN CONFIGURATIONS

DDC PACKAGE
TSOT23-5
(TOP VIEW)



DRV PACKAGE
2mm x 2mm SON-6
(TOP VIEW)



(1) All ground pins must be connected to ground for proper operation.
(2) It is recommended that the thermal pad be grounded.

Table 1. PIN DESCRIPTIONS

PIN			
NAME	DRV	DDC	DESCRIPTION
OUT	1	5	Regulated output voltage pin. A small (1µF) ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* in the Application Information section for more details.
N/C	2	—	Not connected.
EN	4	3	Driving the enable pin (EN) over 1.2V turns ON the regulator. Driving this pin below 0.4V puts the regulator into shutdown mode, reducing operating current to 18nA typical.
GND	3, 5	2, 4	ALL ground pins must be tied to ground for proper operation.
IN	6	1	Input pin. A small capacitor is needed from this pin to ground to assure stability. Typical input capacitor = 1.0µF. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
Thermal pad	Thermal pad	—	It is recommended that the thermal pad on the SON-6 package be connected to ground.

TYPICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

LINE REGULATION
I_{OUT} = 5mA, V_{OUT} = 2.7V (typ)
TPS78227

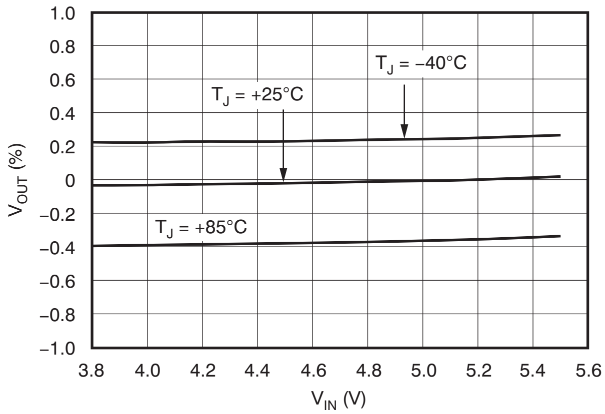


Figure 1.

LINE REGULATION
I_{OUT} = 150mA, V_{OUT} = 2.7V (typ)
TPS78227

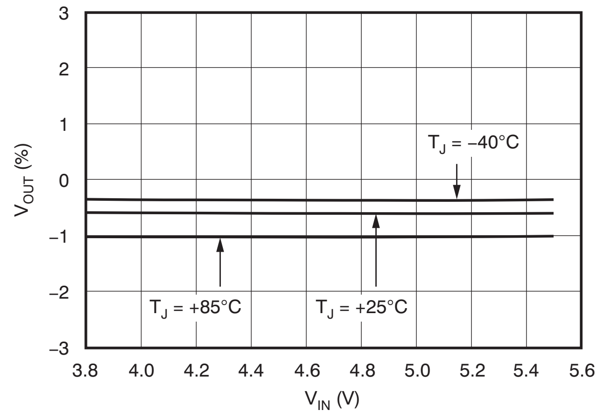


Figure 2.

LOAD REGULATION
V_{IN} = 3.8V, V_{OUT} = 2.7V
TPS78227

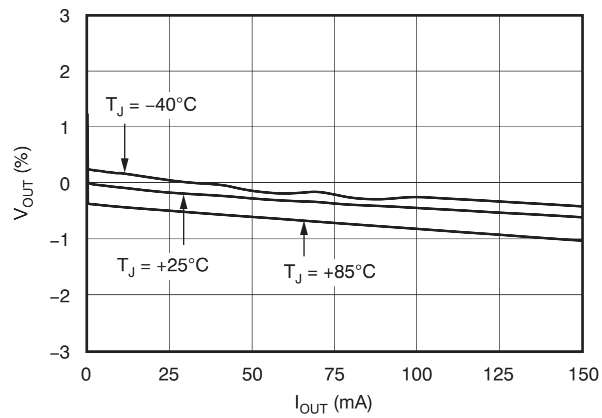


Figure 3.

DROPOUT VOLTAGE vs OUTPUT CURRENT
V_{OUT} = 2.7V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78227

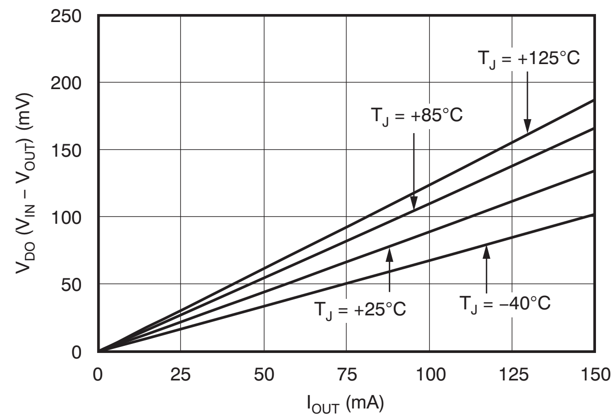


Figure 4.

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE
V_{OUT} = 2.7V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78227

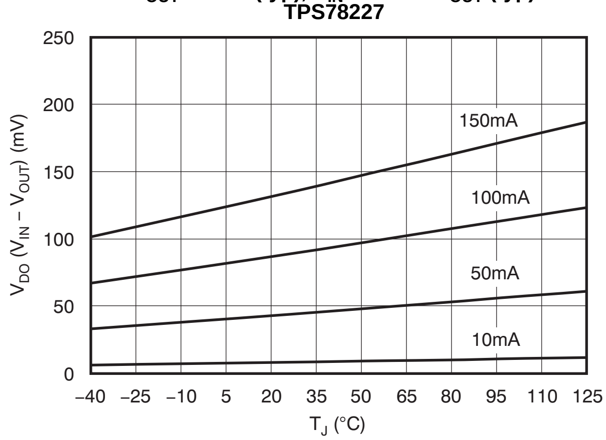


Figure 5.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50mA, V_{OUT} = 2.7V
TPS78227

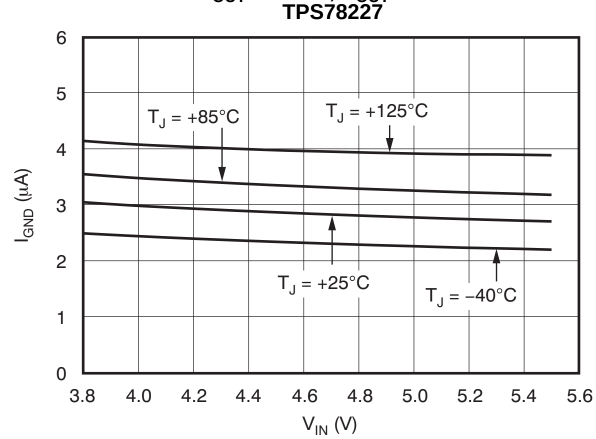


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150mA, V_{OUT} = 2.7V
TPS78227

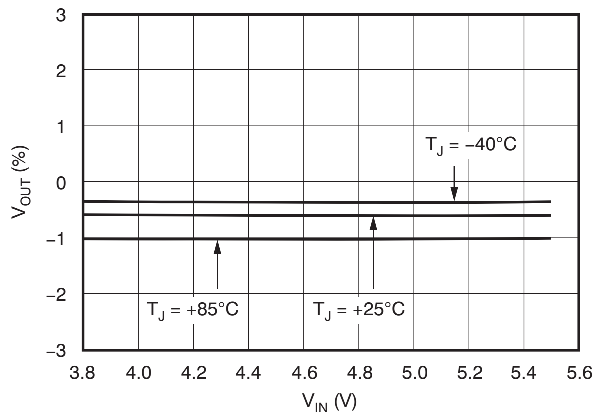


Figure 7.

CURRENT LIMIT vs INPUT VOLTAGE
V_{OUT} = 95% V_{OUT} (typ), V_{OUT} = 2.7V (typ)
TPS78227

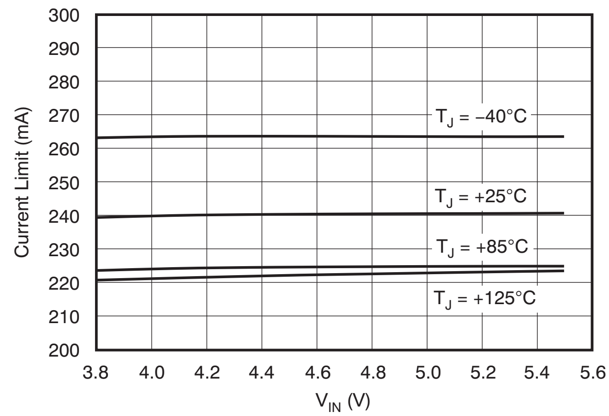


Figure 8.

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{OUT} = 2.7V
TPS78227

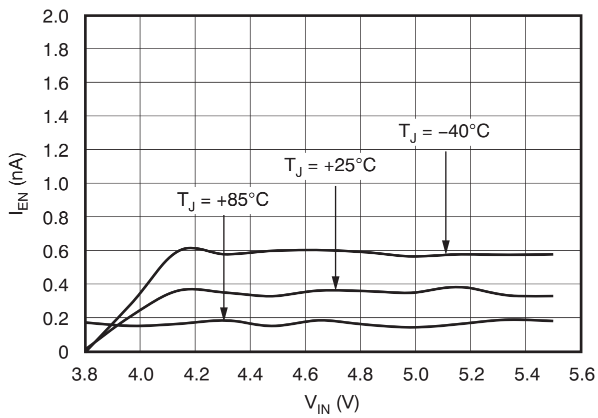


Figure 9.

ENABLE PIN HYSTERESIS vs JUNCTION TEMPERATURE
I_{OUT} = 1mA, TPS78227

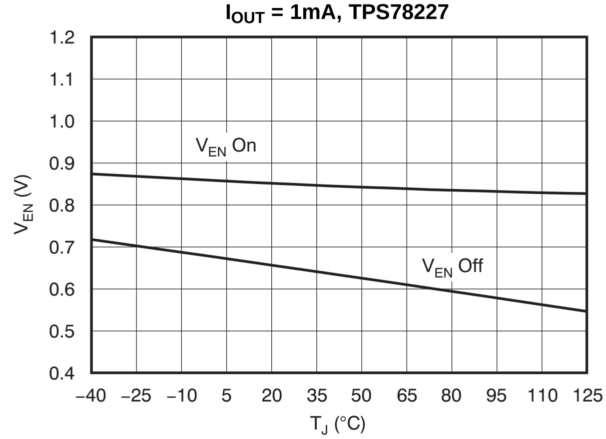


Figure 10.

%ΔV_{OUT} vs JUNCTION TEMPERATURE
V_{IN} = 3.3V, V_{OUT} = 2.7V (typ)
TPS78227

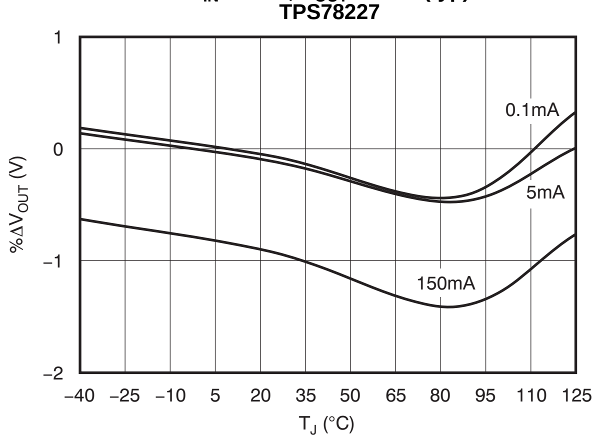


Figure 11.

%ΔV_{OUT} vs JUNCTION TEMPERATURE
V_{IN} = 3.7V, V_{OUT} = 2.7V (typ)
TPS78227

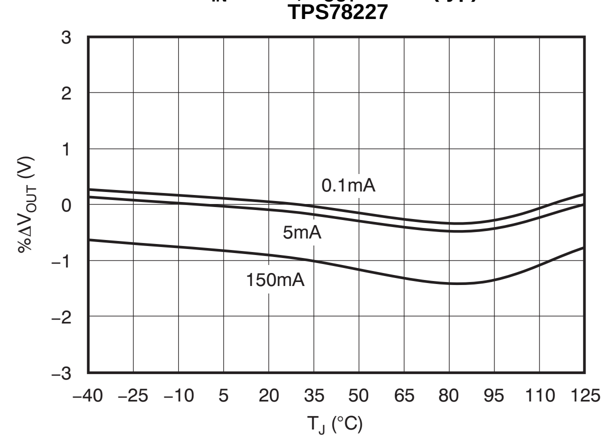


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY
C_{IN} = 1µF, C_{OUT} = 2.2µF, V_{IN} = 3.2V
TPS78227

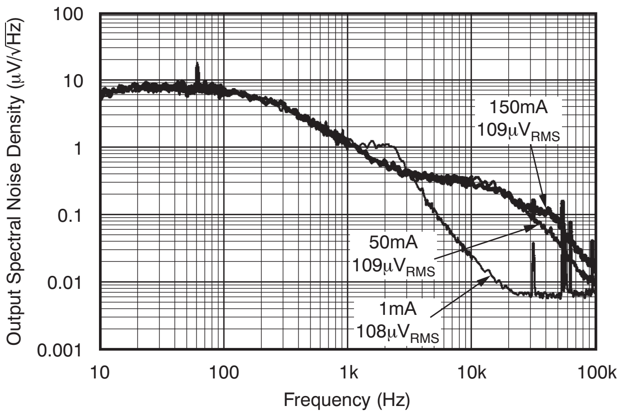


Figure 13.

RIPPLE REJECTION vs FREQUENCY
V_{IN} = 4.2V, V_{OUT} = 2.7V, C_{OUT} = 2.2µF
TPS78227

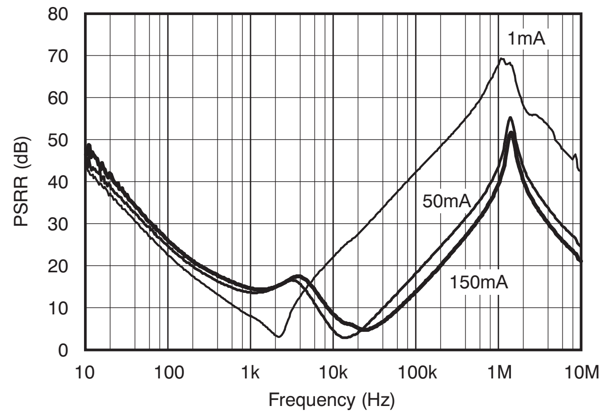


Figure 14.

INPUT VOLTAGE RAMP vs OUTPUT VOLTAGE
TPS78233

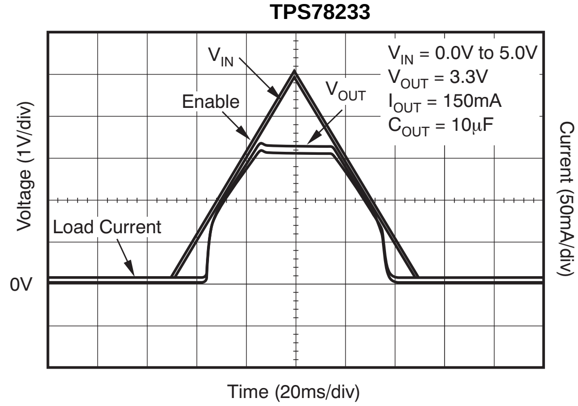


Figure 15.

OUTPUT VOLTAGE vs ENABLE (SLOW RAMP)
TPS78233

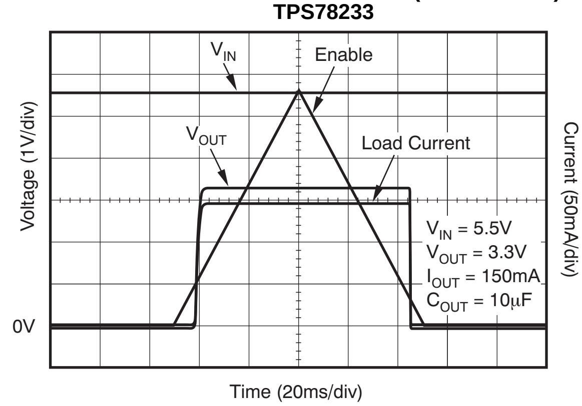


Figure 16.

INPUT VOLTAGE vs DELAY TO OUTPUT
TPS78222

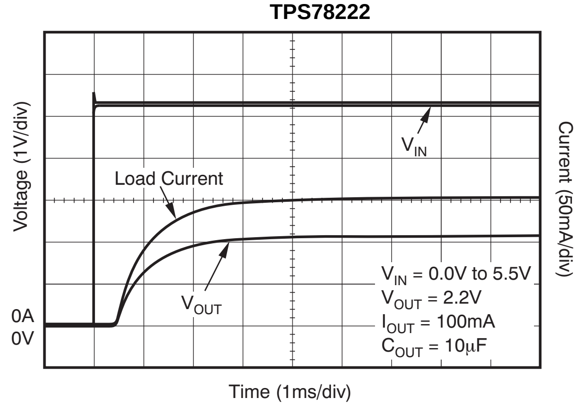


Figure 17.

LOAD TRANSIENT RESPONSE
TPS78233

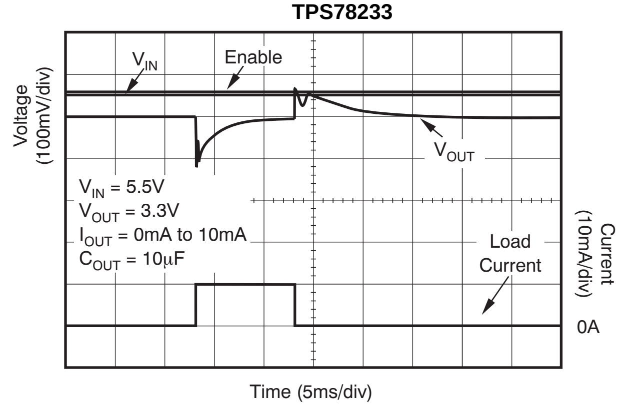


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100μA, V_{EN} = V_{IN}, C_{OUT} = 1μF, and C_{IN} = 1μF, unless otherwise noted.

ENABLE PIN vs OUTPUT VOLTAGE RESPONSE AND OUTPUT CURRENT
TPS78233

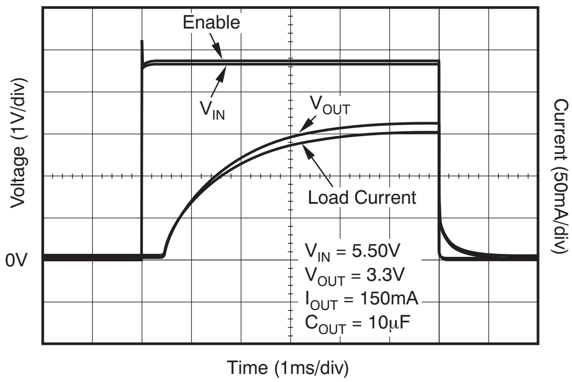


Figure 19.

ENABLE PIN vs OUTPUT VOLTAGE DELAY
TPS78233

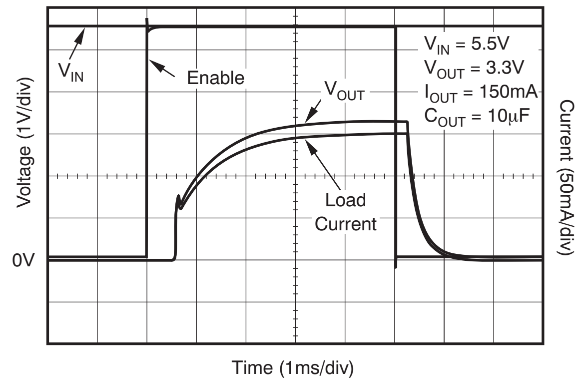


Figure 20.

APPLICATION INFORMATION

APPLICATION EXAMPLES

The TPS782 family of LDOs is factory-programmable to have a fixed output. Note that during startup or steady-state conditions, it is important that the EN pin voltage never exceed V_{IN} + 0.3V.

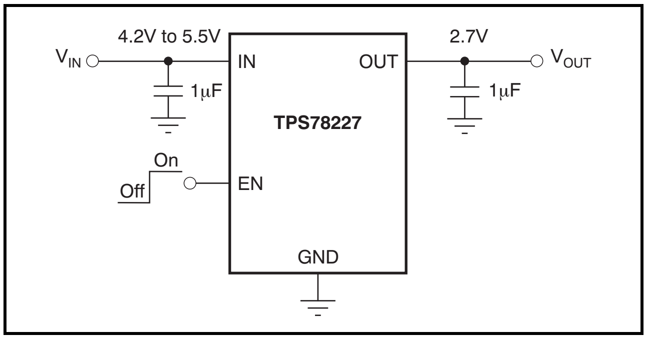


Figure 21. Typical Application Circuit

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS782 series are designed to be stable with standard ceramic capacitors with values of 1.0µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1µF.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TPS782 is internally current-limited to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS782 series has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, EN should be connected to the IN pin, as shown in Figure 22. The TPS782 series, with internal active output pull-down circuitry, discharges the output to within 5% V_{OUT} with a time (*t*) shown in Equation 1:

$$t = 3\left(\frac{10k\Omega \times R_L}{10k\Omega + R_L}\right) \times C_{OUT} \quad (1)$$

Where:

R_L= output load resistance

C_{OUT} = output capacitance

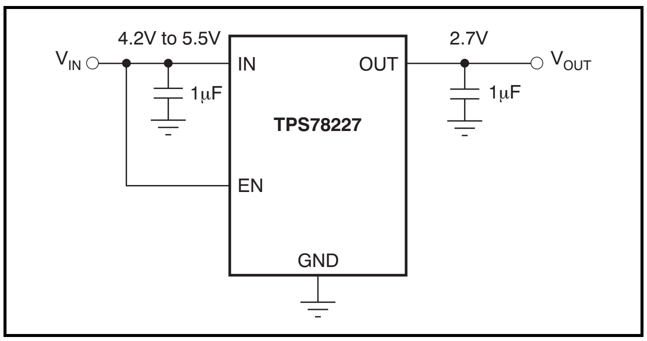


Figure 22. Circuit Showing EN Tied High when Shutdown Capability is Not Required

DROPOUT VOLTAGE

The TPS782 series use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the Typical Characteristics section. Refer to application report SLVA207, *Understanding LDO Dropout*, available for download from www.ti.com.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. For more information, see Figure 18.

ACTIVE V_{OUT} PULL-DOWN

In the TPS782 series, the active pull-down discharges V_{OUT} when the device is off. However, the input voltage must be greater than 2.2V for the active pull-down to work.

MINIMUM LOAD

The TPS782 series are stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS782 employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current. See Figure 18 for the load transient response.

THERMAL INFORMATION

THERMAL PROTECTION

Thermal protection disables the device output when the junction temperature rises to approximately +160°C, allowing the device to cool. Once the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS782 series has been designed to protect against overload conditions. However, it is not intended to replace proper heatsinking. Continuously running the TPS782 series into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the Dissipation Ratings table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS782 series are available from the Texas Instruments web site at www.ti.com through the TPS782 series product folders.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS78225DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78225DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78225DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS78225DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS78227DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78227DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78227DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS78227DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS78228DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78228DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78228DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS78228DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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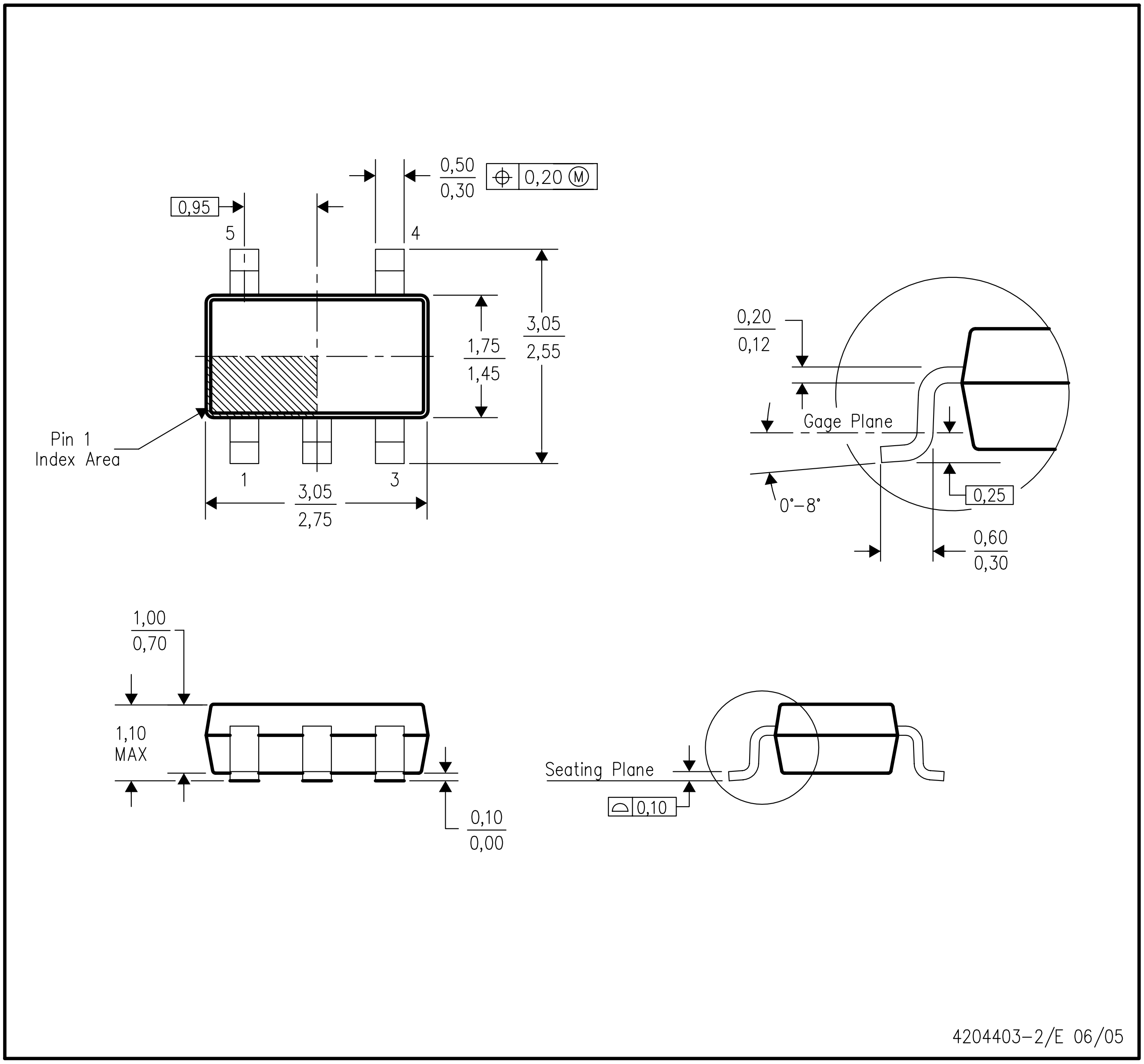
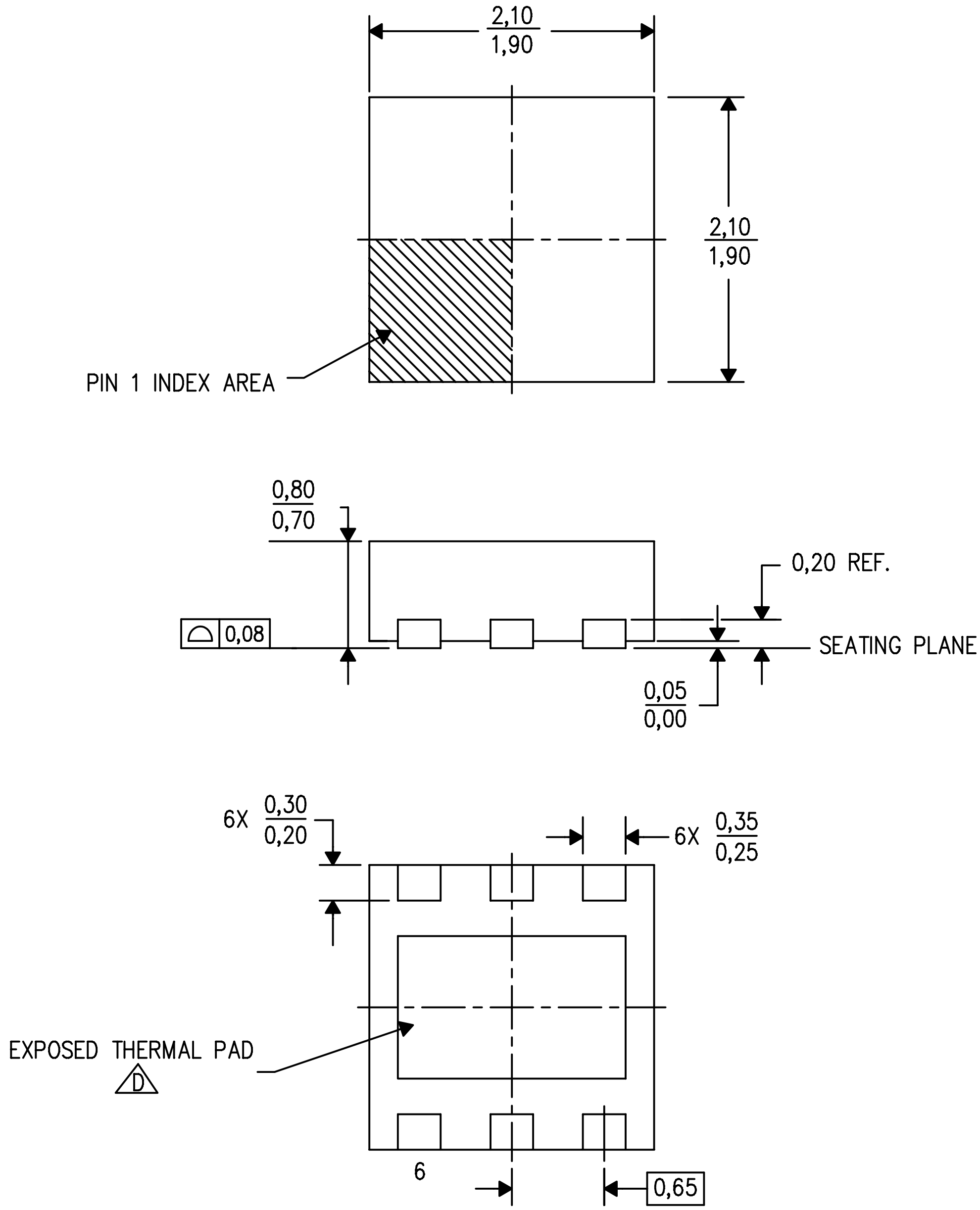
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DRV (S–PDSO–N6) PLASTIC SMALL OUTLINE



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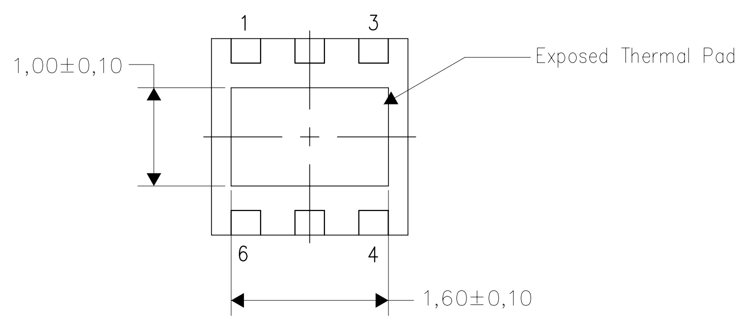
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

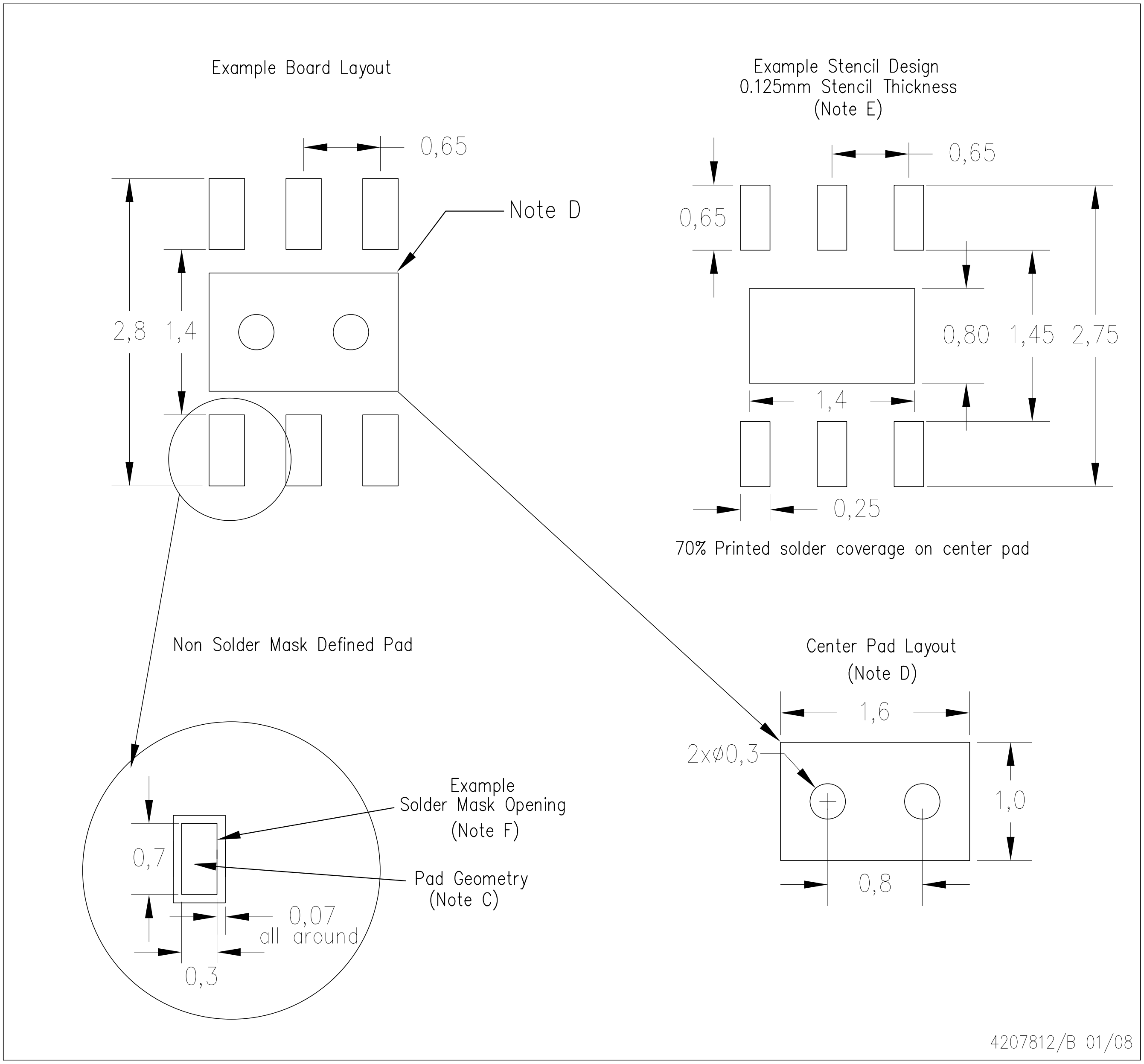


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S-PDSO-N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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