



2Mx64 3.3V Simultaneous Operation Flash Multi-Chip Package

FEATURES

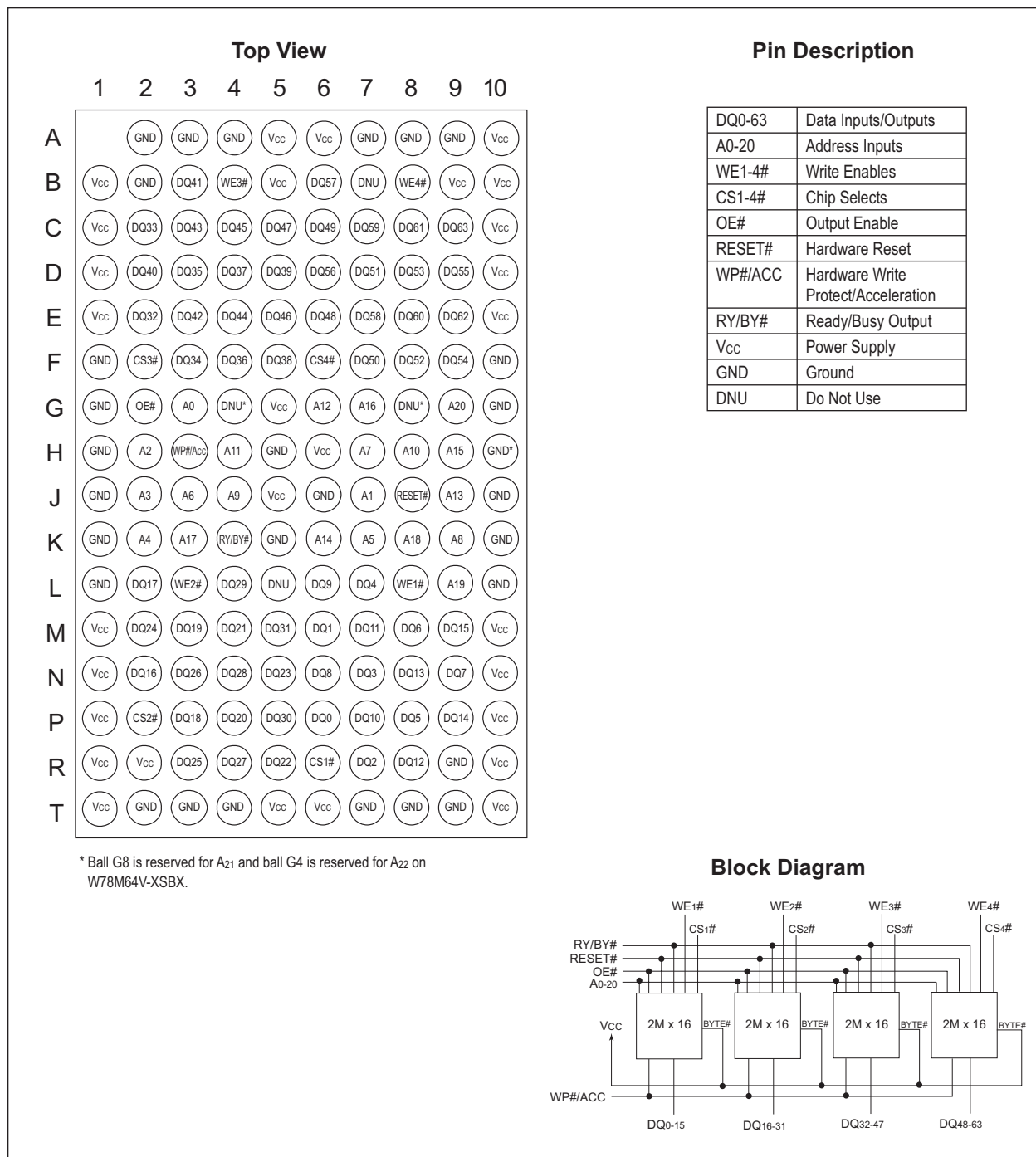
- Access Times of 90, 100, 120ns
- Packaging
 - 159 PBGA, 13x22mm - 1.27mm pitch
- 1,000,000 Erase/Program Cycles
- Sector Architecture
 - Bank 1 (4Mb): eight 4K word, eight 32K word
 - Bank 2 (12Mb): twenty-four 32K word
 - Bank 3 (12Mb): twenty-four 32K word
 - Bank 4 (4Mb): eight 32K word
- Bottom boot block
- Zero Power Operation
- Organized as 2Mx64 or 2x2Mx32
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Simultaneous Read/Write Operation:
 - Data can be continuously read from one bank while executing erase/program functions in another bank
 - Zero latency between read and write operations
- Erase Suspend/Resume
 - Suspends erase operations to allow programming in same bank
- Data# Polling and Toggle Bits
 - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
 - Reduces overall programming time when issuing multiple program command sequences
- Ready/Busy# output (RY/BY#)
 - Hardware method for detecting program or erase cycle completion
- Hardware reset pin (RESET#)
 - Hardware method of resetting the internal state machine to the read mode
- WP#/Acc input pin
 - Write protect (WP#) function allows protection two outermost boot sectors, regardless of sector protect status
 - Acceleration (Acc) function accelerates program timing
- Sector Protection
 - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
 - Temporary Sector Unprotect allows changing data in protected sectors in-system

Note: For programming information refer to Flash Programming W72M64V-XBX Application Note.

This product is subject to change without notice.



FIGURE 1: PIN CONFIGURATION FOR W72M64V-XBX





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V _{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to V _{CC} +0.5	V
Storage Temperature Range	-55 to +150	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

CAPACITANCE

T_A = +25°C, F = 1.0MHz

Parameter	Symbol	Max	Unit
WE1-4# capacitance	C _{WE}	8	pF
CS1-4# capacitance	C _{CS}	8	pF
Data I/O capacitance	C _{I/O}	10	pF
Address input capacitance	C _{AD}	30	pF
RESET# capacitance	C _{RS}	26	pF
RY/BY# capacitance	C _{RB}	26	pF
OE# capacitance	C _{OE}	32	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS – CMOS COMPATIBLE

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 3.6V, V _{IN} = GND to V _{CC}	-10	10	μA
Output Leakage Current	I _{LO}	V _{CC} = 3.6V, V _{OUT} = GND to V _{CC}	-10	10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	CS# = V _{IL} #, OE = V _{IH} , f = 5MHz		65	mA
V _{CC} Active Current for Program or Erase (2,3)	I _{CC2}	CS# = V _{IL} #, OE = V _{IH} , WE# = V _{IL}		120	mA
V _{CC} Standby Current (2)	I _{CC3}	CS# = RESET# = V _{CC} ± 0.3V		400	μA
Automatic Sleep Mode (2,4,5)	I _{CC5}	V _{IH} = V _{CC} ± 0.3V; V _{IL} = V _{SS} ± 0.3V		400	μA
V _{CC} Active Read-While-Program Current (1,2)	I _{CC6}	CS# = V _{IL} #, OE = V _{IH}		180	mA
V _{CC} Active Program-While-Erase Current (1,2)	I _{CC7}	CS# = V _{IL} #, OE = V _{IH}		180	mA
V _{CC} Active Program-While-Erase-Suspended Current (2,5)	I _{CC8}	CS# = V _{IL} #, OE = V _{IH}		140	mA
A _{CC} Accelerated Program Current	I _{ACC}	CS# = V _{IL} #, OE = V _{IH}		40	mA
				120	
		ACC Pin			
		VCC Pin			
Input Low Voltage	V _{IL}		-0.5	0.8	V
Input High Voltage	V _{IH}	V _{CC} = min	2.1	V _{CC} + 0.3	V
Voltage for WP#/A _{CC} Sector Protect/Unprotect and Program Acceleration	V _{HH}	V _{CC} = 3.0V + 0.3V	8.5	9.5	V
Voltage for Autoselect and Temporary Sector Unprotect	V _{ID}	V _{CC} = 3.0V + 0.3V	8.5	12.5	V
Output Low Voltage	V _{OL}	I _{OL} = 4.0 mA, V _{CC} = 3.0V		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.0 mA, V _{CC} = 3.0V	2.55		V
Low V _{CC} Lock-Out Voltage (5)	V _{LKO}		2.3	2.5	V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with OE# at V_{IH}.
- Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} MAX
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns.
- Not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – CS# CONTROLLED

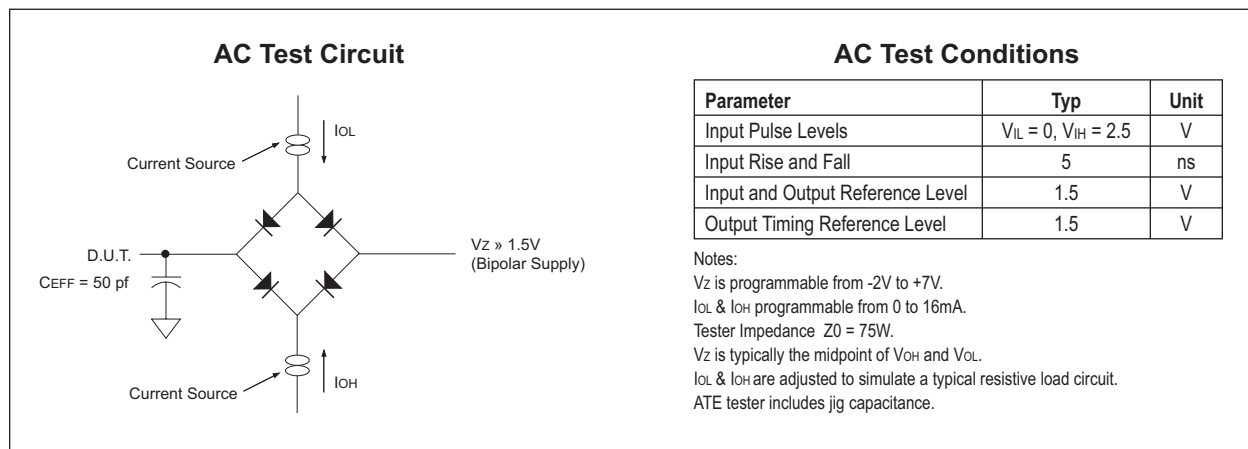
$$V_{CC} = 3.3V \pm 0.3V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$$

Parameter	Symbol		-90		-100		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (3)	t _{AVAV}	t _{WC}	90		100		120		ns
Write Enable Setup Time	t _{WLEL}	t _{WS}	0		0		0		ns
Chip Select Pulse Width	t _{TELEH}	t _{CP}	35		45		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	45		45		50		ns
Data Hold Time	t _{EHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	45		45		50		ns
Chip Select Pulse Width High (3)	t _{EH}	t _{CPH}	30		30		30		ns
Duration of Word Programming Operation (1)	t _{WHWH1}			300		300		300	μs
Sector Erase Time (2)	t _{WHWH2}			5		5		5	sec
Read Recovery Time Before Write (3)	t _{GH}		0		0		0		ns
Chip Programming Time (4)				42		42		42	sec

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 0.4 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

FIGURE 2





AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

$V_{CC} = 3.3V \pm 0.3V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-90		-100		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (3)	t _{AVAV}	t _{WC}	90		100		120		ns
Chip Select Setup Time (3)	t _{ELWL}	t _{CS}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	35		50		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	45		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		50		50		ns
Write Enable Pulse Width High (3)	t _{WHWL}	t _{WPH}	30		30		30		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300	μs
Sector Erase (2)	t _{WHWH2}			5		5		5	sec
Read Recovery Time before Write (3)	t _{GHWL}		0		0		0		ns
VCC Setup Time	t _{VCS}		50		50		50		μs
Chip Programming Time (4)				42		42		42	sec
Address Setup Time to OE# low during toggle bit polling		t _{ASO}	15		15		15		ns
Write Recovery Time from RY/BY# (3)		t _{RB}	0		0		0		ns
Program/Erase Valid to RY/BY#		t _{BUSY}	90		90		90		ns

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 0.4 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

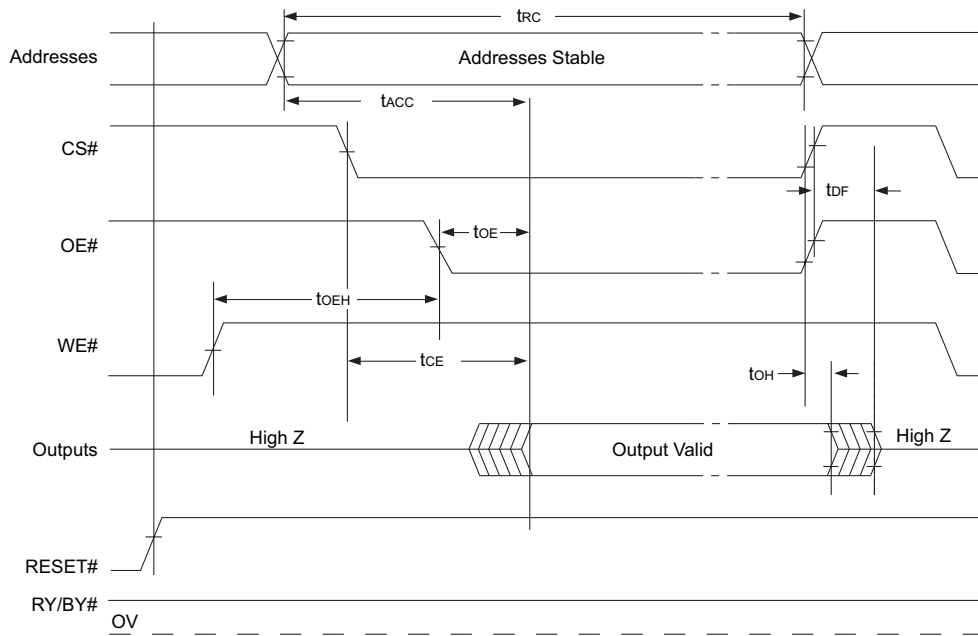
$V_{CC} = 3.3V \pm 0.3V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-90		-100		-120		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time (1)	t _{AVAV}	t _{RC}	90		100		120		ns
Address Access Time	t _{AVQV}	t _{ACC}		90		100		120	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		90		100		120	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		40		40		50	ns
Chip Select High to Output High Z	t _{EHQZ}	t _{DF}		20		20		20	ns
Output Enable High to Output High Z	t _{GHQZ}	t _{DF}		20		20		20	ns
Output Hold from Addresses, CS# or OE# Change, Whichever occurs first	t _{AXQX}	t _{OH}	0		0		0		ns
Output Enable Hold Time (1)	Read	t _{OEH}	0		0		0		
	Toggle and Data# Polling		10		10		10		

1. Guaranteed by design, not tested.



FIGURE 3: AC WAVEFORMS FOR READ OPERATIONS





AC CHARACTERISTICS – HARDWARE RESET (RESET#)

Parameter	Symbol	-90		-100		-120		Unit
		Min	Max	Min	Max	Min	Max	
RESET# Pin Low (During Embedded Algorithms) to Read Mode (1)	t_{ready}		20		20		20	μs
RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (1)	t_{ready}		500		500		500	ns
RESET# Pulse Width	t_{RP}	500		500		500		ns
RESET# High Time Before Read (1)	t_{RH}	50		50		50		ns
RESET# Low to Standby Mode (1)	t_{RPD}	20		20		20		μs

NOTE: 1. Not tested.

FIGURE 4: RESET TIMINGS NOT DURING EMBEDDED ALGORITHMS

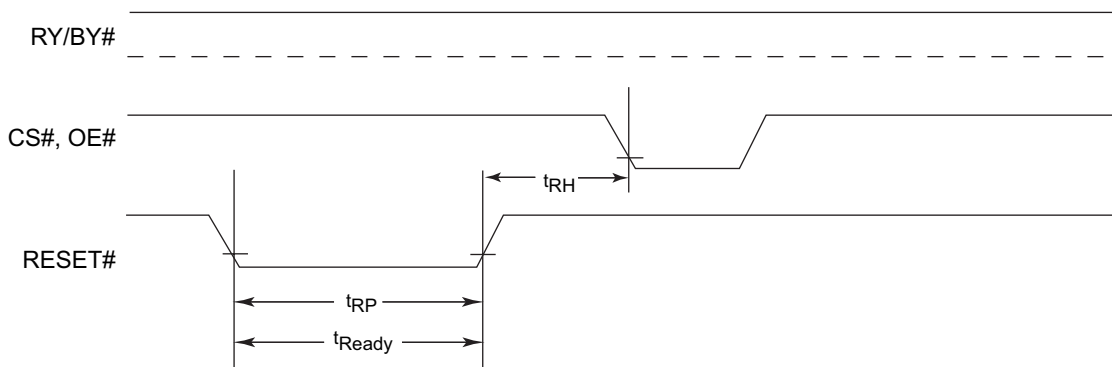


FIGURE 5: RESET TIMINGS DURING EMBEDDED ALGORITHMS

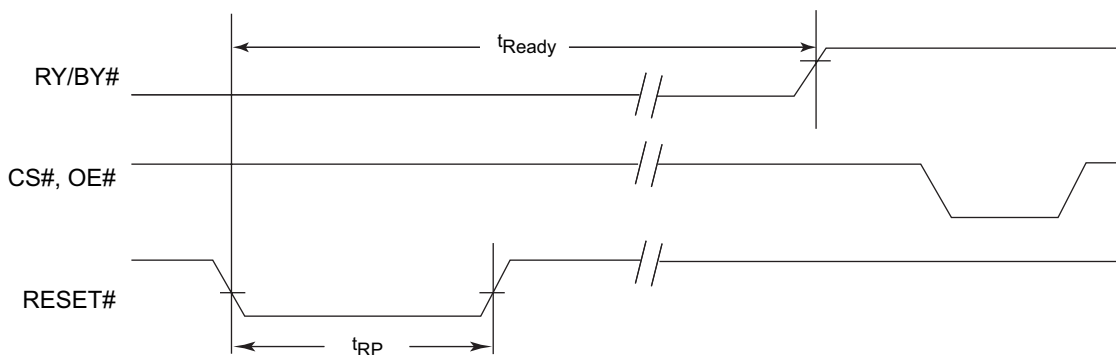
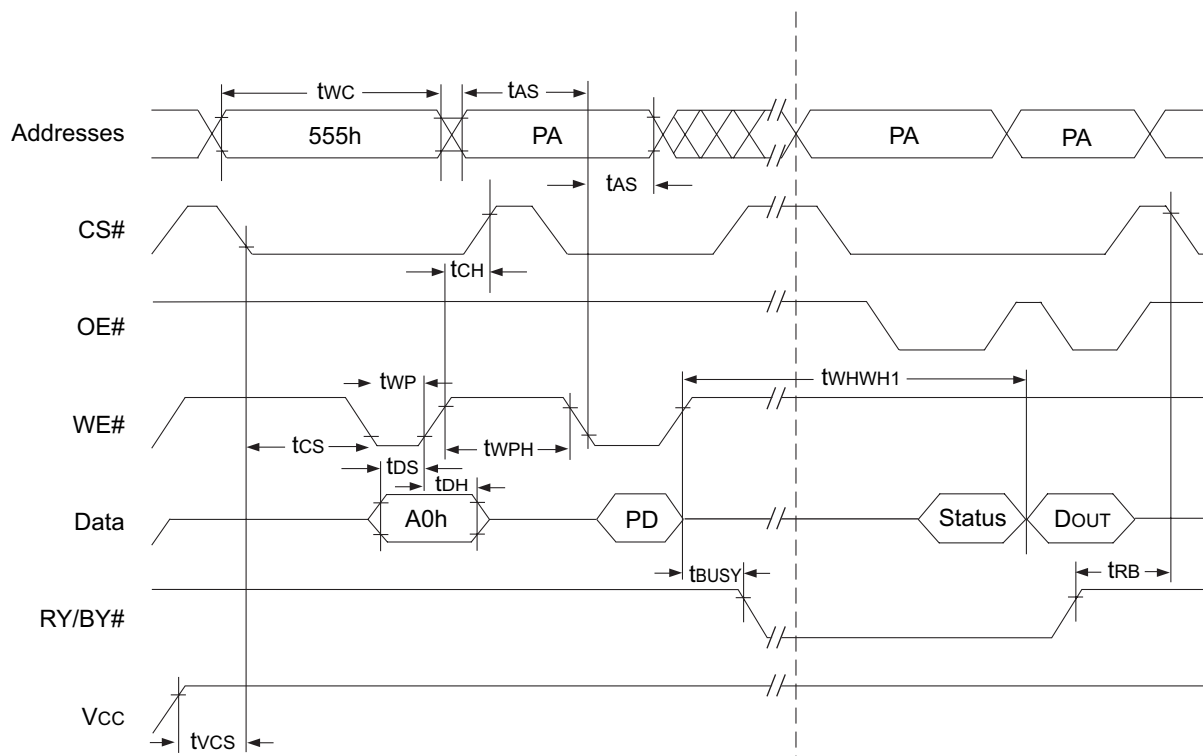




FIGURE 6: PROGRAM OPERATIONS



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. DOUT is the output of the data written to the device.
4. Figure indicates last two bus cycles of four bus cycle sequence.



FIGURE 7: ACCELERATED PROGRAM TIMING DIAGRAM

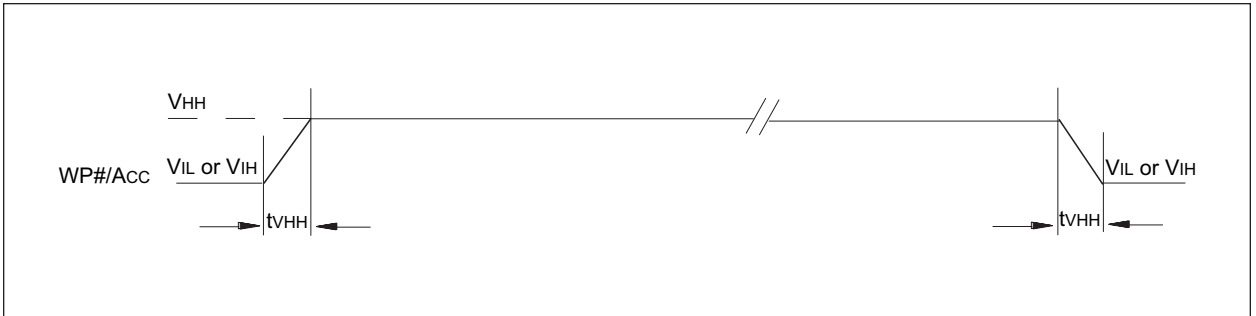
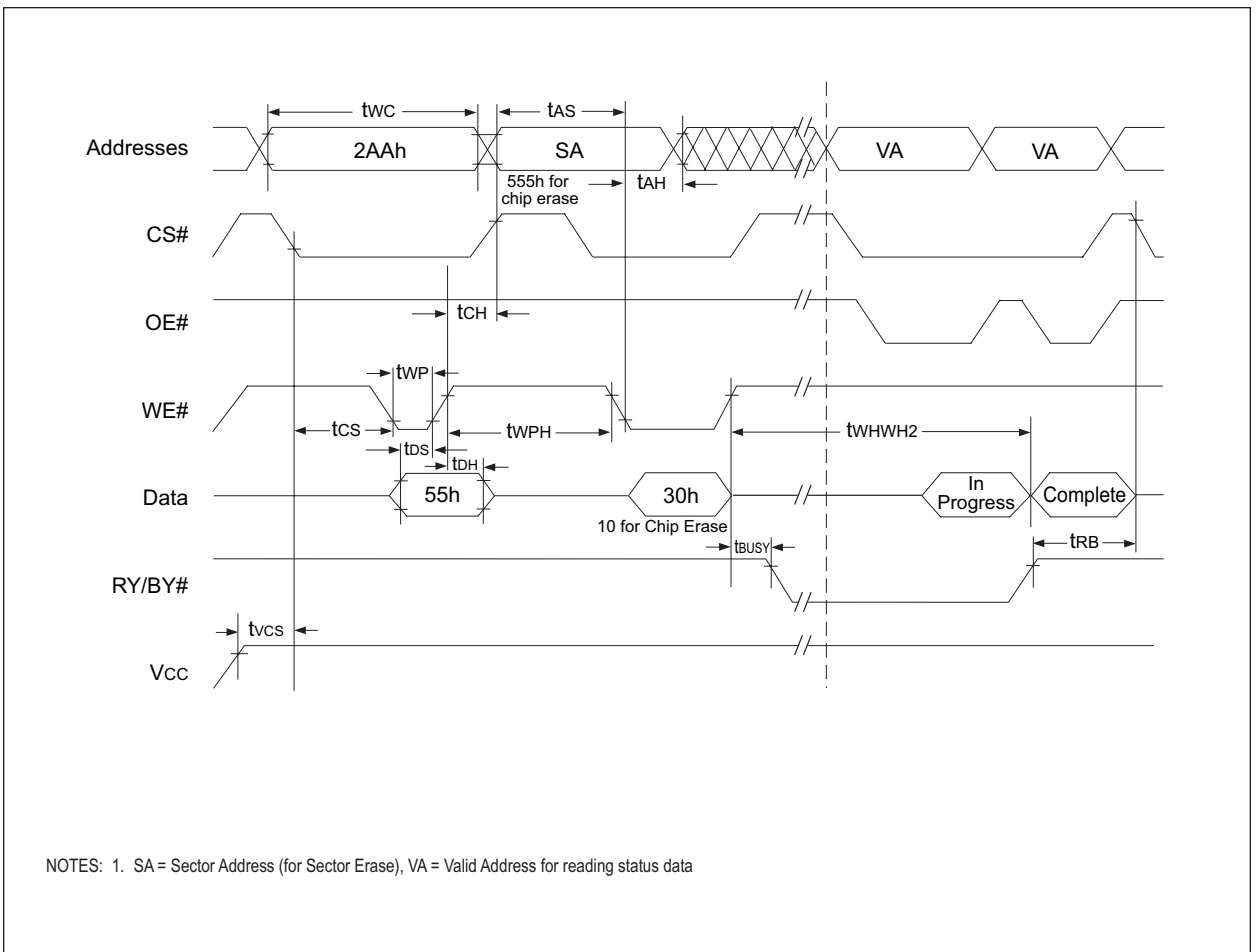


FIGURE 8: CHIP/SECTOR ERASE OPERATION TIMINGS



NOTES: 1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data



FIGURE 9: BACK TO BACK READ/WRITE CYCLE TIMINGS

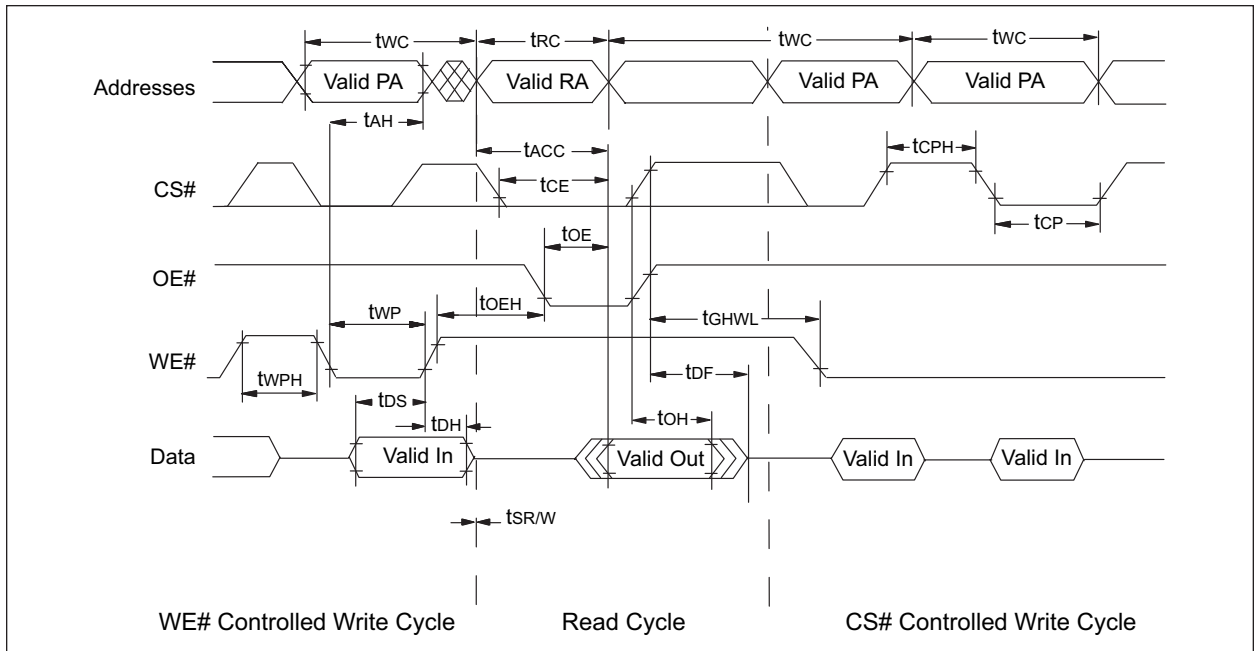
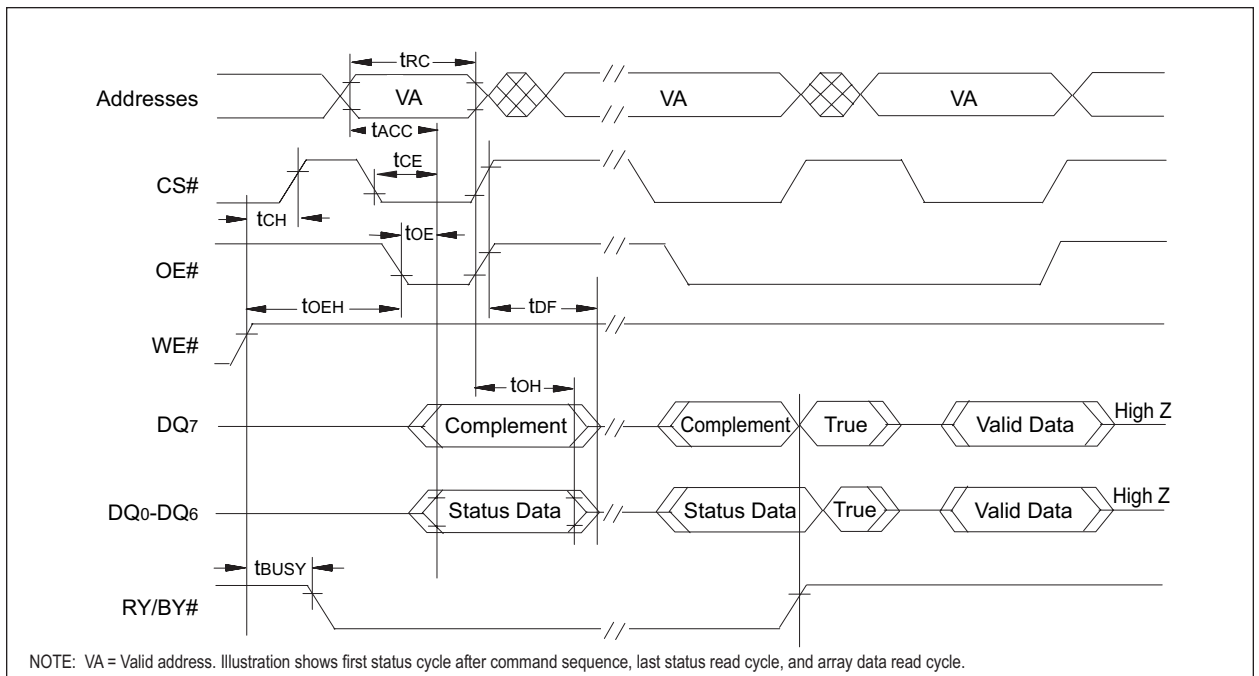


FIGURE 10: DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.



The diagram illustrates the timing relationships for a memory read operation. The signals shown are:

- Addresses:** The data bus for the memory read.
- CS# (Chip Select):** Active-low signal that enables the memory.
- WE# (Write Enable):** Active-low signal that is high during read operations.
- OE# (Output Enable):** Active-low signal that enables the data output.
- DQ6/DQ2:** The data bus showing valid data and status.
- RY/BY# (Read/Byte Enable):** Active-low signal that is high during read operations.

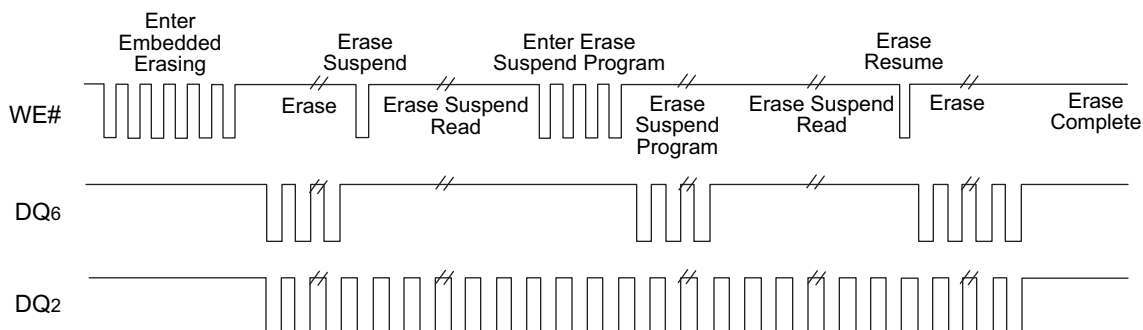
Key timing parameters and events are labeled:

- tAHT:** Address Hold Time, the time the address must remain valid after CS# is asserted.
- tAS:** Address Setup Time, the time the address must be valid before CS# is asserted.
- tSO:** CS# Setup Time, the time CS# must be high before OE# is asserted.
- tCEPH:** CS# Hold Time, the time CS# must remain high after OE# is deasserted.
- tOE:** OE# Setup Time, the time OE# must be high before the data bus becomes valid.
- tOEPH:** OE# Hold Time, the time OE# must remain high after the data bus becomes invalid.
- tDH:** Data Hold Time, the time the data bus must remain valid after OE# is deasserted.

The sequence of events shown is:

- First Read:** CS# is asserted, OE# is asserted, and the data bus becomes valid. The data is valid for a duration of tDH.
- Second Read:** CS# is deasserted, OE# is deasserted, and the data bus becomes invalid. The data is valid for a duration of tOE.
- Stops Toggling:** The data bus becomes invalid and stops toggling. The data is valid for a duration of tOE.

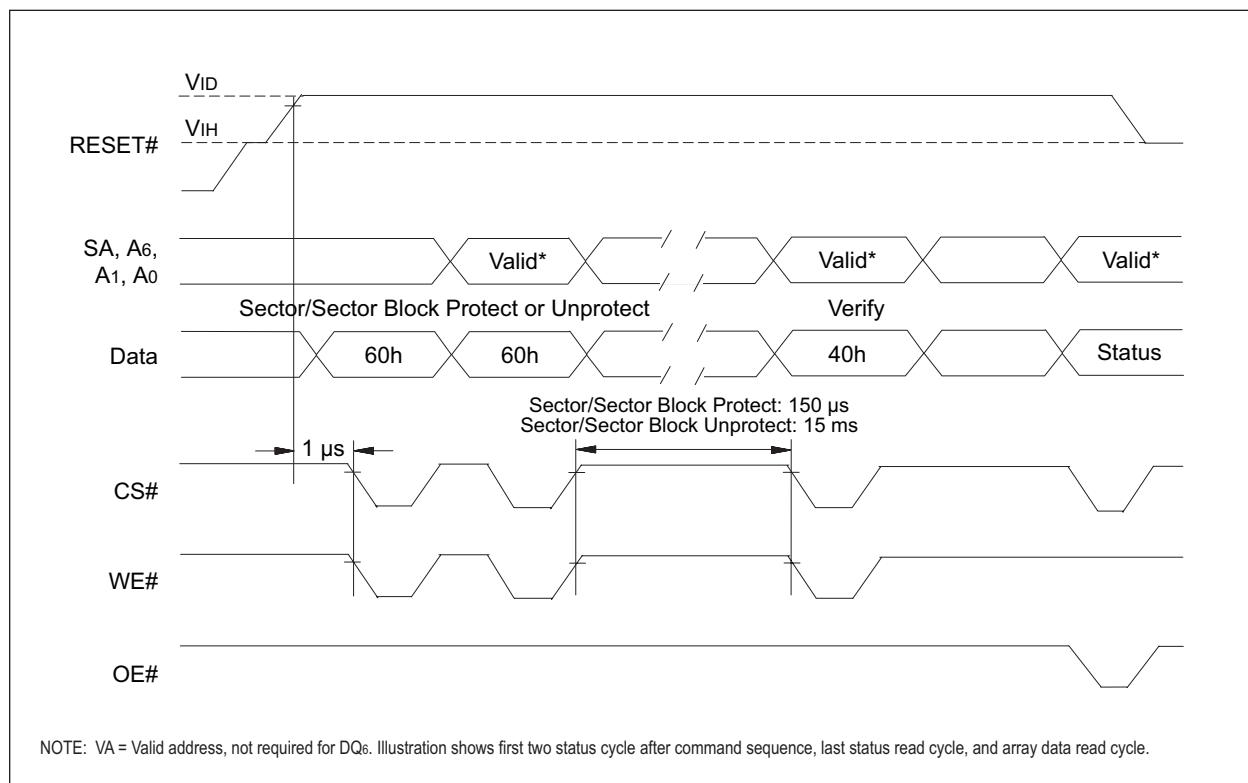
FIGURE 12: DQ2 Vs. DQ6



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FIGURE 13: SECTOR/SECTOR BLOCK PROTECT AND UNPROTECT TIMING DIAGRAM



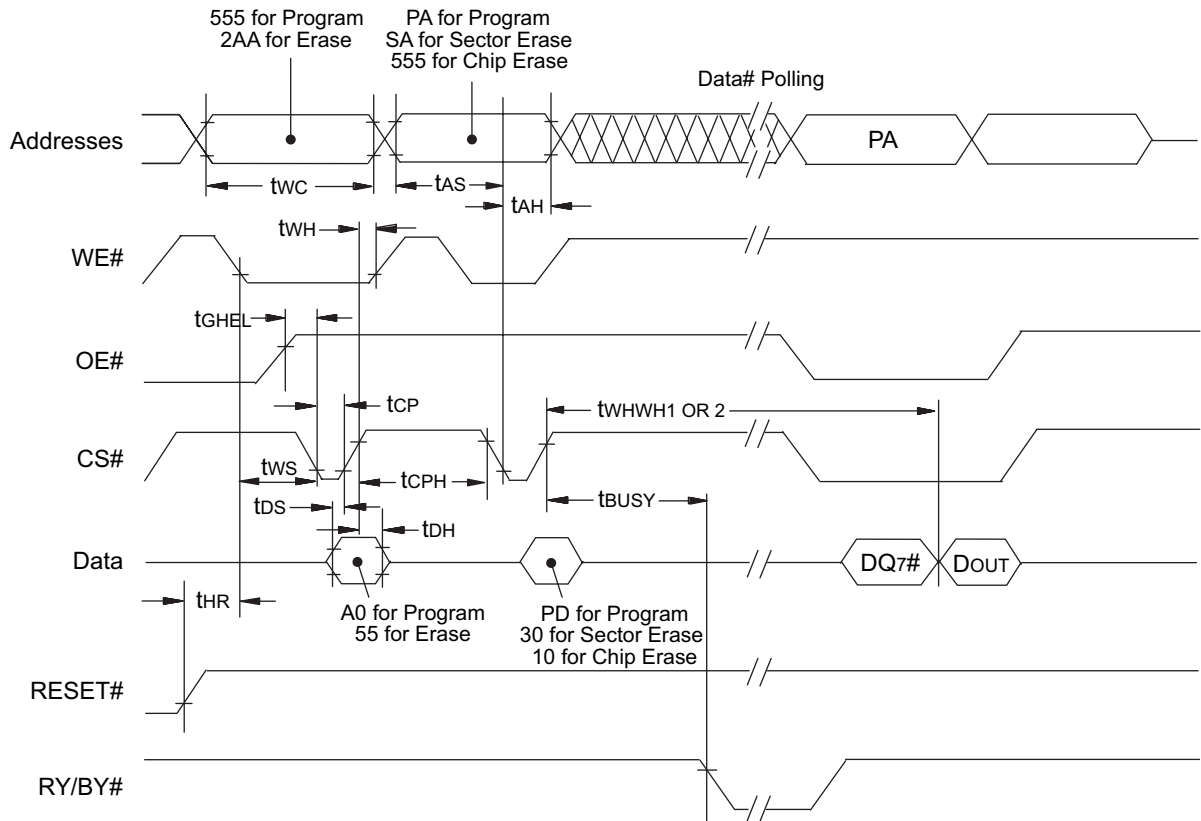
AC CHARACTERISTICS – ALTERNATE CS# CONTROLLED ERASE AND PROGRAM OPERATIONS

Parameter		Description		Speed Options			Unit
JEDEC	Std			90	100	120	
t _{AVAV}	t _{WC}	Write Cycle Time (1)	Min	90	100	120	ns
t _{AVWL}	t _{AS}	Address Setup Time	Min	0	0	0	ns
t _{ELAX}	t _{AH}	Address Hold Time	Min	45	45	50	ns
t _{DVEH}	t _{DS}	Data Setup Time	Min	45	45	50	ns
t _{EDHX}	t _{DH}	Data Hold Time	Min	0	0	0	ns
t _{GHEL}	t _{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	0	0	ns
t _{WLEL}	T _{WS}	WE# Setup Time	Min	0	0	0	ns
t _{EHWH}	t _{WH}	WE# Hold Time	Min	0	0	0	ns
t _{ELEH}	t _{CP}	CS# Pulse Width	Min	35	45	50	ns
t _{EHEL}	t _{CPH}	CS# Pulse Width High	Min	30	30	30	ns
t _{WHWH1}	t _{WHWH1}	Programming Operation	Typ	7	7	7	µs
t _{WHWH1}	t _{WHWH1}	Accelerated Programming Operation	Typ	4	4	4	µs
t _{WHWH2}	t _{WHWH2}	Sector Erase Operation	Typ	0.4	0.4	0.4	sec

NOTE: 1. Not tested.



FIGURE 14: ALTERNATE CS# CONTROLLED WRITE (ERASE/PROGRAM) OPERATION TIMINGS



NOTES:

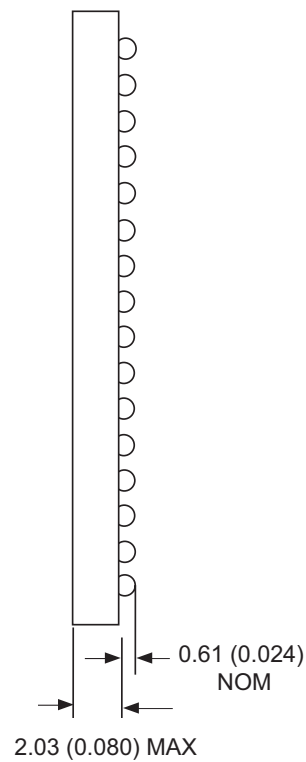
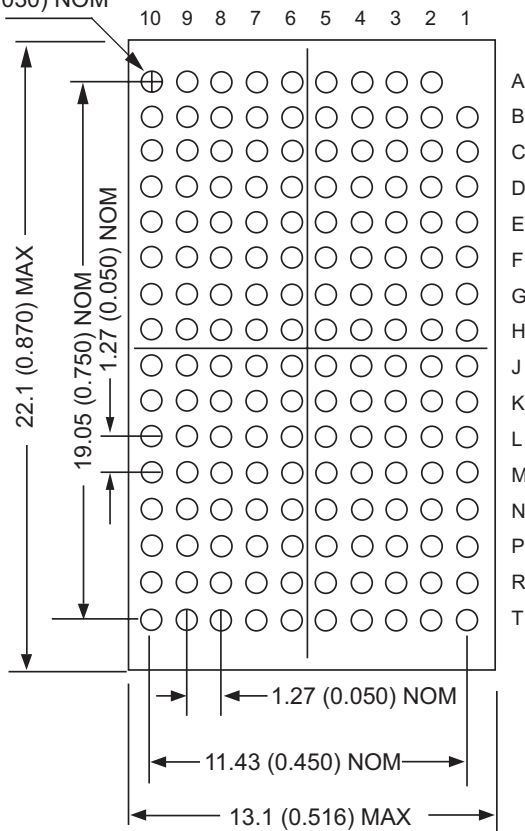
1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. DQ7 is the complement of the data written to the device. DOUT is the data written to the device.



PACKAGE: 159 PBGA

Bottom View

159 X Ø 0.762 (0.030) NOM



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.



PACKAGE: 159 PBGA

WHITE ELECTRONIC DESIGNS CORP.: _____ **W 7 2M64 V K XXX B X**

Flash: _____

Organization, 2M x 64: _____
User Configurable as 2 x 2M x 32

3.3V Power Supply: _____

Internal Bank Architecture: _____
K = 4 bank architecture per 2Mx16 die

Access Time (ns): _____
90 = 90ns
100 = 100ns
120 = 120ns

Package Type: _____
B = 159 Plastic BGA, 13mm x 22mm

Device Grade: _____
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C



Document Title

2M x 64 Simultaneous Operation Flash Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	April 2005	Final