

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4555B

MSI

Dual 1-of-4 decoder/demultiplexer

Product specification
File under Integrated Circuits, IC04

January 1995

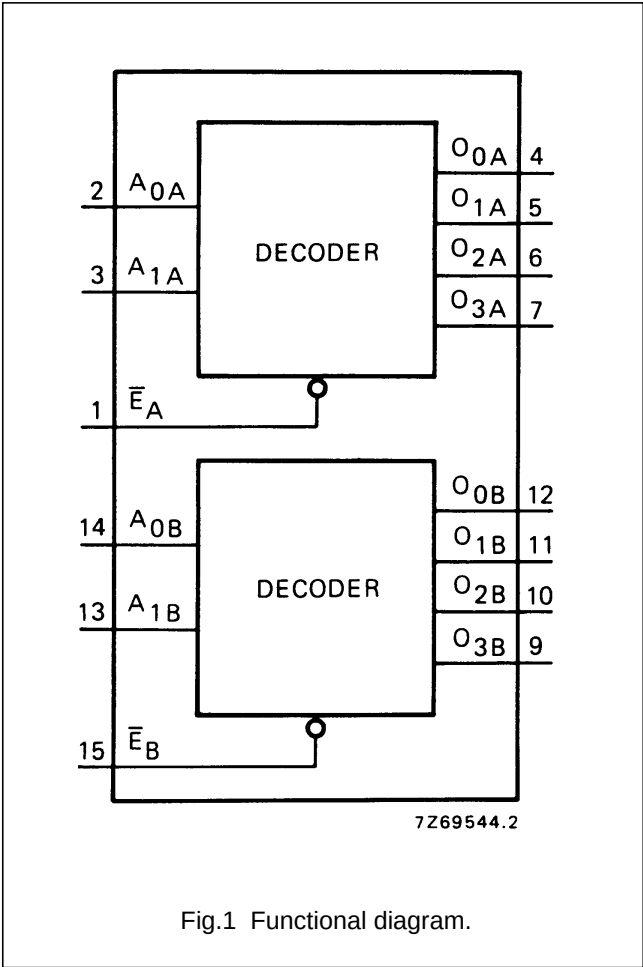
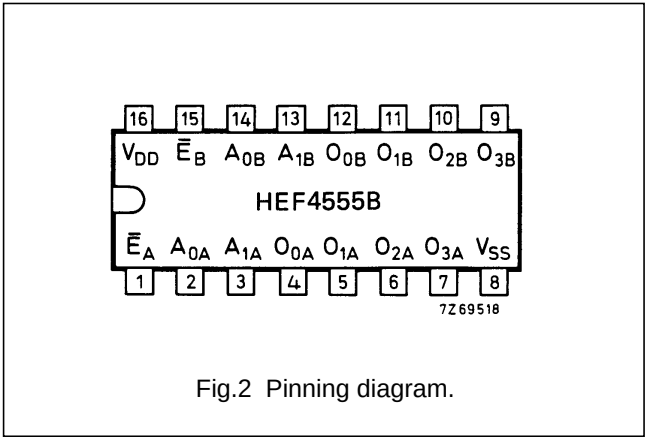
Dual 1-of-4 decoder/demultiplexer

HEF4555B

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DESCRIPTION

The HEF4555B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active HIGH (O_0 to O_3). When used as a decoder, $\overline{E}$ when HIGH, forces O_0 to O_3 LOW. When used as a demultiplexer, the appropriate output is selected by the information on A_0 and A_1 with $\overline{E}$ as data input. All unselected outputs are LOW.



- HEF4555BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4555BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4555BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- $\overline{E}$ enable inputs (active LOW)
- A_0 and A_1 address inputs
- O_0 to O_3 outputs (active HIGH)

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Dual 1-of-4 decoder/demultiplexer

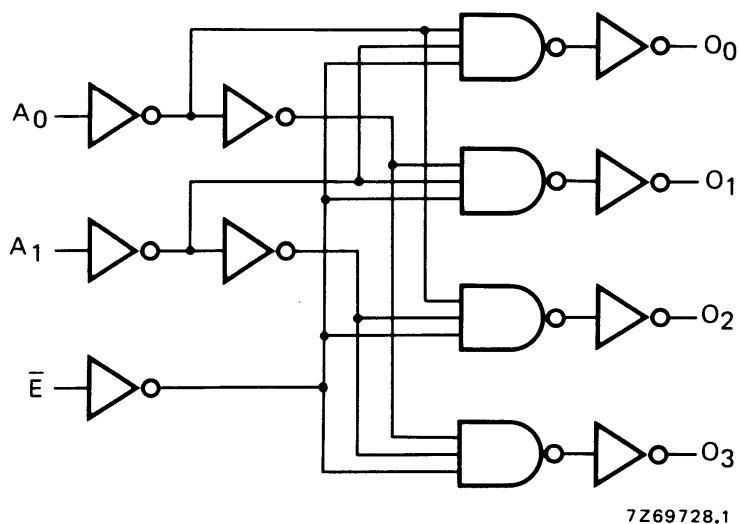
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Fig.3 Logic diagram (one decoder/multiplexer).

TRUTH TABLE

INPUTS			OUTPUTS			
$\bar{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $A_n \rightarrow O_n$ HIGH to LOW LOW to HIGH $\bar{E}_n \rightarrow O_n$ HIGH to LOW LOW to HIGH	5	t_{PHL}		115	230 ns	88 ns + (0,55 ns/pF) C_L
	10			45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PLH}		140	280 ns	113 ns + (0,55 ns/pF) C_L
	10			55	105 ns	44 ns + (0,23 ns/pF) C_L
	15			40	75 ns	32 ns + (0,16 ns/pF) C_L
	5	t_{PHL}		125	250 ns	98 ns + (0,55 ns/pF) C_L
	10			50	95 ns	39 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PLH}		150	295 ns	123 ns + (0,55 ns/pF) C_L
	10			55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	75 ns	32 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW LOW to HIGH	5	t_{THL}		60	120 ns	10 ns + ((1,0 ns/pF) C_L
	10			30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5	t_{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C_L
	10			30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$4500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$18\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$45\,700 f_i + \sum (f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4555B are:

- Code conversion.
- Address decoding.
- Demultiplexing: when using the enable input as data input.