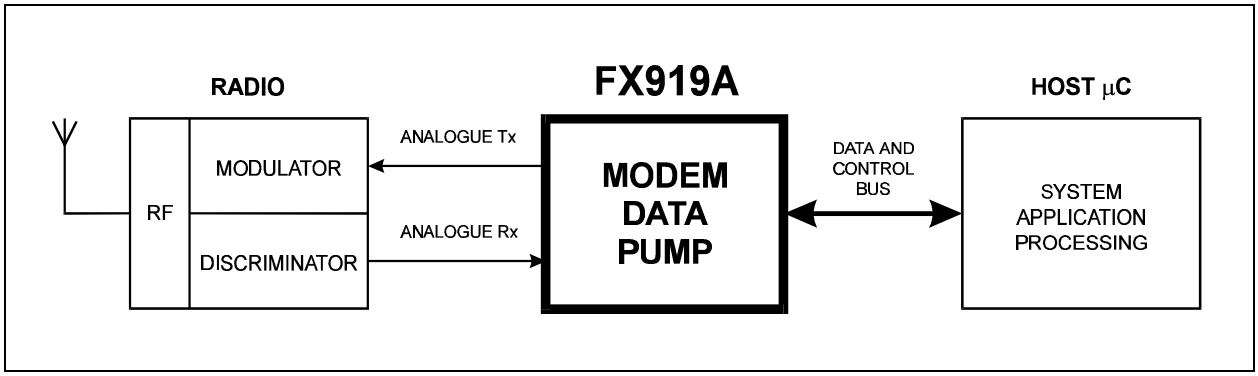
CML Semiconductor Products

4-Level FSK Modem Data Pump FX919A

D/919A/4 June 1996
Advance Information

1.0 Features

- **4-Level FSK Modulation**
- **Half Duplex, 4800 to 19.2k bits/sec**
- **Full Packet Data Framing**
- **Flexible Operating Modes**
- **Host Bus Interface**
- **Low Power 3.3V to 5V Operation**
- **24-Pin Small Form Package Option**



1.1 Brief Description

The FX919A is a CMOS integrated circuit that contains all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance 4-level FSK Wireless Packet Data Modem. It interfaces with the modem host processor and the radio modulation/demodulation circuits to deliver reliable two-way transfer of the application data over the wireless link.

The FX919A assembles application data received from the processor, adds forward error correction (FEC) and error detection (CRC) information and interleaves the result for burst-error protection. After adding symbol and frame sync codewords, it converts the packet into filtered 4-level analogue signals for modulating the radio transmitter.

In receive mode, the FX919A performs the reverse function using the analogue signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the processor. Any residual uncorrected errors in the data will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The FX919A uses data block sizes and FEC/CRC suitable for applications which require the high-speed transfer of data over narrow-band wireless links. The device is programmable to operate at most standard bit-rates from a wide choice of Xtal/clock frequencies.

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Note: As this product is still in development, it is likely that a number of changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

1.2 Block Diagram

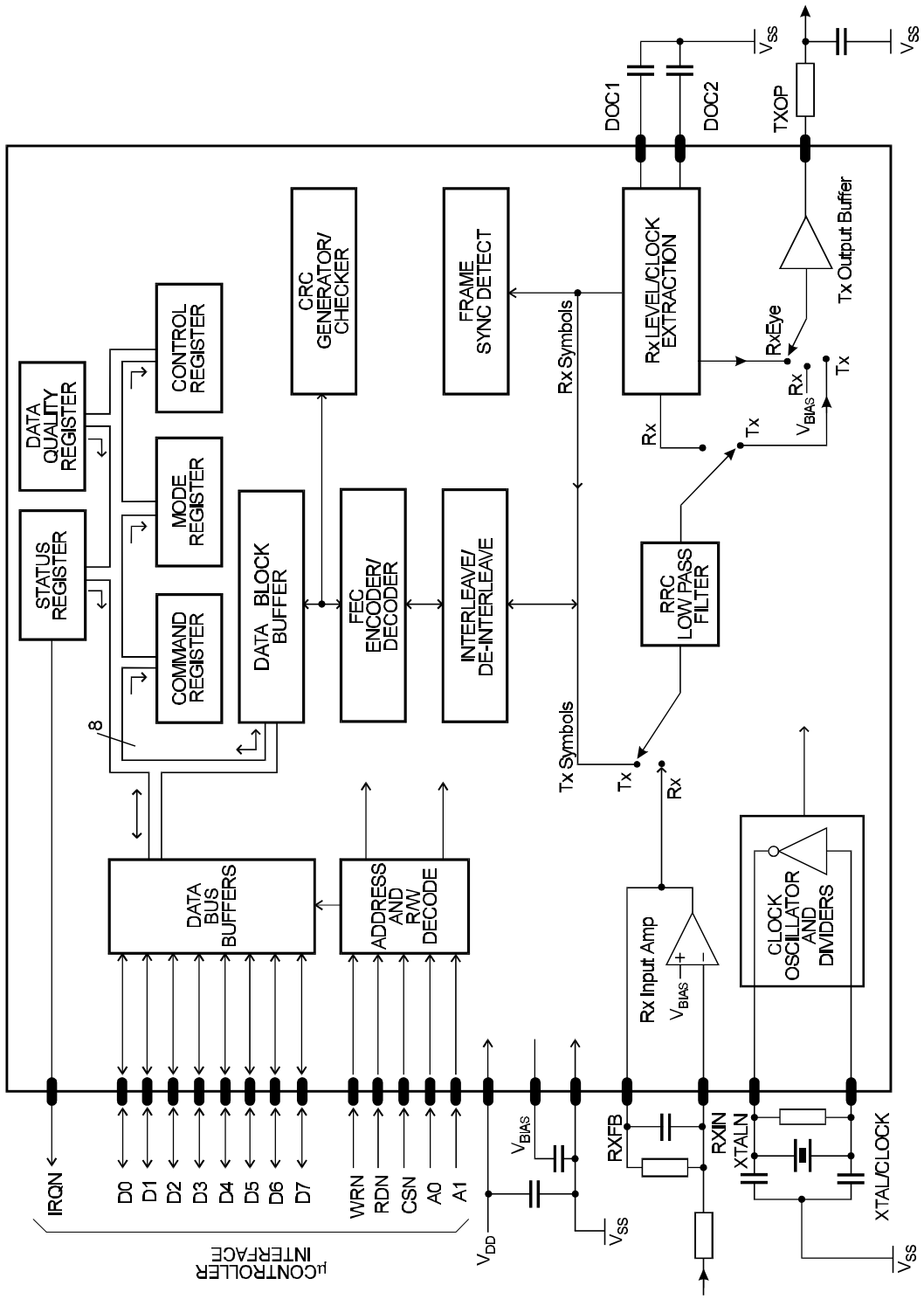


Figure 1 Block Diagram

1.3 Signal List

Package P4/D2/D5	Signal		Description
Pin No.	**Name**	**Type**	
1	IRQN	O/P	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. This output has a low impedance pull down to V_{SS} when active and is high impedance when inactive.
2	D7	BI	)
3	D6	BI	)
4	D5	BI	)
5	D4	BI	) 8-bit bidirectional 3-state µC interface data
6	D3	BI	) lines.
7	D2	BI	)
8	D1	BI	)
9	D0	BI	)
10	RDN	I/P	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	WRN	I/P	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	Power	The negative supply rail (ground).
13	CSN	I/P	Chip Select. An active low logic level input to the modem, used to enable a data read or write operation.
14	A0	I/P	) Two logic level modem register select
15	A1	I/P	) inputs.
16	XTALN	O/P	The output of the on-chip oscillator.
17	XTAL/CLOCK	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
18	DOC 2	O/P	) Connections to the Rx level measurement
19	DOC 1	O/P	) circuitry. A capacitor should be connected
			) from each pin to $V_{SS.}$

Package P4/D2/D5	Signal		Description
Pin No.	**Name**	**Type**	
20	TXOP	O/P	The Tx signal output from the modem.
21	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½ V_{DD}. This pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	I/P	The input to the Rx input amplifier.
23	RXFB	O/P	The output of the Rx input amplifier and the input to the Rx RRC filter.
24	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.

Notes: I/P = Input
O/P = Output
BI = Bidirectional

Internal protection diodes are connected from each signal pin to V_{DD} and V_{SS}.

1.4 External Components

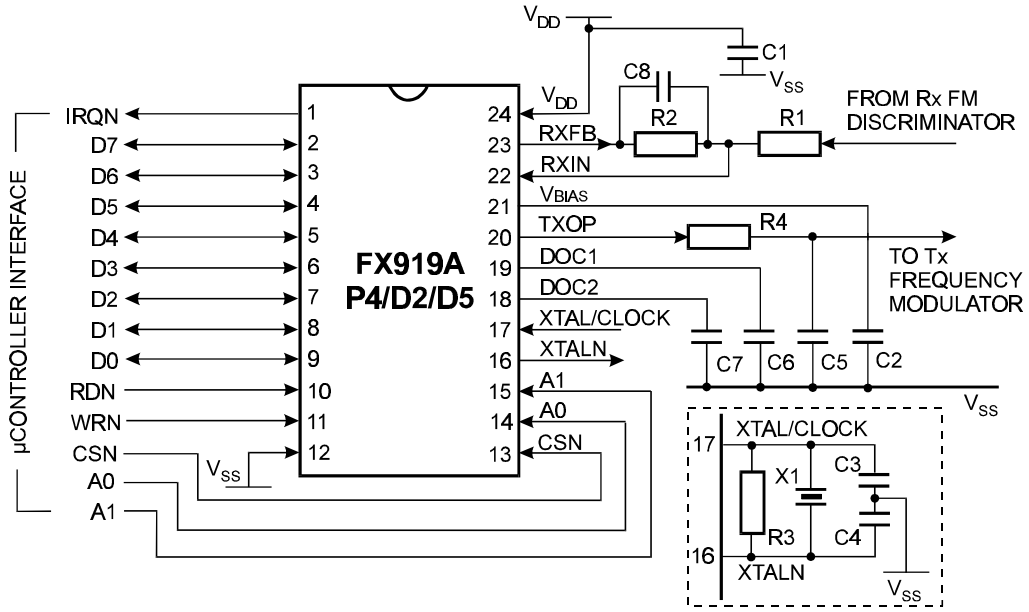


Figure 2 Recommended External Components

R1	See Section 1.5.1	C1	0.1 µF ± 20%	C5	± 5%, see Note 3
R2	100k ohm ± 5%	C2	0.1 µF ± 20%	C6	± 20%, see Note 2
R3	1M ohm ± 20%	C3	± 20%, see Note 1	C7	± 20%, see Note 2
R4	100k ohm ± 5%	C4	± 20%, see Note 1	C8	± 5%, see Note 3
X1	See Section 1.5.5.3				

Note 1: The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitances) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable. The 'Phase-Locked Loop Modes' part of section 1.5.5.3 discusses crystal frequency tolerances.

Note 2: C6 and C7 values (in nano Farads) should be equal to 50000 ÷ symbol rate, e.g.

Symbol Rate	C6/C7 (nF)
2400 symbols/second	22.0
4800 symbols/second	10.0
9600 symbols/second	4.7

Note 3: C5 and C8 values (in pico Farads) should be equal to 750000 ÷ symbol rate, e.g.

Symbol Rate	C5/C8 (pF)
2400 symbols/second	330
4800 symbols/second	150
9600 symbols/second	82

1.5 General Description

1.5.1 Description of Blocks

Data Bus Buffers
Eight bidirectional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

Address and R/W Decode
This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs (WRN and RDN), the Chip Select input (CSN) and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

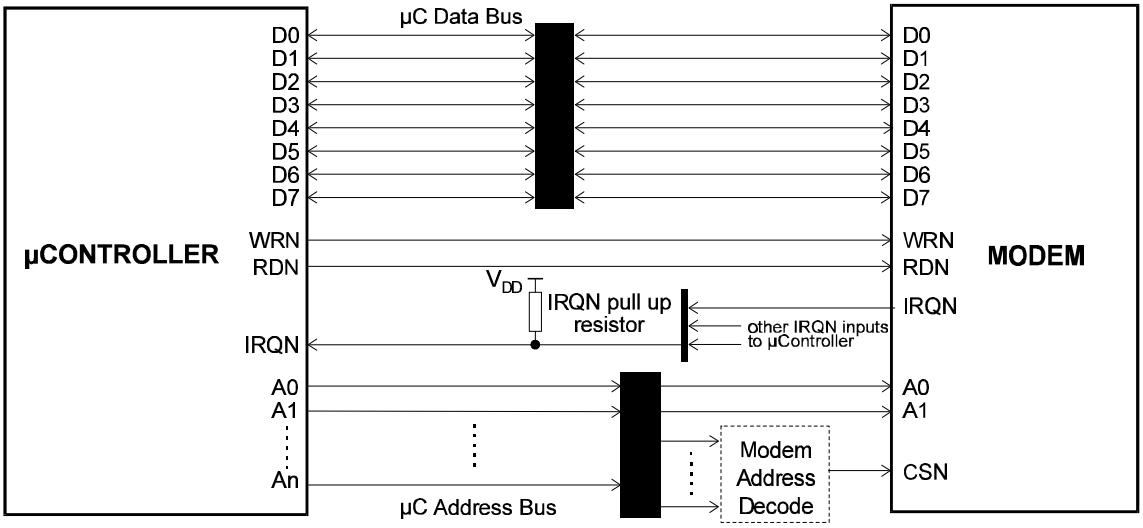


Figure 3 Typical Modem µC Connections

Status and Data Quality Registers
Eight-bit registers which the µC can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers
The values written by the µC to these 8-bit registers control the operation of the modem.

Data Buffer
A 12-byte buffer used to hold receive or transmit data to or from the µC.

CRC Generator/Checker
A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which may be included in transmitted data blocks so that the receive modem can detect transmission errors.

FEC Generator/Checker
In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, then converts the resulting binary data to 4-level symbols. In receive mode, it translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

Interleave/De-interleave Buffer
This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

Frame Sync Detect
This circuit, which is only active in receive mode, is used to look for the 24-symbol Frame Synchronisation pattern which is transmitted to mark the start of every frame.

Rx I/P Amp
This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give 0.2 x V_{DD} pk-pk at the RXFB pin for a received '...+3 +3 -3 -3 ...' sequence.

A capacitor may be fitted in series with R1 if ac coupling of the received signal is desired (see Section 1.6.4), otherwise the dc level of the received signal should be adjusted so that the signal at the modem's RXFB pin is centred around V_{BIAS} (½ V_{DD}).

RRC Low Pass Filter
This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response defined by:

H(f)	= 1	for	0	<= f < (1-b)/(2T)
	= square root of {0.5 [1 - sin(π T (f - 0.5/T)/b)]}	for	(1-b)/(2T)	<= f <= (1+b)/(2T)
	= 0	for	(1+b)/(2T)	< f

where b = 0.2, T = 1/symbol rate

This frequency response is illustrated in Figure 5.

In transmit mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

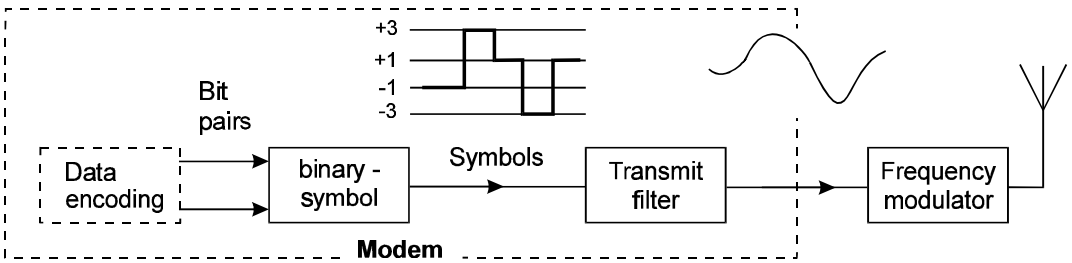


Figure 4 Translation of Binary Data to Filtered 4-Level Symbols in Tx Mode

In receive mode, the filter is used to reject HF noise and to equalise the received signal to a form suitable for extracting the 4-level symbols.

Tx Output Buffer

This is a unity gain amplifier used in transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS} unless the RXEYE bit of the Control Register is '1', when it is connected to the received signal. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 8 symbol times while the RRC filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOP pin and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any dc level-shifting and gain adjustment circuitry. The value used for C5 should take into account stray circuit capacitances, and its ground connection should be positioned to give maximum attenuation of high frequency noise into the modulator.

The signal at the TXOP pin is centred around V_{BIAS} and is approx 0.2 x V_{DD} pk-pk for a continuous '+3 +3 -3 -3 ...' pattern.

A capacitor may be fitted in series with the input to the frequency modulator if ac coupling is desired, see Section 1.6.4.

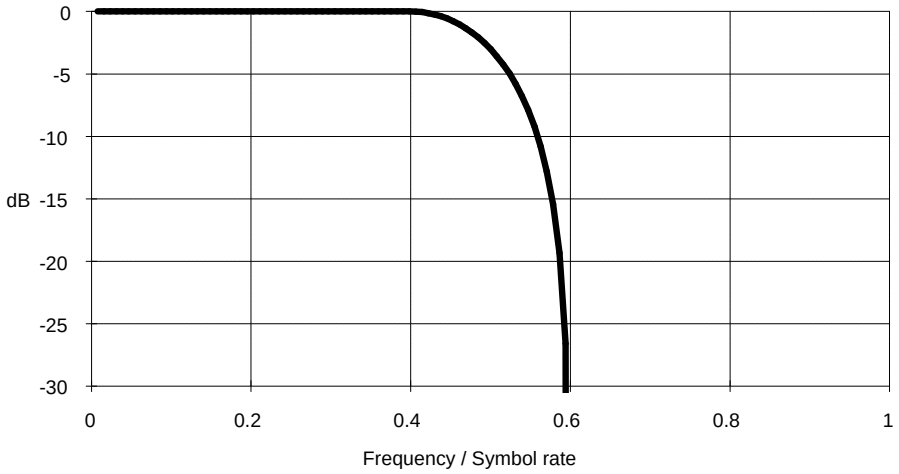


Figure 5 RRC Filter Frequency Response (including the external RC filter R4/C5)

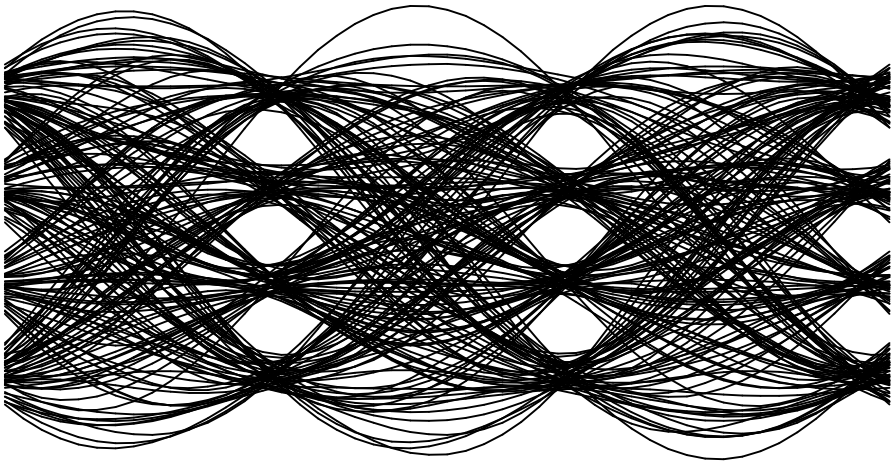


Figure 6 Transmitted Signal Eye Diagram

Rx Level/Clock Extraction
These circuits, which operate only in receive mode, derive a symbol rate clock from the received signal and measure the received signal amplitude and dc offset. This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

The capacitors C6 and C7 are driven from a very high impedance source so any measurement of the voltages on the DOC pins must be made via high input impedance (MOS input) voltage followers to avoid disturbance of the level measurement circuits.

Further details of the level and clock extraction functions are given in section 1.6.3.

Clock Oscillator and Dividers
These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip xtal oscillator is to be used, then the external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the XTALN pin should be left unconnected, and X1, C3, C4 and R3 not fitted.

1.5.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message formats handled by the modem are given in Section 1.5.3 and Figures 7 and 7a.

To reduce the processing load on the associated µC, the FX919A modem has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronising onto the Frame Preamble. In normal operation the modem will only require servicing by the µC once per received or transmitted block.

Thus, to transmit a block, the controlling µC has only to load the - unformatted - 'raw' binary data into the modem's Data Block Buffer then instruct the modem to format and transmit that data. The modem will then

calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding) and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary - using the FEC coding to correct as many errors as possible - and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also transmit and receive un-formatted data using the T4S, T24S and R4S tasks described in sections 1.5.3 and 1.5.5.2. These are normally used for the transmission of Symbol and Frame Synchronisation sequences. They may also be used for the transmission and reception of special test patterns or even for special data formats - although in this case care should be taken to ensure that the transmitted signal contains enough level and timing information for the receiving modem's level and clock extraction circuits to function correctly (see section 1.6.3).

1.5.3 Binary to Symbol Translation

Although the over-air signal, and hence the signals at the modem TXOP and RXIN pins, consists of 4-level symbols, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

Direct: the simplest form, which converts between 2 binary bits and a single symbol.

symbol	ms bit	ls bit
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This is expanded so that an 8-bit byte translates to four symbols for the T4S, T24S and R4S tasks described in Section 1.5.5.2.

	msb							lsb
Bits:	7	6	5	4	3	2	1	0
Symbols:	a		b		c		d	
	sent first						sent last	

With FEC: This is more complicated, but essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, RHB and RILB described in Section 1.5.5.2.

1.5.4 Frame Structure

Figure 7 below shows how an over-air message frame may be constructed from Frame and Symbol Sync patterns, followed by one or more 'Header', 'Intermediate' or 'Last' blocks.

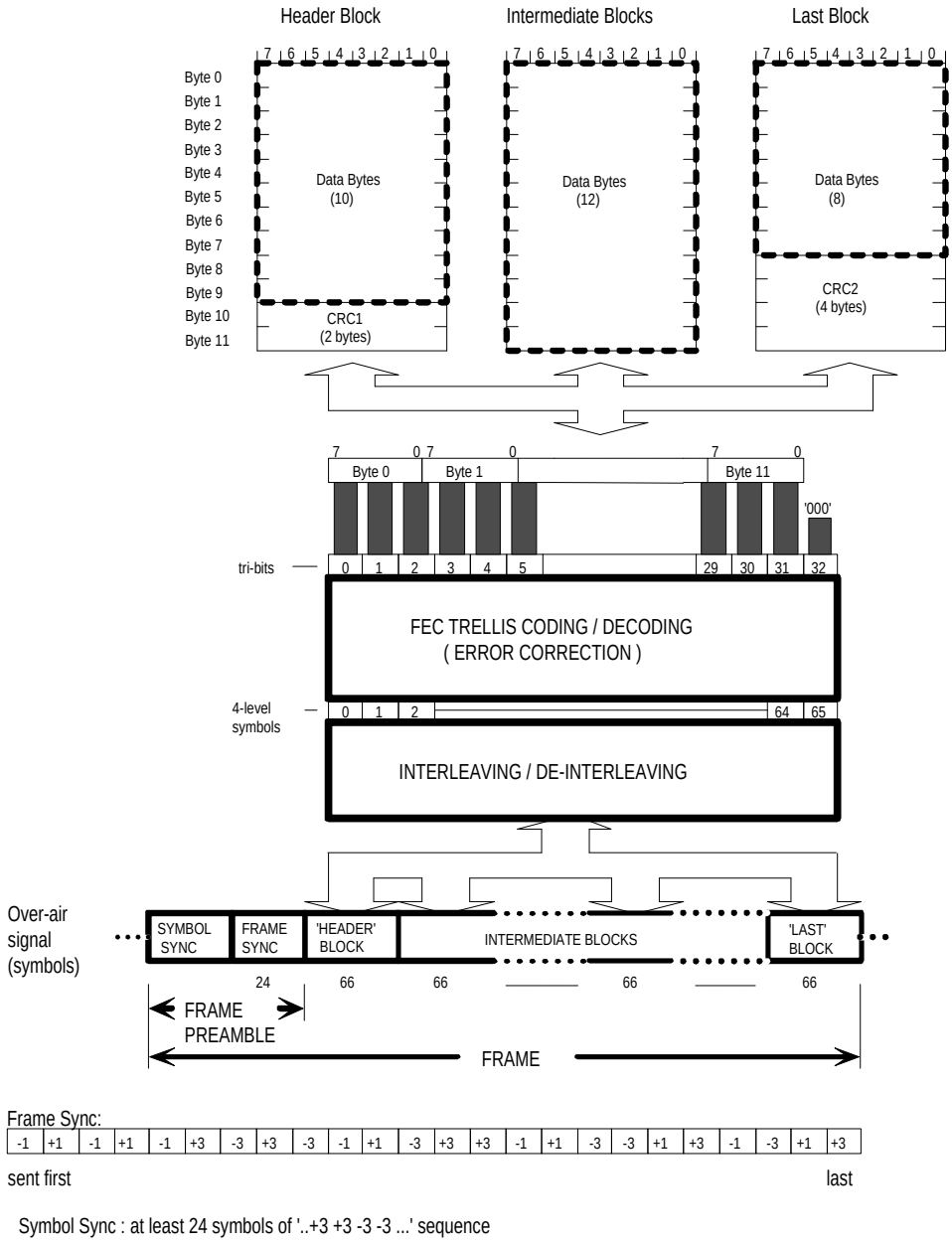


Figure 7 Over Air Signal Format

The 'Header' block is self-contained in that it includes its own checksum (CRC1), and would normally carry information such as the addresses of the called and calling parties, the number of following blocks in the frame (if any) and miscellaneous control information. The 'Intermediate' block(s) contain only data, the checksum for all of the data in the 'Intermediate' and 'Last' blocks (CRC2) being contained at the end of the 'Last' block.

This arrangement, whilst efficient in terms of data capacity, may not be optimum for poor signal-to-noise conditions, since a reception error in any one of the 'Intermediate' or 'Last' blocks would invalidate the whole frame. In these conditions, increased throughput may be obtained by using the 'Header' block format for all blocks of the frame, so that blocks which are received correctly can be identified as such, and need not be re-transmitted. This, and some other possible frame structures, are shown in Figure 7a below.

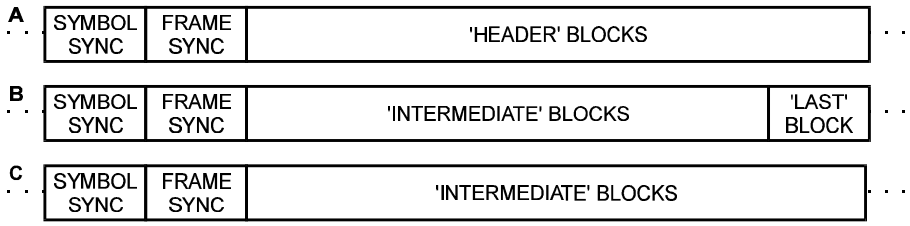


Figure 7a Some Alternative Frame Structures

The FX919A performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC being that enclosed by the thick dashed rectangles near the top of Figure 7.

1.5.5 The Programmer's View

The modem appears to the programmer as 4 write only 8-bit registers shadowed by 3 read only registers, individual registers being selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

Note that there is a minimum allowable time between accesses of the modem's registers, see Section 1.7.1 for details.

1.5.5.1 Data Block Buffer

This is a 12-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality or control information) between the modem and the host µC.

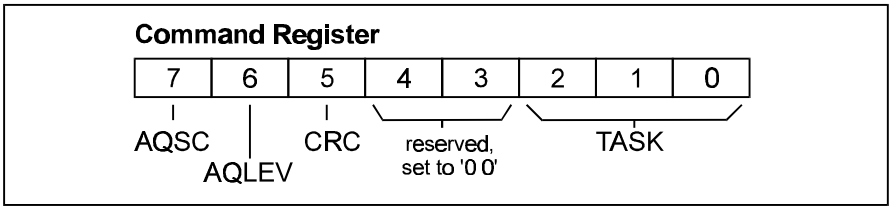
It appears to the µC as a single 8-bit register; the modem ensuring that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode. Note that in receive mode the modem will function correctly even if the received data is not read from the Data Buffer by the µC.

1.5.5.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK, AQLEV and AQSC bits.



When it has no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx RRC filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract symbols from the received signal, supplying them to the de-interleave buffer, but will otherwise ignore the received data.

Command Register B7: AQSC - Acquire Symbol Clock
This bit has no effect in transmit mode.

In receive mode, whenever a byte with the AQSC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve symbol timing synchronisation with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronisation is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQSC bit set to '1'.

The use of the symbol clock acquisition sequence is described in section 1.6.3.

Command Register B6: AQLEV - Acquire Receive Signal Levels
This bit has no effect in transmit mode.

In receive mode, whenever a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, hence improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to '1'.

The use of the level measurement acquisition sequence (AQLEV) is described in section 1.6.3.

Command Register B5: CRC
This bit allows the user to select between two different forms of the CRC1 and CRC2 checksums. When this bit is set to '0' the CRC generators are initialised to 'all ones' as for CCITT X25 CRC calculations. When this bit is set to '1' the CRC generators are initialised to 'all zeros'. Setting this bit to '0' gives compatibility with the older 'non-A' version of the FX919, other systems may set this bit as required.

Command Register B4, B3
These bits should always be set to '0'.

Command Register B2, B1, B0: TASK
Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The µC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

> Set the BFREE (Buffer Free) bit of the Status Register to '0'.
>
> Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.
>
> Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip IRQN output to go low if the IRQNEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

This lets the µC write a task and the associated data to the modem while the modem is still transmitting the data from the previous task.

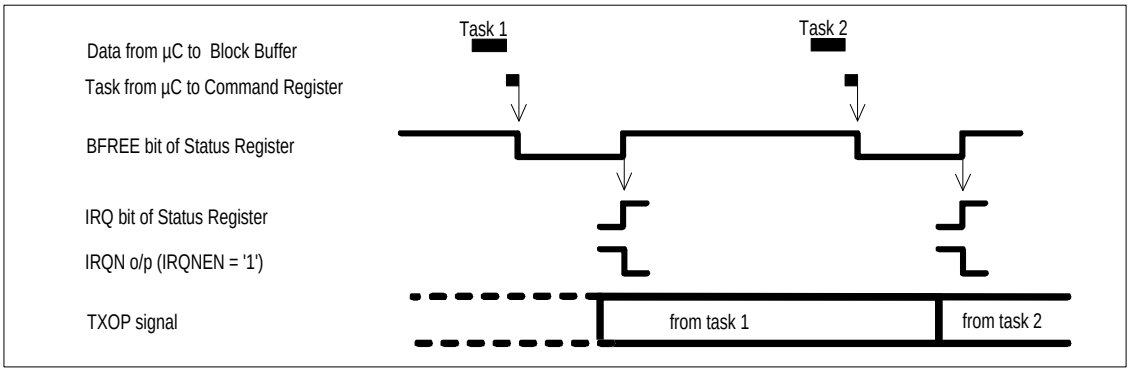


Figure 8 Transmit Task Overlapping

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received symbols are in the De-interleave Buffer.

Decode them as needed, and transfer the resulting binary data to the Data Block Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the IRQN output to go low if the IRQNEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way the µC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

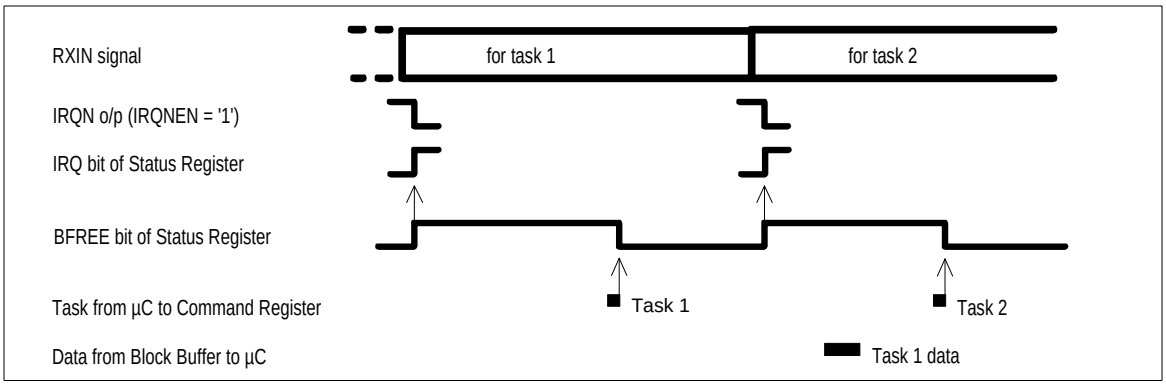


Figure 9 Receive Task Overlapping

Detailed timings for the various tasks are given in Figures 10 and 11.

FX919A Modem Tasks:

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFSH	Search for FS + Header	T24S	Transmit 24 symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 symbols	T4S	Transmit 4 symbols
1	1	0	NULL		NULL	
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

NULL: No effect
This 'task' is provided so that a AQSC or AQLEV command can be initiated without loading a new task.

SFSH: Search for Frame Sync plus Header Block
This task causes the modem to search the received signal for a valid 24-symbol Frame Sync sequence followed by Header Block which has a correct CRC1 checksum.

The task continues until a valid Frame Sync plus Header Block has been found.

The search consists of two stages:

> First of all the modem will attempt to match the incoming symbols against the 24-symbol Frame Synchronisation pattern to within the tolerance defined by the FSTOL bits of the Control Register.
>
> Once a match has been found, the modem will read in the next 66 symbols as if they were a 'Header' block, decoding the symbols and checking the CRC1 checksum. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.
>
> If the received CRC1 is correct, the 10 decoded data bytes will be placed into the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1' and the CRCERR bit cleared to '0'.

On detecting that the BFREE bit of the Status Register has gone to '1', the µC should read the 10 bytes from the Data Block Buffer then write the next task to the modem's Command Register.

RHB: Read Header Block
This task causes the modem to read the next 66 symbols as a 'Header' Block, decoding them, placing the resulting 10 data bytes and the 2 received CRC1 bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to '1' or '0' depending on the validity of the received CRC1 checksum bytes.

RILB: Read 'Intermediate' or 'Last' Block
This task causes the modem to read the next 66 symbols as an 'Intermediate' or 'Last' block (the µC should be able to tell from the 'Header' block how many blocks are in the frame, and hence when to expect the 'Last' block).

In each case, it will decode the 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received then the µC should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum.

SFS: Search for Frame Sync
This task causes the modem to search the received signal for a 24-symbol sequence which matches the Frame Synchronisation pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register to '1' to indicate to the µC that it should write the next task to the Command Register.

R4S: Read 4 Symbols
This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by SFS task.

T24S: Transmit 24 Symbols
This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The tables below show what data has to be written to the Data Block Buffer to transmit the FX919A Symbol and Frame Sync sequences:

'Symbol Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
+3	+3	-3	-3	Byte 5:	11110101	F5

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

THB: Transmit Header Block
This task takes 10 bytes of data (Address and Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

TIB: Transmit Intermediate Block
This task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

TLB: Transmit Last Block
This task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

T4S: Transmit 4 Symbols
This command is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

RESET: Stop any current action
This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied, to set the modem into a known state.

Note that due to delays in the transmit filter, it will take several symbol times for any change to appear at the TXOP pin.

Task Timings

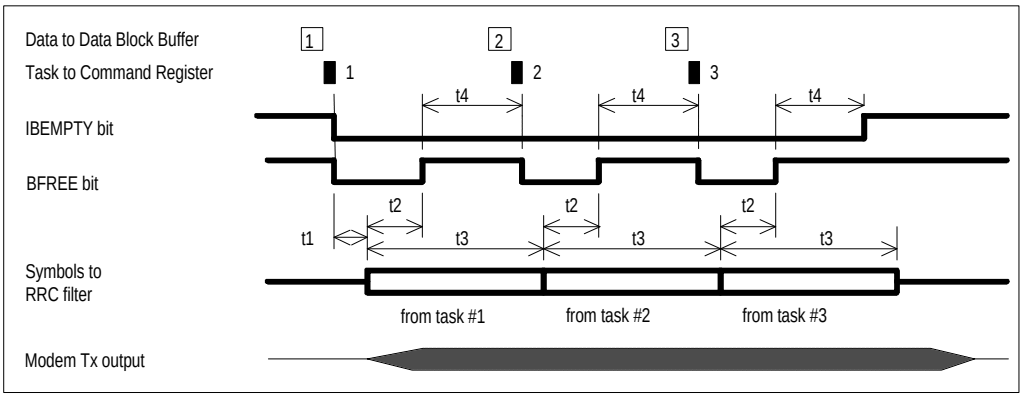


Figure 10 Transmit Task Timing Diagram

		Task	Time (symbol times)
t1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx RRC filter	Any	1 to 2
t2	Time from application of first symbol of the task to the Tx RRC filter until BFREE goes to a logic '1' (high).	T24S	5
		THB/TIB/TLB	16
		T4S	0
t3	Time to transmit all symbols of the task	T24S	24
		THB/TIB/TLB	66
		T4S	4
t4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T24S	18
		THB/TIB/TLB	49
		T4S	3

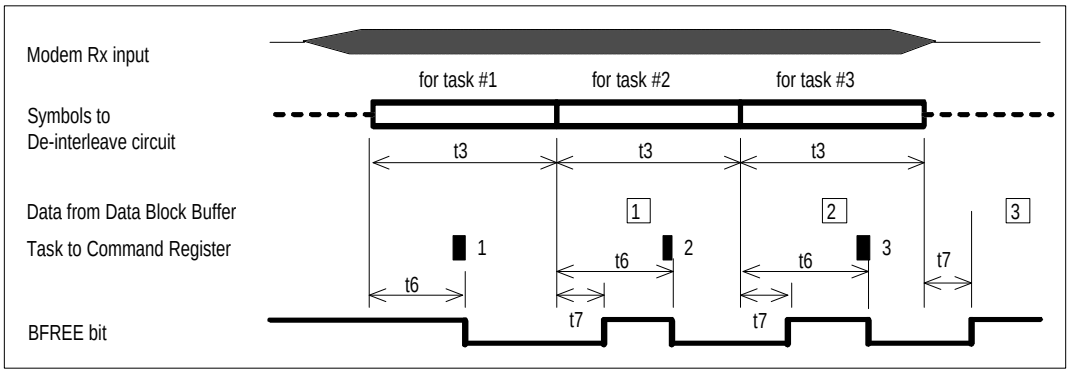


Figure 11 Receive Task Timing Diagram

		Task	Time (symbol times)
t3	Time to receive all symbols of task	SFS	24 (minimum)
		SFSH	90 (minimum)
		RHB/RILB	66
		R4S	4
t6	Maximum time between first symbol of task entering the de-interleave circuit and the task being written to modem.	SFS	21
		SFSH	21
		RHB/RILB	49
		R4S	3
t7	Maximum time from the last bit of the task entering the de-interleave circuit to BFREE going to a logic '1' (high)	Any	1

RRC Filter Delay

The previous task timing figures are based on the signal at the input to the RRC filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 8 symbol times through to the RRC filter in both transmit and receive modes, as illustrated below:

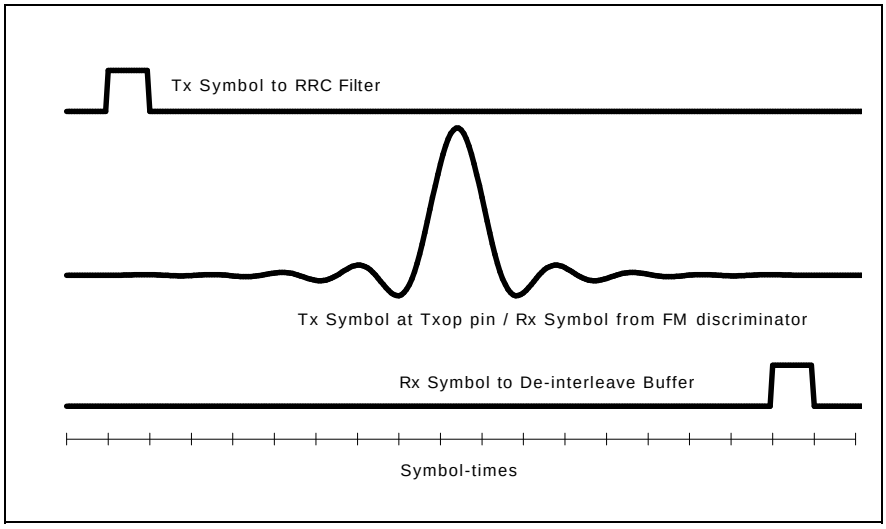
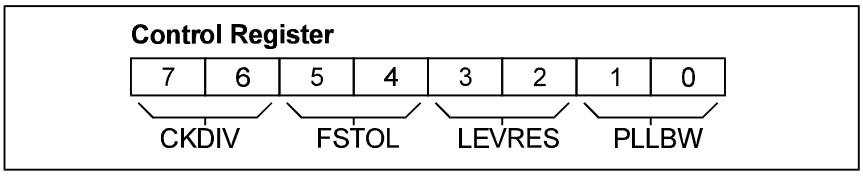


Figure 12 RRC Low Pass Filter Delay

1.5.5.3 Control Register

This 8-bit write-only register controls the modem's symbol rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.



Control Register B7, B6: CKDIV - Clock Division Ratio

These bits control a frequency divider driven from the clock signal present at the XTALN pin, and hence determine the nominal symbol rate. The table below shows how symbol rates of 2400/4800/9600 symbols/sec may be obtained from common Xtal frequencies:

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	**B6**	**Division Ratio: Xtal Frequency/Symbol Rate**	**Symbol Rate (symbols/sec)**		
0	0	512	4800	9600	
0	1	1024	2400	4800	9600
1	0	2048		2400	4800
1	1	4096			2400

Note: Device operation is not guaranteed below 2400 or above 9600 symbols/sec.

Control Register B5, B4: FSTOL - Frame Sync Tolerance
These two bits have no effect in transmit mode. In receive mode, they define the maximum number of mismatches which will be allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches. A setting of '4 mismatches' is recommended for normal use.

Control Register B3, B2: LEVRES - Level Measurement Modes
These two bits have no effect in transmit mode. In receive mode they set the 'normal' operating mode of the received signal amplitude and dc offset measuring circuits (the automatic sequencing of an AQLEV command may temporarily override the 'normal' setting).

B3	B2	Mode
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

In normal use the LEVRES bits should be set to 'Slow Peak Detect', the other modes are intended for special test purposes or are invoked automatically during an AQLEV sequence.

In the 'Slow' and 'Lossy' Peak Detect modes the positive and negative excursions of the received signal (after filtering) are measured by peak rectifiers driving the DOC1 and DOC2 capacitors, to establish the amplitude of the signal and any dc offset wrt V_{BIAS}. The peak rectifiers are disabled in 'Hold' mode.

In 'Clamp' mode the DOC1 and DOC2 pins are connected directly to the output of the circuit that normally drives the peak detectors.

Control Register B1, B0: PLLBW - Phase-Locked Loop Modes
These two bits have no effect in transmit mode. In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequencing of an AQSC command.

B1	B0	PLL Mode
0	0	Hold
0	1	Narrow Bandwidth
1	0	Medium Bandwidth
1	1	Wide Bandwidth

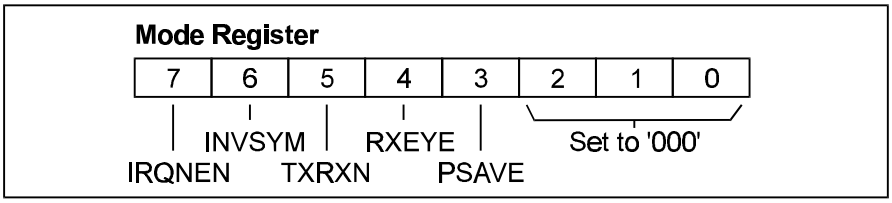
The normal setting for the PLLBW bits should be 'Medium Bandwidth' when the received symbol rate and the frequency of the receiving modem's Xtal are both within ±100ppm of nominal, except at the start of a symbol clock acquisition sequence (AQSC) when 'WIde Bandwidth' should be selected as described in section 1.6.3.

If the received symbol rate and Xtal frequency are both within ±20ppm of nominal then selection of the 'Narrow Bandwidth' setting will give better performance, especially through fades or noise bursts which might otherwise pull the PLL away from its optimum timing, but in this case it is recommended that the PLLBW bits are only set to 'Narrow Bandwidth' after the modem has been running in 'Medium Bandwidth' mode for about 200 symbol times.

The 'Hold' setting disables the feedback loop of the PLL, which continues to run at a rate determined only by the actual Xtal frequency and the setting of the Control Register CKDIV bits.

1.5.5.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



Mode Register B7: IRQNEN - IRQN Output Enable
When this bit is set to '1', the IRQN chip output pin is pulled low (to V_{SS}) whenever the IRQ bit of the Status Register is a '1'.

Mode Register B6: INVSYM - Invert Symbols
This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOP	Signal at RXFB
0	'+3'	Above V_{BIAS}	Below V_{BIAS}
	'-3'	Below V_{BIAS}	Above V_{BIAS}
1	'+3'	Below V_{BIAS}	Above V_{BIAS}
	'-3'	Above V_{BIAS}	Below V_{BIAS}

Mode Register B5: TXRXN - Tx/Rx Mode
Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode. Note that changing between receive and transmit modes will cancel any current task.

Mode Register B4: RXEYE - Show Rx Eye
This bit should normally be set to '0'. Setting it to '1' when the modem is in receive mode configures the modem into a special test mode, in which the input of the Tx o/p buffer is connected to the Rx Symbol/Clock extraction circuit at a point which carries the equalised receive signal. This may be monitored with an oscilloscope (at the TXOP pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters and FM demodulator.

The resulting eye diagram (for reasonably random data) should ideally be as shown in the following Figure 13, with 4 'crisp' and equally spaced crossing points.

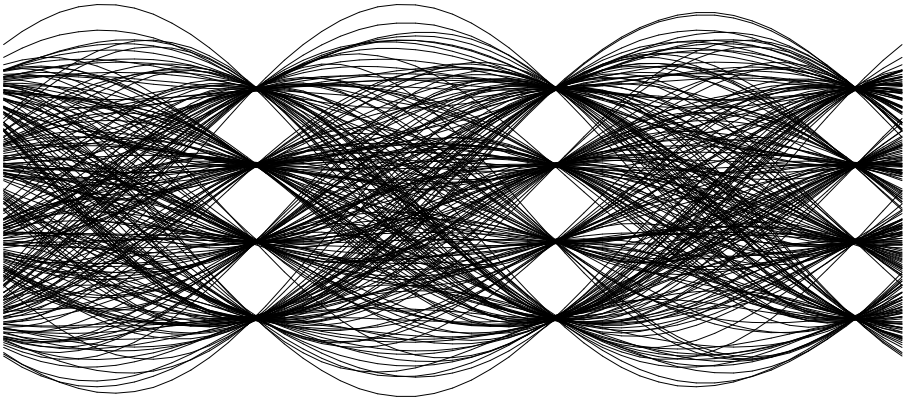


Figure 13 Ideal 'RXEYE' Signal

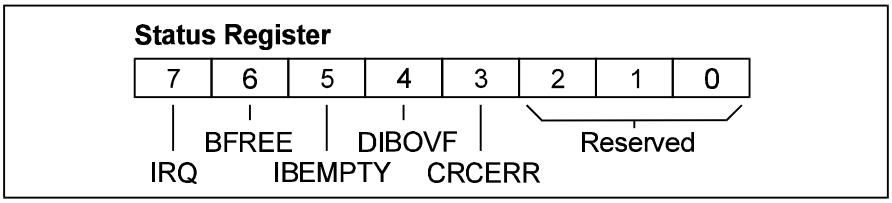
Mode Register B3: PSAVE - Powersave
When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx Symbol & Clock extraction circuits and the Tx o/p buffer will be disabled, and the TxOp pin will be connected to V_{BIAS} through a high value resistance. The Xtal Clock oscillator, Rx i/p amplifier and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry. Note that the internal filters - and hence the TxOp pin in transmit mode - will take about 20 symbol-times to settle after the PSAVE bit is taken from '1' to '0'.

Mode Register B2, B1, B0
These bits should be set to '000'.

1.5.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



Status Register B7: IRQ - Interrupt Request
This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register TXRXN or PSAVE bits.

or The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register TXRXN or PSAVE bits.

or The Status Register DIBOVF bit going from '0' to '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQNEN bit of the Mode Register is '1', then the chip IRQN output will be pulled low (to V_{SS}) whenever the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

Status Register B6: BFREE - Data Block Buffer Free
This bit reflects the availability of the Data Block Buffer and is cleared to '0' whenever a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register TXRXN or PSAVE bits are changed.

Status Register B5: IBEMPTY - Interleave Buffer Empty
In transmit mode, this bit will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TXRXN or PSAVE bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid level (half-way between '+1' and '-1') signal will be sent to the RRC filter.

In receive mode this bit will be '0'.

Status Register B4: DIBOVF - De-Interleave Buffer Overflow
In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the TXRXN or PSAVE bits of the Mode Register.

In transmit mode this bit will be '0'.

Status Register B3: CRCERR - CRC Checksum Error
In receive mode this bit will be updated at the end of a SFSH, RHB or RILB task to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error.

Note that this bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task, or by changing the TXRXN or PSAVE bits of the Mode Register. In transmit mode this bit is '0'.

Status Register B2, B1, B0
These bits are reserved for future use.

1.5.5.6 Data Quality Register

In receive mode, the FX919A continually measures the 'quality' of the received signal, by comparing the actual received waveform over the previous 64 symbol times against an internally generated 'ideal'.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 14 shows how the value (0-255) read from the Data Quality Register varies with received signal-to-noise ratio:

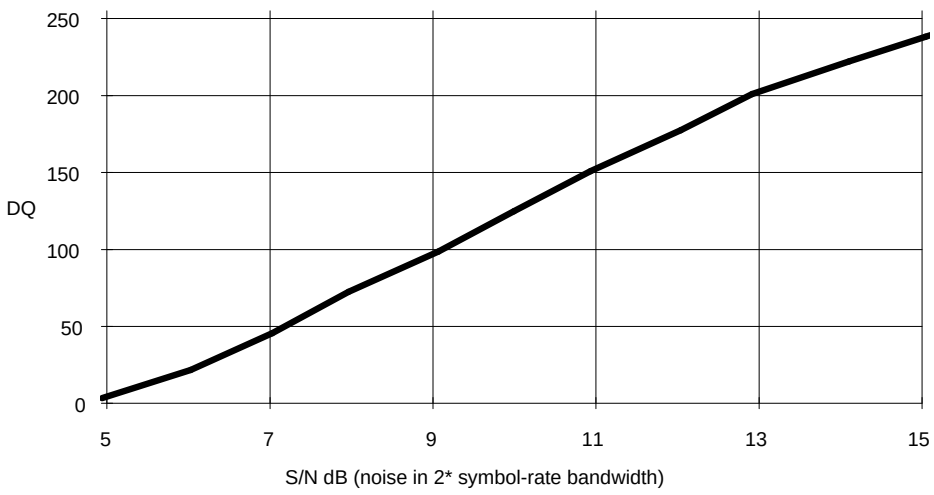


Figure 14 Typical Data Quality Reading vs S/N

The Data Quality readings are only valid when the modem has successfully acquired signal level and timing lock for at least 64 symbol times. It is invalid when an AQSC or AQLEV sequence is being performed or when the LEVRES setting is 'Clamp' or 'Lossy Peak Detect'. A low reading will be obtained if the PLLBW bits are set to 'Wide' or if the received signal waveform is distorted in any significant way.

1.5.6 CRC, FEC and Interleaving

Cyclic Redundancy Codes

CRC1
This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block. It is calculated by the modem from the first 80 bits of the block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^{5} + 1$$

CRC2
This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x^{1} + 1$$

Note: In receive mode the CRC2 checksum circuits are initialised on completion of any task other than NULL or RILB. In transmit mode the CRC2 checksum circuits are initialised on completion of any task other than NULL, TIB or TLB.

Forward Error Correction
In transmit mode, the FX919A uses a Trellis Encoder to translate the 96 bits (12 bytes) of a 'Header', 'Intermediate' or 'Last' Block into a 66-symbol sequence which includes FEC information.

In receive mode, the FX919A decodes the received 66 symbols of a block into 96 bits of binary data using a 'Soft Decision' Viterbi algorithm to perform decoding and error correction.

Interleaving
The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to give protection against the effects of noise bursts and short fades.

In receive mode, the FX919A de-interleaves the received symbols prior to decoding.

1.6 Application Notes

1.6.1 Transmit Frame Examples

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences, and one each Header, Intermediate and Last blocks are shown below:

1. Ensure that the Control Register has been loaded with a suitable CKDIV value, that the IRQNEN and TXRXN bits of the Mode Register are '1', the RXEYE and PSAVE bits are '0' and the INVSYM bit is set appropriately.

2. Read the Status Register to ensure that the BFREE bit is '1', then write 6 Symbol Sync bytes to the Data Block Buffer and a T24S task to the Command Register.

3. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.

4. Write 6 Frame Sync bytes to the Data Block Buffer and a T24S task to the Command Register.

5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.

6. Write 10 Header Block bytes to the Data Block Buffer and a THB task to the Command Register.

7. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.

8. Write 12 Intermediate Block bytes to the Data Block Buffer and a TIB task to the Command Register.

9. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.

10. Write 8 Last Block bytes to the Data Block Buffer and a TLB task to the Command Register.

11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.

12. Wait for another interrupt from the modem, read the Status Register; the IRQ, BFREE and IBEMPTY bits should be '1'.

Note: The final symbol of the frame will start to appear approximately 2 symbol times after the Status Register IBEMPTY bit goes to '1'; a further 16 symbol times should be allowed for the symbol to pass completely through the RRC filter.

Figures 15a and 15b illustrate the host µC routines needed to send a single Frame consisting of Symbol and Frame Sync patterns, a Header block, any number of Intermediate blocks and one Last block. It is assumed that the Tx Interrupt Service Routine (Figure 15b) is called whenever the FX919A's IRQN output line goes low.

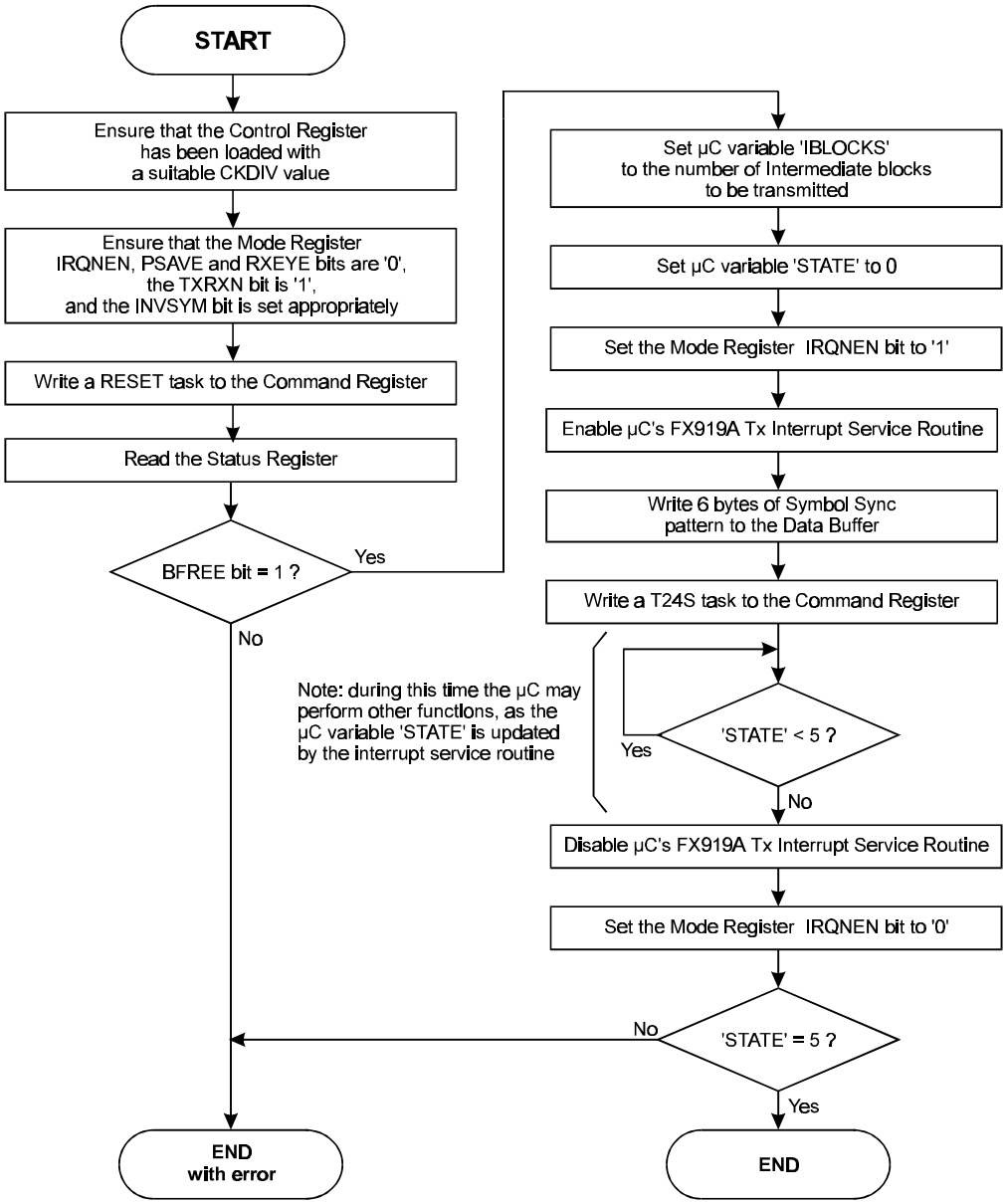


Figure 15a Transmit Frame Example Flowchart, Main Program

Note that the RESET command in Figure 15a and the practice of disabling the FX919A's IRQN output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation.

Note also that the CRC bit should be set appropriately whenever a byte is written to the Command Register.

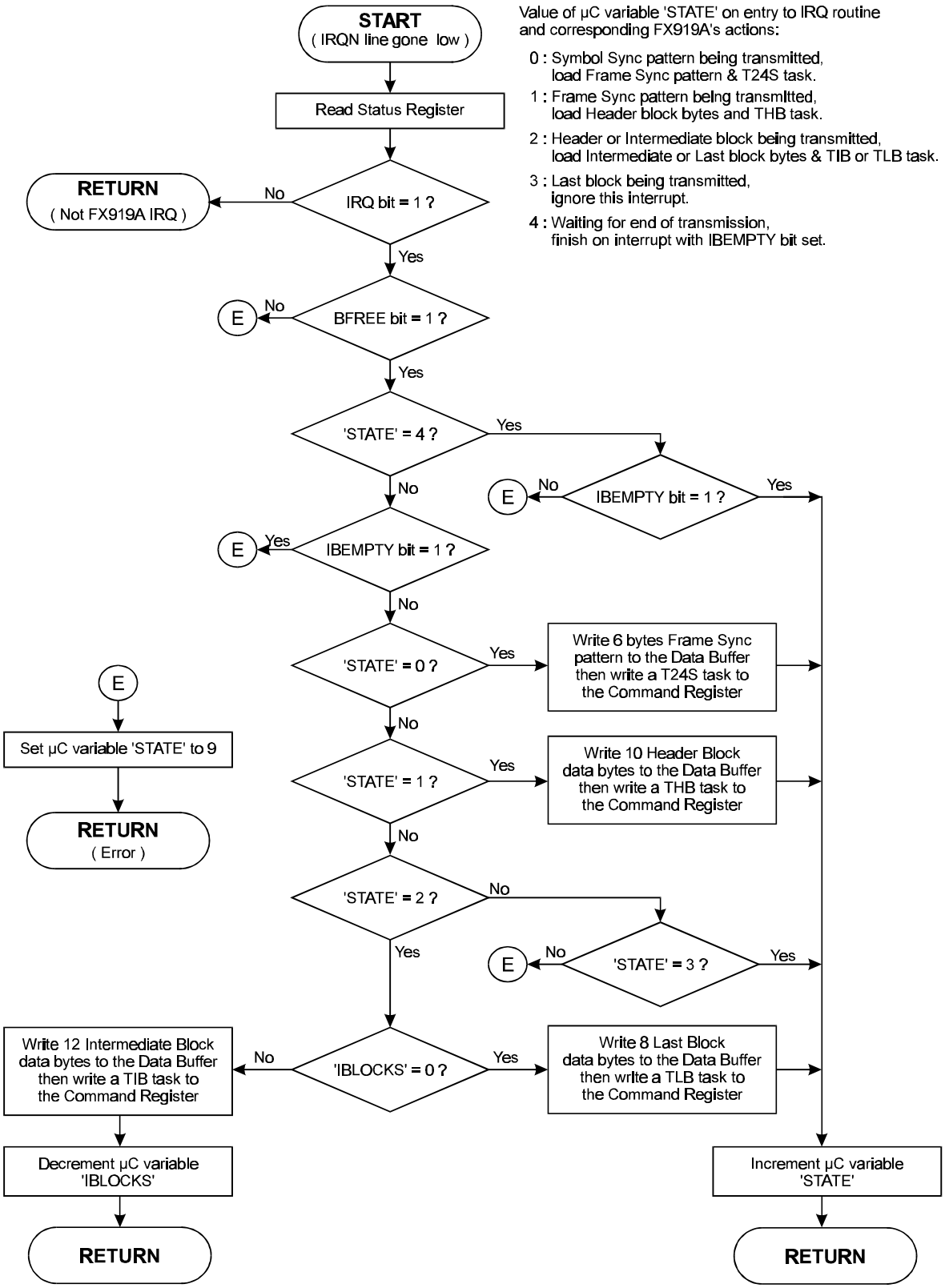


Figure 15b Tx Interrupt Service Routine

1.6.2 Receive Frame Examples

The operations needed to receive a single Frame consisting of Symbol and Frame Sync sequences and one each Header, Intermediate and Last blocks are shown below;

1. Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, and that the IRQNEN bit of the Mode Register is '1', the TXRXN, PSAVE and RXEYE bits are '0', and the INVSYM bit is set appropriately.

2. Wait until the received carrier has been present for at least 8 symbol times (see Section 1.6.3).

3. Read the Status Register to ensure that the BFREE bit is '1'.

4. Write a byte containing a SFSH task and with the AQSC and AQLEV bits set to '1' to the Command Register.

5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the CRCERR and DIBOVF bits should be '0'.

6. Check that the CRCERR bit of the Status Register is '0' and read 10 Header Block bytes from the Data Block Buffer.

7. Write a RILB task to the Command Register.

8. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.

9. Read 12 Intermediate Block bytes from the Data Block Buffer.

10. Write a RILB task to the Command Register.

11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.

12. Check that the CRCERR bit of the Status Register is '0' and read the 8 Last Block bytes from Data Buffer.

Figures 16a and 16b illustrate the host µC routines needed to receive a single Frame consisting of Symbol and Frame Sync patterns, a Header block, any number of Intermediate blocks and one Last block. It is assumed that the Rx Interrupt Service Routine (Figure 16b) is called whenever the FX919A's IRQN output line goes low.

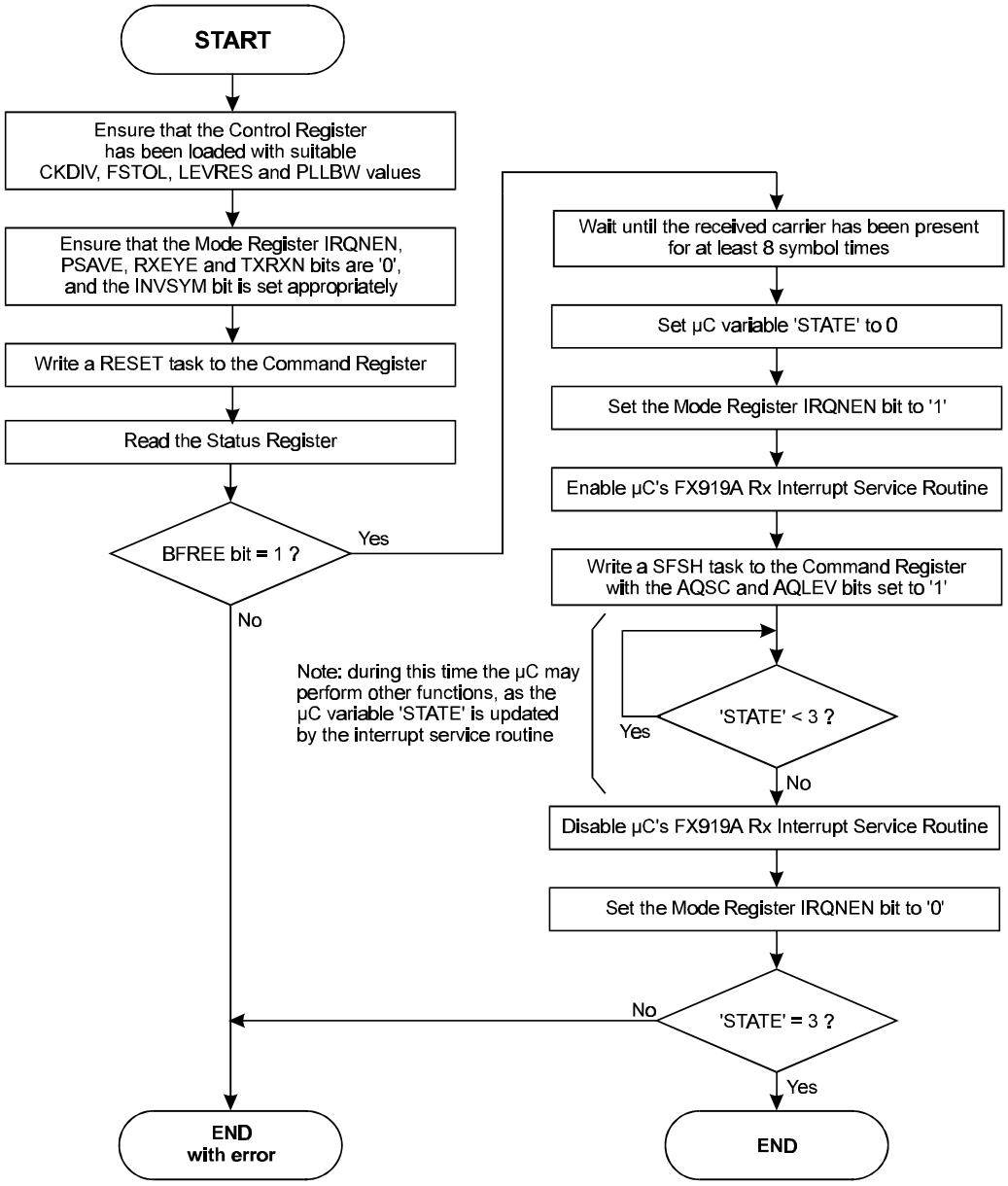


Figure 16a Receive Frame Example Flowchart, Main Program

Note that the RESET command in Figure 16a and the practice of disabling the FX919A's IRQN output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation.

Note also that the CRC bit should be set appropriately whenever a byte is written to the Command Register.

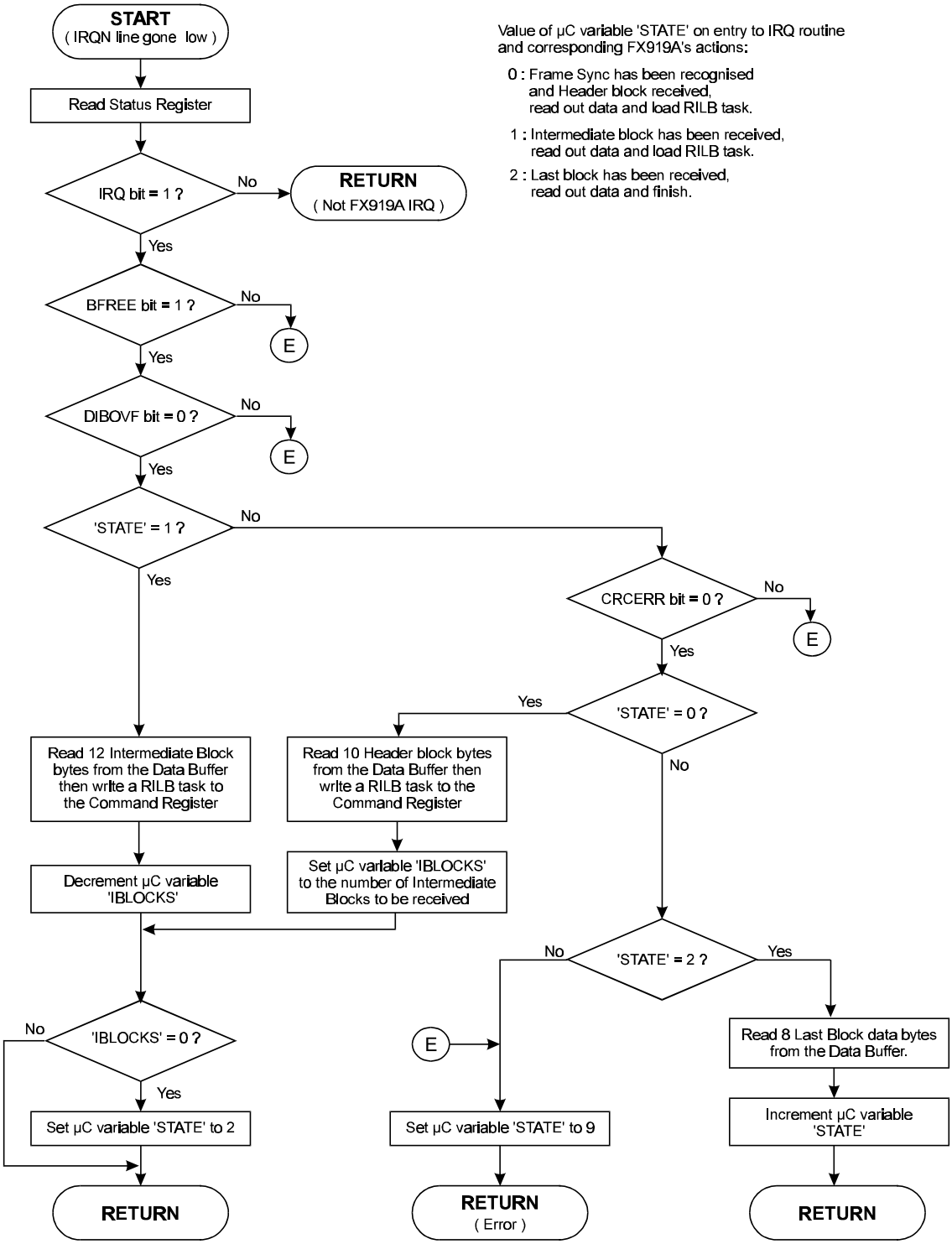


Figure 16b Rx Interrupt Service Routine

Note: This routine assumes that the number of Intermediate blocks in the Frame is contained within the Header Block data.

1.6.3 Clock Extraction and Level Measurement Systems

The FX919A is intended for use in systems where:

- The Symbol Sync pattern is transmitted immediately on start-up of the transmitter, before the first Frame Sync pattern (see Figure 17).

- A terminal may remain powered up indefinitely, transmitting concatenated Frames with or without intervening Symbol Sync patterns (each Frame having a Frame Synch pattern and symbol timing being maintained from one Frame to the next).

- A receiving modem may be switched onto a channel before the distant transmitter has started up, or may be switched onto a channel where the transmitting station is already sending concatenated Frames.

Whenever the receiving modem is enabled or switched onto a channel it needs to establish the received symbol levels and timing and look for a Frame Sync pattern in the incoming signal. This is best done by the following procedure.

1. Ensure that the Control Register's PLLBW bits are set to 'Wide' and the LEVRES bits to 'Slow Peak Detect'.

2. Wait until a received carrier has been present for 8 symbol times. This 8-symbol delay gives time for the received signal to propagate through the modem's RRC filter and can usefully be included in the radio's carrier detect circuitry.

3. Write a SFS or SFSH task to the Command Register with the AQSC and AQLEV bits set to '1'.

4. When the modem interrupts to signal that it has recognised a Frame Sync pattern (or completed the SFSH task) then change the PLLBW bits to 'Medium'.

Once the receiving modem has achieved level and symbol timing synchronisation with a particular channel - as evidenced by recognition of a Frame Sync pattern - then subsequent concatentated Frames can be read by simply issuing SFS or SFSH tasks at appropriate times, keeping the ASQSC and AQLEV bits at zero, and the PLLLBW and LEVRES bits at their current 'Medium' and 'Slow Peak Detect' settings.

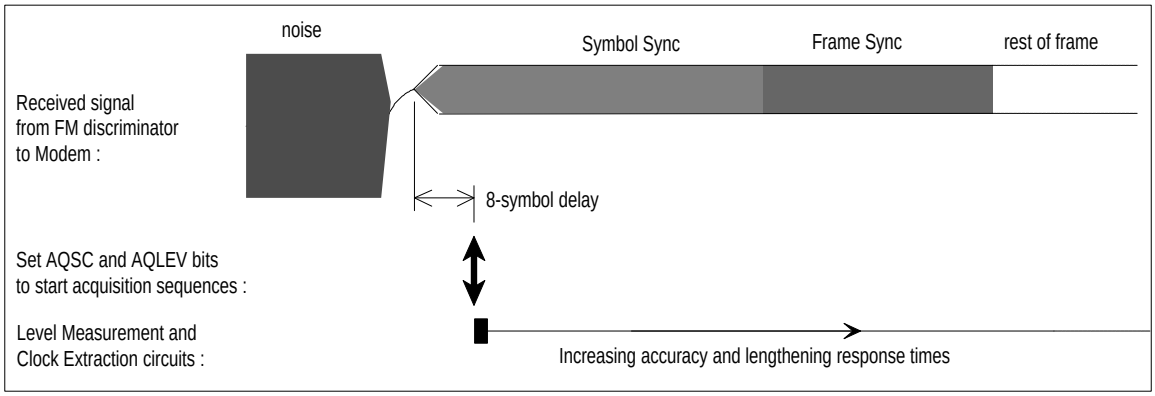


Figure 17 Acquisition Sequence Timing (Transmitter Power-Up)

It is also possible to use the modem in a system where there is an indeterminate delay between the transmitter start-up and the Symbol Sync pattern, or where a receive carrier detect signal is not available to the controlling µC, or where the transmitting terminal can send separate unsynchronised Frames. In these cases each Frame should be preceded by a Symbol Sync pattern which should be extended to about 100 symbols, and the procedure given in paragraphs (1) to (4) above used at all times.

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude and dc offset as quickly as possible before switching to more accurate - but slower - measurement modes. These acquisition sequences act very quickly if triggered at the start of a received Symbol Sync pattern (as shown in Figure 17), but will still function correctly - although more slowly - if started any time during a normal Frame, as when the receiver is switched onto a channel where the transmitter is operating continuously.

The automatic AQLEV Level Measurement acquisition sequence starts with the level measurement circuits being put into 'Clamp' mode for one symbol time to set the voltages on the DOC pins to some point within the range of the received signal excursions. The level measurement circuits are then automatically set to 'Lossy Peak Detect' mode for 15 symbol times, after which the sequence ends and the level measurement circuit modes reverts to the mode set by the LEVRES bits of the Control Register (normally 'Slow Peak Detect').

The peak detectors used in both 'Slow' and 'Lossy Peak Detect' modes include additional low pass filtering of the received signal which greatly reduces the effect of pattern noise on the reference voltages held on the external DOC capacitors, but means that pairs of '+3' (and '-3') symbols need to be received to establish the correct levels. 2 pairs of '+3' and two pairs of '-3' symbols received after the start of an AQLEV sequence are sufficient to set the levels on the DOC capacitors to their optimum levels.

The automatic AQSC Symbol Clock acquisition sequence sets the PLL to 'Extra Wide Bandwidth' mode for 16 symbol times (this mode is not one of those which can be selected by the Control Register PLLBW bits) then changes to 'Wide' bandwidth. After 45 symbol times the PLL mode will revert to that set by the Control Register PLLBW bits.

1.6.4 AC Coupling

For a practical circuit, ac coupling from the modem's transmit output to the frequency modulator and between the receiver's frequency discriminator and the receive input of the modem may be desired. There are, however, two problems:

Firstly, ac coupling of the signal degrades the Bit Error Rate performance of the modem. The following graph illustrates the typical bit error rates at 4800 symbols/sec (without FEC) for differing degrees of ac coupling:

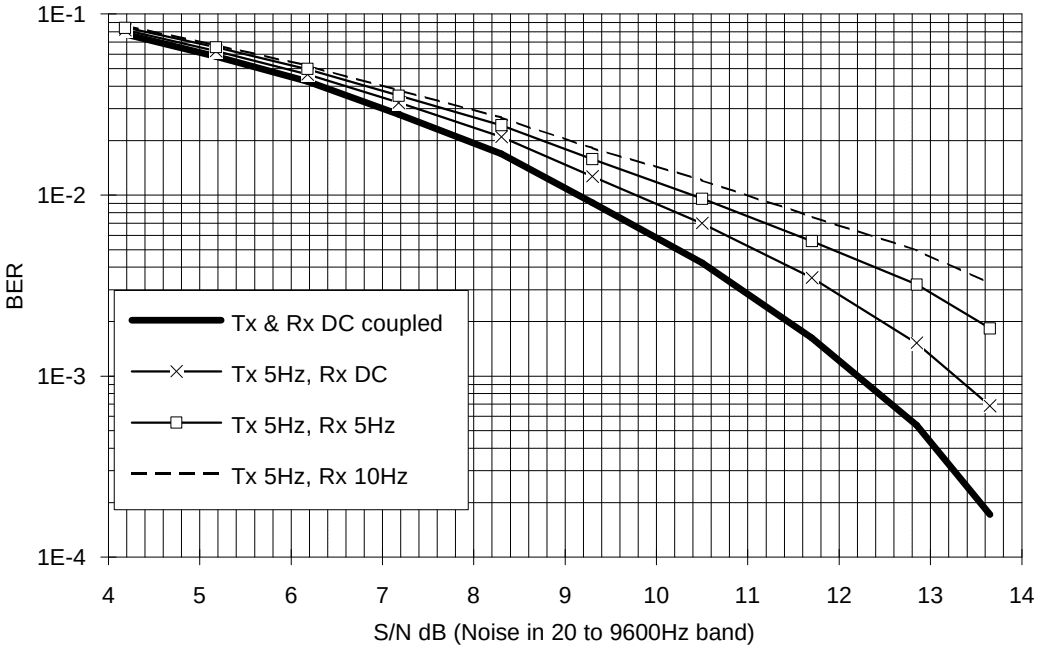


Figure 18 Effect of AC Coupling on BER

Secondly, any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 19 below, the time for this step to decay to 37% of its original value is 'RC' where:

RC = 1/(2 x π x the 3dB cut-off frequency of the RC network)

which is 32 msec, or 153 symbol times at 4800 symbols/sec, for a 5Hz network.

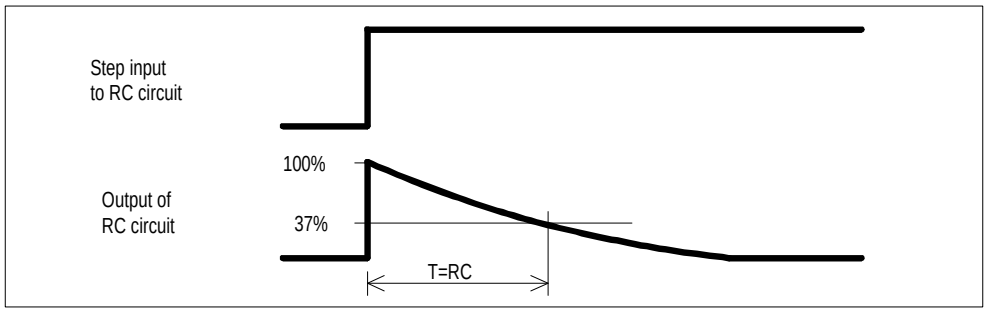


Figure 19 Decay Time - AC Coupling

In general, it will be best to dc couple the receiver discriminator to the modem, and to ensure that any ac coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4800 symbols/sec).

1.6.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using these modems depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec can be achieved - subject to local regulatory requirements - over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive ' +3 +3 -3 -3 ... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio. In particular, attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator. For a 4800 symbols/sec system, the frequency response should be within ±2dB over the range 3Hz to 5kHz, relative to 2400Hz.

- The bandwidth and phase response of the receiver's IF filters.

- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal eye - using the Mode Register RXEYE function - gives a good indication of the overall transmitter/receiver performance.

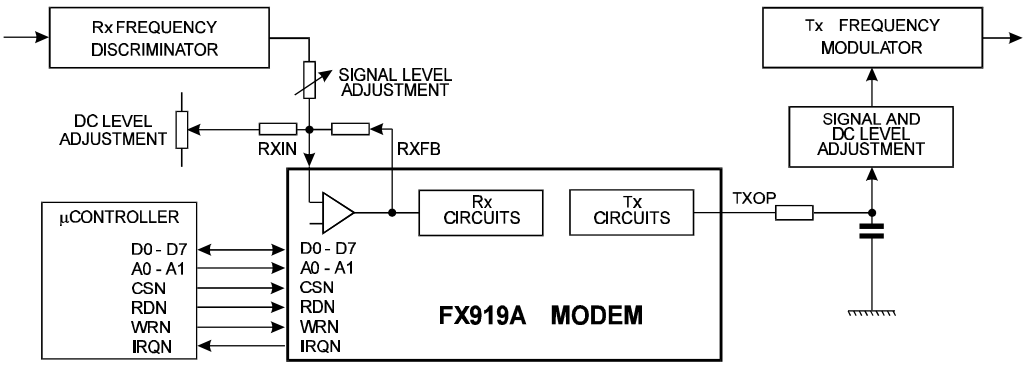


Figure 20 Typical Connections Between Radio and FX919A

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

D2 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

D5 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

P4 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	+85	°C
Symbol Rate		2400	9600	Symbols/sec
Xtal Frequency		1.0	10.0	MHz

Operating Characteristics
For the following conditions unless otherwise specified:

Xtal Frequency = 4.9152MHz, Symbol Rate = 4800 symbols/sec,
Noise Bandwidth = 0 to 9600Hz, V_{DD} = 3.3V to 5.0V, Tamb = - 40°C to +85°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (V_{DD} = 5.0V)	1		4.0	10.0	mA
I_{DD} (V_{DD} = 3.3V)	1		2.5	6.3	mA
I_{DD} (Powersave Mode V_{DD} = 5.0V)	1		1.5		mA
I_{DD} (Powersave ModeV_{DD} = 3.3V)	1		0.6		mA
AC Parameters					
Tx Output					
TXOP Impedance	2		1.0	2.5	kΩ
Signal Level	3	0.8	1.0	1.2	V pk-pk
Output DC Offset wrt V_{DD}/2	4	-0.25		+0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (I/P = 1mVrms at 100Hz)			300		V/V
Input Signal Level	5	0.7	1.0	1.3	V pk-pk
DC Offset wrt V_{DD}/2	5	-0.5		+0.5	V
Xtal/Clock Input					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Gain (I/P = 1mVrms at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (Vin = 0 to V_{DD})	7, 8	–5.0		+5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8,9			8%	V_{DD}
'Off' State Leakage Current (Vout = V_{DD})	9			10	µA

Notes:
1. At 25°C. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
2. Small signal impedance, at V_{DD} = 5.0V and Tamb = 25°C.
3. Measured after the external RC filter (R4/C5) for a "+3 +3 -3 -3...." symbol sequence, at V_{DD} = 5.0V and Tamb = 25°C (output level is proportional to V_{DD}).
4. Measured at the TXOP pin with the modem in the Tx idle mode.
5. For optimum performance, measured at RXFB pin, for a "...+3 +3 -3 -3..." symbol sequence, at V_{DD} = 5.0V and Tamb = 25°C. Optimum level is proportional to V_{DD}.
6. Timing for an external input to the CLOCK/XTAL pin.
7. WRN, RDN, CSN, A0 and A1 pins.
8. D0 - D7 pins.
9. IRQN pin.

		Notes	Min.	Typ.	Max.	Units
µC Parallel Interface Timings (ref. Figure 21)						
t_{ACSL}	Address valid to CSN low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	CSN hold time		0			ns
t_{CSHI}	CSN high time	10	6			clock cycles
t_{CSRWL}	CSN to WRN or RDN low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	RDN high to CSN low time (write)		0			ns
t_{RACL}	Read access time from CSN low	11			175	ns
t_{RARL}	Read access time from RDN low	11			145	ns
t_{RL}	RDN low time		200			ns
t_{RX}	RDN high to D0-D7 3-state time				50	ns
t_{WHCSL}	WRN high to CSN low time (read)		0			ns
t_{WL}	WRN low time		200			ns

Notes: 10. Xtal/Clock cycles at the XTAL/CLOCK pin.
11. With 30pF max to V_{SS} on D0 - D7 pins.

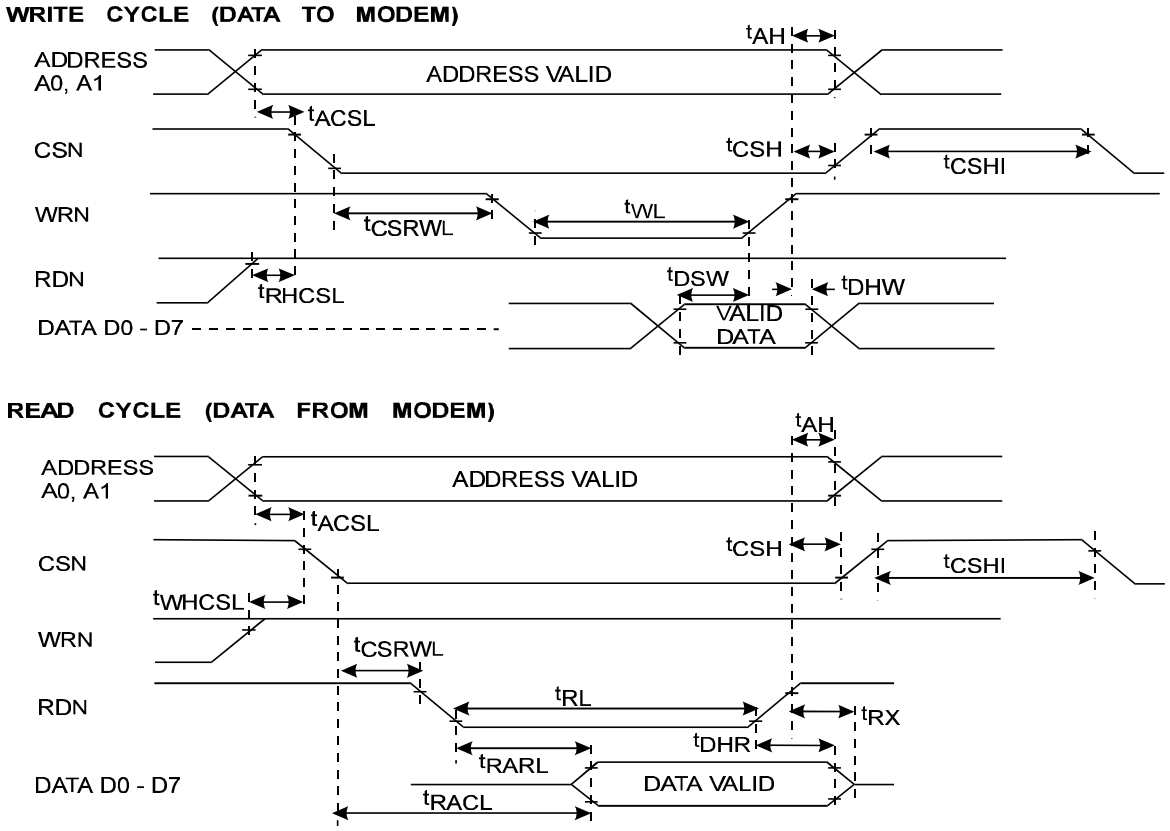


Figure 21 µC Parallel Interface Timings

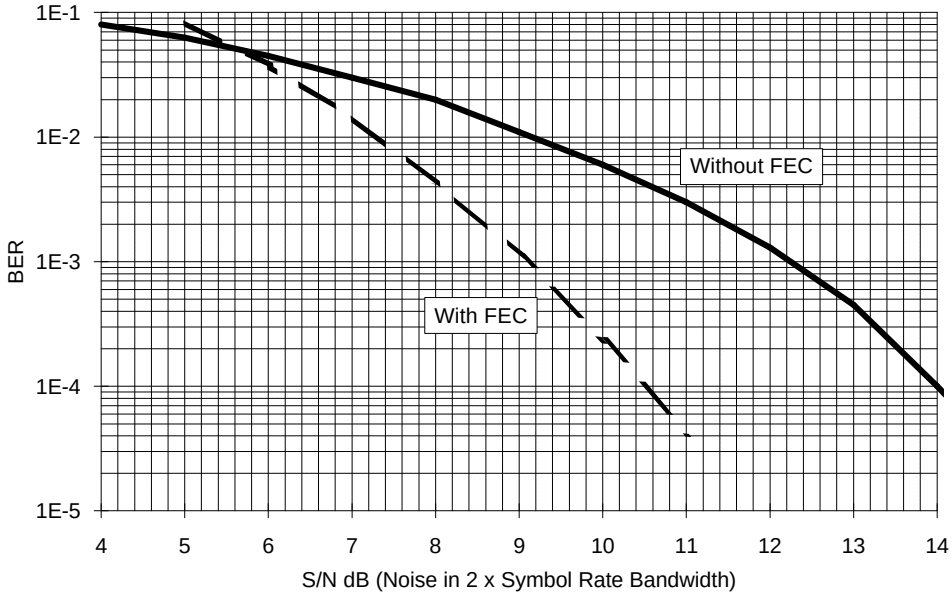


Figure 22 Typical Bit Error Rate With and Without FEC

Measured under nominal working conditions, LEVRES bits set to 'Slow Peak Detect' and PLLBW bits set to 'Narrow Bandwidth' , with pseudo-random data.

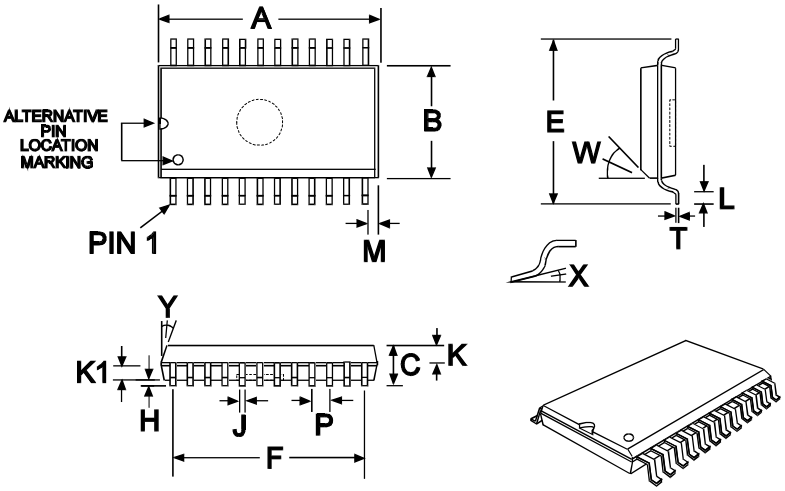
Note: S/N calculated as $20 \times LOG_{10}$(Signal Voltage ÷ Noise Voltage)

Where Signal Voltage is the measured rms. voltage of a random 4-level signal.

Noise Voltage is the rms. voltage of a flat Gaussian noise signal having a bandwidth from a few Hz to twice the symbol rate (e.g. to 9600Hz when measuring a 4800 symbol/sec system).

Both signals are measured at the same point in the test circuit.

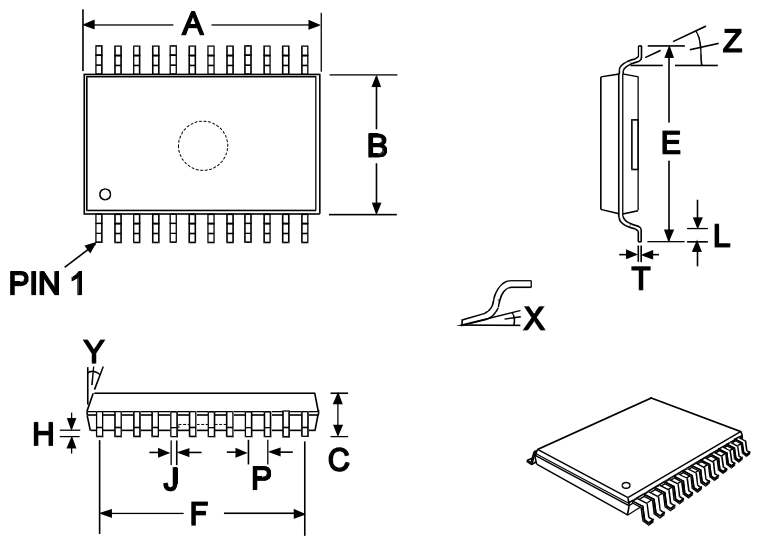
1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.566 (14.37)	
H	0.004 (0.10)		0.012 (0.30)
J	0.014 (0.36)		0.018 (0.46)
K	0.036 (0.91)		0.046 (1.17)
K1	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

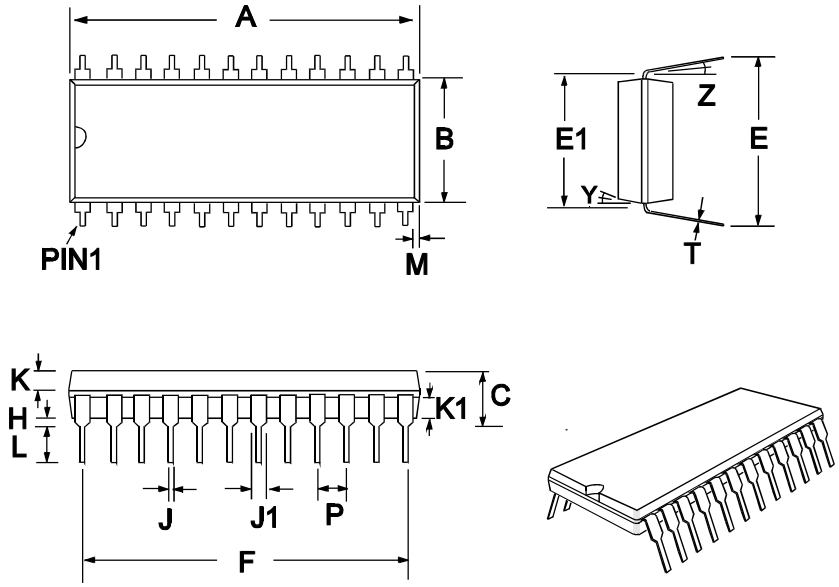
Figure 23 D2 Mechanical Outline: ***Order as part no. FX919AD2***



DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 24 D5 Mechanical Outline: ***Order as part no. FX919AD5***



DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.552 (14.02)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.150 (3.81)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 25 P4 Mechanical Outline: ***Order as part no. FX919AP4***

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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