TPS54320 4.5- to 17-V Input, 3-A Synchronous Step Down SWIFT™ Converter

1 Features

- Integrated 57-mΩ / 50-mΩ MOSFETs
- Split Power Rail: 1.6 to 17 V on PVIN
- 200-kHz to 1.2-MHz Switching Frequency
- Synchronizes to External Clock
- 0.8-V Voltage Reference With ±1% Accuracy
- Low 2-µA Shutdown Quiescent Current
- Hiccup Overcurrent Protection
- Monotonic Start-Up into Prebiased Outputs
- –40°C to 150°C Operating Junction Temperature Range
- Pin-to-Pin Compatible With the TPS54620
- Adjustable Slow Start/Power Sequencing
- Power Good Output for Undervoltage and Overvoltage Monitoring
- Adjustable Input Undervoltage Lockout (UVLO)
- Supported by SwitcherPro™ Software Tool
- For SWIFT™ Documentation and SwitcherPro, Visit www.ti.com/swift

2 Applications

- Broadband, Networking, and Communication Infrastructure
- Automated Test and Medical Equipment
- DSP and FPGA Point-of-Load Applications from 12-V Bus

3 Description

The TPS54320 is a full featured 17-V, 3-A synchronous step-down converter which is optimized for small designs through high efficiency and integrated high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and by selecting a high switching frequency, reducing the inductor's footprint.

The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins.

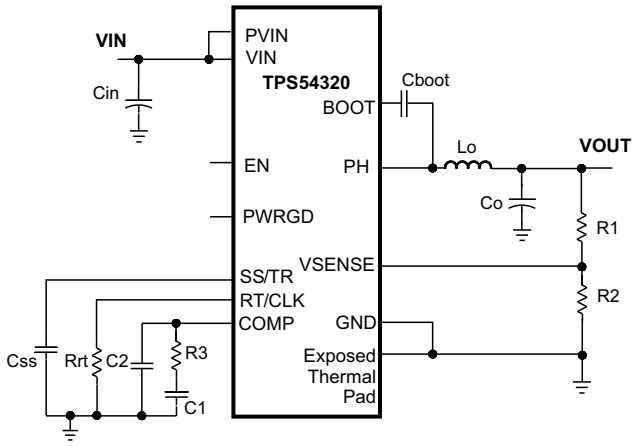
Cycle by cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. Hiccup protection will be triggered if the overcurrent condition has persisted for longer than the preset time. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature. The TPS54320 is available in a 14-pin, 3.5-mm × 3.5-mm VQFN, thermally-enhanced package.

Device Information(1)

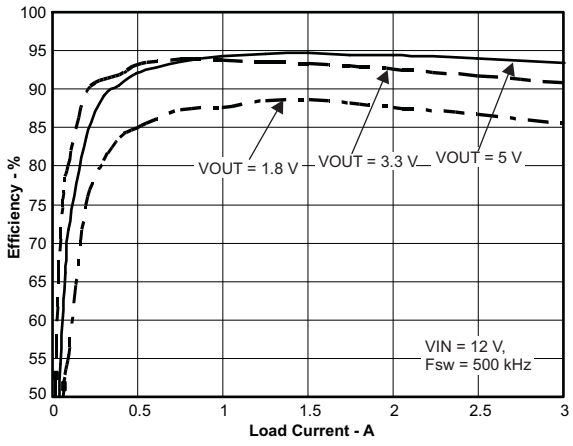
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54320	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2010) to Revision B **Page**

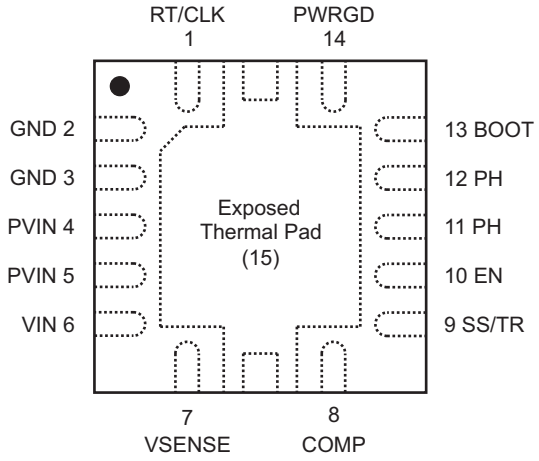
- Added *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Bill of Materials* ... 31

Changes from Original (August 2010) to Revision A **Page**

- Changed *Applications* itemized list ... 1
- Changed Figure 34 - Typical App Circuit ... 23
- Changed Figure 51 image with new plot ... 29
- Changed Figure 47 image with new plot ... 30
- Changed Figure 55 Thermal Signature image ... 30
- Added C6 to Bill of Material and changed C8 RefDes to C9 with size 1210 to match SLVU380 User's Guide BoM ... 31

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5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
RT/CLK	1	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; In CLK mode, the device synchronizes to an external clock.
GND	2	Return for control circuitry and low-side power MOSFET.
	3	
PVIN	4	Power input. Supplies the power switches of the power converter.
	5	
VIN	6	Supplies the control circuitry of the power converter.
VSENSE	7	Inverting input of the gm error amplifier.
COMP	8	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	9	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
EN	10	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
PH	11	The switch node
	12	
BOOT	13	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
PWRGD	14	Open-drain Power Good fault pin. Asserts low due to thermal shutdown, undervoltage, overvoltage, EN shutdown, or during slow start.
Exposed thermal PAD	15	Thermal pad of the package and signal ground. It must be soldered down for proper operation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	20	V
	PVIN	–0.3	20	V
	EN	–0.3	6	V
	BOOT	–0.3	27	V
	VSENSE	–0.3	3	V
	COMP	–0.3	3	V
	PWRGD	–0.3	6	V
	SS/TR	–0.3	3	V
	RT/CLK	–0.3	6	V
Output voltage	BOOT-PH	0	7	V
	PH	–1	20	V
	PH 10-ns transient	–3	20	V
Vdiff	GND to exposed thermal pad	–0.2	0.2	V
Source current	RT/CLK		±100	µA
	PH	Current limit		A
Sink current	PH	Current limit		A
	PVIN	Current limit		A
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Operating junction temperature		–40	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Input voltage range	VIN	4.5		17	V
	Power stage input voltage range	PVIN	1.6		17	V
	Output current		0		3	A
T_J	Operating junction temperature range		–40		150	°C

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6.4 Thermal Information

THERMAL METRIC[1][2]		TPS54320 VQFN 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance[3]	32	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	14.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 150°C for best performance and long-term reliability. See power dissipation estimate in application section of this data sheet for more information.
(3) Test board conditions:
(a) 2.5 inches × 2.5 inches, 4 layers, thickness: 0.062 inch
(b) 2-oz. copper traces located on the top of the PCB
(c) 2-oz. copper ground planes on the 2 internal layers and bottom layer
(d) 40.010-inch thermal vias located under the device package

6.5 Electrical Characteristics

T_J= –40°C to 150°C, VIN = 4.5 to 17 V, PVIN = 1.6 to 17 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)					
PVIN operating input voltage		1.6		17	V
VIN operating input voltage		4.5		17	V
VIN internal UVLO threshold	VIN rising		4.0	4.5	V
VIN internal UVLO hysteresis			150		mV
VIN shutdown supply Current	EN = 0 V		2	5	µA
VIN operating – non switching supply current	VSENSE = 810 mV		600	800	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.21	1.26	V
Enable threshold	Falling	1.10	1.17		V
Input current	EN = 1.1 V		1.15		µA
Hysteresis current	EN = 1.3 V		3.4		µA
VOLTAGE REFERENCE					
Voltage reference	0 A ≤ I_{OUT} ≤ 3 A	0.792	0.800	0.808	V
MOSFET					
High-side switch resistance[1]	BOOT-PH = 3 V		77	116	mΩ
High-side switch resistance[1]	BOOT-PH = 6 V		57	103	mΩ
Low-side Switch Resistance[1]	VIN = 12 V		50	87	mΩ
ERROR AMPLIFIER					
Error amplifier Transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		1300		µMhos
Error amplifier dc gain	VSENSE = 0.8 V	1000	3100		V/V
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100-mV input overdrive		±110		µA
Start switching threshold			0.25		V
COMP to Iswitch gm			12		A/V

(1) Measured at pins

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Electrical Characteristics (continued)

T_J= –40°C to 150°C, VIN = 4.5 to 17 V, PVIN = 1.6 to 17 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT					
High-side switch current limit threshold		4.2	6.2		A
Low-side switch sourcing current limit		3.8	5.8		A
Low-side switch sinking current limit		1	2.6		A
Hiccup wait time before triggering hiccup			512		cycles
Hiccup time before restart			16384		cycles
THERMAL SHUTDOWN					
Thermal shutdown		160	175		°C
Thermal shutdown hysteresis			10		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Minimum switching frequency	Rrt = 240 kΩ (1%)	160	200	240	kHz
Switching frequency	Rrt = 100 kΩ (1%)	400	480	560	kHz
Maximum switching frequency	Rrt = 40.2 kΩ (1%)	1080	1200	1320	kHz
Minimum pulse width			20		ns
RT/CLK high threshold				2	V
RT/CLK low threshold		0.8			V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		62		ns
Switching frequency range (RT mode set point and PLL mode)		200		1200	kHz
PH (PH PIN)					
Minimum on time	Measured at 90% to 90% of PH, T_A = 25°C, I_{PH} = 2 A		97	135	ns
Minimum off time	BOOT-PH ≥ 3 V		0		ns
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.1	3	V
SLOW START AND TRACKING (SS/TR PIN)					
SS charge current			2.3		µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		29	60	mV
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91		% Vref
	VSENSE rising (Good)		94		% Vref
	VSENSE rising (Fault)		109		% Vref
	VSENSE falling (Good)		106		% Vref
Output high leakage	VSENSE = Vref, $V_{(PWRGD)}$ = 5.5 V		30	100	nA
Output low	$I_{(PWRGD)}$ = 2 mA			0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5V at 100 µA		0.6	1	V
Minimum SS/TR voltage for PWRGD valid			1.2	1.4	V

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6.6 Typical Characteristics

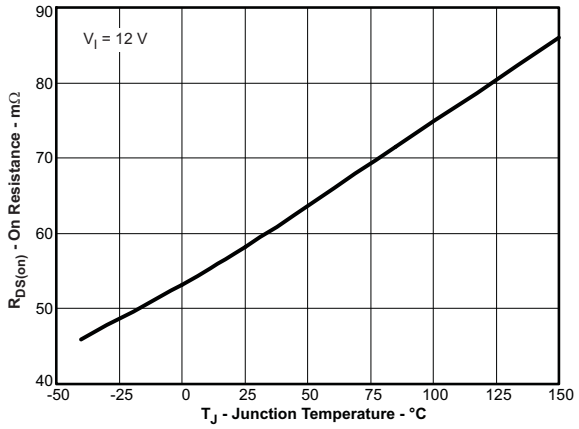


Figure 1. High-Side Rdson vs Temperature

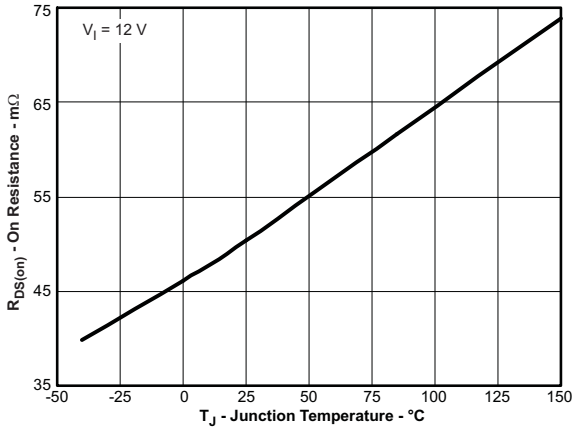


Figure 2. Low-Side Rdson vs Temperature

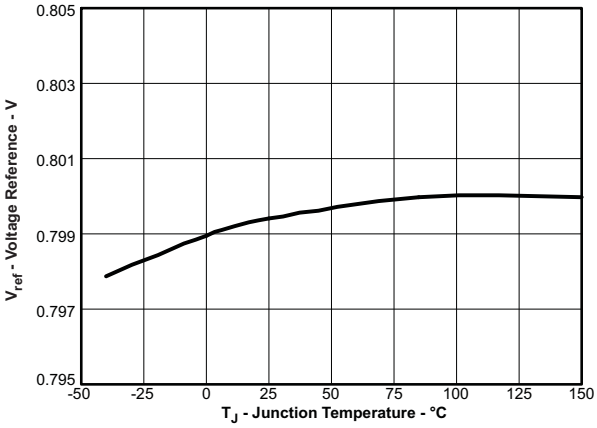


Figure 3. Voltage Reference vs Temperature

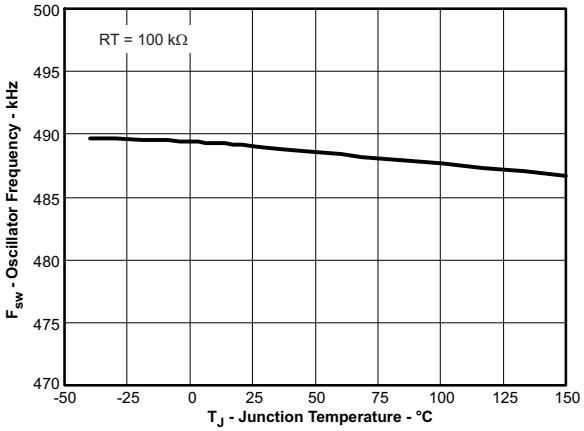


Figure 4. Oscillator Frequency vs Temperature

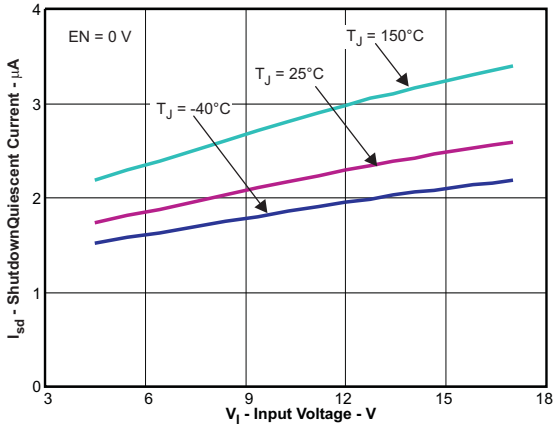


Figure 5. Shutdown Quiescent Current vs Input Voltage

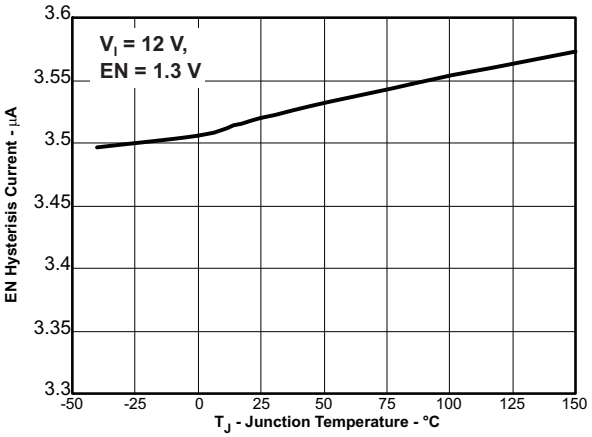


Figure 6. EN Pin Hysteresis Current vs Temperature

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Typical Characteristics (continued)

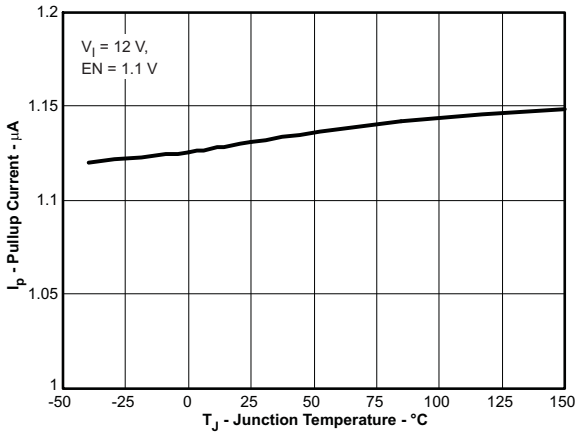


Figure 7. EN Pin Pullup Current vs Temperature

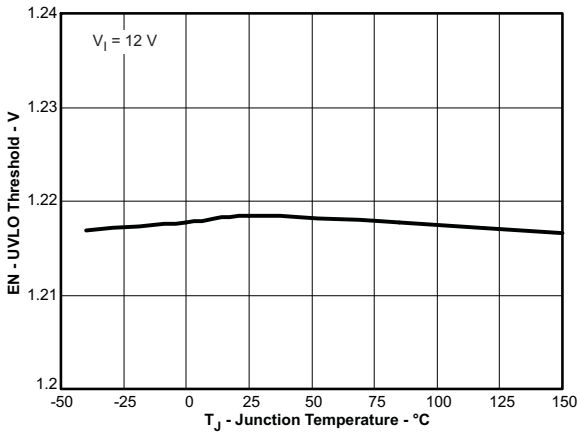


Figure 8. EN Pin UVLO Threshold vs Temperature

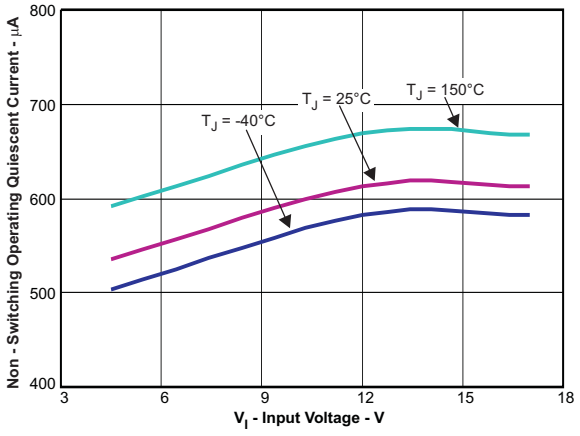


Figure 9. Non-Switching Operating Quiescent Current vs Input Voltage

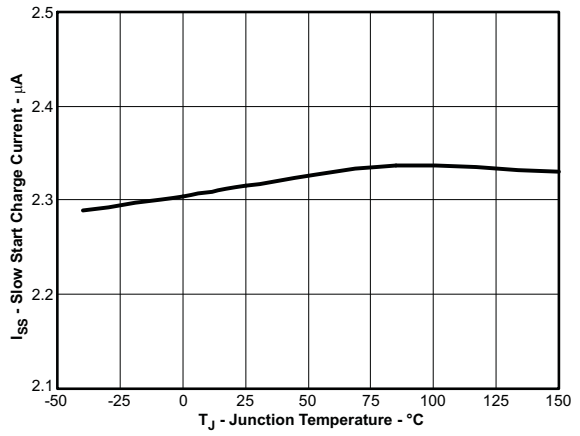


Figure 10. Slow-Start Charge Current vs Temperature

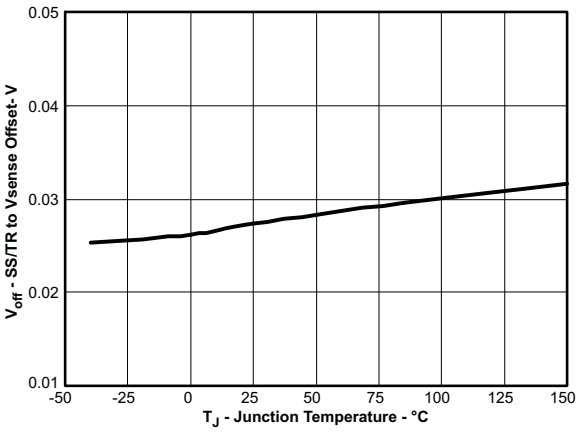


Figure 11. (SS/TR - VSENSE) Offset vs Temperature

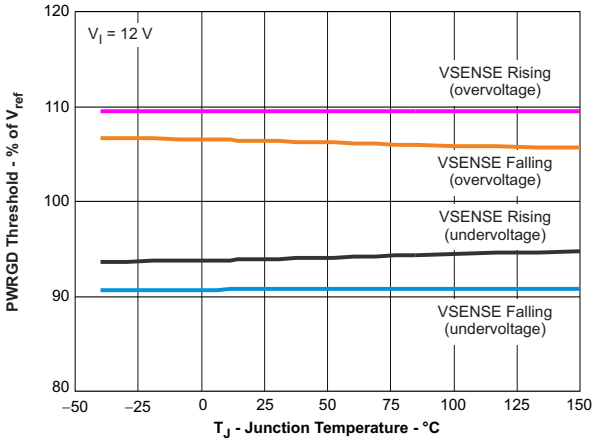


Figure 12. PWRGD Threshold vs Temperature

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Typical Characteristics (continued)

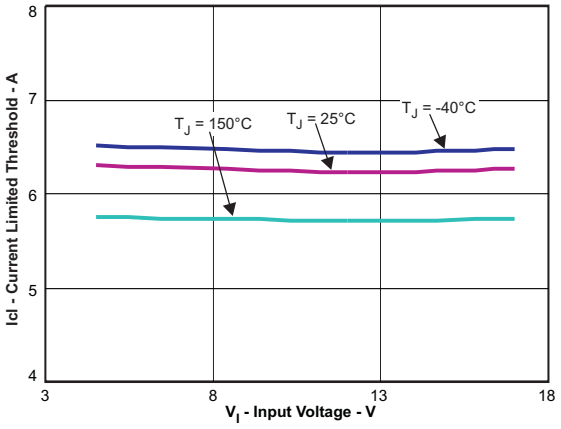


Figure 13. High-Side Current Limit Threshold vs Input Voltage

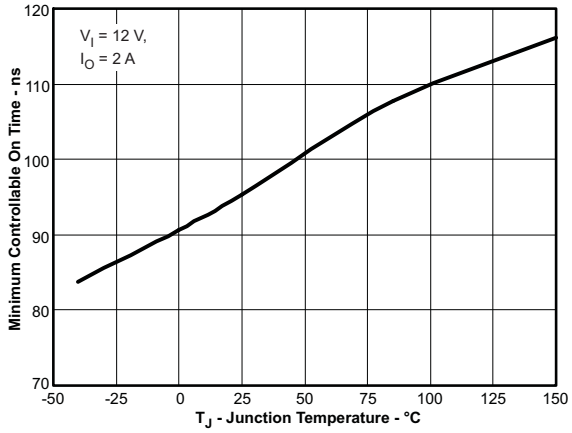


Figure 14. Minimum Controllable On-Time vs Temperature

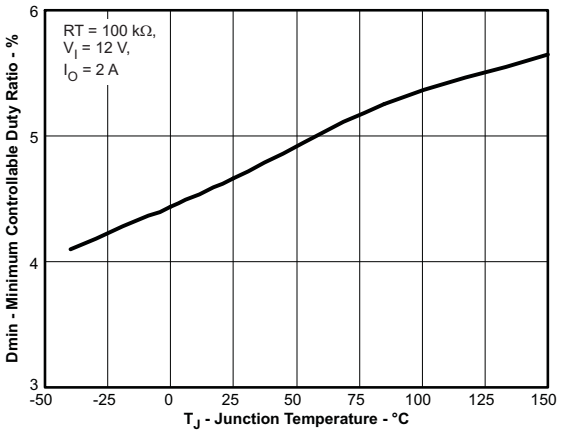


Figure 15. Minimum Controllable Duty Ratio vs Junction Temperature

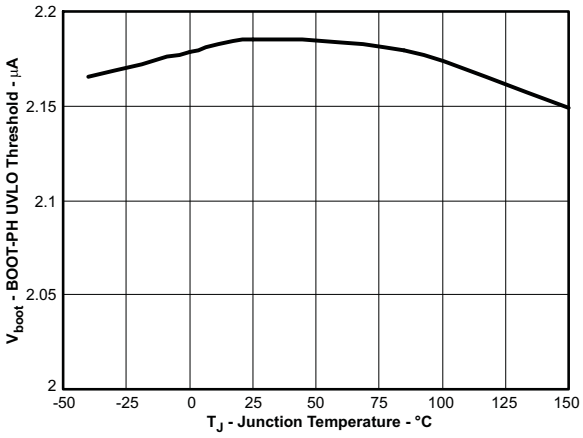


Figure 16. BOOT-PH UVLO Threshold vs Temperature

7 Detailed Description

7.1 Overview

The device is a 17-V, 3-A, synchronous step-down (buck) converter with two integrated N-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which also simplifies external frequency compensation. The wide switching frequency of 200 to 1200 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device also has an internal phase lock loop (PLL) controlled by the RT/CLK pin that can be used to synchronize the switching cycle to the falling edge of an external system clock.

The device has been designed for safe monotonic startup into prebiased loads. The default start up is when VIN is typically 4.0 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage UVLO with two external resistors. In addition, the EN pin can be left floating for the device to automatically start with the internal pullup current. The total operating current for the device is approximately 600 µA when not switching and under no load. When the device is disabled, the supply current is typically less than 2 µA.

The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 3 A. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by a BOOT to PH UVLO (BOOT-PH UVLO) circuit allowing PH pin to be pulled low to recharge the boot capacitor. The device can operate at 100% duty cycle, as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold, which is typically 2.1 V. The output voltage can be stepped down to as low as the 0.8-V voltage reference (Vref).

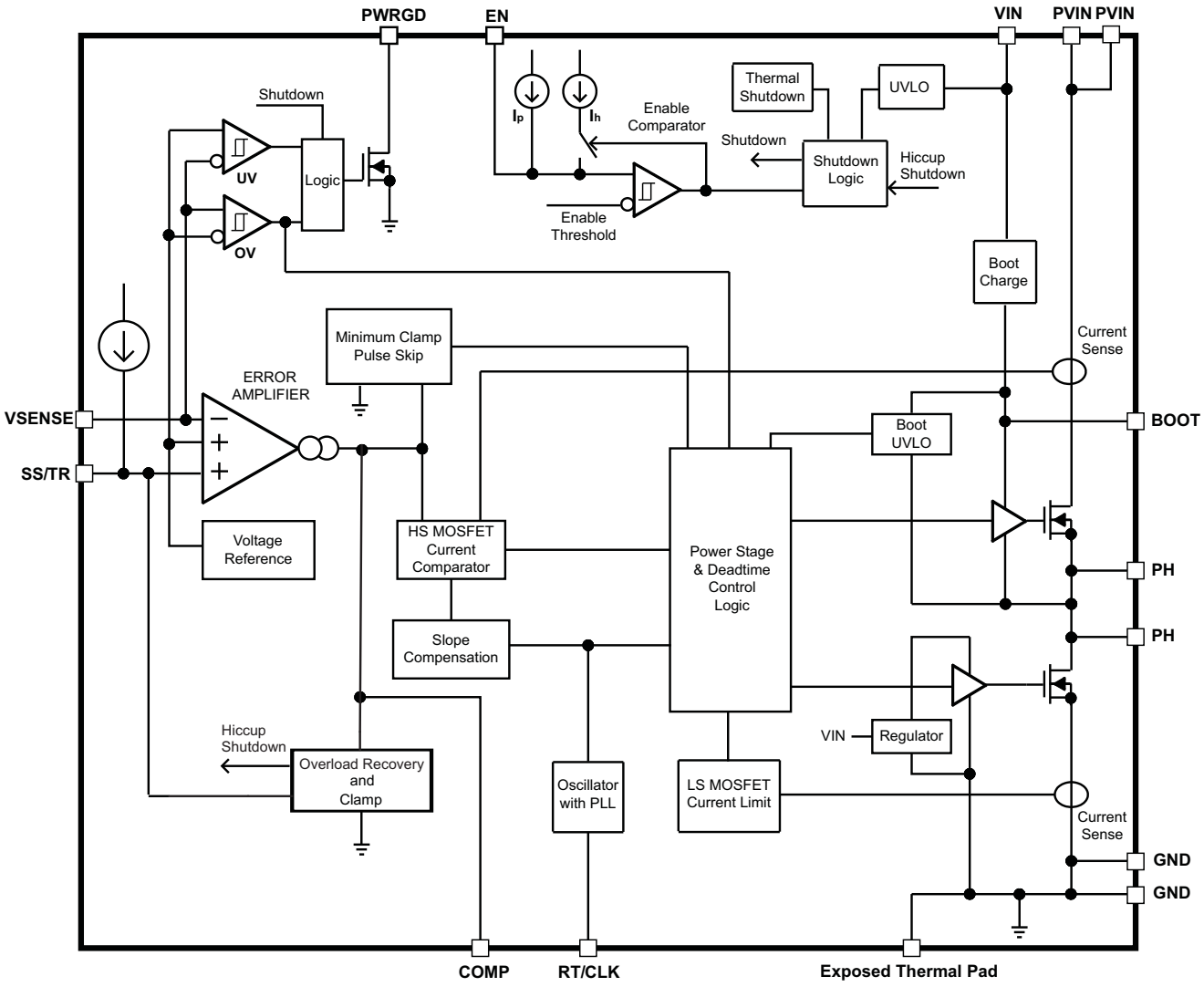
The device has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open drain MOSFET which is pulled low when the VSENSE pin voltage is less than 91% or greater than 109% of the reference voltage Vref and floats high when the VSENSE pin voltage is 94% to 106% of the Vref.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be attached to the pin for slow-start or critical power supply sequencing requirements.

The device is protected from output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the Vref. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. If the overcurrent condition has lasted for more than the hiccup wait time, the device will shut down and restart after the hiccup time. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow-start circuit automatically when the junction temperature drops 10°C typically below the thermal shutdown trip point.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The device uses adjustable, fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which is compared to the high-side power switch current. When the power switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

7.3.2 Continuous Current Mode Operation (CCM)

As a synchronous buck converter, the device normally works in CCM under all load conditions.

7.3.3 VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system.

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Feature Description (continued)

If tied together, the input voltage for VIN and PVIN can range from 4.5 to 17 V. If using the VIN separately from PVIN, the VIN pin must be between 4.5 and 17 V, and the PVIN pin can range from as low as 1.6 to 17 V. A voltage divider connected to the EN pin can adjust either input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior.

7.3.4 Voltage Reference

The voltage reference system produces a precise voltage reference by scaling the output of a temperature stable bandgap circuit.

7.3.5 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. TI recommends to use 1% tolerance or better divider resistors. Referring to the application schematic of Figure 34, start with a 10-kΩ resistor for R9 and use Equation 1 to calculate R8. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R8 = \frac{Vout - Vref}{Vref} R9 \quad (1)$$

where

- Vref = 0.8 V

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. See *Minimum Output Voltage* and *Bootstrap Voltage (BOOT) and Low Dropout Operation* for more information.

7.3.6 Safe Start-up into Prebiased Outputs

The device is designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased startup, the low-side MOSFET is not allowed to turn on until the SS/TR pin voltage is higher than the VSENSE pin voltage.

7.3.7 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 1300 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

7.3.8 Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents subharmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

7.3.9 Enable and Adjusting UVLO

The EN pin provides an electrical on/off control of the device. After the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low Iq state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use an open-drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150 mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN pin, in split rail applications, then the EN pin can be configured as shown in Figure 17, Figure 18, or Figure 19. When using the external UVLO function, TI recommends to set the hysteresis to be >500 mV.

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Feature Description (continued)

The EN pin has a small pullup current Ip which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2 and Equation 3.

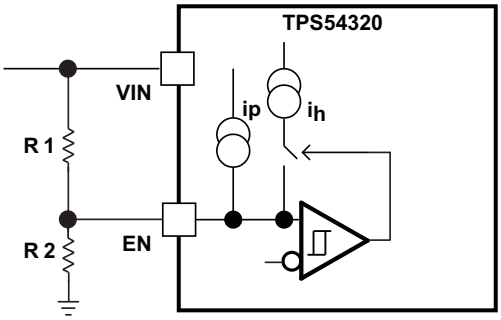


Figure 17. Adjustable VIN UVLO

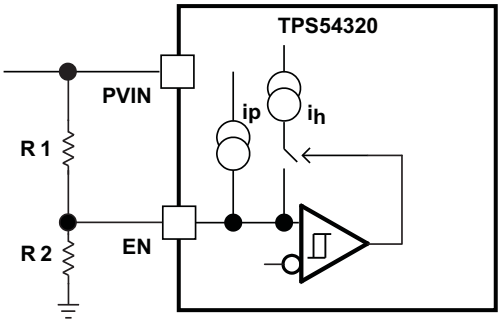


Figure 18. Adjustable PVIN UVLO, VIN ≥ 4.5 V

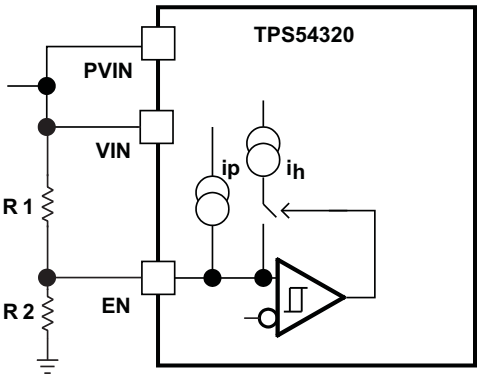


Figure 19. Adjustable VIN and PVIN UVLO

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1-\frac{V_{ENFALLING}}{V_{ENRISING}}\right)+I_h}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (2)$$

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Feature Description (continued)

where

- I_h = 3.4 µA
- I_p = 1.15 µA
- $V_{ENRISING}$ = 1.21 V
- $V_{ENFALLING}$ = 1.17 V (3)

7.3.10 Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The device has an internal pullup current source of 2.3 µA that charges the external slow-start capacitor. Equation 4 shows the calculations for the slow-start time (t_{SS}, 10% to 90%) and slow-start capacitor (Css). The voltage reference (Vref) is 0.8 V and the slow-start charge current (Iss) is 2.3 µA.

$$t_{SS}\ (ms) = \frac{Css\ (nF) \times Vref\ (V)}{Iss\ (\mu A)} \quad (4)$$

When the input UVLO is triggered, the EN pin is pulled below 1.21 V or a thermal shutdown event occurs; the device stops switching and enters low current operation. At the subsequent power-up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

7.3.11 Power Good (PWRGD)

The PWRGD pin is an open-drain output. When the VSENSE pin is between 94% and 106% of the internal voltage reference, the PWRGD pin pull-down is deasserted and the pin floats. TI recommends to use a pullup resistor between the values of 10 and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state when the VIN input voltage is >1 V, but with reduced current sinking capability. The PWRGD achieves full current sinking capability when the VIN input voltage is above 4.5 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low, or the SS/TR pin is below 1.2 V typically.

7.3.12 Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve dropout, the device is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than the BOOT-PH UVLO threshold which is typically 2.1 V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails, 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

Never use a boot resistor in series with the boot capacitor on the TPS54320.

7.3.13 Sequencing (SS/TR)

Many of the common power-supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins.

Figure 20 shows the sequential method using two TPS54320 devices. The power good of the first device is coupled to the EN pin of the second device which enables the second power supply once the primary supply reaches regulation. Figure 21 shows the results of Figure 20.

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Feature Description (continued)

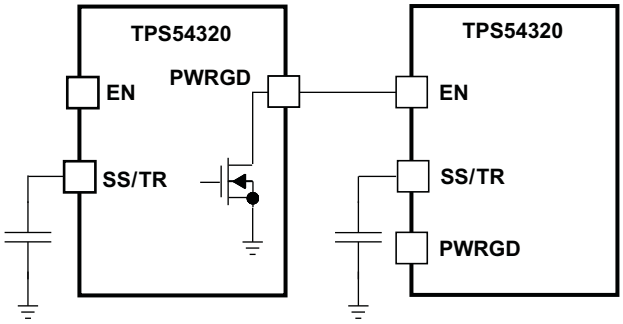


Figure 20. Sequential Start-Up Sequence

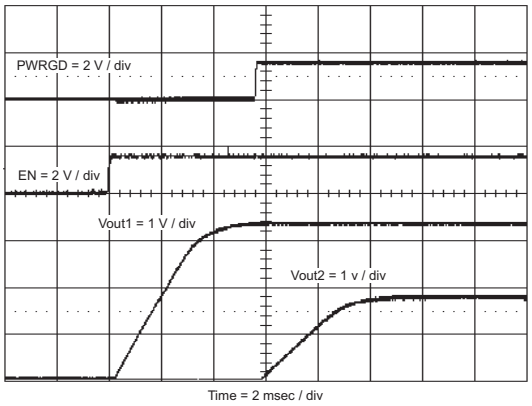


Figure 21. Sequential Start-Up Using EN and PWRGD

Figure 22 shows the method implementing ratiometric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup current source must be doubled in Equation 4. Figure 23 shows the results of Figure 22.

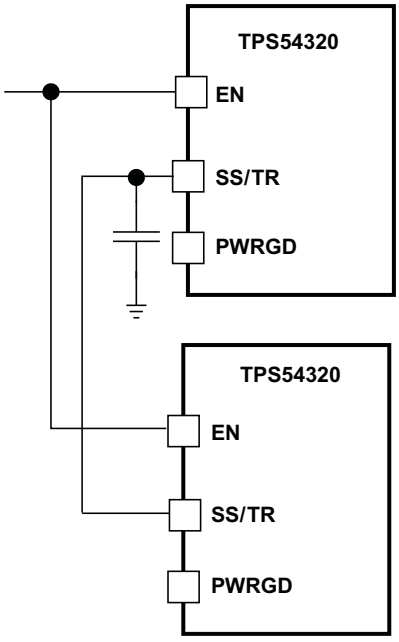


Figure 22. Ratiometric Start-Up Sequence

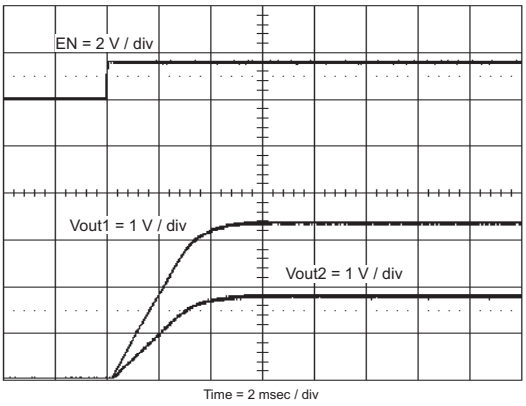


Figure 23. Ratiometric Startup Using Coupled SS/TR Pins

Ratiometric and simultaneous power-supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 24 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 5 and Equation 6, the tracking resistors can be calculated to initiate the Vout2 slightly before, after, or at the same time as Vout1. Equation 7 is the voltage difference between Vout1 and Vout2.

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Feature Description (continued)

To design a ratiometric start-up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 5 and Equation 6 for ΔV. Equation 7 results in a positive number for applications where the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved. Figure 25 and Figure 26 show the results for positive ΔV and negative ΔV respectively.

The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset, 29 mV) in the slow-start circuit and the offset created by the pullup current source (Iss, 2.3 μA) and tracking resistors, the Vssoffset and Iss are included as variables in the equations. Figure 27 shows the result when ΔV = 0 V.

To ensure proper operation of the device, the calculated R1 value from Equation 5 must be greater than the value calculated in Equation 8.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \quad (5)$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \quad (6)$$

$$\Delta V = Vout1 - Vout2 \quad (7)$$

$$R1 > 2800 \times Vout1 - 180 \times \Delta V \quad (8)$$

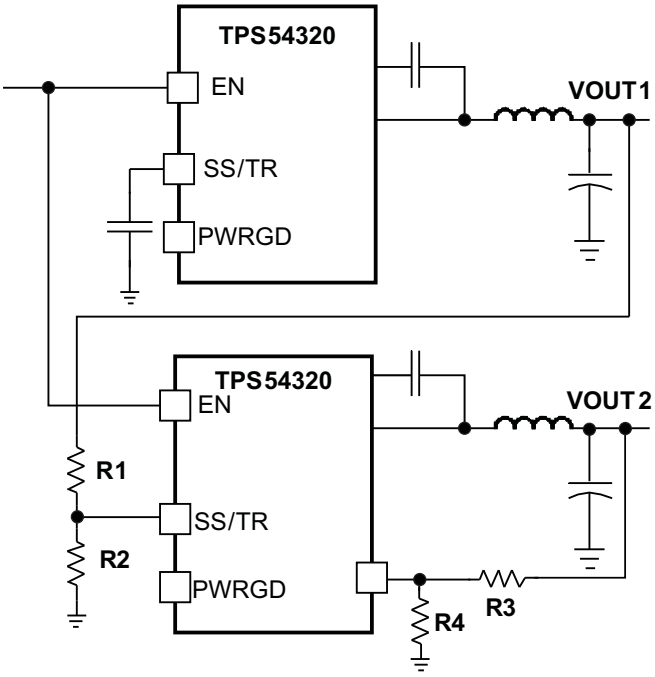


Figure 24. Ratiometric and Simultaneous Startup Sequence

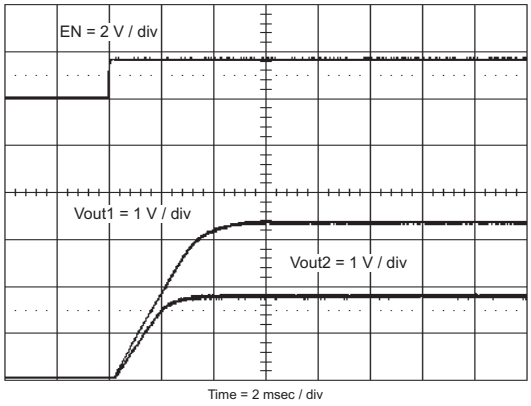


Figure 25. Ratiometric Startup With Vout1 Leading Vout2

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Feature Description (continued)

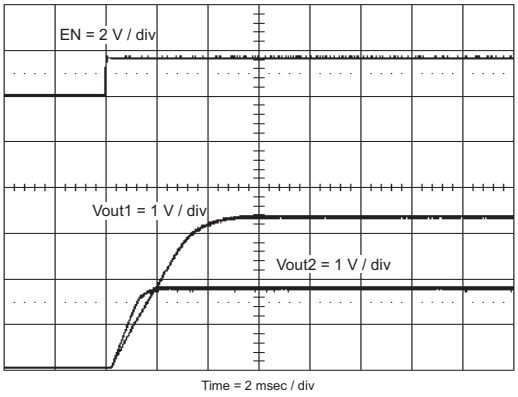


Figure 26. Ratiometric Startup With Vout2 Leading Vout1

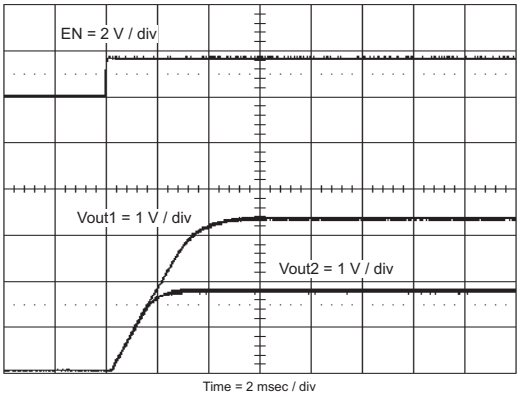


Figure 27. Simultaneous Startup

7.3.14 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

7.3.15 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and low-side MOSFET.

7.3.15.1 High-Side MOSFET Overcurrent Protection

High-side MOSFET overcurrent protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET on a cycle-by-cycle basis. If this current exceeds the current limit threshold, the high-side MOSFET is turned off for the remainder of that switching cycle.

During normal operation, the device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET, on a cycle-by-cycle basis. Each cycle, the switch current and the current reference generated by the COMP pin voltage are compared. When the peak switch current intersects the current reference, the high-side switch is turned off.

7.3.15.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

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Feature Description (continued)

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time, which is set for 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.3.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 165°C typically.

7.3.17 Small Signal Model for Loop Response

Figure 28 shows an equivalent model for the device's control loop, which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Roea (2.38 MΩ) and capacitor Coea (20.7 pF) model the open-loop gain and frequency response of the error amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b shows the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

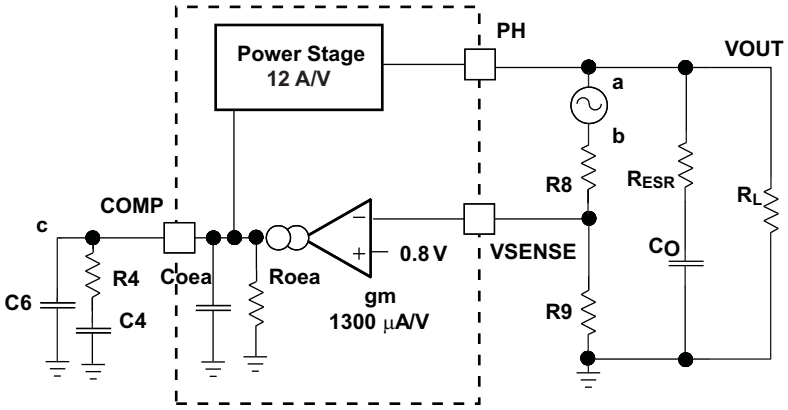


Figure 28. Small Signal Model for Loop Response

7.3.18 Simple Small Signal Model for Peak Current Mode Control

Figure 29 is a simple small signal model that can be used to understand how to design the frequency compensation. The device's power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 9 and consists of a dc gain, one dominant pole, and one equivalent series resistance (ESR) zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 28) is the power stage transconductance (gm_{ps}), which is 12 A/V for the device. The DC gain of the power stage is the product of gm_{ps} and the load resistance (R_L), as shown in Equation 10 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 11). The combined effect is highlighted by the dashed line in Figure 30. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation.

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Feature Description (continued)

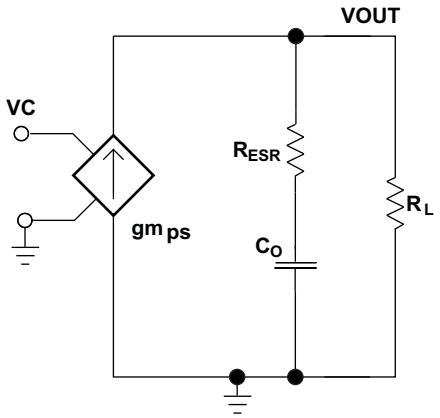


Figure 29. Simplified Small Signal Model for Peak Current Mode Control

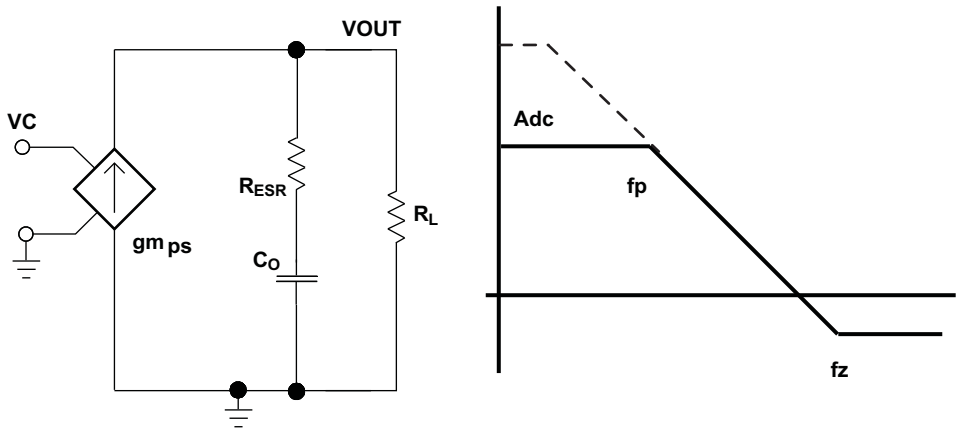


Figure 30. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (9)$$

$$Adc = gm_{ps} \times R_L \quad (10)$$

$$fp = \frac{1}{C_O \times R_L \times 2\pi} \quad (11)$$

$$fz = \frac{1}{C_O \times R_{ESR} \times 2\pi} \quad (12)$$

where

- gm_{ea} is the GM amplifier gain (1300 µA/V).
- gm_{ps} is the power stage gain (12 A/V).
- R_L is the load resistance.
- C_O is the output capacitance.
- R_{ESR} is the equivalent series resistance of the output capacitor.

Feature Description (continued)

7.3.19 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 31. In Type 2A, one additional high-frequency pole, C6, is added to attenuate high frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The design guidelines below are provided for advanced users who prefer to compensate using the general method. The following equations only apply to designs which have ESR zero above the bandwidth of the control loop. This is usually true with ceramic output capacitors.

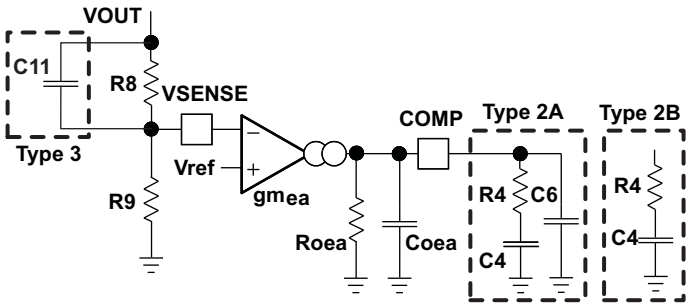


Figure 31. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, f_c. A good starting point is 1/10 of the switching frequency, $f$sw.
2. R4 can be determined by:

$$R4 = \frac{2\pi \times fc \times VOUT \times Co}{gm_{ea} \times Vref \times gm_{ps}} \quad (13)$$

   where
   - gm_{ea} is the GM amplifier gain (1300 µA/V).
   - gm_{ps} is the power stage gain (12 A/V).
   - Vref is the reference voltage (0.8 V).

3. Place a compensation zero at the dominant pole: $\left(fp = \frac{1}{C_O \times R_L \times 2\pi} \right)$

   C4 can be determined by:

$$C4 = \frac{R_L \times Co}{R4} \quad (14)$$

4. C6 is optional. It can be used to cancel the zero from the ESR of the output capacitor, C_O.

$$C6 = \frac{R_{ESR} \times Co}{R4} \quad (15)$$

5. Type III compensation can be implemented with the addition of one capacitor, C11. This allows for slightly higher loop bandwidths and higher phase margins. If used, C11 is calculated from Equation 16.

$$C11 = \frac{1}{(2 \cdot \pi \cdot R8 \cdot fc)} \quad (16)$$

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7.4 Device Functional Modes

7.4.1 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes.

In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200 to 1200 kHz by using a maximum of 240 kΩ and minimum of 40.2 kΩ respectively. In CLK mode, an external clock is connected directly to the RT/CLK pin. The device is synchronized to the external clock frequency with a PLL.

The CLK mode overrides the RT mode. The device is able to detect the proper mode automatically and switch from the RT mode to CLK mode.

7.4.2 Adjustable Switching Frequency (RT Mode)

To determine the RT resistance for a given switching frequency, use Equation 17 or the curve in Figure 32. To reduce the solution size, one would set the switching frequency as high as possible, but consider the tradeoffs of the supply efficiency and minimum controllable on-time.

$$Rrt(k\Omega) = 60281 \cdot Fsw\left(kHz\right)^{-1.033} \quad (17)$$

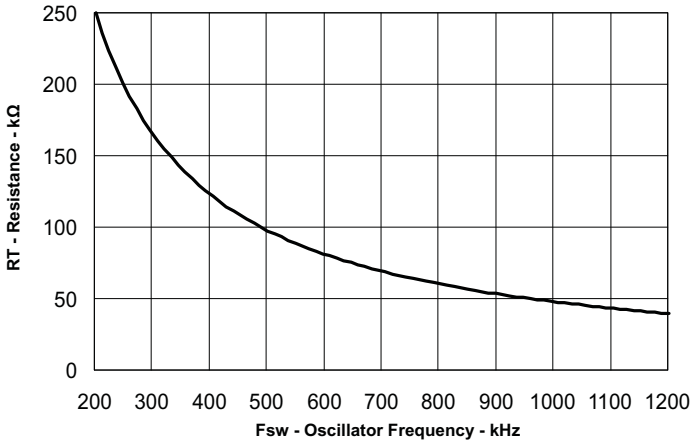


Figure 32. RT Set Resistor vs Switching Frequency

7.4.3 Synchronization (CLK Mode)

An internal PLL has been implemented to allow synchronization between 200 kHz and 1.2 MHz, and to easily switch from RT mode to CLK mode.

To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin.

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Device Functional Modes (continued)

In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 33. Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the SYNC pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from the RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. TI does not recommend to switch from the CLK mode back to the RT mode, because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by RT resistor.

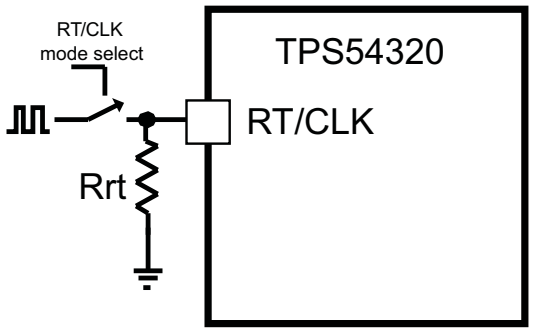


Figure 33. Works With Both RT Mode and CLK Mode

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54320 device is an integrated synchronous step-down DC-DC converter. The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 3 A.

8.2 Typical Application

The application schematic of Figure 34 was developed to meet the requirements. This circuit is available as the TPS54320EVM-513 evaluation module. The design procedure is provided in the following sections.

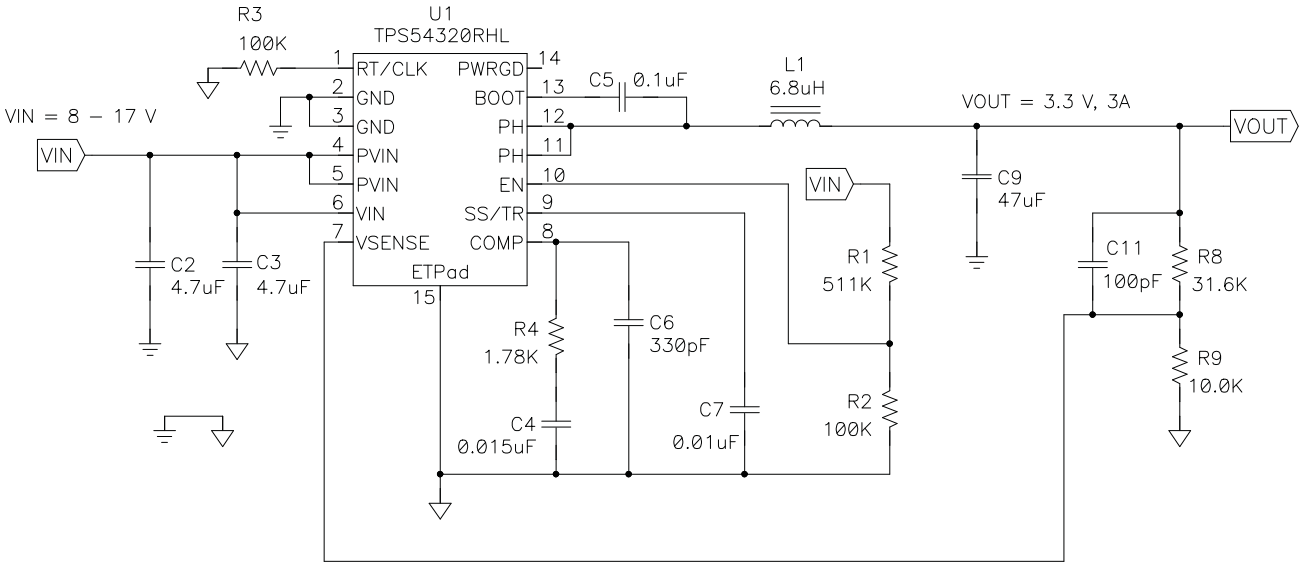


Figure 34. Typical Application Circuit

8.2.1 Design Requirements

This example details the design of a high-frequency switching regulator using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, start with the following known parameters:

Table 1. Design Parameters

PARAMETER	VALUE
Output voltage	3.3 V
Output current	3 A
Transient response 0.75-A (25%) load step	ΔV_{OUT} = 4%
Input voltage	12 V nominal, 8 to 17 V
Output voltage ripple	1% (33 mV_{PP})
Start input voltage (rising Vin)	6.806 V
Stop input voltage (falling Vin)	4.824 V
Switching frequency	480 kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes additional switching losses, which negatively impact the converter's efficiency and thermal performance. In this design, a moderate switching frequency of 480 kHz is selected to achieve both a small solution size and a high-efficiency operation. This frequency is set using the resistor at the RT/CLK pin (R3). Using Equation 17, the resistance required for a switching frequency of 480 kHz is 102 kΩ. A 100-kΩ resistor is used for this design.

8.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, Equation 18 is used. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Usually, the inductor ripple value is at the discretion of the designer; however, KIND is normally from 0.2 to 0.4 for the majority of applications.

$$L1 = \frac{Vinmax - Vout}{Iout \cdot KIND} \cdot \frac{Vout}{Vinmax \cdot fsw} \tag{18}$$

For this design example using KIND = 0.3, the inductor value is calculated to be 6.2 µH. The nearest standard value of 6.8 µH was chosen. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The inductor ripple current, RMS current, and peak inductor current can be found from Equation 19, Equation 20, and Equation 21.

$$Iripple = \frac{Vinmax - Vout}{L1} \cdot \frac{Vout}{Vinmax \cdot fsw} \tag{19}$$

$$ILrms = \sqrt{Iout^2 + \frac{1}{12} \cdot \left(\frac{Vout \cdot (Vinmax - Vout)}{Vinmax \cdot L1 \cdot fsw} \right)^2} \tag{20}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{21}$$

For this design, the inductor ripple current is 815 mA, the RMS inductor current is 3.01 A, and the peak inductor current is 3.41 A. A 6.8-µH TDK VLP8040 series inductor was chosen for its small size and low DCR. It has a saturation current rating of 3.6 A and a RMS current rating of 4 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

8.2.2.3 Output Capacitor Selection

The three primary considerations for selecting the value of the output capacitor are:

- Minimum capacitance to meet the load transient requirement
- Minimum capacitance to meet the output voltage ripple requirement
- Maximum ESR to meet the output voltage ripple requirement

The output capacitor must be selected based on the most stringent of these three criteria.

The first criterion is the desired response to a large change in the load current. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning

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from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 22 shows the minimum output capacitance necessary to accomplish this.

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout}$$

where

- ΔIout is the change in output current.
- $f$sw is the regulator's switching frequency.
- ΔVout is the allowable change in the output voltage. (22)

For this example, the transient load response is specified as a 4% change in Vout for a load step of 0.75 A. Using these numbers (ΔI_{OUT} = 0.75 A and ΔVout = 0.04 × 3.3 = 0.132 V) gives a minimum capacitance of 23.7 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 23 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where $f$sw is the switching frequency, Voripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 33 mV. Under this requirement, Equation 23 yields 6.4 µF.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{Voripple}{Iripple}} \quad (23)$$

Equation 24 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 24 indicates the ESR should be less than 40 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 40 mΩ.

$$Resr < \frac{Voripple}{Iripple} \quad (24)$$

The capacitance of ceramic capacitors is highly dependent on the DC output voltage. Equation 25 is used to select output capacitors based on their voltage rating. For 6.3-V ceramic capacitors, the minimum capacitance that meets the load step specification is 49.7 µF. For this example, one 47-µF, 6.3-V, X5R ceramic capacitor with 4 mΩ of ESR is used.

$$C = \frac{(Ceff \times Vrating)}{(Vrating - Vout)} \quad (25)$$

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. The designer must specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 26 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 26 yields 235 mA.

$$Icorms = \frac{Vout \cdot (Vinmax - Vout)}{\sqrt{12} \cdot Vinmax \cdot L1 \cdot fsw} \quad (26)$$

8.2.2.4 Input Capacitor Selection

The TPS54320 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of 4.7 µF on each input voltage rail. In some applications, additional bulk capacitance may also be required for the PVIN input. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54320. The input ripple current for this design, using Equation 27, is 1.48 A.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vinmin} \cdot \frac{(Vinmin - Vout)}{Vinmin}} \quad (27)$$

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The value of a ceramic capacitor varies significantly over both temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because of the high capacitance to volume ratio and stability over temperature. The capacitance value of a capacitor decreases as the DC bias across it increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this example, two 4.7-µF 25-V capacitors were used in parallel as the VIN and PVIN inputs are tied together, so the TPS54320 may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 28. Using the design example values, Ioutmax = 3 A, C_{IN} = 9.4 µF, $f$sw = 480 kHz, Equation 28 yields an input voltage ripple of 166 mV.

$$\Delta Vin = \frac{Ioutmax \cdot 0.25}{Cin \cdot f sw} \tag{28}$$

8.2.2.5 Slow-Start Capacitor Selection

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large and requires a large amount of current to charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may either make the TPS54320 reach the current limit or the excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft-start capacitor value can be calculated using Equation 29. The example circuit has the soft-start time set to an arbitrary value of 3.5 ms, which requires a 10-nF capacitor. In the TPS54320, Iss is 2.3 µA and Vref is 0.8 V.

$$C5(nF) = \frac{Tss(ms) \text{ x } Iss(\mu A)}{Vref(V)} \tag{29}$$

8.2.2.6 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

8.2.2.7 UVLO Set Point

The UVLO can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin of the TPS54320 and R2 is connected between EN and GND. The UVLO has two thresholds, one for power-up when the input voltage is rising and one for power-down or brownouts when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 6.806 V (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.824 V (UVLO stop or disable). Equation 2 and Equation 3 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified, the nearest standard resistor value for R1 is 511 kΩ and for R2 is 100 kΩ.

8.2.2.8 Output Voltage Feedback Resistor Selection

The resistor divider network, R8 and R9, is used to set the output voltage. For this example design, 10 kΩ was selected for R9. Using Equation 30, R8 is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ.

$$R8 = \frac{Vout - Vref}{Vref} R9 \tag{30}$$

8.2.2.8.1 Minimum Output Voltage

Due to the internal design of the TPS54320, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, the output voltage may be limited by the minimum controllable on-time. The minimum output voltage in this case is given by Equation 31.

$$V_{OUT}min = Ontimemin \times Fsmax \left(V_{IN}max + I_{OUT}min \left(RDS2min - RDS1min\right)\right) - I_{OUT}min \left(R_L + RDS2min\right)$$

where

- V_{OUT}min = Minimum achievable output voltage

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- Ontimemin = Minimum controllable on-time (135 ns maximum)
- Fsmax = Maximum switching frequency including tolerance
- V_{IN}max = Maximum input voltage
- I_{OUT}min = Minimum load current
- RDS1min = Minimum high-side MOSFET on resistance (57 mΩ typical)
- RDS2min = Minimum low-side MOSFET on resistance (50 mΩ typical)
- R_L = Series resistance of output inductor (31)

8.2.2.9 Compensation Component Selection

There are several industry techniques used to compensate DC/DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. The method presented here ignores the effects of the slope compensation that is internal to the TPS54320. Since the slope compensation is ignored, the actual crossover frequency is usually lower than the crossover frequency used in the calculations. Use SwitcherPro software for a more accurate design.

Type III compensation is used to achieve a high-bandwidth, high-phase margin design. This design targets a crossover frequency (bandwidth) of 48 kHz (1/10 of the switching frequency). Using Equation 32 and Equation 33, the power stage pole and zero are calculated at 6.46 and 1778 kHz, respectively. For the output capacitance, C_O, use a derated value of 22.4 µF.

$$fpmod = \frac{Iout}{2 \cdot \pi \cdot Vout \cdot Co} \quad (32)$$

$$fzmod = \frac{1}{2 \cdot \pi \cdot RESR \cdot Co} \quad (33)$$

Now the compensation components can be calculated. First, calculate the value for R4 which sets the gain of the compensated network at the crossover frequency. Use Equation 34 to determine the value of R4.

$$R4 = \frac{2\pi \cdot fc \cdot Vout \cdot Co}{gm_{ea} \cdot Vref \cdot gm_{ps}} \quad (34)$$

Next calculate the value of C4. Together with R4, C4 places a compensation zero at the modulator pole frequency. Use Equation 35 to determine the value of C4.

$$C4 = \frac{Vout \cdot Co}{Iout \cdot R4} \quad (35)$$

Using Equation 34 and Equation 35, the standard values for R4 and C4 are 1.78 kΩ and 0.015 µF. The next higher standard value for C4 is selected to give a compensation zero that is slightly lower in frequency than the power stage pole.

To provide a zero around the crossover frequency to boost the phase at crossover, a capacitor (C11) is added parallel to R8. The value of this capacitor is given by Equation 36. The nearest standard value for C11 is 100 pF.

$$C11 = \frac{1}{2 \cdot \pi \cdot R8 \cdot fc} \quad (36)$$

Use of the feed-forward capacitor, C11, creates a low-AC impedance path from the output voltage to the VSENSE input of the IC that can couple noise at the switching frequency into the control loop. TI does not recommend use of a feed-forward capacitor for high-output voltage ripple designs (greater than 15-mV peak to peak at the VSENSE input) operating at duty cycles of less than 30%. When using the feed-forward capacitor, C11, always limit the closed loop bandwidth to no more than 1/10 of the switching frequency, $f$sw.

An additional high-frequency pole can be used if necessary by adding a capacitor in parallel with the series combination of R4 and C4. Equation 37 gives the pole frequency. This pole is set at roughly half of the switching frequency (of 480 kHz) by use of a 330-pF capacitor for C6. This helps attenuate any high-frequency signals that might couple into the control loop.

$$fp = \frac{1}{2 \cdot \pi \cdot R4 \cdot C6} \quad (37)$$

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8.2.3 Application Curves

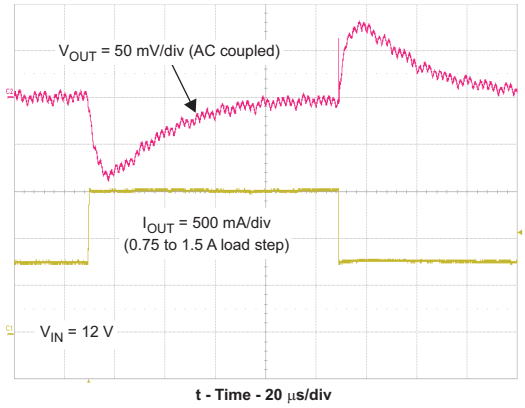


Figure 35. Load Transient

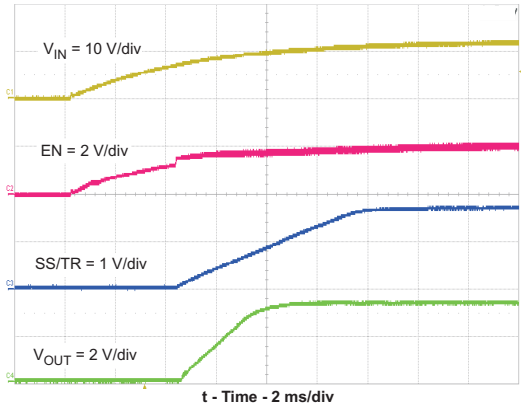


Figure 36. Startup With VIN (1.1-Ω Load)

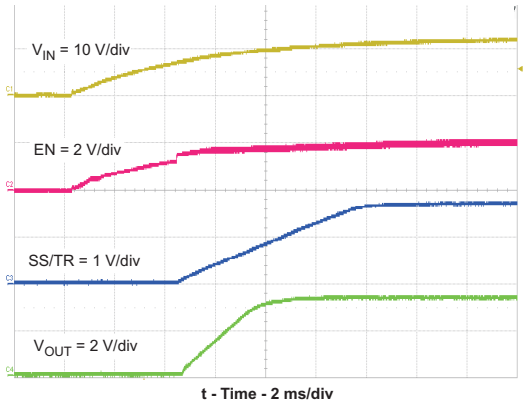


Figure 37. Startup With VIN (No Load)

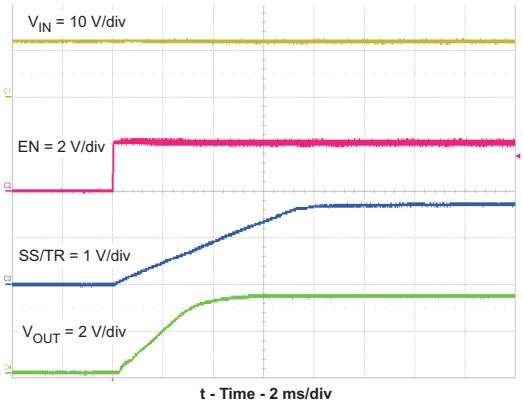


Figure 38. Startup With EN (1.1-Ω Load)

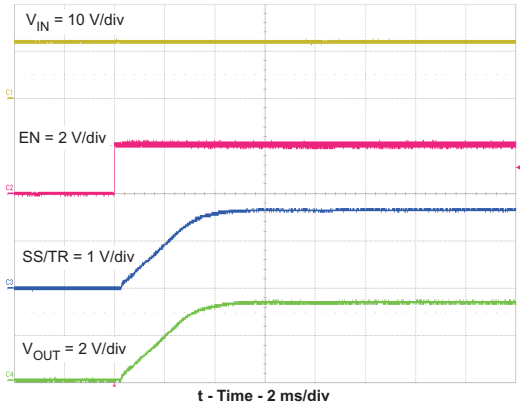


Figure 39. Startup With EN (No Load)

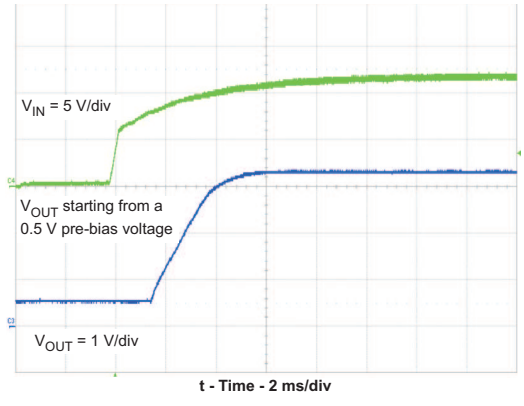


Figure 40. Startup With Prebias on VIN (1.1-Ω Load)

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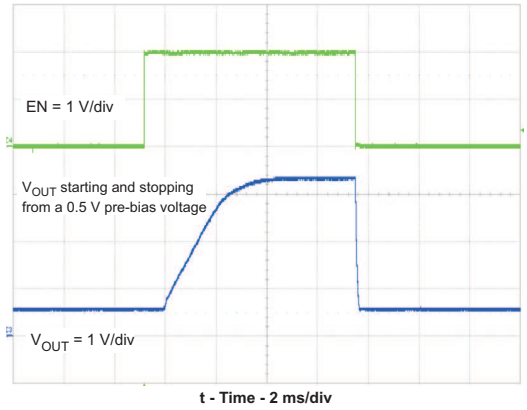


Figure 41. Startup and Shutdown With Prebias on EN (1.1-Ω Load)

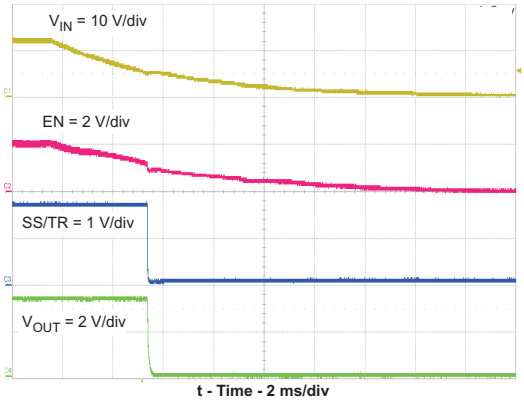


Figure 42. Shutdown With VIN (1.1-Ω Load)

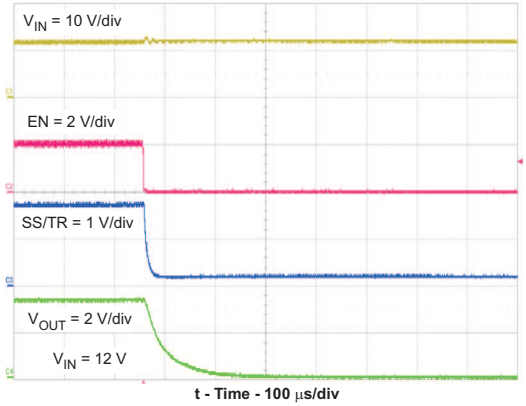


Figure 43. Shutdown With EN (1.1-Ω Load)

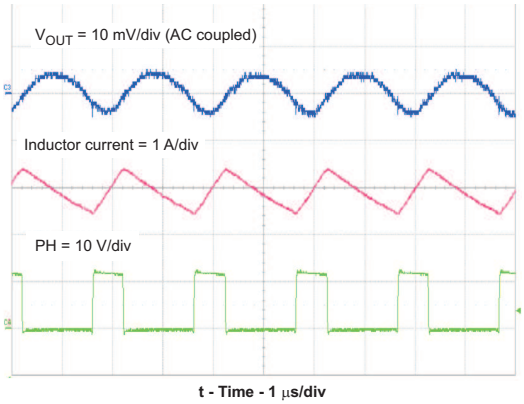


Figure 44. Output Voltage Ripple (1.1-Ω Load)

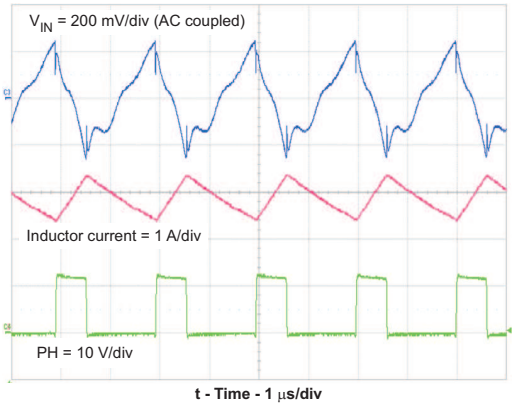


Figure 45. Input Voltage Ripple (1.1-Ω Load)

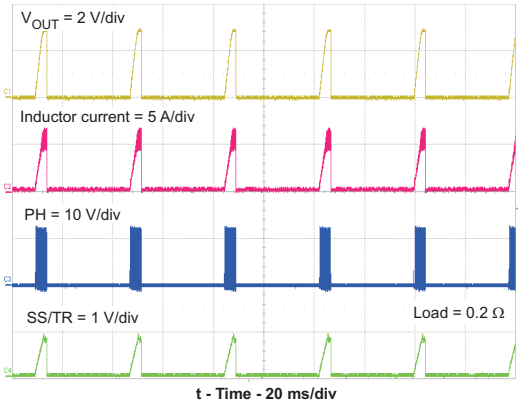


Figure 46. Overcurrent Hiccup Mode

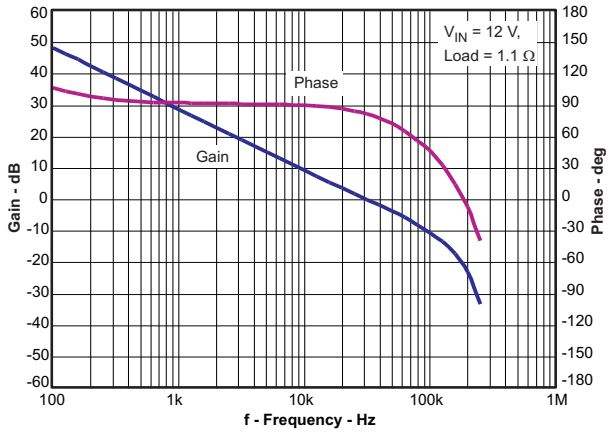


Figure 47. Closed Loop Response

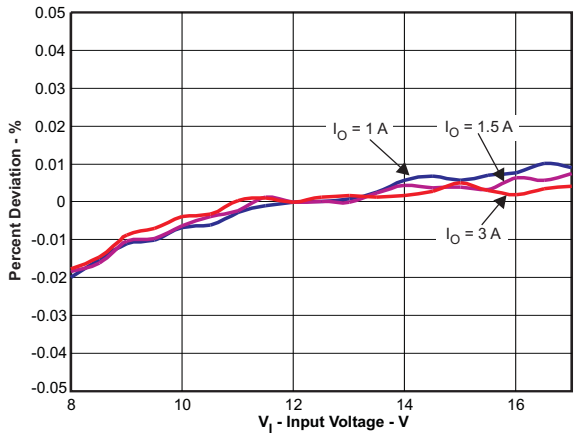


Figure 48. Line Regulation

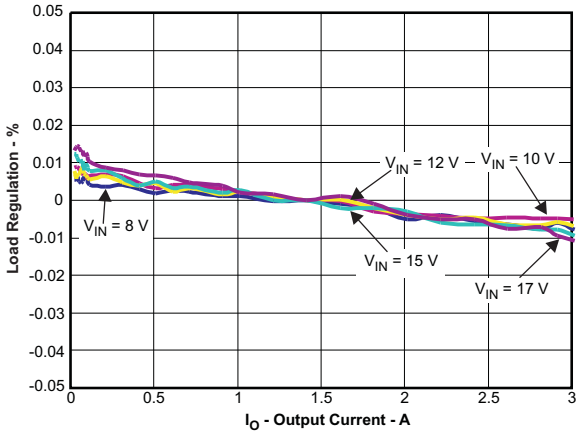


Figure 49. Load Regulation

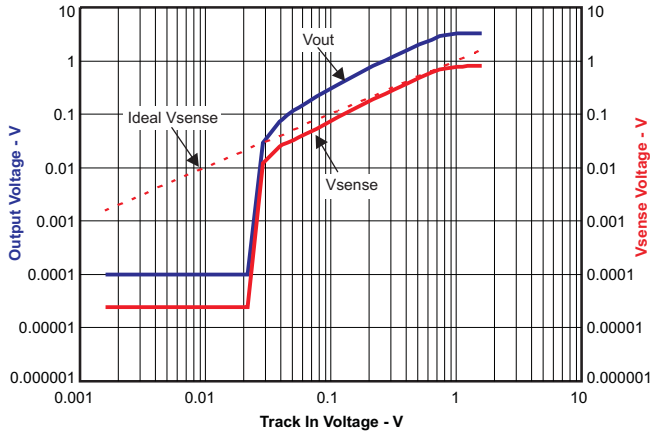


Figure 50. Tracking Performance

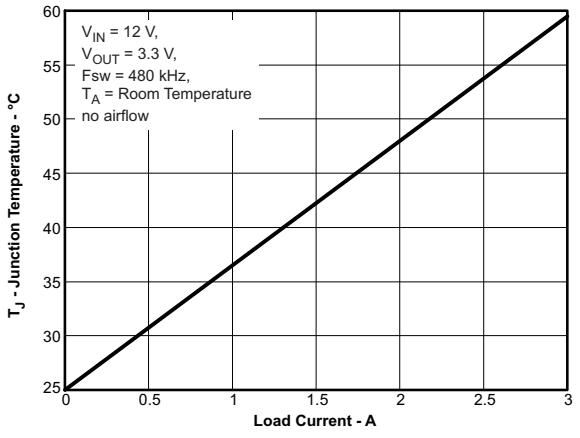


Figure 51. Maximum Ambient Temperature vs Load Current

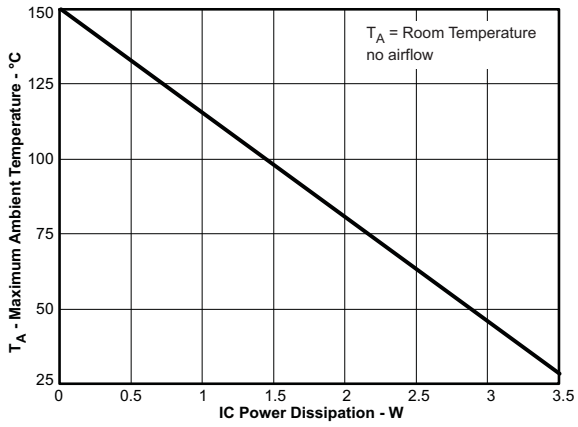


Figure 52. Maximum Ambient Temperature vs IC Power Dissipation

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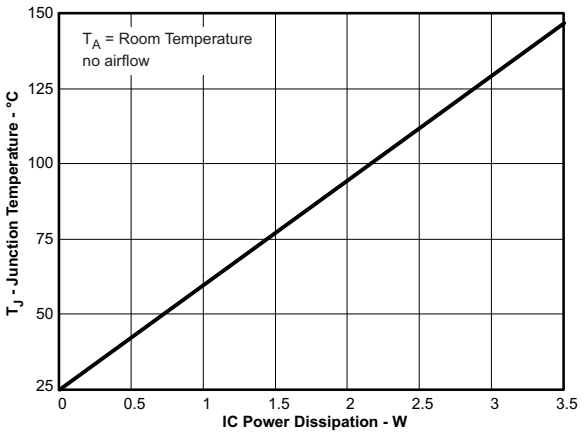


Figure 53. Junction Temperature vs IC Power Dissipation

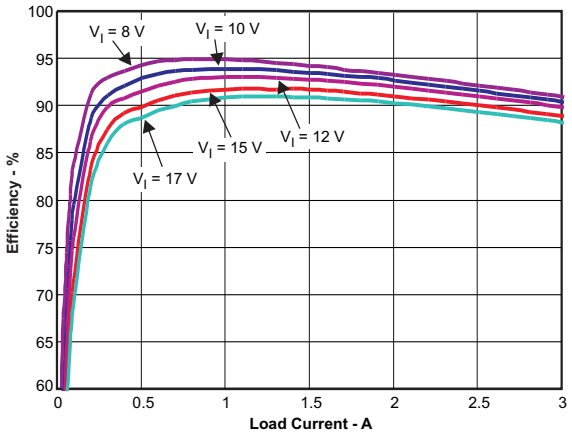
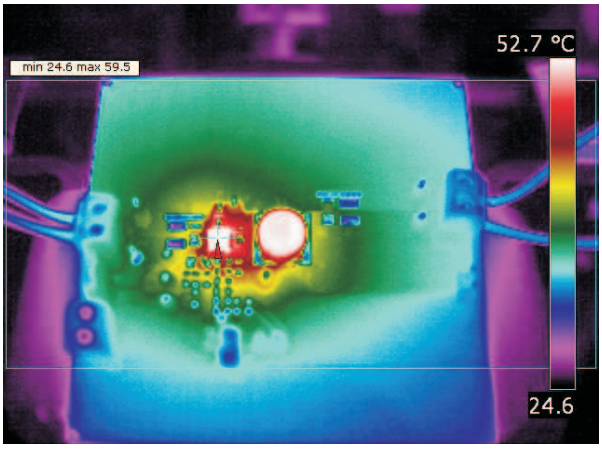


Figure 54. Efficiency vs Load Current



VIN = 12 V VOUT = 3.3 V / 3 A
T_A = Room temperature

Figure 55. Thermal Signature of TPS54320EVM-513

9 Power Supply Recommendations

The TPS54320 is designed to operate from an input voltage supply range between 4.5 and 17 V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 4.7 µF (after derating) ceramic capacitor, type X5R or better from PVIN to GND, and from VIN to GND. Additional local ceramic bypass capacitance may be required in systems with small input ripple specifications, in addition to bulk capacitance if the TPS54320 device is located more than a few inches away from its input power supply. In systems with an auxiliary power rail available, the power stage input, PVIN, and the analog power input, VIN, may operate from separate input supplies. See Figure 56 (layout recommendation) for recommended bypass capacitor placement.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. See Figure 56 for a PCB layout example. The top layer contains the main power traces for VIN, VOUT, and the PH node. Also on the top layer are connections for the remaining pins of the TPS54320 and a large top-side area filled with ground. The top layer ground area should be connected to the internal ground layer or layers using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS54320 device to provide a thermal path from the exposed thermal pad land to ground. The GND pin should be tied directly to the exposed thermal pad under the IC.

For operation at full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipating area. Several signals paths conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric. Make sure to connect this capacitor to the quiet analog ground trace rather than the power ground trace of the PVIN bypass capacitor.

Because the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path as shown. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts. However, this layout has been shown to produce good results and is meant as a guideline.

The estimated PCB area for the components used in the design of Figure 34 is 0.35 in^2 (227 mm^2). This area does not include test points or connectors.

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10.2 Layout Example

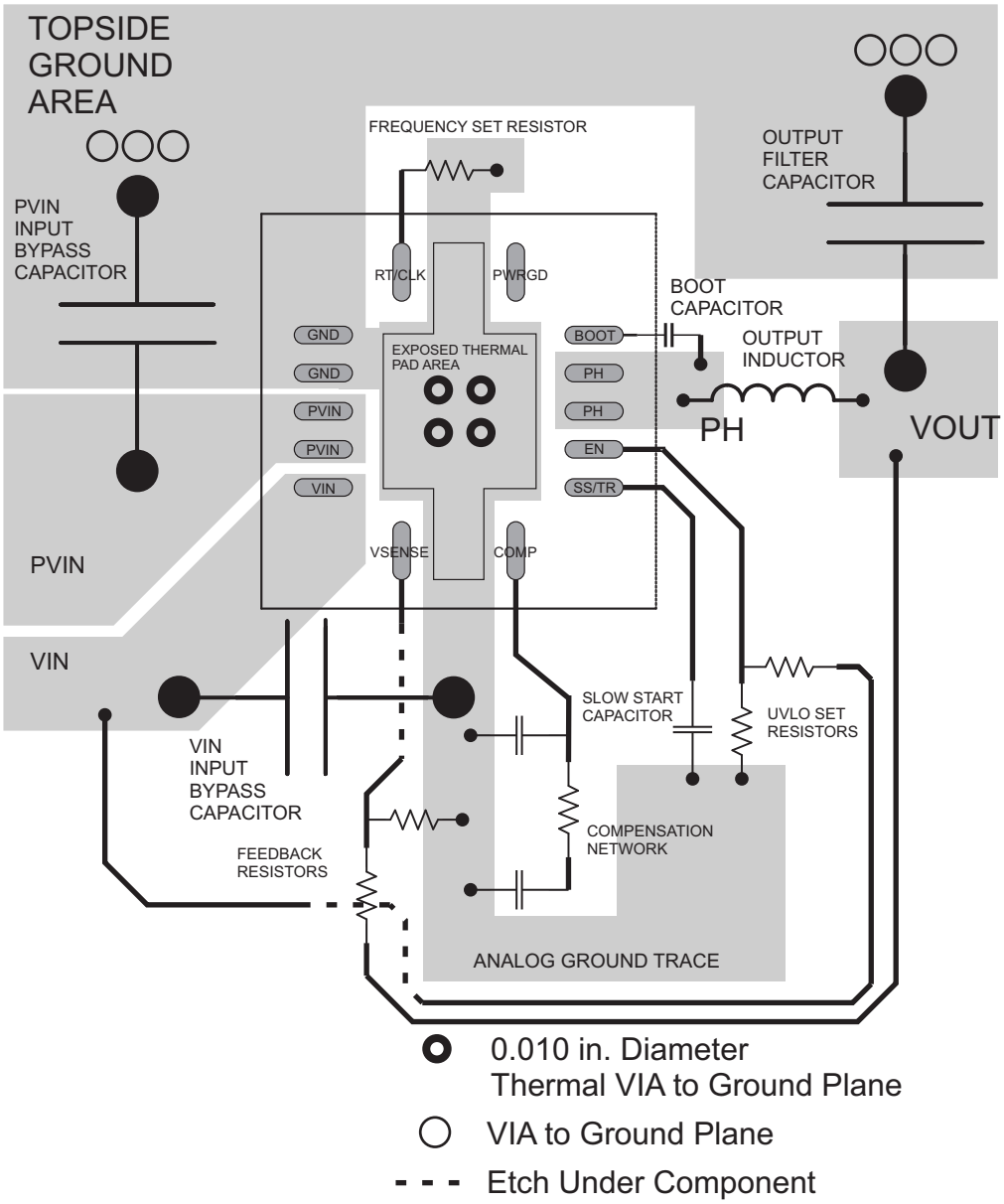


Figure 56. PCB Layout

11 Device and Documentation Support

11.1 Documentation Support

For more information about Type II and Type III frequency compensation circuits, see *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) and *Design Calculator* (SLVC219).

11.2 Trademarks

SwitcherPro, SWIFT are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54320RHLR	ACTIVE	VQFN	RHL	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54320	Samples
TPS54320RHLT	ACTIVE	VQFN	RHL	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54320	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

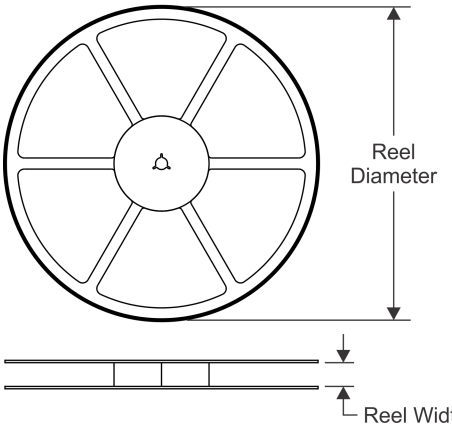
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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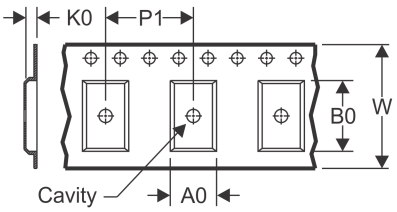
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

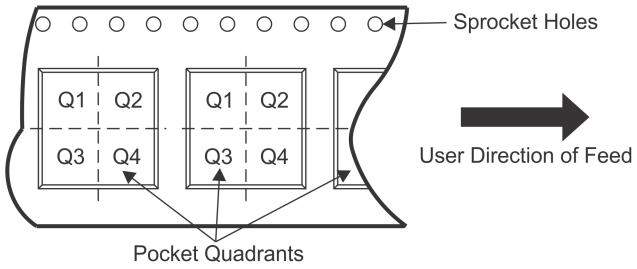


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

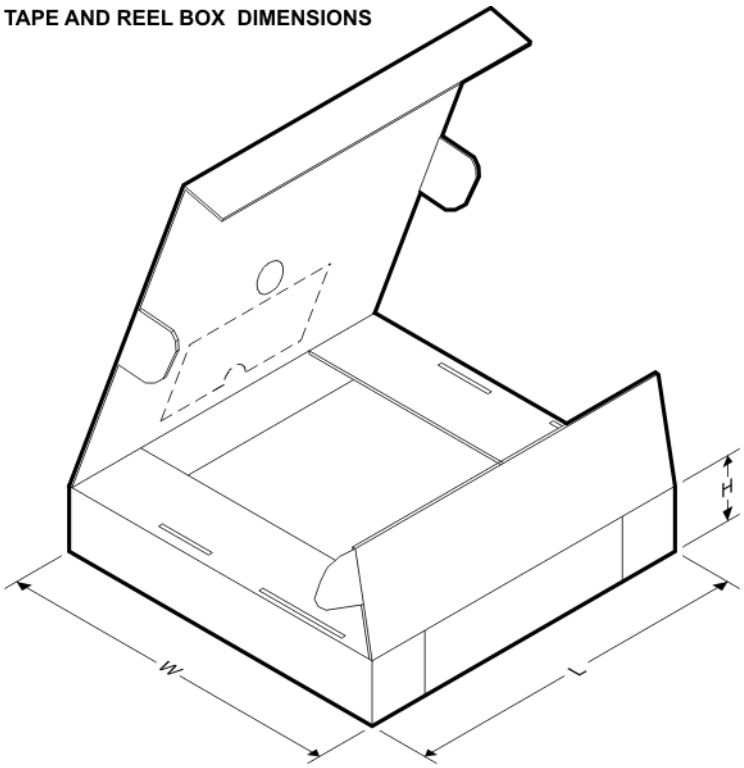
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54320RHLR	VQFN	RHL	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54320RHLT	VQFN	RHL	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

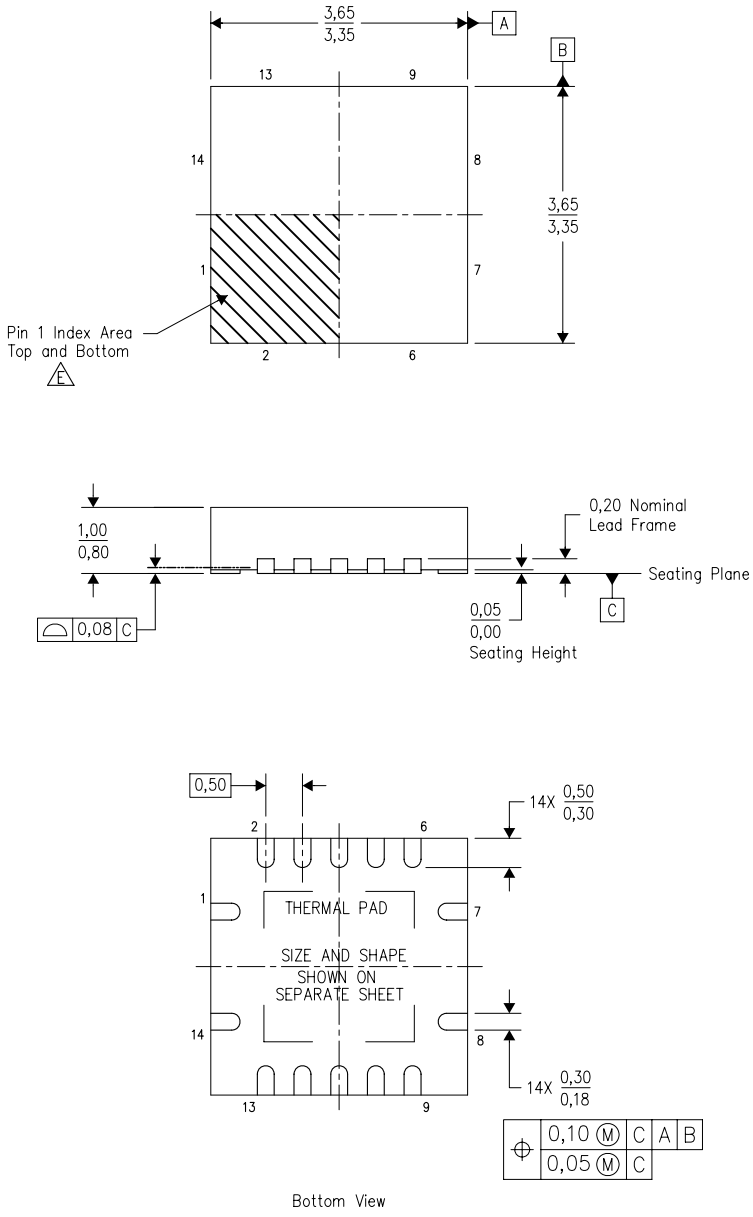
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54320RHLR	VQFN	RHL	14	3000	367.0	367.0	35.0
TPS54320RHLT	VQFN	RHL	14	250	210.0	185.0	35.0

RHL (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



4205346–2/J 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

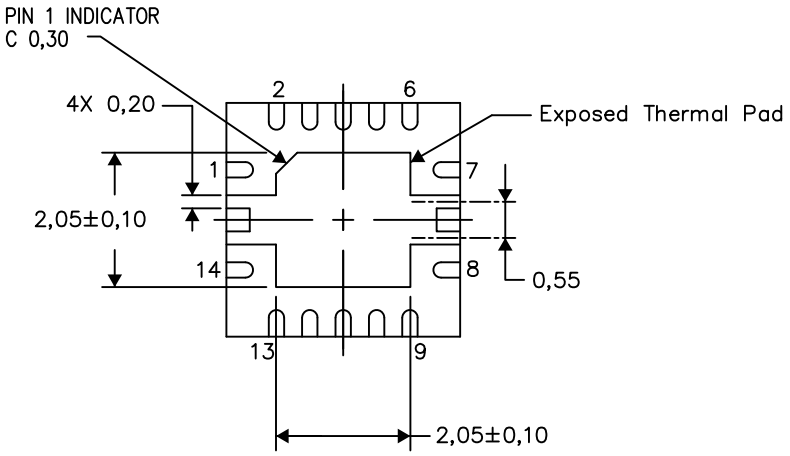
RHL (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



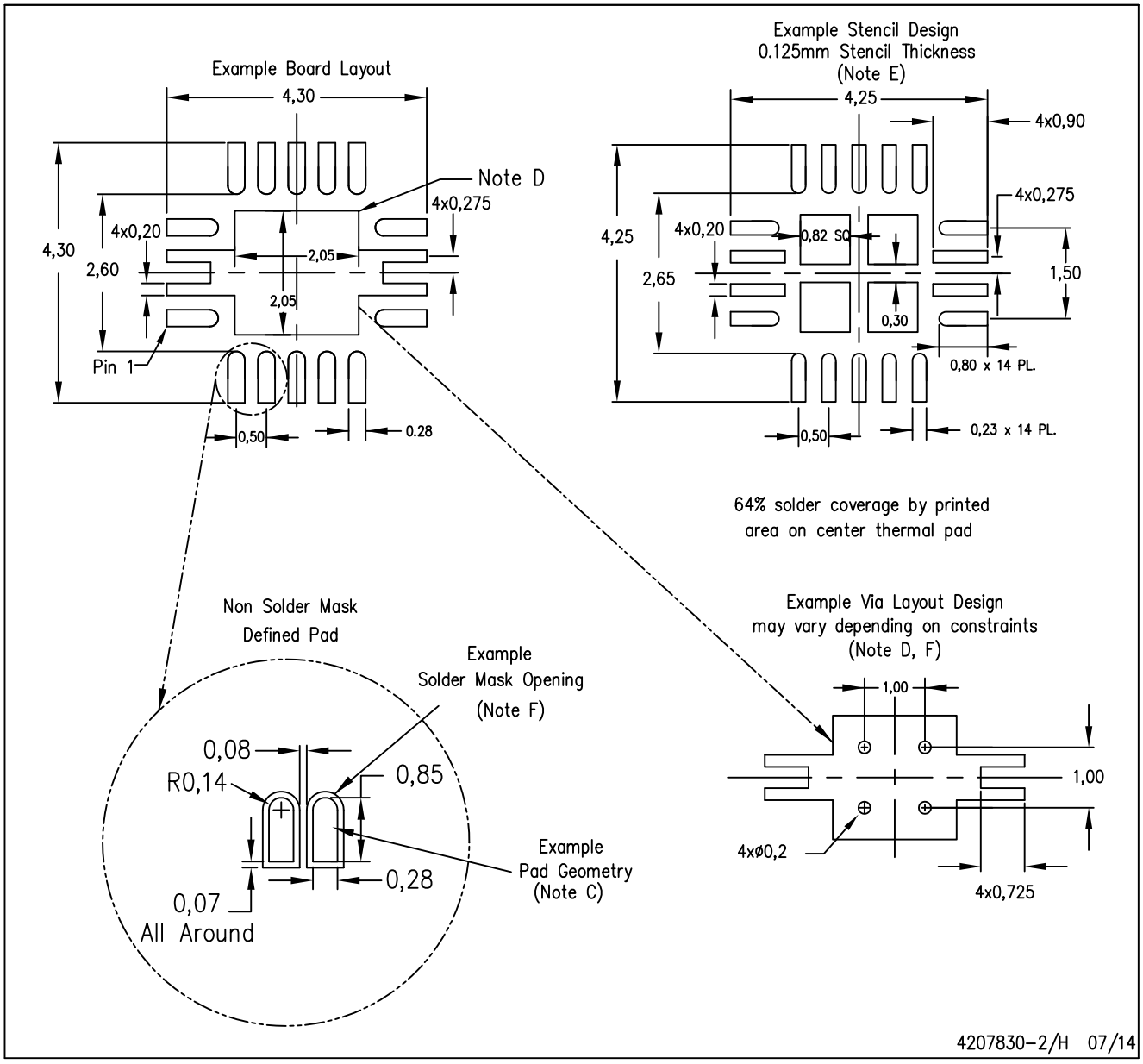
Bottom View

Exposed Thermal Pad Dimensions

4206363–2/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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