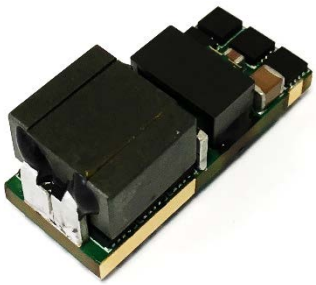
MAIN AND SATELLITE POWER STAMP

48V-to-PoL isolated DC-DC converters

The MAIN and SATELLITE Power Stamp are isolated DC-DC converters that converts a 48V or 54V bus voltage into a low voltage suitable for typical server's motherboard subsystems.



Key Features and Benefits

- **Over 94% efficiency at 1.8Vout**
- **Over 91% efficiency at 1.0Vout**
- **Up to 140W continuous output power / 200W peak**
- **Up to 70A continuous output current / 100A peak**
- **Wide 40V to 60V input voltage range**
- **Power density exceeding 300W/in^3**
- **Parallelable with automatic phase shedding**
- **Flat efficiency curve over wide load ranges**
- **Source and sink mode for fast transient response**
- Isolated power train
- Secondary side fully digital control
- PMBUs with configurable AVS or Intel SVID interface
- Industry standard SMT package
- Reference designs for selected applications

Applications

- **Direct conversion from 48V or 54V bus**
- **High performance computing**
- **Servers, storage and data processing equipment**
- **Communication systems**
- **Intel VR13 HC CPUs**
- **DDR4 memory**
- **Low voltage, high current ASICs and FPGAs**

www.powerstamp.org
belfuse.com/power-solutions

Model Selection

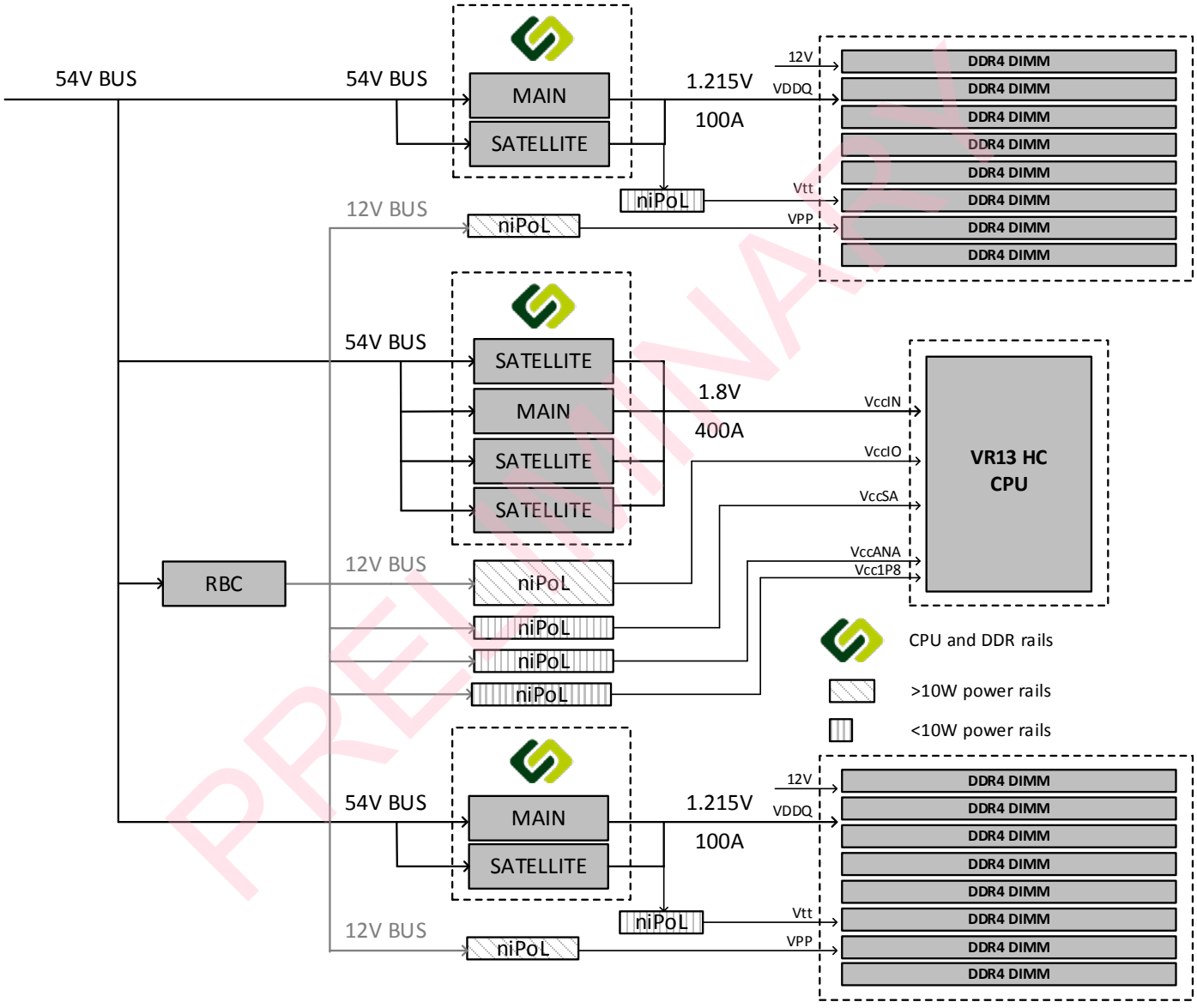
Part Number	Input Voltage [V]	Output Voltage* [V]	Output Current [A]	Output Current [A peak]	Efficiency (typical)
MAIN Power Stamps					
STM48-1V8M070-xxx	40 – 60	1.6 – 2.0	70	100	94%
STM48-1V2M070-xxx	40 – 60	1.16 – 1.26	70	100	91.6%
STM48-1V0M070-xxx	40 – 60	0.9 – 1.1	70	100	91%
SATELLITE Power Stamps					
STM48-1V8S070-xxx	40 – 60	1.6 – 2.0	70	100	94%
STM48-1V2S070-xxx	40 – 60	1.16 – 1.26	70	100	91.6%
STM48-1V0S070-xxx	40 – 60	0.9 – 1.1	70	100	91%
Controller IC					
STPSA60	-	-	-	-	-

* Contact factory for NVM configuration files for different output voltage settings

Order Information

Product Family	Input Voltage	-	Output Voltage	Module style	Output Current	-	Options
STM	**48**	**-**	**1V8**	**M**	**070**	**-**	**xxx**
Power Stamp form factor	48= 40 – 60V 54= 46 – 59V	-	1V8= 1.8V 1V2= 1.215V 1V0= 1.0V	M= MAIN S= SATELLITE	050= 50A 060= 60A 070= 70A 080= 80A 090= 90A 100= 100A	-	0 – 9= custom Z= RoHS G= Tray pkg. EBx= Eval. Bd. (x= number of populated stamps)

Typical Intel VR13 HC CPU and DDR4 Memory Application



Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Operating outside maximum recommended conditions for extended periods may affect product reliability and result in device failures.

Symbol	Parameter	Min	Max	Units
+IN to -IN	Non-operating continuous input voltage	-0.3	76	V
Vout to GND	Continuous output voltage	-0.3	TBD	V
VDD	Primary auxiliary bias voltage	-0.3	14	V
VCC	Secondary auxiliary bias voltage	-0.3	7	V
PWM_X, PWM_Y	(2)	-0.3	6.65	V
PWM_S, START	(3)	-0.3	7	V
START	(3)	-0.3	7	V
TMN, TMP	(3)	-0.3	7	V
CSP, CSN	(3) (4)	-0.3	2.5	V
CSP, CSN	(3) (4)	-0.3	2.5	V
All other pins	(3)	-0.3	7	V
Tmax	Ambient temperature	-40	+85	°C
Tstg	Storage temperature	-40	+100	°C

Notes:
1) All voltages referenced to GND unless otherwise specified
2) Need to be lower than VDD under any condition
3) Need to be lower than VCC under any condition
4) Max differential voltage to be limited within 100mV

Specifications

Specifications are typical and apply for the conditions: VDD= 5V, VCC= 5V, Tamb= 25°C unless otherwise noted.

Input Specifications – All models

Parameter	Symbol	Min	Typ	Max	Units
Input voltage Continuous; VDD, VCC applied	V_{IN}	40	48	60	V
Maximum input current V_{IN}= 40V – 60V, I_O = I_{O_max}	I_{IN_max}	-	-	4	A
Input quiescent current V_{IN}= 48V, I_O = 0A, enabled	I_{IN_NL}		TBD		mA
Input stand by current V_{IN}= 48V, disabled	I_{IN_stdby}		TBD		mA
Inrush transient	I^2t				A^2s
Input reflected ripple current 5Hz to 20MHz, 1µH source impedance; V_{IN}= 40V to 60V, I_O= I_{O_max}	I_{IN_rr}		TBD		mA_{p-p}
Input ripple rejection	PSRR		TBD		dB
Internal input capacitance	C_{IN}		TBD		µF

Output Specifications – 1.8V

Parameter	Symbol	Min	Typ	Max	Units
Output voltage setpoint	V_{OUT}	1.820	1.83	1.839	V
Output voltage trim range	V_{OUT_adj}	1.6		2.0	V
Trim VID resolution			10		mV
Output Regulation Line (V_{IN}= V_{IN_min} to V_{IN_max}) Load (I_{OUT}= I_{OUTmin} to I_{OUTmax}) Temperature (T_{ref}= T_{amb_min} to T_{amb_max})			 - - -	 8 10 TBD	 mV mV %V_{OUT_nom}
Total regulation band AC, I_{OUT}= I_{OUT_min} to I_{OUT_max}			-	44	mV_{p-p}
Output voltage ripple and noise V_{IN}= 48V and I_{OUT}= I_{OUT_min} to I_{OUT_max} 5Hz to 20 MHz bandwidth, nominal output capacitance	V_r		-	20	mV_{p-p}
Output capacitance ESR > 0.15mΩ ESR > 10mΩ	C_{OUT}		 - -	 TBD TBD	µF
Continuous output current in either source or sink mode	I_{OUT}	0		70	A
Peak output current TBD, in either source or sink mode	I_{OUT_peak}		-	100	A_{peak}
Output current limit TBD	I_{OUT_CL}		150	180	% I_{OUT_max}
Output short circuit current TBD	I_{OUT_SC}			TBD	A_{RMS}
Efficiency V_{IN}= 48V, T_{amb}= 25°C I_{OUT}= 50% of I_{OUT_max} , V_{OUT}= V_{OUT_nom}	η	94.0	94.1		%
Switching frequency	f_{SW}	200	450	600	kHz

Output Specifications – 1.2V

Parameter	Symbol	Min	Typ	Max	Units
Output voltage setpoint	V_{OUT}	1.194	1.2	1.206	V
Output voltage trim range	V_{OUT_adj}	1.16		1.26	V
Trim VID resolution			5		mV
Output Regulation Line (V_{IN}= V_{IN_min} to V_{IN_max}) Load (I_{OUT}= I_{OUTmin} to I_{OUTmax}) Temperature (T_{ref}= T_{amb_min} to T_{amb_max})			 - - -	 2 8 TBD	 mV mV %V_{OUT_nom}
Total regulation band AC, I_{OUT}= I_{OUT_min} to I_{OUT_max}			-	-	mV_{p-p}
Output voltage ripple and noise V_{IN}= 48V and I_{OUT}= I_{OUT_min} to I_{OUT_max} 5Hz to 20 MHz bandwidth, nominal output capacitance	V_r		-	12	mV_{p-p}
Output capacitance ESR > 0.15mΩ ESR > 10mΩ	C_{OUT}		- -	TBD TBD	µF
Continuous output current in either source or sink mode	I_{OUT}	0		70	A
Peak output current TBD, in either source or sink mode	I_{OUT_peak}		-	100	A_{peak}
Output current limit TBD	I_{OUT_CL}		150	180	% I_{OUT_max}
Output short circuit current TBD	I_{OUT_SC}			TBD	A_{RMS}
Efficiency V_{IN}= 48V, T_{amb}= 25°C I_{OUT}= 50% of I_{OUT_max} , V_{OUT}= V_{OUT_nom}	η	91.3	91.6		%
Switching frequency	f_{SW}	200	450	600	kHz

Output Specifications – 1.0V

Parameter	Symbol	Min	Typ	Max	Units
Output voltage setpoint	V_{OUT}	0.995	1.0	1.005	V
Output voltage trim range	V_{OUT_adj}	0.9		1.1	V
Trim VID resolution			5		mV
Output Regulation Line (V_{IN}= V_{IN_min} to V_{IN_max}) Load (I_{OUT}= I_{OUTmin} to I_{OUTmax}) Temperature (T_{ref}= T_{amb_min} to T_{amb_max})			 - - -	 TBD TBD TBD	 mV mV $\%V_{OUT\_nom}$
Total regulation band AC, I_{OUT}= I_{OUT_min} to I_{OUT_max}			180		mV_{p-p}
Output voltage ripple and noise V_{IN}= 48V and I_{OUT}= I_{OUT_min} to I_{OUT_max} 5Hz to 20 MHz bandwidth, nominal output capacitance	V_r		-	TBD	mV_{p-p}
Output capacitance ESR > 0.15mΩ ESR > 10mΩ	C_{OUT}		- -	TBD TBD	µF
Continuous output current in either source or sink mode	I_{OUT}	0		70	A
Peak output current TBD, in either source or sink mode	I_{OUT_peak}		-	100	A_{peak}
Output current limit TBD	I_{OUT_CL}		150	180	$\%\ I_{OUT\_max}$
Output short circuit current TBD	I_{OUT_SC}			TBD	A_{RMS}
Efficiency V_{IN}= 48V, T_{amb}= 25°C I_{OUT}= 50% of I_{OUT_max} , V_{OUT}= V_{OUT_nom}	η	91.0	91.3		%
Switching frequency	f_{SW}	200	450	600	kHz

Feature Specifications

Pin or Pad	Parameter	Min	Typ	Max	Units
Supply pins					
VDD	VDD supply voltage	4.5	5	5.5	V
	VDD supply current		-	150	mA
VCC	VCC supply voltage	4.5	5	5.5	V
	VCC supply current		-	150	mA
VREG	Not used		-		
VCTRL	Not used		-		
Under Voltage Lock Out					
VDD	VDD rising threshold		4.2	4.3	V
	Hysteresis			500	mV
Output Enable					
	Input HIGH, rising			0.7	mV
	Input LOW, falling	0.4			mV
	Leakage, V_{EN}= 1.1V			1	µA

Protections					
+S	Feedback disconnection		700		mV
-S	Feedback disconnection		500		mV
VRSMON	Peak protection		3.045		V
PMBus Interface					
SDA SCL	Input HIGH, rising	1.8			V
	Input LOW, falling			1.4	V
SDA SALERT	Output pull down, I_{SINK}= 5mA			13	Ω
SADDR	R_{DOWN} resistor (see PMBus Address section)		10		kΩ
SVID / AVS Interface					
SVDAT / AVSMDAT SVCLK / AVSCLK	Input HIGH, rising	0.65			V
	Input LOW, falling			0.45	V
SVDAT / AVSMDAT SV_ALRT / AVSSDAT	Output pull down, I_{SINK}= 5mA			13	Ω
CPU Link Interface					
VR_HOT#	Output pull down, I_{SINK}= 5mA			13	Ω
VR_RDY				13	Ω
FAULT#				45	Ω
VCCIO_OK	Input HIGH, rising	1.7			V
	Input LOW, falling			1.5	V
PFAULT_IN#	Pull up current		10		µA
PIN_ALERT#	Output pull down, I_{SINK}= 5mA			13	Ω
Primary uController Interface					
PUCCS, PUCCK PUCDTI	Input HIGH, rising	1.7			V
	Input LOW, falling			1.5	V
PUCDTO	Output HIGH voltage, I_{SOURCE}= 1mA	4.5V			
	Output LOW voltage, I_{SINK}= 5mA		125	250	mV
Output Pins					
PWMx STARTx	Output HIGH voltage, I_{SOURCE}= 1mA	4.90	4.95		V
	Output LOW voltage, I_{SINK}= 1mA		25	50	mV
STARTx	Active high impedance (HiZ)	1.55.	1.60	1.65	V

General Specifications

Parameter	Symbol	Min	Typ	Max	Units
Relative humidity Operating, non-condensing	RH	10		90	%
Altitude		-500		4000	ft.
Calculated MTBF Calculated Per Telcordia SR-332, Issue2, Method 1, Case 3 V_{IN}= 48 V, V_{OUT}=1.83 V, I_{OUT}= 70 A, T_{amb}= 40°C , FIT=10^9/MTBF	MTBF		TBD		Hours
Weight			12		g
Dimensions L x W x H		30	12.7	18	mm

Performance Characteristics – 1.8V

Please contact Bel Power Solutions for information about the performance of this product

Efficiency and Power Dissipation

Please contact Bel Power Solutions for information about the performance of this product

Thermal Derating Curves

Please contact Bel Power Solutions for information about the performance of this product

Ripple and Noise

Please contact Bel Power Solutions for information about the performance of this product

Switching Frequency vs. Output Current

Please contact Bel Power Solutions for information about the performance of this product

Transient Response – 10% I_{OUT} to 100% I_{OUT}, V_{IN}= 48V

Please contact Bel Power Solutions for information about the performance of this product

Transient Response – 100% I_{OUT} to 10% I_{OUT}, V_{IN}= 48V

Performance Characteristics – 1.2V

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Efficiency and Power Dissipation

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Thermal Derating Curves

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Ripple and Noise

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Switching Frequency vs. Output Current

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Transient Response – 10% I_{OUT} to 100% I_{OUT}, V_{IN}= 48V

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Transient Response – 100% I_{OUT} to 10% I_{OUT}, V_{IN}= 48V

Performance Characteristics – 1.0V

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Efficiency and Power Dissipation

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Thermal Derating Curves

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Ripple and Noise

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Switching Frequency vs. Output Current

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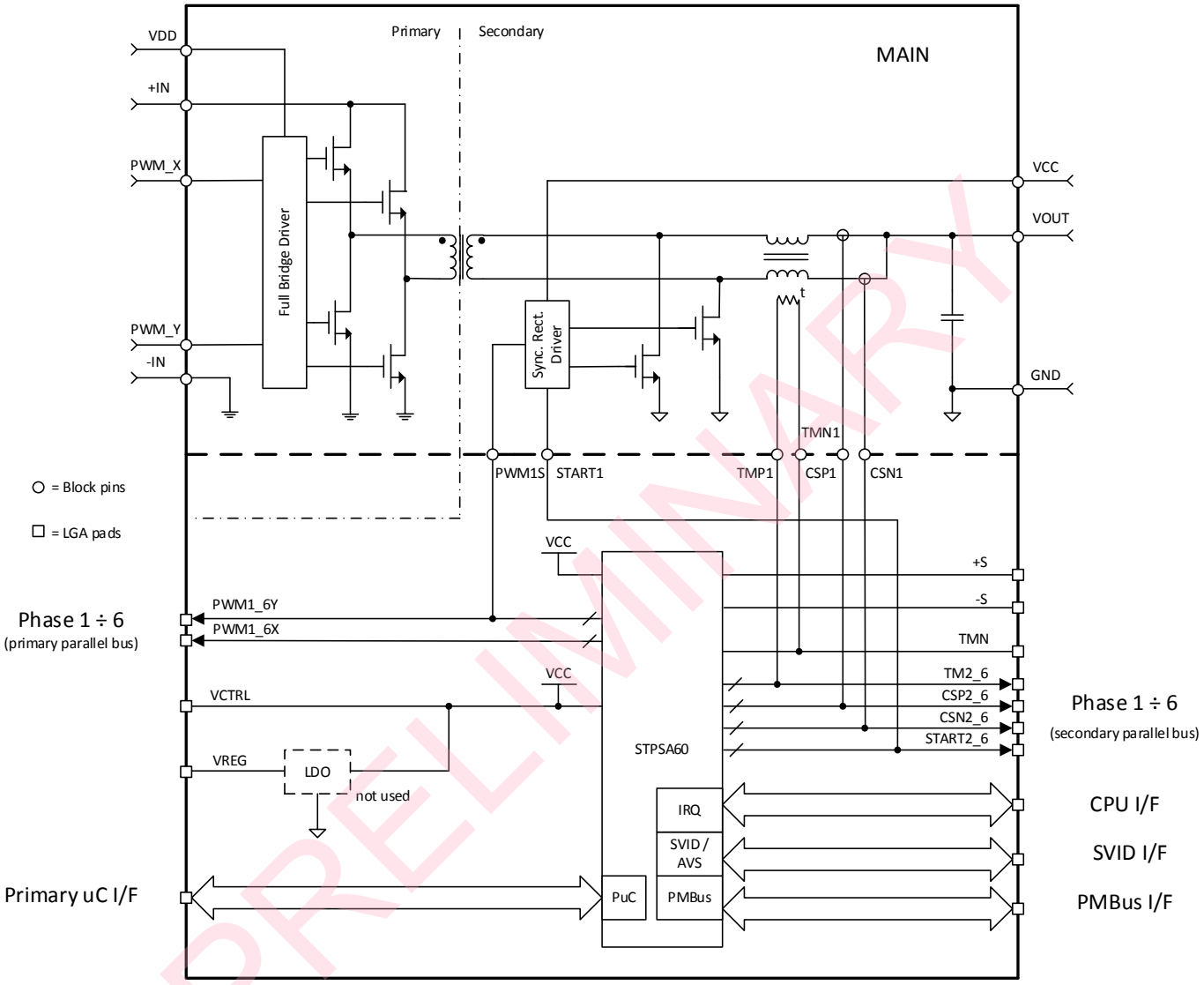
Transient Response – 10% I_{OUT} to 100% I_{OUT}, V_{IN}= 48V

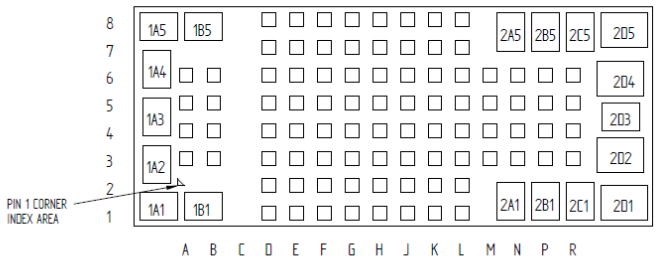
Please contact Bel Power Solutions for information about the performance of this product

Transient Response – 100% I_{OUT} to 10% I_{OUT}, V_{IN}= 48V

Block Diagram - MAIN



Package Pinout – MAIN



TOP VIEW THROUGH THE PRODUCT

INPUT	
PAD #	FUNCTION
1A1	+IN
1A2	PWM_Y
1A3	VDD
1A4	PWM_X
1A5	+IN
1B1	-IN
1B5	-IN

OUTPUT	
PAD #	FUNCTION
2A1	START
2A5	PWM_S
2B1	TMN
2B5	VCC
2C1	TMP
2C5	CSP
2D1	GND
2D2	VOUT
2D3	CSN
2D4	VOUT
2D5	GND

LAND GRID ARRAY PAD DESIGNATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
1	N/A	N/A	N/A	PFAULT_IN#	PUCDTO	PUCDTI	PWM1Y	PWM2Y	PWM3Y	PWM4Y	PWM5Y	N/A	N/A	N/A	N/A
2	N/A	N/A	N/A	VSRMON	PUCCS	PUCCK	PWM1X	PWM2X	PWM3X	PWM4X	PWM5X	N/A	N/A	N/A	N/A
3	-IN	-IN	N/A	TMP5	CSP5	CSN5	GND	GND	GND	GND	PWM6X	PWM6Y	START5	GND	GND
4	-IN	-IN	N/A	TMP3	CSP3	CSN3	GND	GND	GND	GND	FAULT#	START6	START3	GND	GND
5	-IN	-IN	N/A	TMP2	CSP2	CSN2	GND	GND	GND	GND	VR_RDY	VREG	START2	GND	GND
6	-IN	-IN	N/A	TMP4	CSP4	CSN4	GND	GND	GND	GND	EN	VCTRL	START4	GND	GND
7	N/A	N/A	N/A	TMP6	CSP6	CSN6	SALERT	SDA	SVDAT / AVSMDAT	VR_HOT#	VCCIO_OK	N/A	N/A	N/A	N/A
8	N/A	N/A	N/A	TMN	+S	-S	SADDR	SCL	SVCLK / AVSCLK	SV_ALRT / AVSSDAT	PAD_ALERT#	N/A	N/A	N/A	N/A

Land designator per JEP95, SEC. 3, SPP-010 AND SPP-020, Zero orientation with pin 1 in lower left corner

Pin Description – MAIN

Pad #	Pad name	Pad Function
A1	N/A	No Pad present
B1	N/A	No Pad present
C1	N/A	No Pad present
D1	PFAULT_IN#	Primary side fault indicator
E1	PUCDTO	Primary side uC data output
F1	PUCDTI	Primary side uC data input
G1	PWM1Y	PWM signal for Satellite 1
H1	PWM2Y	PWM signal for Satellite 2
J1	PWM3Y	PWM signal for Satellite 3
K1	PWM4Y	PWM signal for Satellite 4
L1	PWM5Y	PWM signal for Satellite 5
M1	N/A	No Pad present
N1	N/A	No Pad present
P1	N/A	No Pad present
R1	N/A	No Pad present
A2	N/A	No Pad present
B2	N/A	No Pad present
C2	N/A	No Pad present
D2	VSRMON	Feed-forward sensor input
E2	PUCCS	Primary side uC chip select
F2	PUCCK	Primary side u-controller clock

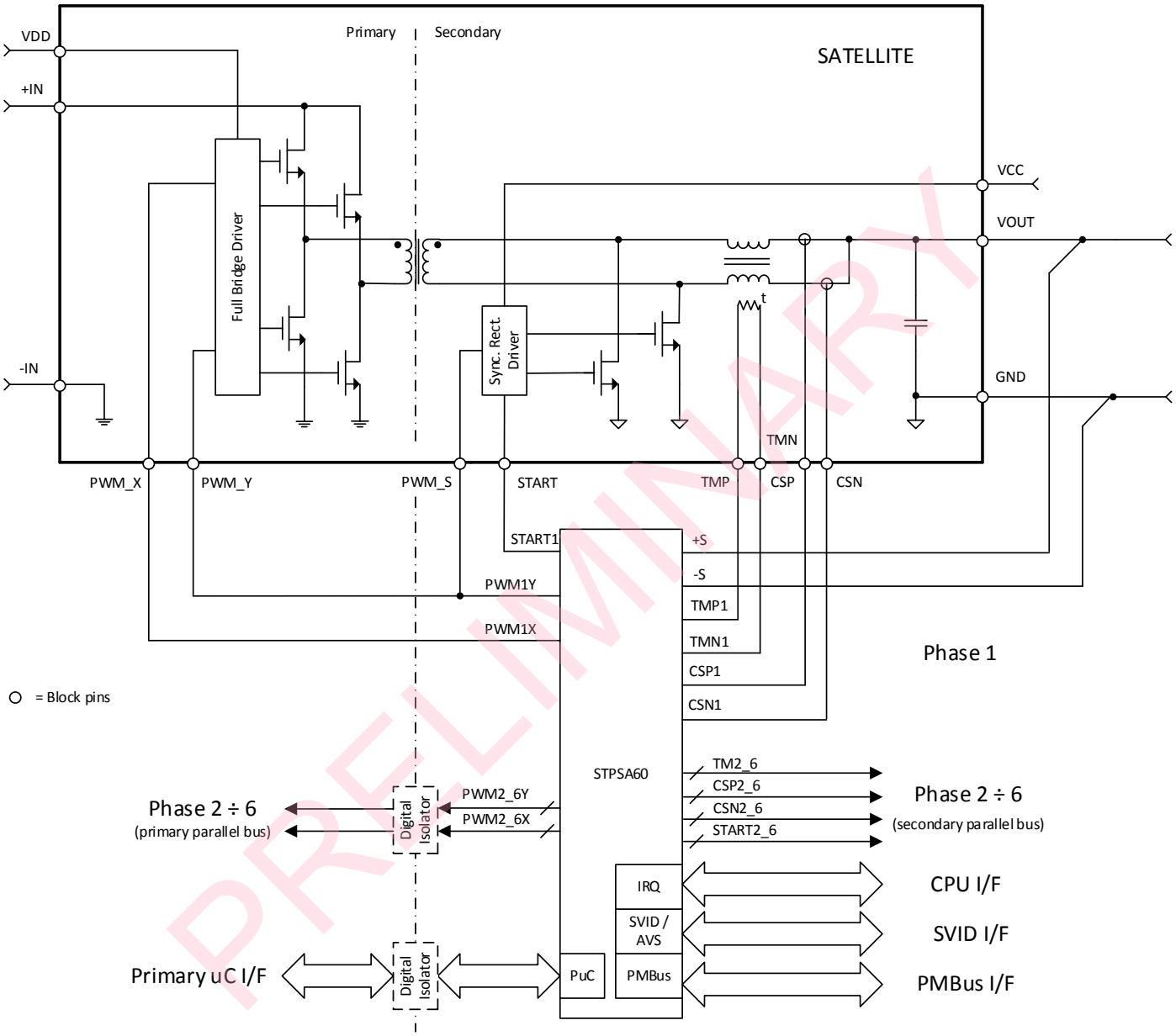
Pad #	Pad name	Pad Function
A4	N/C (-In)	Pad present, N/C, Thermal via
B4	N/C (-In)	Pad present, N/C, Thermal via
C4	N/A	No Pad present
D4	TMP3	Temperature sense Satellite 3
E4	CSP3	Current sense +v Satellite 3
F4	CSN3	Current sense -v Satellite 3
G4	GND	Secondary side ground
H4	GND	Secondary side ground
J4	GND	Secondary side ground
K4	GND	Secondary side ground
L4	FAULT#	Programmable fault indicator
M4	START6	Start for Satellite 6
N4	START3	Start for Satellite 3
P4	GND	Secondary side ground
R4	GND	Secondary side ground
A5	N/C (-In)	Pad present, N/C, Thermal via
B5	N/C (-In)	Pad present, N/C, Thermal via
C5	N/A	No Pad present
D5	TMP2	Temperature sense Satellite 2
E5	CSP2	Current sense +v Satellite 2
F5	CSN2	Current sense -v Satellite 2

Pad #	Pad name	Pad Function
G2	PWM1X	PWM signal for Satellite 1
H2	PWM2X	PWM signal for Satellite 2
J2	PWM3X	PWM signal for Satellite 3
K2	PWM4X	PWM signal for Satellite 4
L2	PWM5X	PWM signal for Satellite 5
M2	N/A	No Pad present
N2	N/A	No Pad present
P2	N/A	No Pad present
R2	N/A	No Pad present
A3	N/C (-In)	Pad present, N/C, Thermal via
B3	N/C (-In)	Pad present, N/C, Thermal via
C3	N/A	No Pad present
D3	TMP5	Temperature sense Satellite 5
E3	CSP5	Current sense +v Satellite 5
F3	CSN5	Current sense -v Satellite 5
G3	GND	Secondary side ground
H3	GND	Secondary side ground
J3	GND	Secondary side ground
K3	GND	Secondary side ground
L3	PWM6X	PWM signal for Satellite 6
M3	PWM6Y	PWM signal for Satellite 6
N3	START5	Start for Satellite 5
P3	GND	Secondary side ground
R3	GND	Secondary side ground
A7	N/A	No Pad present
B7	N/A	No Pad present
C7	N/A	No Pad present
D7	TMP6	Temperature sense Satellite 6
E7	CSP6	Current sense +v Satellite 6
F7	CSN6	Current sense -v Satellite 6
G7	SALERT	PMBus Alert
H7	SDA	PMBus data
J7	SVDAT / AVSMDAT	SVID data_/ AVS MData
K7	VR_HOT#	SVI VR hot
L7	VCCIO_OK	VCC fault shutdown – immediate unit shutdown
M7	N/A	No Pad present
N7	N/A	No Pad present
P7	N/A	No Pad present
R7	N/A	No Pad present

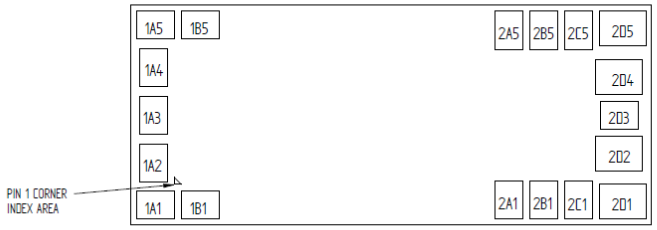
Pad #	Pad name	Pad Function
G5	GND	Secondary side ground
H5	GND	Secondary side ground
J5	GND	Secondary side ground
K5	GND	Secondary side ground
L5	VR_RDY	Voltage regulator ready signal
M5	VREG	Optional regulator input
N5	START2	Start for Satellite 3
P5	GND	Secondary side ground
R5	GND	Secondary side ground
A6	N/C (-Vin)	Pad present, N/C, Thermal via
B6	N/C (-Vin)	Pad present, N/C, Thermal via
C6	N/A	No Pad present
D6	TMP4	Temperature sense Satellite 4
E6	CSP4	Current sense +v Satellite 4
F6	CSN4	Current sense -v Satellite 4
G6	GND	Secondary side ground
H6	GND	Secondary side ground
J6	GND	Secondary side ground
K6	GND	Secondary side ground
L6	EN	Enable signal
M6	VCTRL	Controller supply voltage
N6	START4	Start for Satellite 4
P6	GND	Secondary side ground
R6	GND	Secondary side ground
A8	N/A	No Pad present
B8	N/A	No Pad present
C8	N/A	No Pad present
D8	TMN	Temperature sense -v common for TMN of all Satellites.
E8	+S	Remote sense +v
F8	-S	Remote sense -v
G8	SADDR	PMBus address setting
H8	SCL	PMBus clock
J8	SVCLK / AVSCLK	SVID clock / AVS clock
K8	SVALRT / AVSSDAT	SVID alert / AVS SData
L8	PAD_ALERT#	SVI Pad Alert #
M8	N/A	No Pad present
N8	N/A	No Pad present
P8	N/A	No Pad present
R8	N/A	No Pad present

For the description of large pads numbered from 1A1 to 2D5, please refer to the table in: Pin Description – SATELLITE

Block Diagram – SATELLITE (with external STPSA60 Controller)



Package Pinout – SATELLITE



TOP VIEW THROUGH THE PRODUCT

INPUT	
PIN #	FUNCTION
1A1	+IN
1A2	PWM_Y
1A3	VDD
1A4	PWM_X
1A5	+IN
1B1	-IN
1B5	-IN

OUTPUT	
PIN #	FUNCTION
2A1	START
2A5	PWM_S
2B1	TMN
2B5	VCC
2C1	TMP
2C5	CSP
2D1	GND
2D2	VOUT
2D3	CSN
2D4	VOUT
2D5	GND

Land designator per JEP95, SEC. 3, SPP-010 AND SPP-020, Zero orientation with pin 1 in lower left corner

Pin Description – SATELLITE

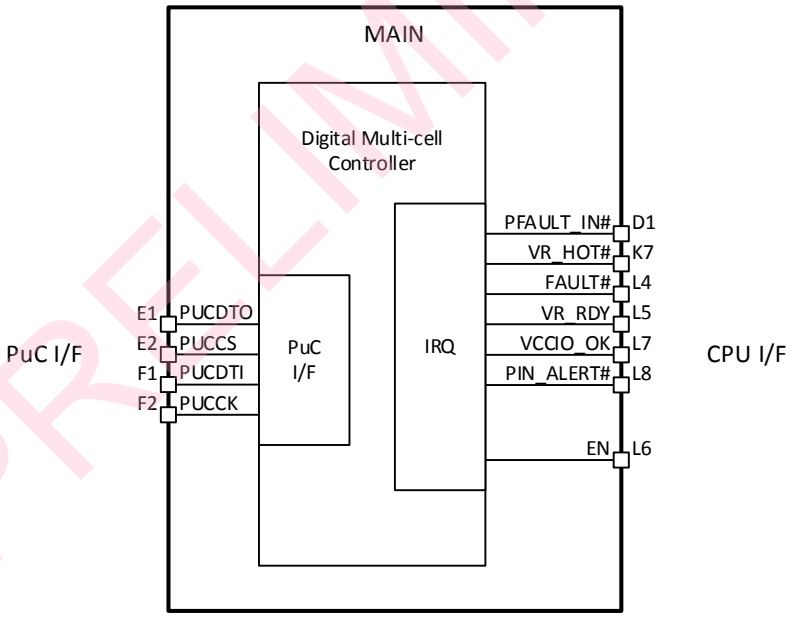
Pin #	Pin name	Pin Function
1A1	+IN	Positive input voltage supply
1A2	PWM_Y	PWM input Y
1A3	VDD	Primary side auxiliary voltage supply
1A4	PWM_X	PWM input X
1A5	+IN	Positive input voltage supply
1B1	-IN	Primary side ground
1B5	-IN	Primary side ground
2A1	START	Synchronous rectifier START signal
2A5	PWM_S	Synchronous rectifier PWM signal
2B1	TMN	Temperature monitor negative output
2B5	VCC	Secondary side auxiliary voltage supply
2C1	TMP	Temperature monitor positive output
2C5	CSP	Current monitor positive output
2D1	GND	Secondary side ground
2D2	VOUT	Positive output voltage
2D3	CSN	Current monitor negative output
2D4	VOUT	Positive output voltage
2D5	GND	Secondary side ground

Feature Description - MAIN

The MAIN Power Stamp is a standalone DC-DC PoL converter designed to control multi-phase, interleaved arrays of SATELLITE Power Stamps. It includes an on-board SATELLITE and an STPSA60 Digital Multi-cell Controller in a single package. MAIN and SATELLITE are using the same pinout for signals available in both modules. The MAIN module additionally includes an LGA connector for control signals not present on SATELLITE. A single MAIN can control up to five SATELLITE for an array of six phases, maximum. Several digital interfaces are included for ease of integration into complex microprocessor applications.

Primary Microcontroller Interface

The digital multi-cell controller embedded in the MAIN Power Stamp monitors input/output voltage, power and current in order to manage OV, UV and OC events and to provide telemetry data to the CPU and PMBus interfaces. The Primary Microcontroller Interface (PuC I/F) transmits information about the telemetry from the primary side. Either digital or analog transmission methods are available. A serial interface is conveniently used in isolated configurations (PUCDTO, PUCDTI, PUCCK and PUCCS pins) with external digital isolators. Non-isolated configurations can take advantage of the analog VRSMON signal. User can program how and when to use such configurations and telemetry data information. Following standard PMBus implementation, each protection features a programmable warning and fault limits and actions. Protections are configurable and used to trigger special outputs of the CPU interface. Please refer to the STPSA60 Data Sheet and GUI User Manual for a list of the specific commands supported.



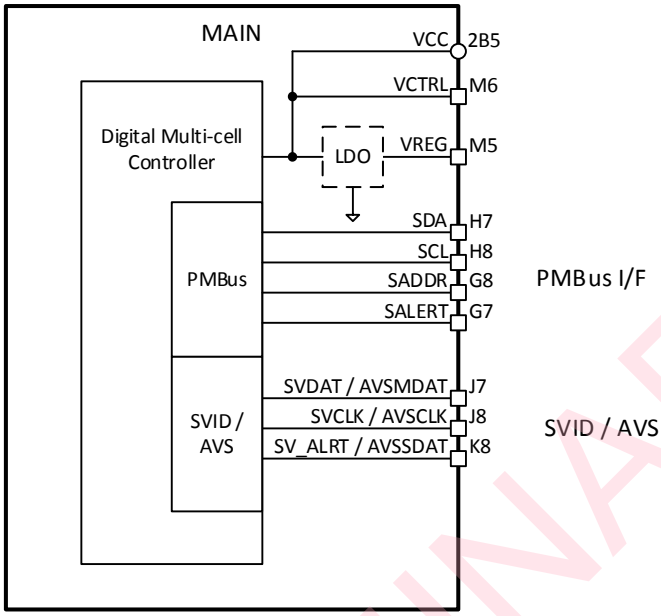
CPU Interface

The EN pin is an active-high signal that enables the converter when pulled up to VCC, connect to GND to disable. Please contact Intel for detailed information regarding the CPU interface and a list of the specific signals supported.

PMBus Interface

The MAIN Power Stamp has a PMBus interface that supports both communication and control. The PMBus Power Management Protocol Specification can be obtained from www.pmbus.org. The modules support a subset of version 1.2 of the standard and is fully compatible with the PMBus™ specification for read/write access in the byte, word, block mode. More than 110 commands are implemented, covering all the basic and advanced functions of the device.

Parameters are programmed using PMBus and stored in the embedded Non Volatile Memory as defaults for later use. Only those specifically identified as capable of being stored are saved. The write protection capability of the device prevents any unintended writing.



The device also supports the SALERT response protocol whereby the module can alert the bus master if it wants to talk. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification. Please refer to the STPSA60 Data Sheet and GUI User Manual for a list of the specific commands supported.

PMBus Address

The PMBus slave address is configured at the startup of the device by reading the voltage on the ADDR pin. The proper resistor divider must be connected from the ADDR pin to the GND and VCC pins. Additional configurations are stored into the NVM and corresponding System Registers. For a list of MAIN unit System Registers please see the STPSA60 data sheet.

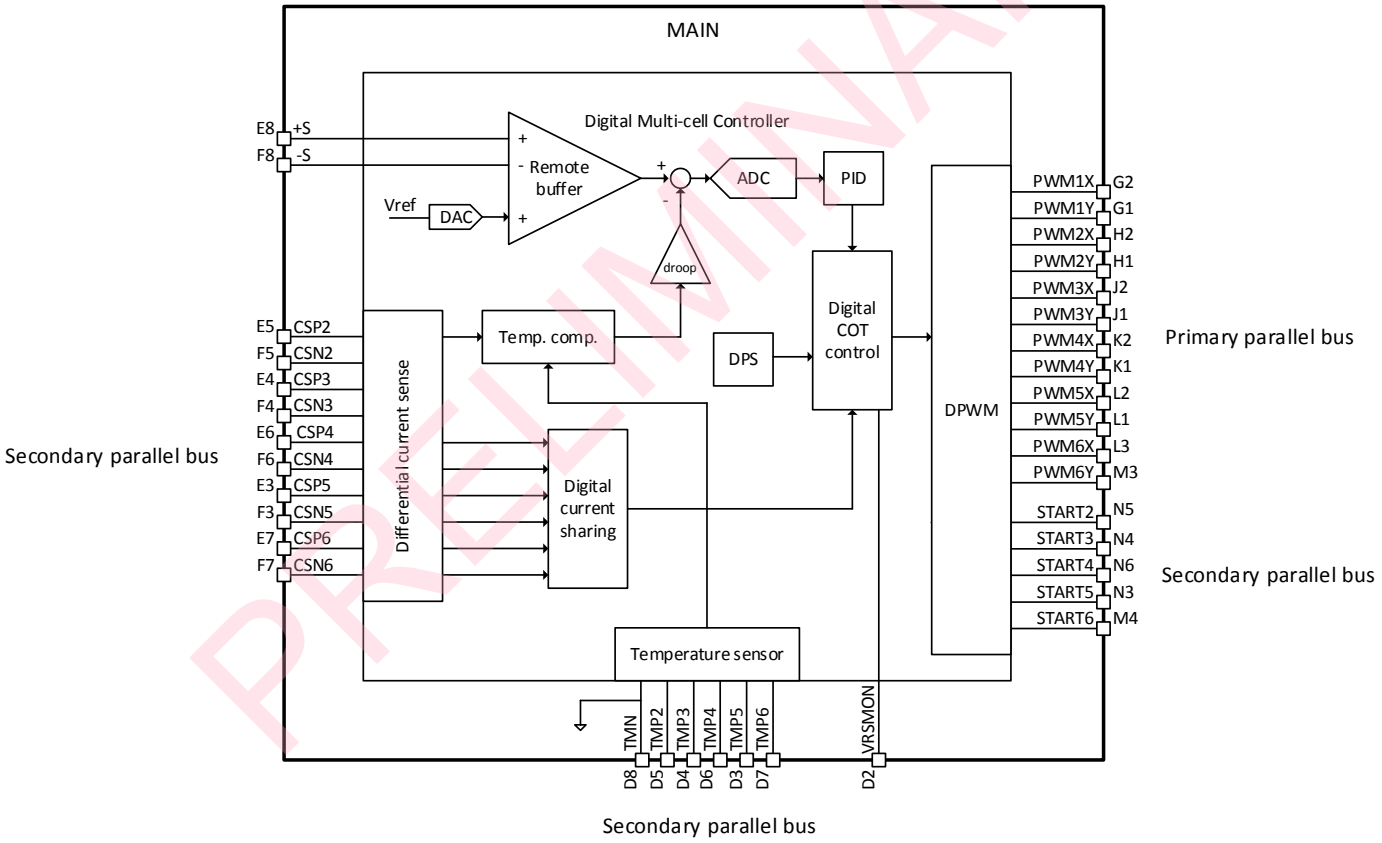
PMBus Address	R_{UP} (on the host board)		R_{DOWN} (inside the MAIN unit)	
	Resistor series	Resistor value Ω	Resistor series	Resistor value Ω
B8	E12	OPEN	E12	10,000
B4	E12	220,000	E12	10,000
B2	E12	120,000	E12	10,000
B0	E12	82,000	E12	10,000
E8	E24	62,000	E12	10,000
E4	E96	48,700	E12	10,000
E2	E12	39,000	E12	10,000
E0	E12	33,000	E12	10,000
D8	E48	27,400	E12	10,000
D4	E48	23,700	E12	10,000
D2	E96	20,500	E12	10,000
D0	E48	17,800	E12	10,000
C8	E96	15,800	E12	10,000
C4	E96	13,700	E12	10,000
C2	E48	12,100	E12	10,000
C0	E96	10,700	E12	10,000

SVID / AVS Interface

The MAIN Power Stamp supports alternatively Intel Serial VID interface (SVID) or PMBus Adaptive Voltage Scaling interface (AVS) for output voltage positioning. The SVID interface communicates with Intel microprocessor through three wires, SVCLK, SVDAT, and SV_ALRT, and controls the VID code change rate. It is fully compliant with Intel VR13 PWM rev 1.1, document # 544905 and Intel SVID protocol Rev1.7, document # 456098. To guarantee proper device and CPU operations, refer to these documents for bus design and layout guidelines. Different platforms may require different pull-up impedance on the bus. Please contact Intel for detailed information regarding the SVID interface. FPGAs, ASICs, SoCs and non-Intel processors can adaptively change their supply voltages using AVS. The SVID and AVS interfaces share the same hardware and switching between the two can happen at run time. The corresponding AVS pin names are AVSCLK, AVSMDAT and AVSSDAT.

Paralleling

The block diagram of the MAIN Power Stamp digital control loop is illustrated in the figure:



The converter output voltage is differentially sensed by the +S and –S inputs of the remote buffer and compared with a digitally adjustable voltage reference Vref. The output of the remote buffer is summed to a temperature compensated (TMP) droop signal for load line generation and converted by the analog to digital converter (ADC) into digital. Digital PID compensation is then applied before the signal is transmitted to the digital constant on time (COT) control. Output currents of each individual phase are differentially sensed by the CSN and CSP inputs. A digital current sharing block drives the digital COT control. Input voltage feedforward is applied to the digital COT control via the VRSMON signal. Dynamic Phase Shedding (DPS) is computed as a function of the output current conditions and concurs

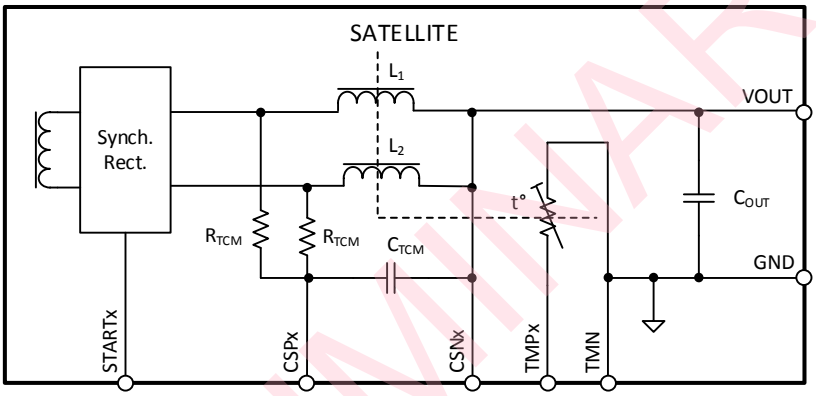
to determine the switching frequency / duty cycle generated by the digital COT control. The digital PWM (DPWM) modulator demultiplexes the resulting switching frequency for automatic phase shedding and interleaving.

Primary Parallel Bus

The primary parallel bus carries the PWM signals generated by the digital PWM modulator. Two out-of-phase signals, PWMX and PWMY, are transmitted to the primary side, either directly or through optional digital isolators, to drive the two sides of the full bridge power train.

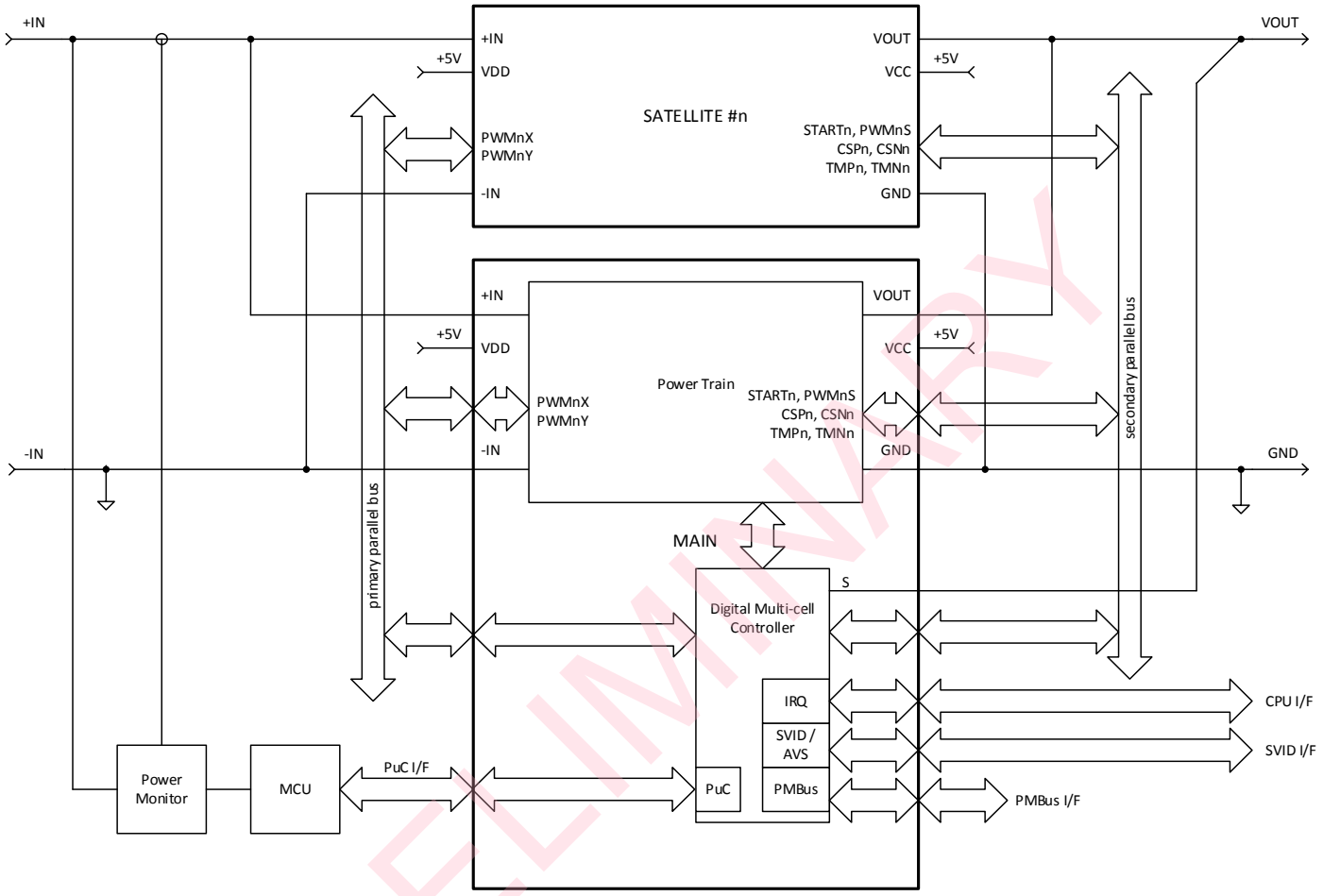
Secondary Parallel Bus

The secondary parallel bus contains multiple input and output signals to/from the digital multi-cell controller. Each SATELLITE in a parallel array, including the on-board power train of the MAIN converter, provides output current information through the differential CSPx and CSNx signals.



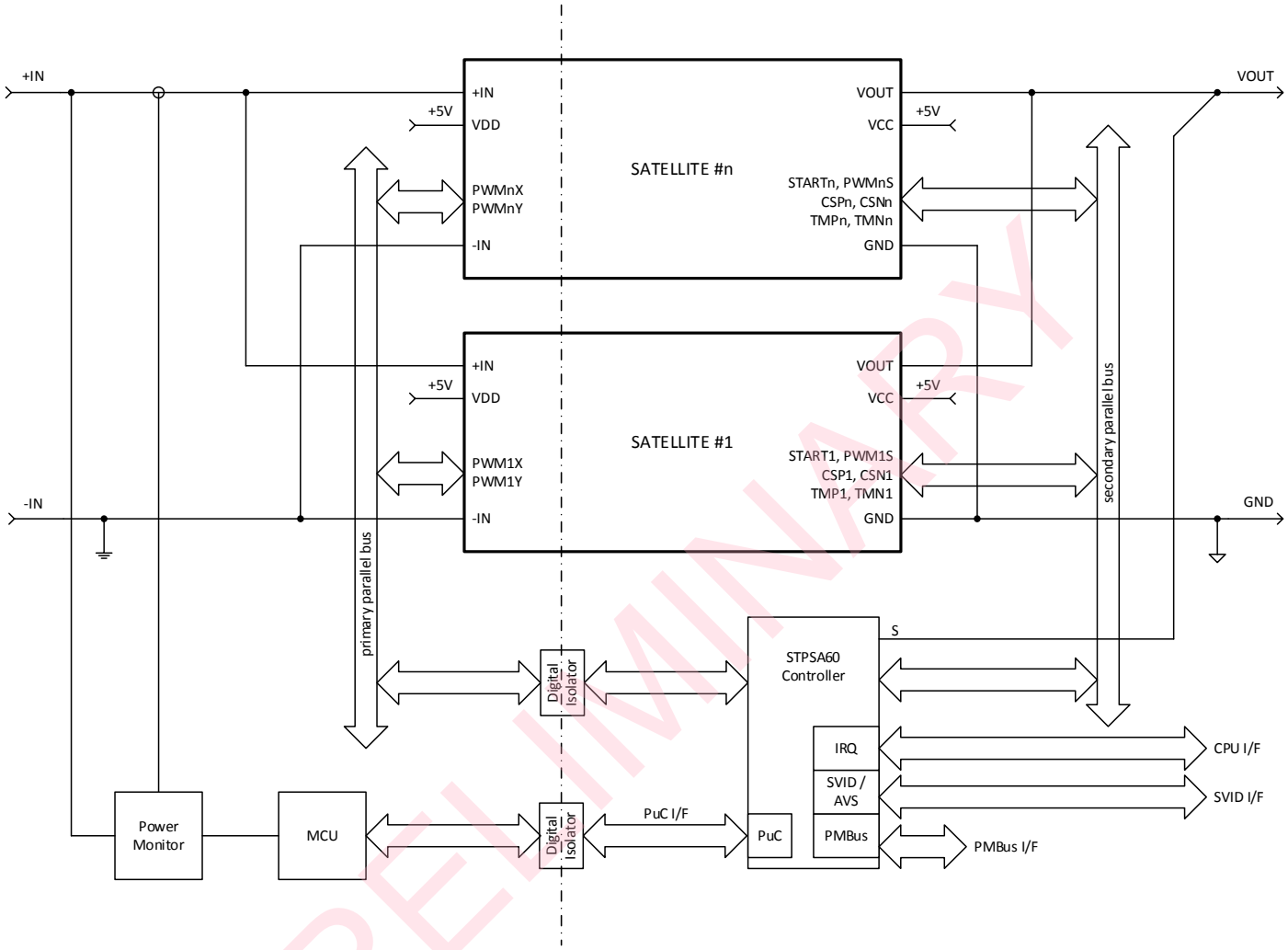
An NTC sensor is installed in proximity of each output inductor for temperature compensated output current measurement and the corresponding signal is fed to the digital multi cell controller via the TMPx pins. The TMN pin provides pseudo-differential transmission of the TMPx signals. The DPWM modulator generates the STARTx signal to synchronize the operation of the output synchronous rectifier with the PWMX and PWMY signals driving the input full bridge.

Paralleling – MAIN and SATELLITE Configuration



Paralleled MAIN and SATELLITE in a non-isolated configuration. The power train of both MAIN and SATELLITE Power Stamps is inherently isolated; the power path isolation can be shorted on the motherboard in non-isolated applications. Optional digital isolators can provide isolated feedback and isolated input telemetry.

Paralleling – STPSA60 and SATELLITE Configuration

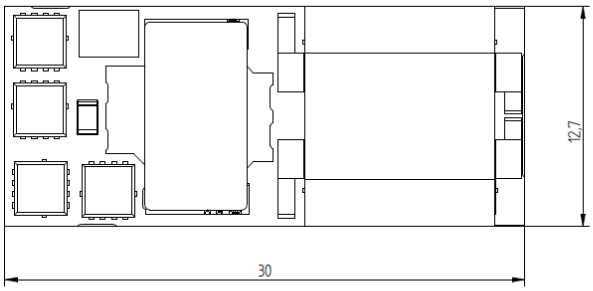


Paralleled SATELLITEs using an external STPSA60 controller installed on the motherboard. Digital isolators provide isolated feedback on the primary parallel bus and isolated input telemetry via the primary microcontroller interface.

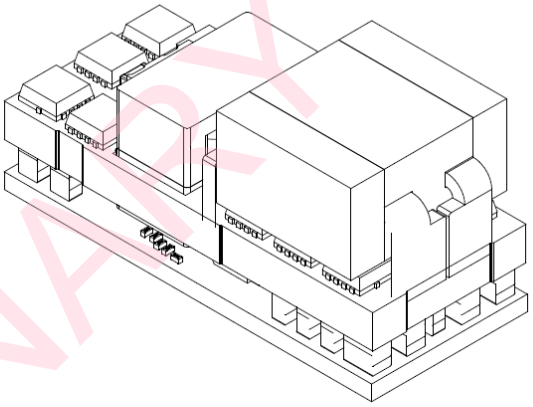
Safety Considerations

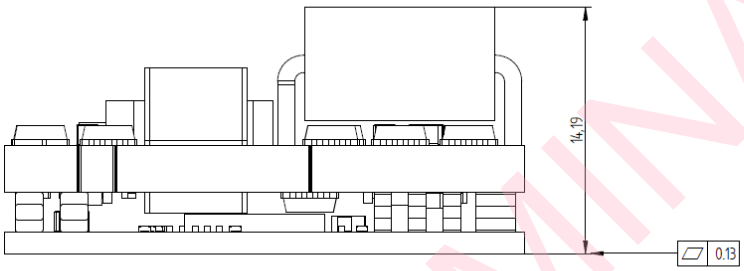
For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e. UL 60950-1 2nd, CSA C22.2 No. 60950-1-07, DIN EN 60950-1:2006 + A11 (VDE0805 Teil 1 + A11):2009-11; EN 60950-1:2006 + A11:2009-03.
For the converter output to meet the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements as well. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.
The Power Stamp series was tested using an external fast-acting fuse rated at TBD A, TBD VDC in the ungrounded input.

Mechanical Drawings – MAIN



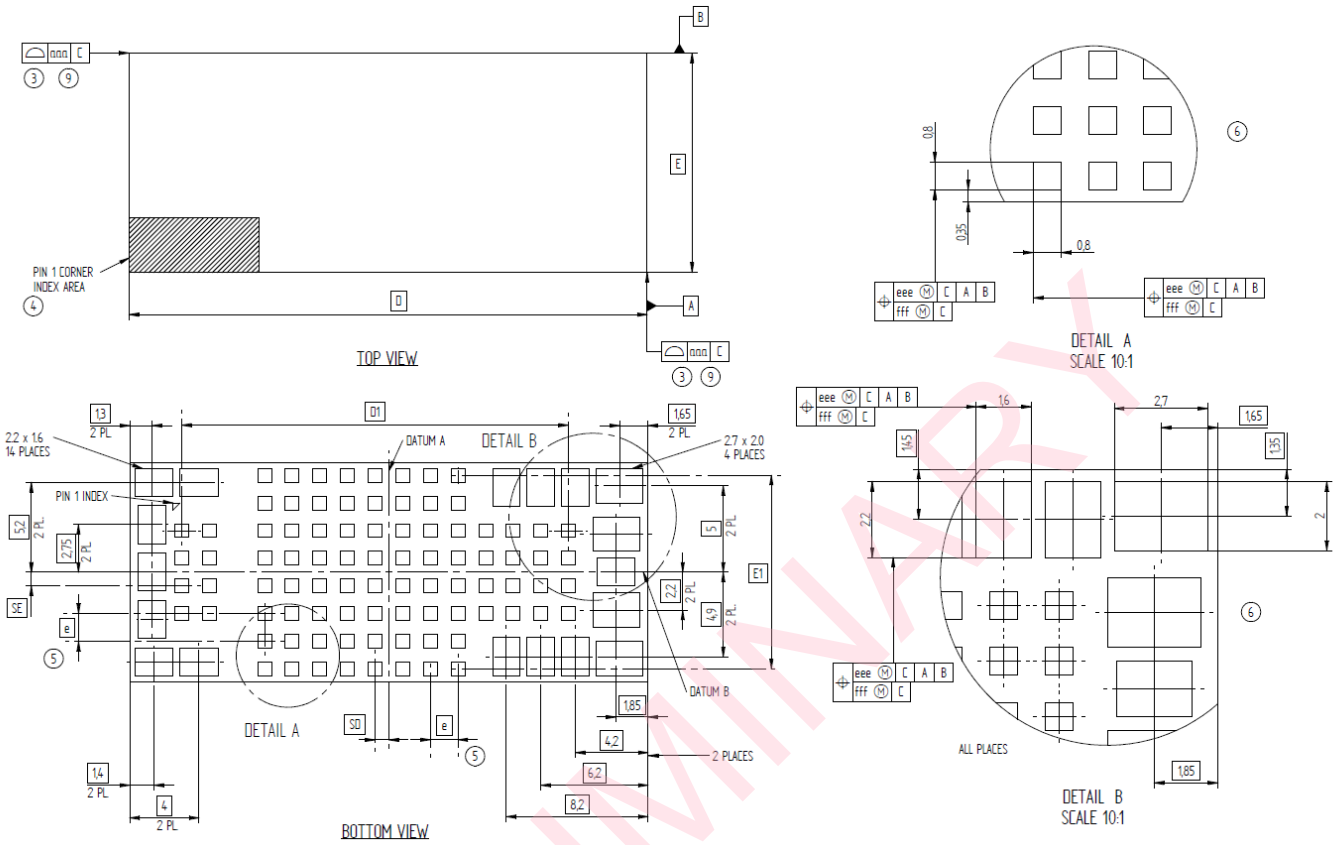
TOP VIEW

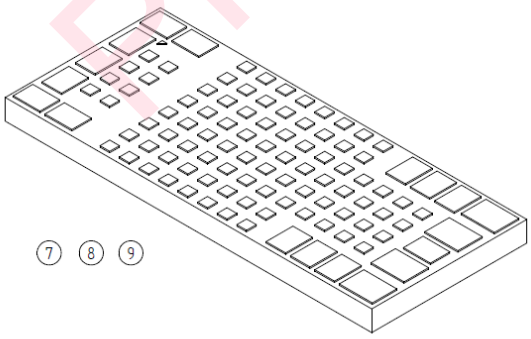




SIDE VIEW

PCB Pattern Design – MAIN





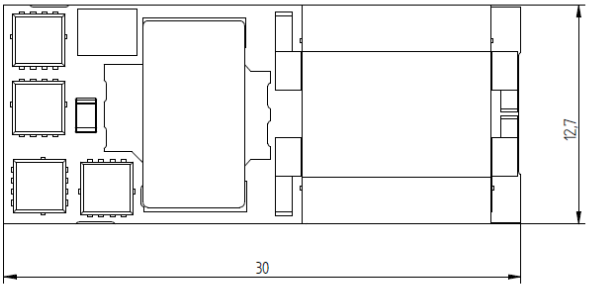
BOTTOM VIEW (typical)

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
D	–	30.00	–
E	–	12.70	–
D1		22.40 BSC	
E1		11.20 BSC	
e		1.60 BSC	
MD	–	15	–
ME	–	8	–
n	–	88	–
SD	–	0.80	–
SE	–	0.80	–

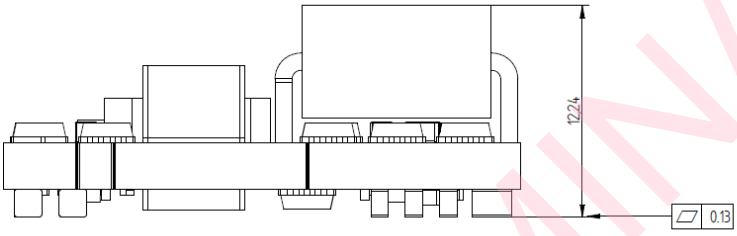
DIMENSION VARIATIONS	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.15
eee	0.15
fff	0.08

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DATUM "E" IS THE SEATING PLANE
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED, THE PIN IDENTIFIER MAY BE EITHER A LABEL, A MARKED FEATURE OR A CHAMFERED EDGE
5. DIMENSION 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS
6. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION
7. BOTTOM VIEW OF TYPICAL MODULE PCB SHOWN FOR ILLUSTRATION PURPOSES ONLY
8. OVERALL MODULE HEIGHT NOT TO EXCEED 18mm
9. SEE INDIVIDUAL MODULE DATA SHEET FOR DETAILED TOP AND SIDE VIEW

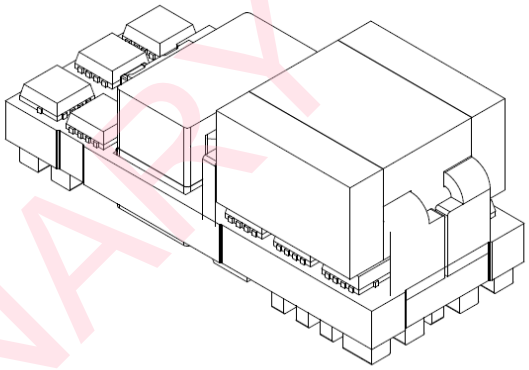
Mechanical Drawings – SATELLITE



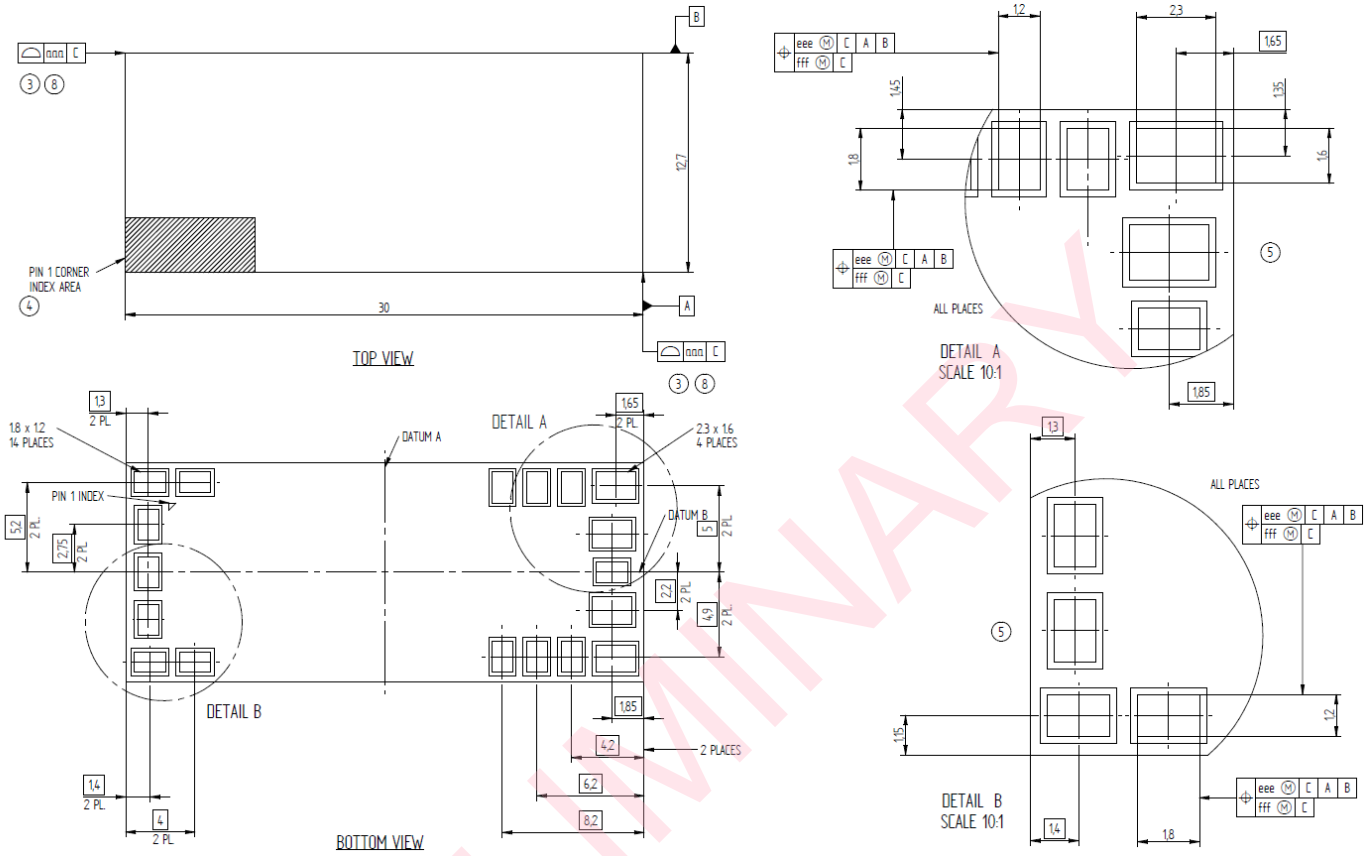
TOP VIEW



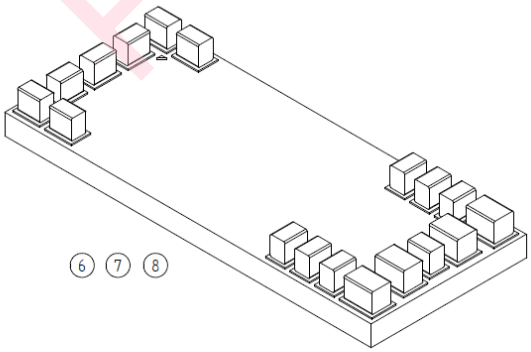
SIDE VIEW



PCB Pattern Design – SATELLITE



DIMENSION VARIATIONS	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.15
eee	0.15
fff	0.08



BOTTOM VIEW (typical)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DATUM "C" IS THE SEATING PLANE
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED, THE PIN IDENTIFIER MAY BE EITHER A LABEL, A MARKED FEATURE OR A CHAMFERED EDGE
5. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION
6. BOTTOM VIEW OF TYPICAL MODULE PCB SHOWN FOR ILLUSTRATION PURPOSES ONLY
7. OVERALL MODULE HEIGHT NOT TO EXCEED 18mm
8. SEE INDIVIDUAL MODULE DATA SHEET FOR DETAILED TOP AND SIDE VIEW

Surface Mount Information

Pick and Place
The Power Stamp modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300°C. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations
The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

Bottom Side / First Side Assembly
This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Lead Free Soldering
The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

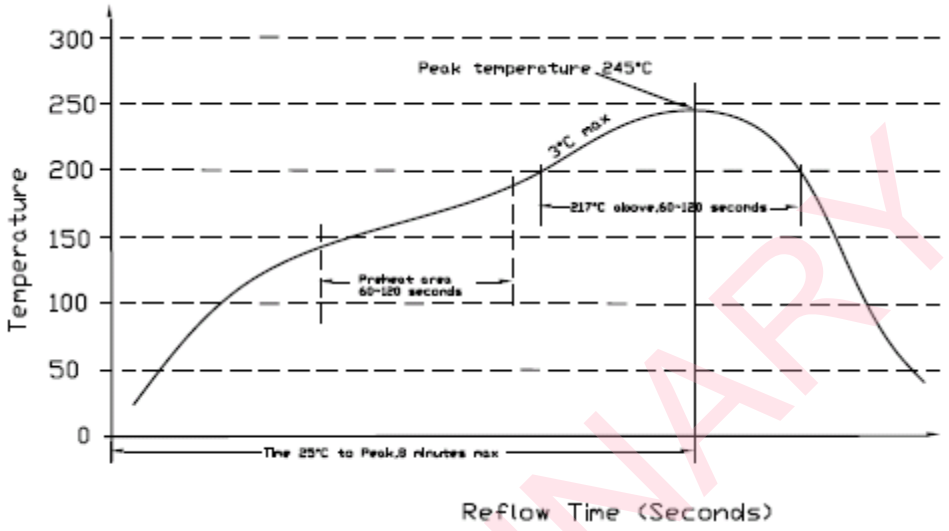
Pb-free Reflow Profile
Power Systems will comply with J-STD-020 Rev. C (Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in the Soldering Information section. Soldering outside of the recommended profile requires testing to verify results and performance.

MSL Rating
The Power Stamp modules have a MSL rating of TBD.

Pre-baking
This component has been designed, handled, and packaged ready for Pb-free reflow soldering. If the assembly shop follows JSTD-033 Rev. A guidelines, no pre-bake of this component is required before being reflowed to a PCB. However, if the J-STD-033 Rev A guidelines are not followed by the assembler, Bel recommends that the modules should be pre-baked @ 120~125°C for a minimum of 4 hours (preferably 24 hours) before reflow soldering.

Storage and Handling
The recommended procedures for moisture-sensitive surface mount packages are detailed in J-STD-033 Rev. A. Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of < 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40° C, < 90% relative humidity.

Soldering Information



The Power Stamp Alliance

The Power Stamp Alliance defines a standard product footprint and functions that provide a multiple-sourced, standard board-mounted solution for power conversion for 48Vin to low voltage, high current applications.

These 48V direct conversion DC-DC modules - or 'power stamps' - primarily target devices being used in large data centers (e.g. CPU, DDR, FPGA, ASIC), many of which are following the principles of the Open Compute Project (OCP).

Some of the first processor architectures addressed by the Power Stamp Alliance are the Intel VR13 Skylake CPUs, Intel VR13-HC Ice Lake CPUs, DDR4 memories, IBM POWER9 (P9) architecture processors and devices using the PMBus AVS protocol or SVID protocol.

48V single stage power conversion offers Open Compute Project and data center companies a range of business and technical benefits.

www.powerstamp.org

Revision History

Date	Revision	Notes	Approved
23/02/2018	1.0	First release	GM

For more information about these products, please consult tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS
Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

TECHNICAL REVISIONS
The appearance of products, including safety agency certifications pictured on labels, may change depending on the date of manufacturing. Specifications are subject to change without notice.