Features

- Supply Voltage: 2.7V to 5.5V
- Low Supply Current: 600μA per channel
- Rail to Rail Input and Output
- Bandwidth: 6 MHz
- Slew Rate: 4.5V/μs
- Excellent EMI Suppress Performance
- Offset Voltage: ±3mV Maximum
- Offset Voltage Temperature Drift: 1 μV/°C
- Low Noise: 19 nV/√Hz at 1kHz
- High Output Capability: 100mA
- –40°C to 125°C Operation Temperature Range
- Green, Popular Type Package
  - TP10-2: SOP-8
  - TP10-4: SOP-14

Applications

- E-Bike
- Motor Control
- Portable Audio

Description

The TP10 series are CMOS dual, and quad RRIO op-amps with low offset, low power and stable high frequency response. They incorporate 3PEAK's proprietary and patented design techniques to achieve very good AC performance with 6MHz bandwidth, 4.5V/μs slew rate and low distortion while drawing only 600μA of quiescent current per amplifier. The input common-mode voltage range extends 300mV beyond V– and V+, and the outputs swing rail-to-rail. The TP10 family can be used as plug-in replacements for many commercially available op-amps to reduce power and improve input/output range and performance.

The combination of features makes the TP10 ideal choices for motor control and portable audio amplification, sound ports, and other consumer Audio. The TP10 Op-amp is very stable, and it is capable of driving heavy capacitive loads such as those found in LCDs. The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

Order Information

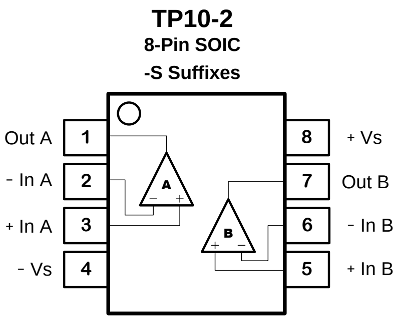
Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TP10-2-SR	-40 to 125°C	8-Pin SOP	TP102	3	Tape and Reel, 4000
TP10-4-SR	-40 to 125°C	14-Pin SOP	TP104	3	Tape and Reel, 2500

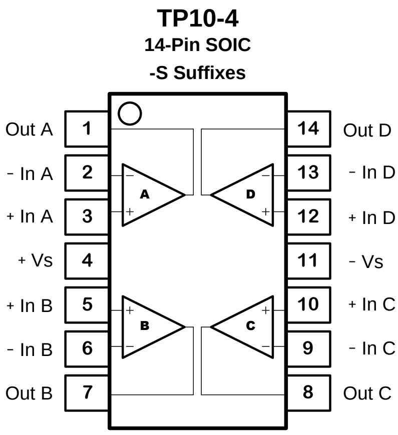
Table of Contents

Revision History

Date	Revision	Notes
2017/3/1	Rev.Pre	Pre-Release Version
2017/7/5	Rev.0	Release Version, confirm spec limit

Pin Configuration





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TP10-4-SR	-40 to 125°C	14-Pin SOP	TP104	3	Tape and Reel, 2500

Absolute Maximum Ratings Note 1

Parameters	Rating
Supply Voltage, $(+V_S)-(-V_S)$	7 V
Input Voltage	$(-V_S)-0.3$ to $(+V_S)+0.3$
Differential Input Voltage	±7V
Input Current: +IN, –IN Note 2	±10mA
Output Short-Circuit Duration Note 3	Infinite
Maximum Junction Temperature	150°C
Operating Temperature Range	–45 to 125°C
Storage Temperature Range	–65 to 150°C
Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD Rating

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP-8	158	43	°C/W
SOP-14	120	36	°C/W

Electrical Characteristics

All test condition is V_S = 5V, T_A = 25°C, R_L = 2kΩ, C_L =100pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_S	Supply Voltage Range		2.7		5.5	V
I_Q	Quiescent Current per Amplifier			600	900	μA
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V	70	95		dB
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V to 3V	-3		3	mV
V_{OS} TC	Input Offset Voltage Drift	T_A = -40°C to 125°C		2		μV/°C
I_B	Input Bias Current	T_A = 25 °C		1		pA
		T_A = 85 °C		25		pA
I_{OS}	Input Offset Current			1		pA
C_{IN}	Input Capacitance	Differential Mode		10		pF
		Common Mode		10		pF
Av	Open-loop Voltage Gain	R_{LOAD} = 10kΩ	80	100		dB
V_{CMR}	Common-mode Input Voltage Range		(V-) - 0.1		(V+) - 0.1	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3V	70	100		dB
Xtalk	Channel Separation	f = 1kHz, RL = 2kΩ		110		dB
Output Characteristics						
V_{OH}, V_{OL}	Maximum Output Voltage Swing	R_{LOAD} = 10kΩ		5	15	mV
I_{SC}	Output Short-Circuit Current			100		mA
I_O	Output Current	1V Output Drop Voltage		50		mA
AC Specifications						
GBW	Gain-Bandwidth Product			6		MHz
SR	Slew Rate	A_V = 1, V_{OUT} = 1.5V to 3.5V, C_{LOAD} = 60pF, R_{LOAD} = 1kΩ		4.5		V/μs
t_S	Settling Time, 0.1%	AV = 1, 2V Step, C_{LOAD} = 60pF, R_{LOAD} = 1kΩ		0.8		μs
	Settling Time, 0.01%			1		μs
PM	Phase Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 60pF		60		°
GM	Gain Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 60pF		15		dB
Noise Performance						
E_N	Input Voltage Noise	f = 0.1Hz to 10Hz		8		$μV_{PP}$
e_N	Input Voltage Noise Density	f = 1kHz		19		nV/√Hz
i_N	Input Current Noise	f = 1kHz		2		fA/√Hz
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, AV =1, RL = 2kΩ, VOUT = 1Vp-p		0.003		%

Typical Performance Characteristics

V_S = 5V, V_{CM} = 2.5V, RL = Open, unless otherwise specified.

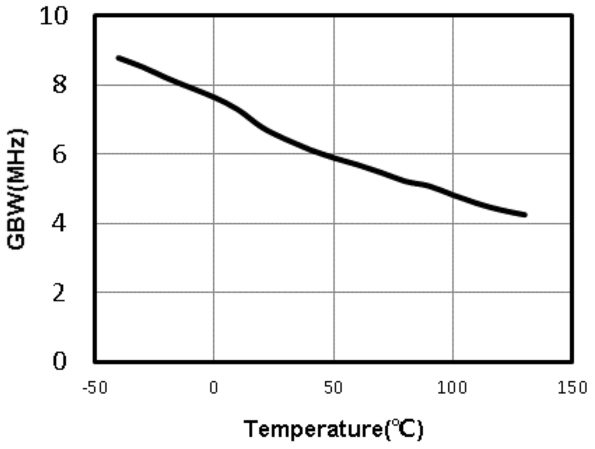


Figure 1. Unity Gain Bandwidth vs. Temperature

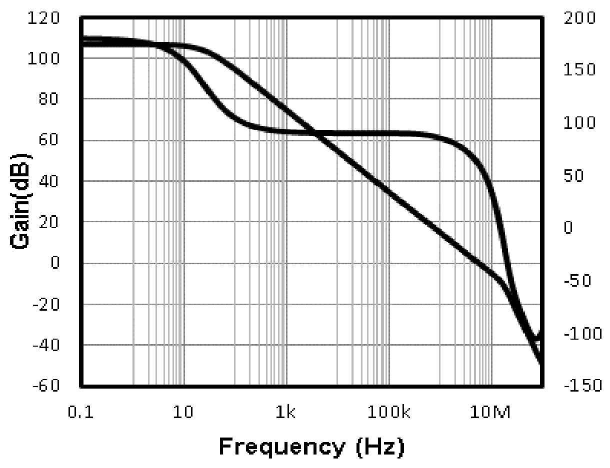


Figure 2. Open-Loop Gain and Phase

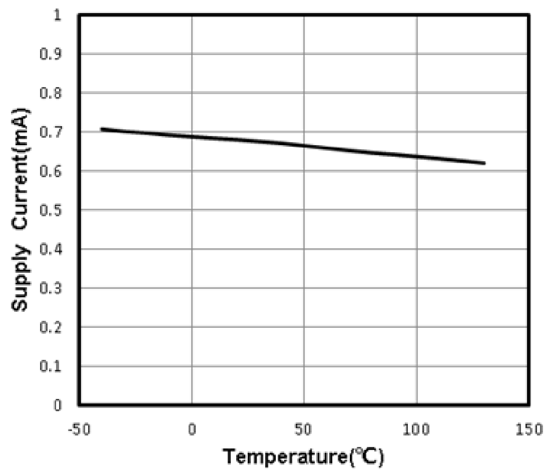


Figure 3. Supply Current vs. Temperature

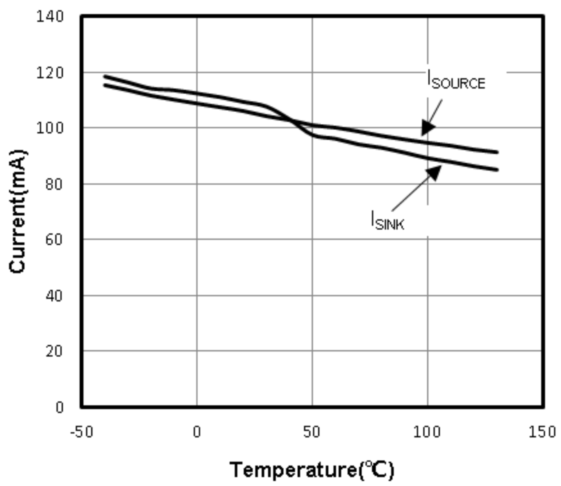


Figure 4. Short Circuit Current vs. Temperature

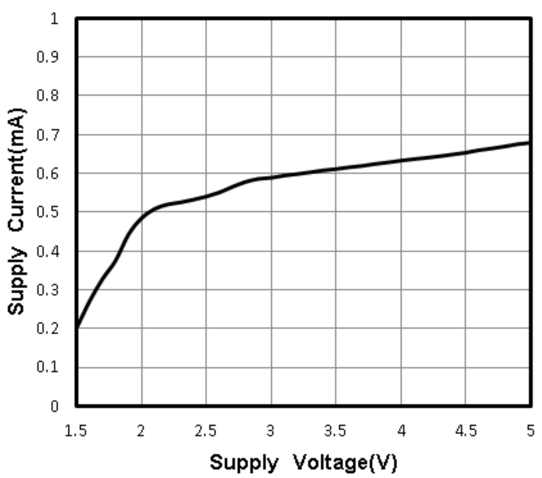


Figure 5. Quiescent Current vs. Supply Voltage

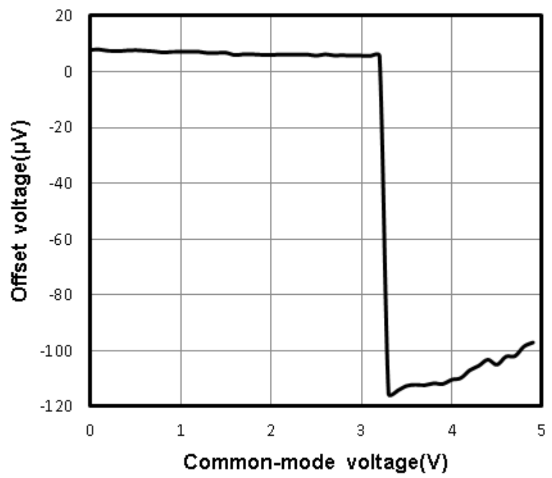


Figure 6. Offset Voltage vs. Common-Mode Voltage

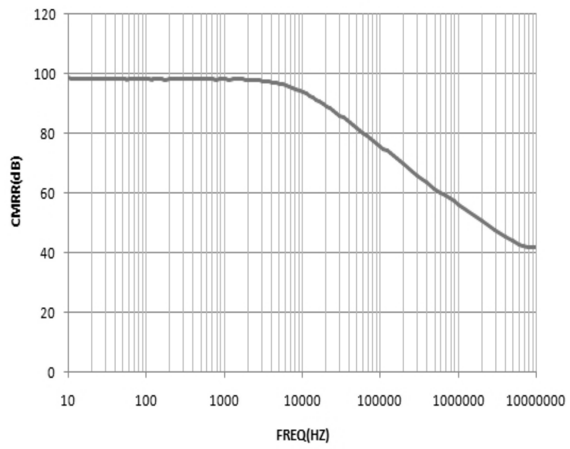


Figure 7. CMRR vs. Frequency

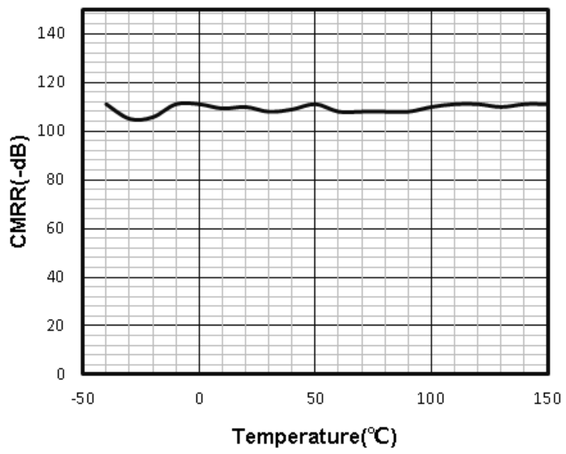


Figure 8. CMRR vs. Temperature

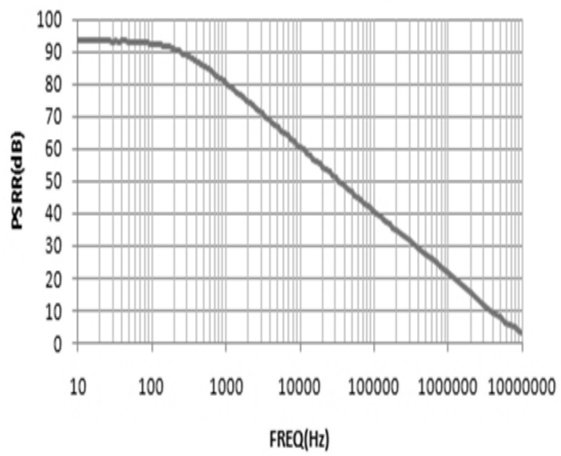


Figure 9. Power-Supply Rejection Ratio

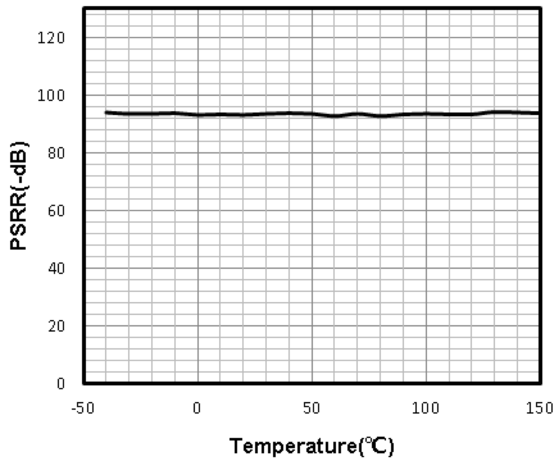


Figure 10. PSRR vs. Temperature

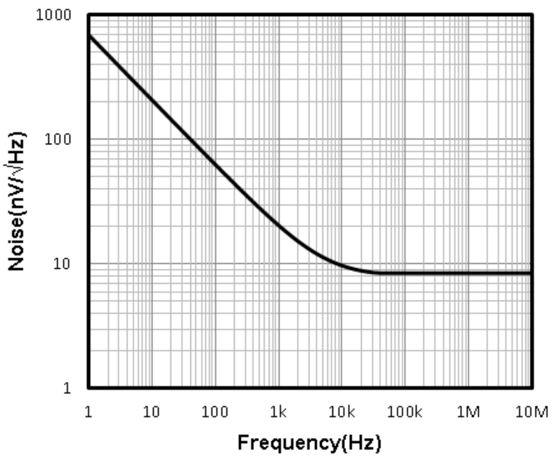


Figure 11. Input Voltage Noise Spectral Density

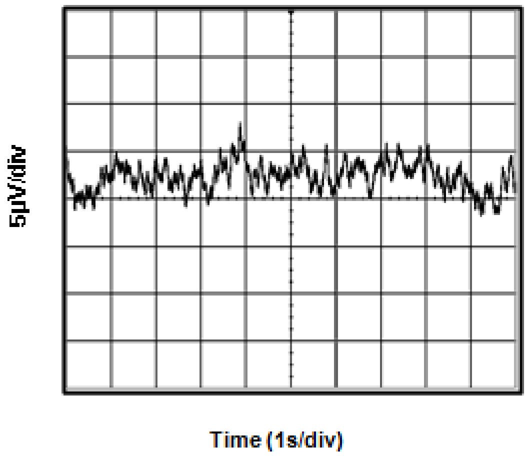


Figure 12. 0.1 Hz to 10 Hz Input Voltage Noise

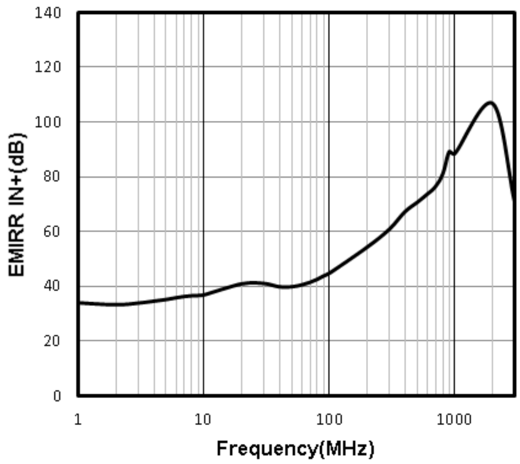


Figure 13. EMIRR IN+ vs. Frequency

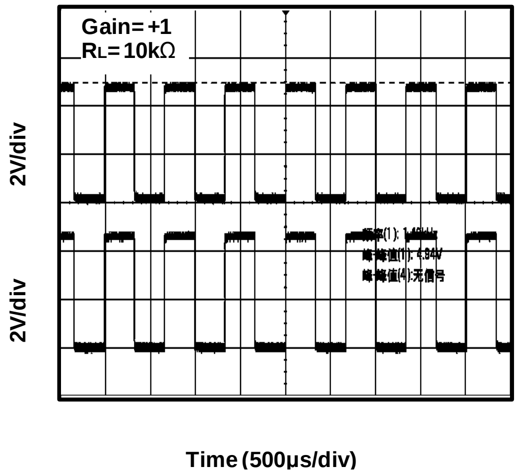


Figure 14. Large-Scale Step Response

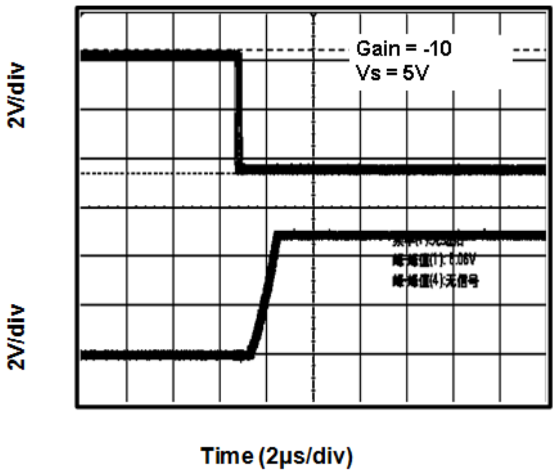


Figure 15. Negative Over-Voltage Recovery

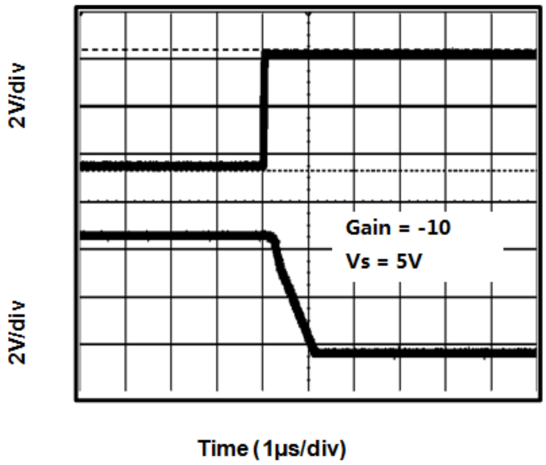


Figure 16. Positive Over-Voltage Recovery

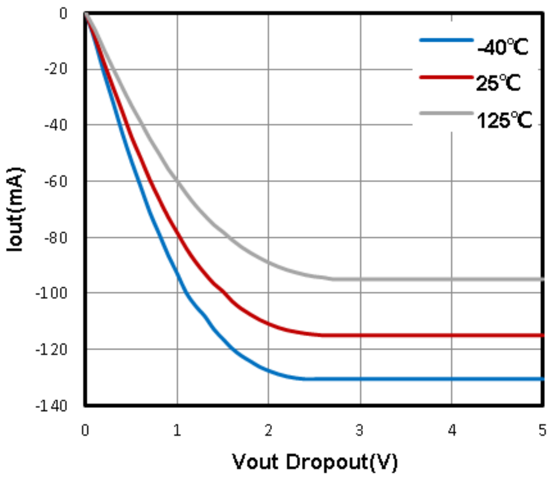


Figure 17. Negative Output Swing vs. Load Current

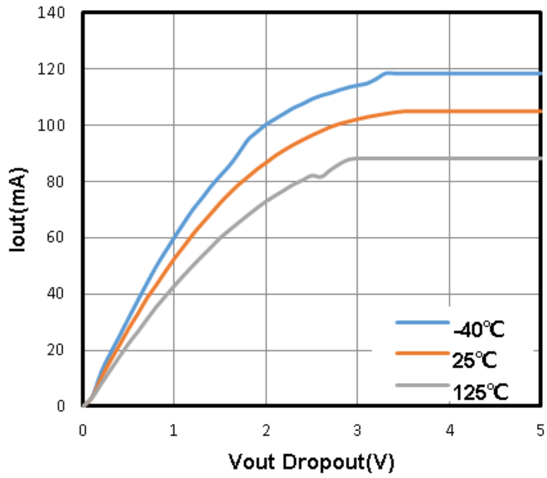


Figure 18. Positive Output Swing vs. Load Current

Application Information

Low Supply Voltage and Low Power Consumption

The TP10 family of operational amplifiers can operate with power supply voltages from 2.7 V to 5.5 V. Each amplifier draws only 600 μA quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding high capacitive load driving capability and stable wide bandwidth. The TP10 family is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable for any capacitive load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

Ground Sensing and Rail to Rail Output

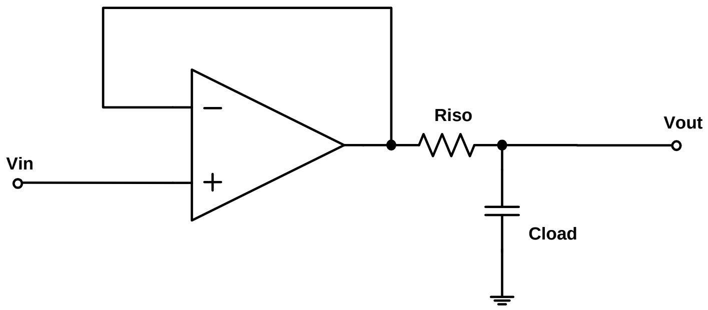
The TP10 family has excellent output drive capability, delivering over 100 mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300 mV beyond either rail, the op-amp can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

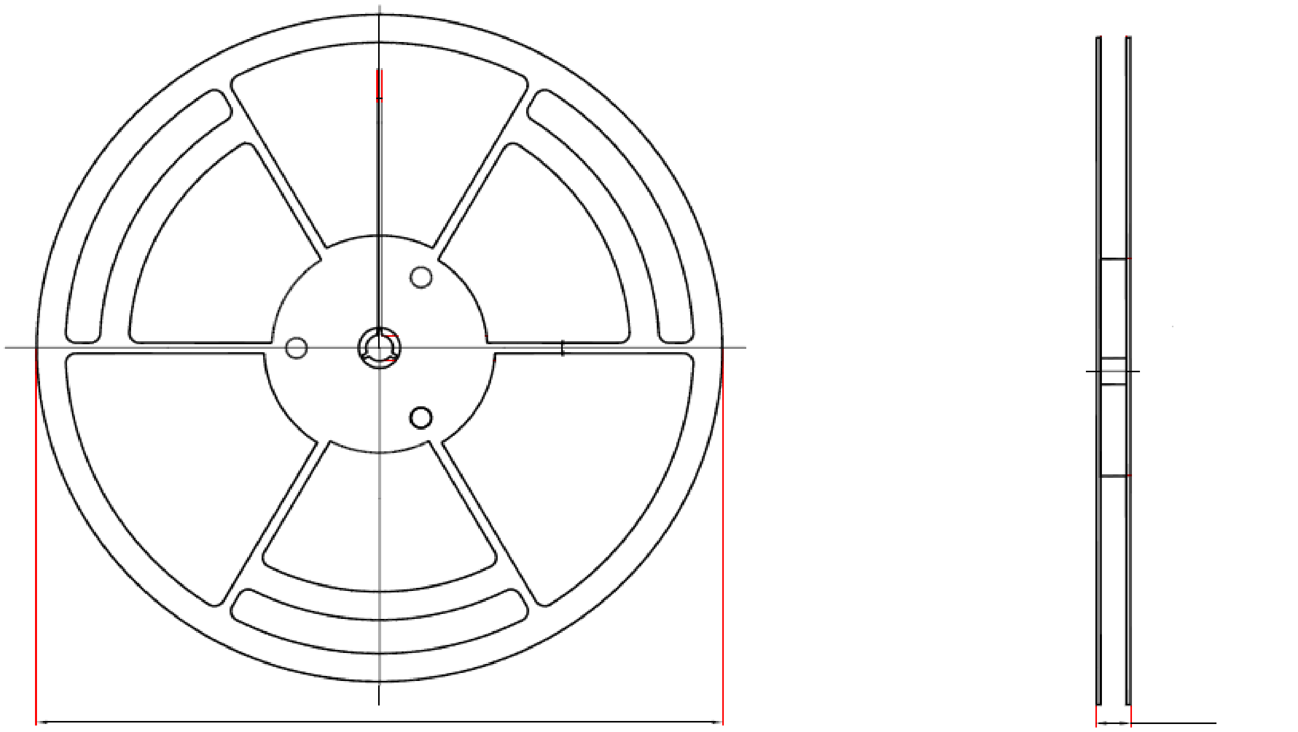
Driving Large Capacitive Load

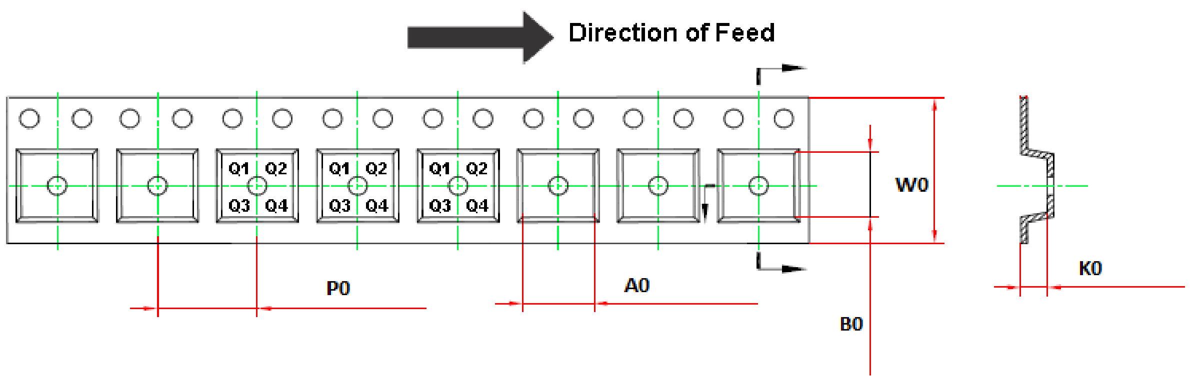
The TP10 family of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for "Phase Margin vs. Load Capacitance". As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP10 OPA family (e.g., > 200 pF when G = +1V/V), a small series resistor at the output (RISO in Figure 3) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies.



Tape And Reel Information





Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TP10-2-SR	8-Pin SOIC	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TP10-4-SR	14-Pin SOIC	330.0	21.6	6.5	9.0	2.1	8.0	16.0	Q1

Package Outline Dimensions

SOIC-8

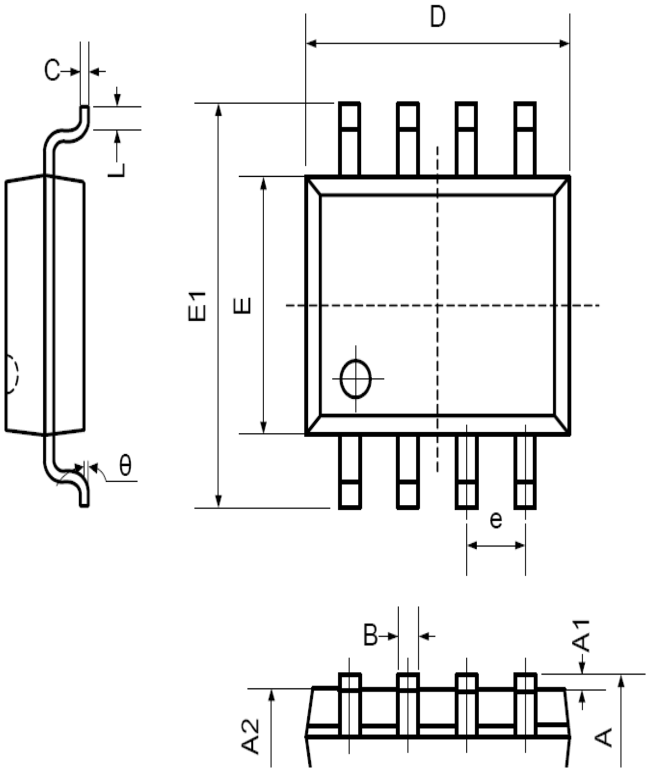
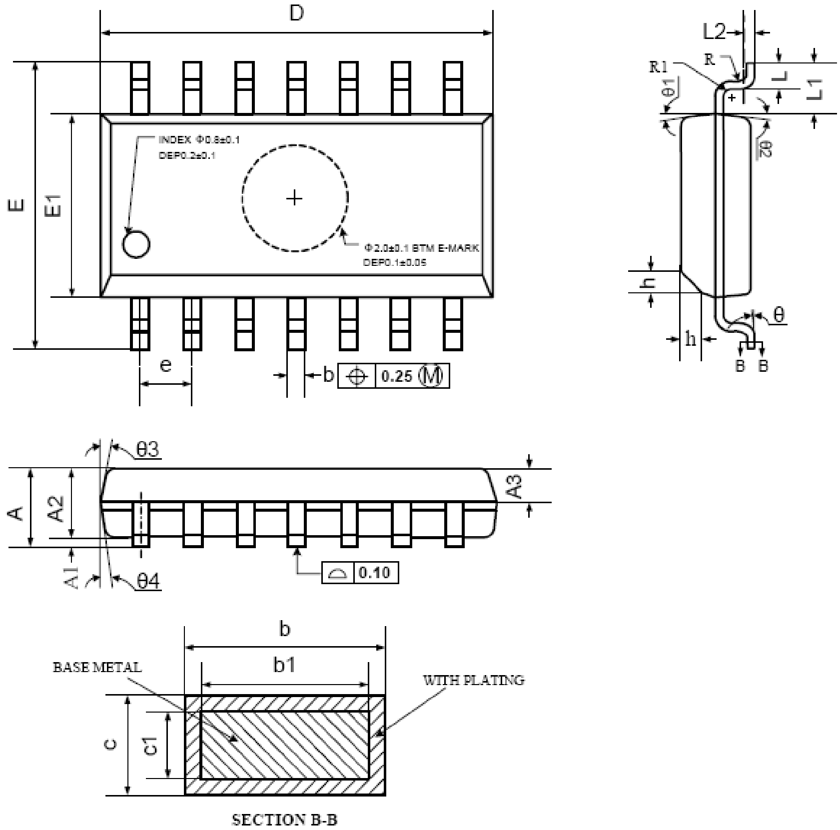


Table 1.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-14



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36		0.49
b1	0.35	0.40	0.45
c	0.16		0.25
c1	0.15	0.20	0.25
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07		
R1	0.07		
h	0.30	0.40	0.50
θ	0°		8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°