SPC574S60E3, SPC574S64E3

32-bit Power Architecture microcontroller for automotive ASILD applications

Datasheet - production data



eTQFP100 (14 x 14 x 1.0 mm)

Features



- AEC-Q100 qualified
- High performance e200z4d dual core
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 140 MHz
  - Dual issue 5-stage pipeline in-order execution core
  - Variable Length Encoding (VLE)
  - Core MPU
  - Floating Point, End-to-End Error Correction
  - 8 KB instruction cache with error detection code
  - 32 KB local data RAM and 4 KB data cache along with 8 KB instruction cache
- 1600 KB (1.5 MB code + 64 KB data) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 128 KB on-chip RAM (96 KB on chip RAM + 32 KB local data RAM)
- Multi-channel direct memory access controller (eDMA) with 32 channels
- Comprehensive new generation ASILD safety concept
  - ASILD SEooC approach (Safety Element out of Context)
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - End-to-end Error Correction Code (e2eECC) logic
  - Cyclic redundancy check (CRC) unit
- 8 enhanced 12-bit SAR analog converters
  - 2 sets of: 3 ADCs and one supervisor ADC
  - 1.5 µs conversion time at 12 MHz
  - Up to 32 physical channels
  - Dual Programmable CTU
- 4 general purpose eTimer units (6 channels each)
- 4 FlexPWM units
  - 2 (4 channels each) used for motor control with hardware synchronization between the control systems
  - 2 (2 channels each) used for SWG emulation
- Communication interfaces
  - 4 LINFlexD modules
  - 4 deserial serial peripheral interface (DSPI) modules
  - 2 MCAN interfaces with advanced shared memory scheme (808 x 32-bit words for MCAN0 and 520 x 32-bit words for MCAN1) and CAN-FD support
  - 1 FlexRay module with 2 channels, 128 message buffers
  - 2 SENT interfaces (3 channels each)
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus Class 3 debug and trace interface
- On-chip CAN/UART Bootstrap loader with BAF. Physical Interface (PHY) can be UART
- Advanced and flexible supply scheme
  - On-chip voltage regulator for 1.2 V core logic supply. Bypass mode supported for external 1.2 V core logic supply
  - 3.3 V or 5 V IO and ADC supply (2 independent power domains available)
- Junction temperature range -40 °C to 150 °C

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Contents

1 Introduction 4

1.1 Document overview 4

1.2 Description 4

1.3 Feature overview 7

1.4 Block diagram 9

2 Package pinouts and signal descriptions 13

2.1 Package pinouts 13

2.2 Pin descriptions 14

2.3 Package pads/pins 14

3 Electrical characteristics 20

3.1 Introduction 20

3.2 Parameter classification 20

3.3 Absolute maximum ratings 21

3.4 Electromagnetic compatibility (EMC) 22

3.5 Electrostatic discharge (ESD) 22

3.6 Operating conditions 22

3.7 Thermal characteristics 25

3.7.1 Package thermal characteristics 25

3.7.2 Power considerations 26

3.8 Current consumption 28

3.9 I/O pad electrical characteristics 29

3.9.1 I/O pad types 29

3.9.2 I/O input DC characteristics 29

3.9.3 I/O output DC characteristics 32

3.10 RESET electrical characteristics 35

3.11 Power management 38

3.11.1 Overview 38

3.11.2 Voltage regulator electrical characteristics 39

3.11.3 Power Schemes 41

3.11.4 Decoupling capacitors 44

3.11.5 Power management electrical characteristics 47
3.12 PMU monitor specifications 48
3.12.1 Nomenclature 48
3.12.2 Power up/down sequencing 49
3.13 Platform Flash controller configuration 50
3.14 Flash memory electrical characteristics 50
3.15 PLL0/PLL1 electrical characteristics 53
3.16 External oscillator (XOSC) electrical characteristics 54
3.17 Internal RC oscillator (16 MHz) electrical characteristics 57
3.18 ADC electrical characteristics 57
3.18.1 Introduction 57
3.18.2 ADC electrical characteristics 58
3.19 Temperature sensor 62
3.20 JTAG interface timings 62
3.21 Nexus interface timing 64
3.22 DSPI CMOS master mode timing 66
3.22.1 Classic timing 66
3.22.2 Modified timing 69

4 Package information 72
4.1 eTQFP100 package information 72
4.2 eTQFP144 package information 76

5 Ordering information 78

6 Revision history 79

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The SPC574Sx is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC574Sx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of Chassis and Safety electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 140 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. SPC574Sx device feature summary (superset configuration)

Feature		Description
Processor	Main Core	e200z420n3
	Checker core	e200z419
	Local data RAM	32 KB Data
	VLE	Yes
	Main processor frequency	140 MHz
	Instruction cache	8 KB
	Data cache	4 KB
Interrupt controller (including interrupt controller checker)		1
Software watchdog timer		1
System timers		1 AUTOSAR® STM 1 PIT with eight 16-bit channels
DMA (including DMA checker)		1
DMA channels		32
SMPU		Yes (8 regions)
System SRAM (in addition to core local data RAM)		96 KB
Code Flash memory		1.5 MB

Table 1. SPC574Sx device feature summary (superset configuration) (continued)

Feature	Description
Data Flash memory (EEPROM)	64 KB
UTEST Flash memory	16 KB
Boot assist Flash (BAF)	16 KB
CRC	1
LINFlexD	4
DSPI	4
MCAN	2
FlexRay	1 (128 MB)
SENT	2 x 3 channels
FlexPWM	2 x 4 channels (for motor control) + 2 x 2 channels (for SWG emulation via PWM)
eTimer	4 x 6 channels
ADC (SAR)	8
CTU (Cross Triggering Unit)	2
Temperature sensor	2
Self-test control unit (memory and logic BIST)	1
FCCU	1
MEMU	1
RCOSC	1
XOSC	1
PIT	1 x 8 channels
STM	1
PLL	Dual PLL with FM
Nexus	3(1)
Sequence processing unit (SPU)	1
External power supplies	Single supply mode: 3.3 V or 5 V
Junction temperature	-40 °C to 150 °C
Package	eTQFP100

1. Including trace for the crossbar masters (data & instruction trace on core and data trace on eDMA). 4 MDO pins Nexus trace port.

Table 2. SPC574S60Ex, SPC574S64Ex device configuration differences

	SPC574S60 (full option configuration)	SPC574S64 (full option configuration)
Flash	1 MB(1)	1.5 MB
RAM	96 KB(2)	128 KB

Table 2. SPC574S60Ex, SPC574S64Ex device configuration differences (continued)

	SPC574S60 (full option configuration)	SPC574S64 (full option configuration)
FlexRay	—	1
Others	Aligned to *Table 1: SPC574Sx device feature summary (superset configuration)*.	

1. Flash blocks excluded on SPC574S60:
   256K Block B0F12 [0x010C_0000 … 0x010F_FFFF]
   256K Block B0F13 [0x0110_0000 … 0x0113_FFFF]
2. SRAM area excluded on SPC574S60 [0x4001_0000…0x4001_7FFF]

1.3 Feature overview

On-chip modules within the SPC574Sx include the following features:

- Operating parameters
  - Fully static operation, up to 140 MHz
  - Up to -40 °C to 150 °C junction temperature operating range
- Power management features
  - HALT mode — core clocks are stopped but the PLL is configurable
  - STOP mode — all clocks are stopped including the PLLs
  - Software-controlled clock gating of peripherals
- High performance, low cost e200z420 core processor
  - 32-bit CPU core complex (e200z420n3)
  - Compliant with the Power Architecture® embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. Optional encoding of mixed 16-bit and 32-bit instructions makes it possible to achieve significant code size footprint reduction.
- Advanced and flexible supply scheme
  - Internal or External regulator mode for 1.2 V supply
  - 3.3 V +/- 5% or 5 V +/- 5%
  - Up to 2 power rails for GPIOs and 2 power rails for analog/input pins enabling supply redundancy concept.
  - The 4 power rails can be supplied in independent way (depending on selected package and device configuration)
- Designed with EMI reduction techniques
  - Internal phase-locked loop
  - Frequency modulation of system clock frequency
  - On-chip regulator
  - Controlled I/O slew rate
- Advanced microcontroller bus architecture (AMBA) crossbar switch (XBAR) providing concurrent access to peripherals, Flash memory and SRAM
  - 4 master ports: FlexRay, DMA, CPU instruction bus and CPU data bus
  - 5 slave ports: Flash Controller, TCM Back-door (Port to local Data RAM), RAM controller, PBRIDGE0 and PBRIDGE1
- 32-bit internal address bus, 32-bit internal data bus
- ECC (Error Correction Code) Flash memory with Flash controller
  - Up to 1.5 MB Code Flash—single module with prefetch buffer and 256-bit data access port
  - 64 KB Data Flash—single module with prefetch buffer and 256-bit data access port
- Up to 96 KB ECC SRAM with RAM controller (in addition to 32 KB core local data RAM)
- 16 KB dedicated OTP Flash for embedded boot code
  - Boot Assisted Flash (BAF)
  - Supports internal Flash programming via a serial link (UART and MCAN)

- System timers:
  - 1 x STM (AUTOSAR®) (4 compare channels)
    1 x PIT (8 channels)
    4 x eTimers (6 channels each)
  - System watchdog timer (SWT)
    32-bit timer
    Oscillator clock for timer operation
    Programmable selection of reset or interrupt on an initial time-out
    Enabled out of reset
- Safety and integrity features:
  - Clock Monitor Unit (CMU) for safe oscillator/PLL control using internal RC oscillator reference
  - Watchdog with time window for reload
  - Memory Protection Unit (MPU): 8 regions with 32-bit granularity
  - Register protected accesses to critical peripherals
- Interrupt controller (INTC) with dedicated interrupt source channels, including software interrupts and 32 priority levels
- 12-bit analog-to-digital converter (ADC) with a conversion time of 1.5 µs at maximum operating frequency
  - 16 high-precision channels for each group of 4 ADCs
- 4 general purpose eTimer units, with 6 channels each
- 4 FlexPWM units (2 units with 4 channels each and 2 units with 2 channels each)
- Up to 4 Local Interconnect Network (LIN) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev. 2.1
- 4 DSPI (Deserial Serial Peripheral Interface) modules for full-duplex, synchronous, communications with external devices
- 2 MCAN (with CAN-FD support)
- Frequency-modulated phase-locked loop (FMPLL)
- Configurable general purpose pins supporting input and output operations: 62 GPIO + 17 GPI/ADC input only (eTQFP100 - default bonding option) and 64 GPIO + 15 GPI/ADC input only (eTQFP100 - bonding option upon demand)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class 3
- Device/board boundary scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- SPC574Sx family members are offered in the 100-pin eTQFP, 0.5 mm pitch, 14 mm × 14 mm outline package type.

Note: One of four sources can be used as the system clock for this device:

- *External crystal oscillator 4–40 MHz (XOSC)*
- *Internal RC oscillator 16 MHz (IRCOSC)*
- *Primary PLL*
- *Secondary PLL*

1.4 Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. Block diagram

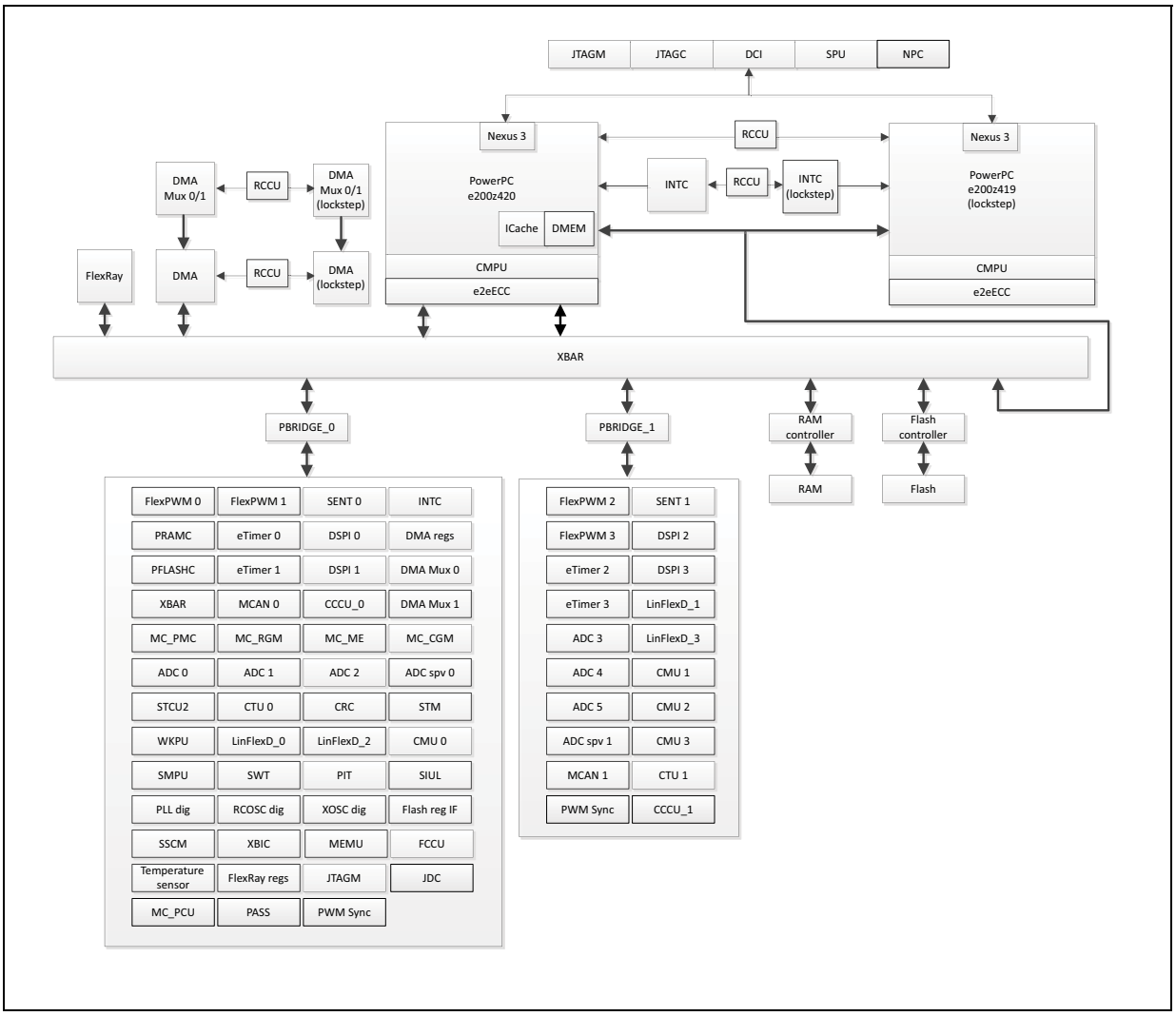


Table 3 summarizes the functions of all blocks present in the SPC574Sx series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Table 3. SPC574Sx series block summary

Block	Function
e200z4 CPU	Allows single clock instruction execution
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to-digital converter
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the PIT

Table 3. SPC574Sx series block summary (continued)

Block	Function
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Direct Memory Access (DMA)	Performs complex data transfers with minimal intervention from a host processor via 32 programmable channels.
DMACHMUX	Allows to route a defined number of DMA peripheral sources to the DMA channels
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase locked loop (PLL0)	Output independent of core clock frequency
Frequency-modulated phase-locked loop (PLL1)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
PBRIDGE	System bus to peripheral bus interface
RAM controller	Acts as an interface between the system bus and the integrated system RAM
System RAM	Supports read/write accesses mapped to the SRAM memory from any master
Flash memory controller	Acts as an interface between the system bus and the Flash memory module
Flash memory	Up to 1.5 M of programmable, non-volatile Flash memory for code and 32 KB for data
IRCOSC	Controls the internal 16 MHz RC oscillator system
XOSC	Controls the on-chip oscillator (XOSC) and provides the register interface for the programmable features
JTAG Master	Provides software the option to write data for driving JTAG
JTAG Data Communication Module (JDC)	Provides the capability to move register data between the IPS and JTAG domains
PASS	Programs a set of Flash memory access protections, based on user programmable passwords
Sequence Processing Unit (SPU)	Provides on-device trigger functions similar to those found on a logic analyzer
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
MC_PMC	Contains registers that enable/disable the various voltage monitors
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device

Table 3. SPC574Sx series block summary (continued)

Block	Function
eTimer	Has six 16-bit general purpose counters, where each counter can be used as an input capture or output compare function
FCCU	Collects fault event notifications from the rest of the system and translates them into internal and/or external system reactions
RCCU	Compares input signals and issues an alarm in the case of a mismatch
MEMU	Collects and reports error events associated with ECC (Error Correction Code) logic used on SRAM, DMA RAM and Flash memory
XBIC	Verifies the integrity of the attribute information for crossbar transfers and signals the Fault Collection and Control Unit (FCCU) when an error is detected
STCU2	Handles the BIST procedure
CRC	Controls the computation of CRC, off-loading this work from the CPU
RegProt	Protects several registers against accidental writing, locking their value till the next reset phase
Temperature sensor	Monitors the device temperature
Debug Control Interface	Provides debug features for the MCU
Nexus Port Controller	Monitors a variety of signals including addresses, data, control signals, status signals, etc.
Nexus Multimaster Trace Client	Monitors the system bus and provides real-time trace information to debug or development tools
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
System integration unit (SIUL)	Provides control over all the electrical pad controls and up to 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which one can cause non-maskable interrupt requests or wakeup events.
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Decorated Storage Memory Controller (DSMC)	Decorated Storage Memory Controller
CMU	Used to validate the target clock within a specific frequency range and to measure the clock frequency.
Power Management Controller (MC_PMC)	Contains registers that enable/disable the various voltage monitors

Table 3. SPC574Sx series block summary (continued)

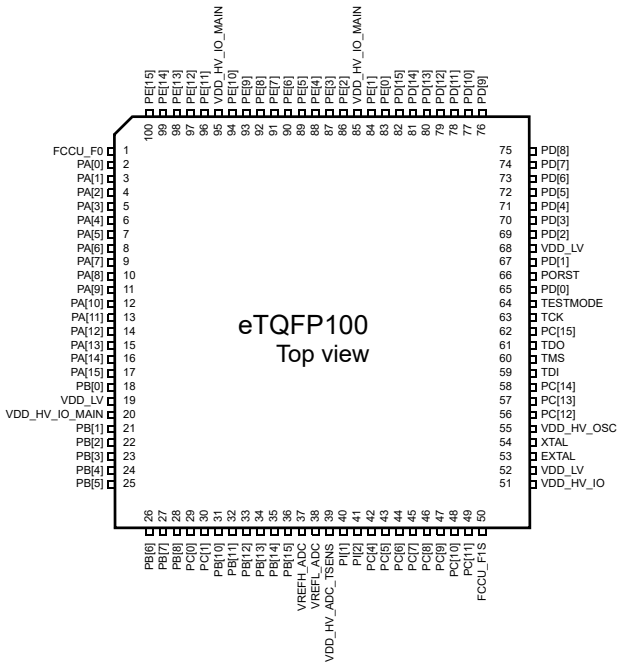
Block	Function
FlexPWM	Comprises a set of PWM sub-modules where each sub-module drives three PWM output signals.
PWMSync	Synchronizes the FlexPWM IPs during the motor control operation.
MCAN	Filters the incoming messages, using dedicated filter structures organized in an external Message RAM.
SENT	Enable the SENT protocol transmission.

2 Package pinouts and signal descriptions

2.1 Package pinouts

The eTQFP100 pinout is provided in the following figure. For pin signal descriptions, please refer to the device reference manual.

Figure 2. eTQFP 100-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC574Sx devices.

For information on the signal descriptions and related information about the functionality and configuration of the SPC574Sx devices, refer to the “Signal description” chapter in the devices’ reference manual.

2.3 Package pads/pins

Table 4 shows the cross-mapping between pads and the eTQFP100 pinout.

Table 4. Cross-mapping between pads and package pins

PAD	Port pin name	eTQFP 100 pin
PAD_FCCU_F0	FCCU_F0	1
PAD[0]	PA[0]	2
PAD[1]	PA[1]	3
PAD[2]	PA[2]	4
PAD[3]	PA[3]	5
PAD[4]	PA[4]	6
PAD[5]	PA[5]	7
PAD[6]	PA[6]	8
PAD[7]	PA[7]	9
PAD[8]	PA[8]	10
PAD[9]	PA[9]	11
PAD[10]	PA[10]	12
PAD[11]	PA[11]	13
PAD[12]	PA[12]	14
PAD[13]	PA[13]	15
PAD[14]	PA[14]	16
PAD[15]	PA[15]	17
PAD[16]	PB[0]	18
PAD[17]	PB[1]	21
PAD[18]	PB[2]	22
PAD[19]	PB[3]	23
PAD[20]	PB[4]	24
PAD[21]	PB[5]	25
PAD[22]	PB[6]	26
PAD[23]	PB[7]	27
PAD[24]	PB[8]	28
PAD[25]	PB[9]	—
PAD[26]	PB[10]	31
PAD[27]	PB[11]	32
PAD[28]	PB[12]	33
PAD[29]	PB[13]	34
PAD[30]	PB[14]	35
PAD[31]	PB[15]	36
PAD[32]	PC[0]	29
PAD[33]	PC[1]	30

Table 4. Cross-mapping between pads and package pins (continued)

PAD	Port pin name	eTQFP 100 pin
PAD[34]	PC[2]	—
PAD[35]	PC[3]	—
PAD[36]	PC[4]	42
PAD[37]	PC[5]	43
PAD[38]	PC[6]	44
PAD[39]	PC[7]	45
PAD[40]	PC[8]	46
PAD[41]	PC[9]	47
PAD[42]	PC[10]	48
PAD[43]	PC[11]	49
PAD_FCCU_F1S	FCCU_F1S	50
PAD[44]	PC[12]	56
PAD_FCCU_F1E	FCCU_F1E	—
PAD[45]	PC[13]	57
PAD[46]	PC[14]	58
PAD_TDI	TDI	59
PAD_TMS	TMS	60
PAD_TDO	TDO	61
PAD[47]	PC[15]	62
PAD_TCK	TCK	63
PAD_JCOMP	JCOMP	—
PAD[48]	PD[0]	65
PAD[49]	PD[1]	67
PAD[50]	PD[2]	69
PAD[51]	PD[3]	70
PAD[52]	PD[4]	71
PAD[53]	PD[5]	72
PAD[54]	PD[6]	73
PAD[55]	PD[7]	74
PAD[56]	PD[8]	75
PAD[57]	PD[9]	76
PAD[58]	PD[10]	77
PAD[59]	PD[11]	78
PAD[60]	PD[12]	79
PAD[61]	PD[13]	80

Table 4. Cross-mapping between pads and package pins (continued)

PAD	Port pin name	eTQFP 100 pin
PAD[62]	PD[14]	81
PAD[63]	PD[15]	82
PAD[64]	PE[0]	83
PAD[65]	PE[1]	84
PAD[66]	PE[2]	86
PAD[67]	PE[3]	87
PAD[68]	PE[4]	88
PAD[69]	PE[5]	89
PAD[70]	PE[6]	90
PAD[71]	PE[7]	91
PAD[72]	PE[8]	92
PAD[73]	PE[9]	93
PAD[74]	PE[10]	94
PAD[75]	PE[11]	96
PAD[76]	PE[12]	97
PAD[77]	PE[13]	98
PAD[78]	PE[14]	99
PAD[79]	PE[15]	100
PAD[80]	PF[0]	—
PAD[81]	PF[1]	—
PAD[82]	PF[2]	—
PAD[83]	PF[3]	—
PAD[84]	PF[4]	—
PAD[85]	PF[5]	—
PAD[86]	PF[6]	—
PAD[87]	PF[7]	—
PAD[88]	PF[8]	—
PAD[89]	PF[9]	—
PAD[90]	PF[10]	—
PAD[91]	PF[11]	—
PAD[92]	PF[12]	—
PAD[93]	PF[13]	—
PAD[94]	PF[14]	—
PAD[95]	PF[15]	—
PAD[96]	PG[0]	—

Table 4. Cross-mapping between pads and package pins (continued)

PAD	Port pin name	eTQFP 100 pin
PAD[97]	PG[1]	—
PAD[98]	PG[2]	—
PAD[99]	PG[3]	—
PAD[100]	PG[4]	—
PAD[101]	PG[5]	—
PAD[102]	PG[6]	—
PAD[103]	PG[7]	—
PAD[104]	PG[8]	—
PAD[105]	PG[9]	—
PAD[106]	PG[10]	—
PAD[107]	PG[11]	—
PAD[108]	PG[12]	—
PAD[109]	PG[13]	—
PAD[110]	PG[14]	—
PAD[111]	PG[15]	—
PAD[112]	PH[0]	—
PAD[113]	PH[1]	—
PAD[114]	PH[2]	—
PAD[115]	PH[3]	—
PAD[116]	PH[4]	—
PAD[117]	PH[5]	—
PAD[118]	PH[6]	—
PAD[119]	PH[7]	—
PAD[120]	PH[8]	—
PAD[121]	PH[9]	—
PAD[122]	PH[10]	—
PAD[123]	PH[11]	—
PAD[124]	PH[12]	—
PAD[125]	PH[13]	—
PAD[126]	PH[14]	—
PAD[127]	PH[15]	—
PAD[128]	PI[0]	—
PAD[129]	PI[1]	40
PAD[130]	PI[2]	41
PAD[131]	PI[3]	—

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 5* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 5. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 6. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	T	Lifetime power cycles	—	—	1000k	—
V_{SS}	C	Ground voltage	—	—	—	—
V_{DD_LV}	C	1.2 V core supply voltage(2)	—	-0.3	1.5	V
$V_{DD_HV_IO}$	C	I/O and power management unit supply voltage(3)	—	-0.3	6.0	V
$V_{DD_HV_OSC}$	C	OSC power supply	—	-0.3	6.0	V
$V_{DD_HV_ADC_TSENS}$	C	ADC & TSENS power supply	—	-0.3	6.0	V
V_{REFH_ADC}	C	ADC reference supply	—	0	$V_{DD_HV_ADC_TSENS}$	V
V_{IN}	C	I/O input voltage range(4)	—	-0.3	6.0	V
			Relative to V_{SS}	-0.3	—	
			Relative to $V_{DD_HV_IO}$	—	0.3	
I_{INJD}	T	Maximum DC injection current for digital pad during overload condition	Per pin, applies to all digital pins	-3	3	mA
I_{INJA}	T	Maximum DC injection current for analog pad during overload condition	Per pin, applies to all analog pins	-3	3	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	-7	8	mA
			Fast	-10	10	
			Very fast	-11	11	
I_{MAXSEG} (IO rail #0)	SR	Maximum current per power segment(5)	—	-90	90	mA
I_{MAXSEG} (IO rail #1)	SR	Maximum current per power segment(5)	—	-90	90	mA
T_{STG}	SR	Storage temperature range and non-operating times	—	-55	175	°C
STORAGE	SR	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range -40 °C to 85 °C	—	20	years
T_{SDR}	SR	Maximum solder temperature(6) Pb-free package	—	—	260	°C
MSL	SR	Moisture sensitivity level(7)	—	—	3	—
X-rays dose	T	Maximum cumulated dose allowable	Range for x-rays source during inspection: 80÷130 KV; 20÷50 µA	—	1	Grey

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device. During overload conditions (V_{IN} > $V_{DD_HV_IO}$ or V_{IN} < V_{SS}), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.
2. External regulator mode.
3. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J =°C remaining time at or below 5.5 V.
4. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
5. Analog and digital controller pins must not exceed mA. A $V_{DD_HV_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD_HV_IO}$ supply pins.
6. Solder profile per IPC/JEDEC J-STD-020D.
7. Moisture sensitivity per JEDEC test method A112.

3.4 Electromagnetic compatibility (EMC)

Information about EMC performance is available from STMicroelectronics on request.

3.5 Electrostatic discharge (ESD)

Table 7 describes the ESD ratings of the device.

Table 7. ESD ratings(1),(2)

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(3)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(4)	T	All pins	500	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”.
3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing.
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level.

3.6 Operating conditions

Table 8. Device operating conditions(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Frequency								
f_{SYS}	SR		Device operating frequency(2)	T_J -40 °C to 150 °C	—	—	140	MHz
Temperature								

Table 8. Device operating conditions[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_J	SR	P	Operating temperature range - junction	—	-40.0	—	150.0	°C
T_A (T_L to T_H)	SR	P	Ambient operating temperature range[3]	—	-40.0	—	125.0[4]	°C
Voltage								
V_{DD_LV}		C	1.2 V core supply voltage[5]		1.19	1.255	1.32	V
$V_{DD_HV_IO_L0}$[6],[7]	SR	D	I/O rail #0[8] and PMC supply voltage (with NOMINAL supply = 3.3 V)	LVD290_C/HVD400_C enabled	2.99	—	3.6	V
			I/O rail #0 and PMC supply voltage (with NOMINAL supply = 5 V)	LVD400_IOL0 enabled	4.305	—	5.5	V
$V_{DD_HV_IO_L1}$[6],[7]	SR	D	I/O rail #1 supply voltage (with NOMINAL supply = 3.3 V)	LVD290_L1 enabled	2.99	—	3.6	V
			I/O rail #1 supply voltage (with NOMINAL supply = 5 V)	LVD400_IOL1 enabled	4.305	—	5.5	V
$V_{DD_HV_XOSC}$[6],[7]	SR	D	XOSC supply voltage	LVD290_XOSC enabled	2.99	—	5.5	V

Table 8. Device operating conditions[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD_HV_ADC_TSENS_L0}$	SR	D	SAR ADC rail #0 supply voltage (with NOMINAL supply = 3.3 V)	LVD290_ADL0 enabled	2.99	—	3.6	V
			SAR ADC rail #0 supply voltage (with NOMINAL supply = 5 V)	LVD400_ADL0 enabled	4.305	—	5.5	V
$V_{DD_HV_ADC_TSENS_L1}$	SR	D	SAR ADC rail #1 supply voltage (with NOMINAL supply = 3.3 V)	LVD290_ADL1 enabled	2.99	—	3.6	V
			SAR ADC rail #1 supply voltage (with NOMINAL supply = 5 V)	LVD400_ADL1 enabled	4.305	—	5.5	V
V_{REFH_ADC}	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
		C		—	2.0	—	3.0	
V_{REFH_ADC} - $V_{DD_HV_ADC_TSENS}$	SR	D	SAR ADC reference differential voltage	—	—	—	25	mV
V_{RAMP}	SR	D	Slew rate on power supply pins	—	—	—	0.5	V/us
V_{IN}	SR	C	I/O input voltage range	—	0	—	5.5	V
Injection current								
I_{IC}	SR	T	DC injection current (per pin)[9],[10],[11]	Digital pins and analog pins	-3	—	3	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the *SPC574Sx Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.
3. This value depends on the thermal resistance $R_{\theta JA}$ and power consumption for the device.
4. Depending on the thermal features of the package and PCB.
5. Applicable in external regulator mode.

6. Core voltage as measured on device pin to guarantee published silicon performance.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor external supply voltage may result in erroneous operation of the device.
8. The IO rail #0 and #1 are independent only in external regulator mode. In internal regulator mode a single unique IO rail is applicable. In the QFP100 package only the internal regulator mode is supported.
9. Full device lifetime without performance degradation.
10. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Table 6: Absolute maximum ratings* for maximum input current for reliability requirements.
11. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature. For more information, see the device characterization report.

3.7 Thermal characteristics

3.7.1 Package thermal characteristics

Table 9. Thermal characteristics for eTQFP100

Symbol	C	Parameter	Boundary Conditions	Value	Unit
$R_{\theta JA}$	D	Junction to ambient, natural convection(1)	Four layer board 2s2p board	28	°C/W
$R_{\theta JB}$		Junction to board(2)	Four layer board 2s2p board	11	
$R_{\theta JCtop}$		Junction to top case(3)	1s board Top cold plate	13	
$R_{\theta JCbottom}$		Junction to bottom case(4)	Bottom cold plate	1.1	
Ψ_{JT}		PSI j-top-case, natural convection(5)	Operating conditions	0.6	

1. JESD51-7
2. JESD51-8, ring cold plate
3. Thermal resistance between the die and the case top surface as measured by the cold plate best practice guidelines (JESD51)
4. Thermal resistance between the die and the case bottom surface as measured by the cold plate best practice guidelines (JESD51) without any interface resistance
5. Thermal characterization parameter, not properly a thermal resistance, indicating the temperature difference between package top and the junction in operating conditions as per JESD51-2

3.7.2 Power considerations

An estimation of the chip junction temperature, T_J can be obtained from the equation:

Equation 1: $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the

values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2: $T_J = T_B + (R_{qJB} \times P_D)$

where:

T_B = board temperature for the package perimeter (°C)

R_{qJB} = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3: $R_{qJA} = R_{qJC} + R_{qCA}$

where:

R_{qJA} = junction-to-ambient thermal resistance (°C/W)

R_{qJC} = junction-to-case thermal resistance (°C/W)

R_{qCA} = case to ambient thermal resistance (°C/W)

RqJC is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, R_{qCA}. For example, change

the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (YJT) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4: $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5: $T_J = T_B + (\Psi_{JPB} \times P_D)$

where:

T_B = thermocouple temperature on bottom of the package (°C)

Ψ_{JPB} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

3.8 Current consumption

The following table describes the consumption figures.

Table 10. Current consumption

Use Case[1]	Conditions	Regulator Mode	C	IDD_LV	IDD_HV	Unit
Full function[2]	F1[3] (system clock freq) = 140 MHz F0[4] (motor clock freq) = 120 MHz	Internal	P		310	mA
		External	P	265	55	mA
	F1[3] (system clock freq) = 100 MHz F0[4] (motor clock freq) = 84 MHz	Internal	T		265	mA
		External	T	210	55	mA
	F1[3] (system clock freq) = 70 MHz F0[4] (motor clock freq) = 60 MHz	Internal	T		230	mA
		External	T	175	55	mA
Stop mode	—	Internal	C		110	mA
		External	C	100	30	mA
Full Self test (semi-parallel)	LBIST configuration = L0//L1 + L2//L3 MBIST configuration = parallel Freq = 35 MHz (PLL)	Internal	C		240	mA
		External	C	230	15	mA
Full Self test (parallel)	LBIST configuration = parallel MBIST configuration = parallel Freq = 16 MHz (RCOSC)	Internal	C		215	mA
		External	C	205	15	mA

1. The IDD values are based on the following operating conditions: T_J = 150 °C, HV = 5.5 V, LV = 1.32 (external regulator mode).
2. Values are based on typical application code executing from Flash memory, where the DMA is running in continuous mode, the ADC is in continuous conversion, the timers are running to maximum counter values and communication IPs are in loopback or transmitting mode. IOs are unloaded.
3. F1 stands for System clock frequency.
4. F0 stands for Motor clock frequency.

3.9 I/O pad electrical characteristics

3.9.1 I/O pad types

Table 11 describes the different pad type configurations.

Table 11. I/O pad specification descriptions

Pad type	Description
Slow configuration	Provides a good compromise between transition time and low electromagnetic emission. Pad impedance is centered around 800 Ω
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission. Pad impedance is centered around 200 Ω
Fast configuration	Provides fast transition speed; used for fast interface. Pad impedance is centered around 50 Ω
Very fast configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interfaces, like FlexRay, requiring fine control of rising/falling edge jitter. Pad impedance is centered around 40 Ω
Input only pads	These pads are associated to ADC channels and the external 8-40 MHz crystal oscillator (XOSC) providing low input leakage

3.9.2 I/O input DC characteristics

Table 12 provides input DC electrical characteristics as described in *Figure 3*.

Figure 3. I/O input DC electrical characteristics definition

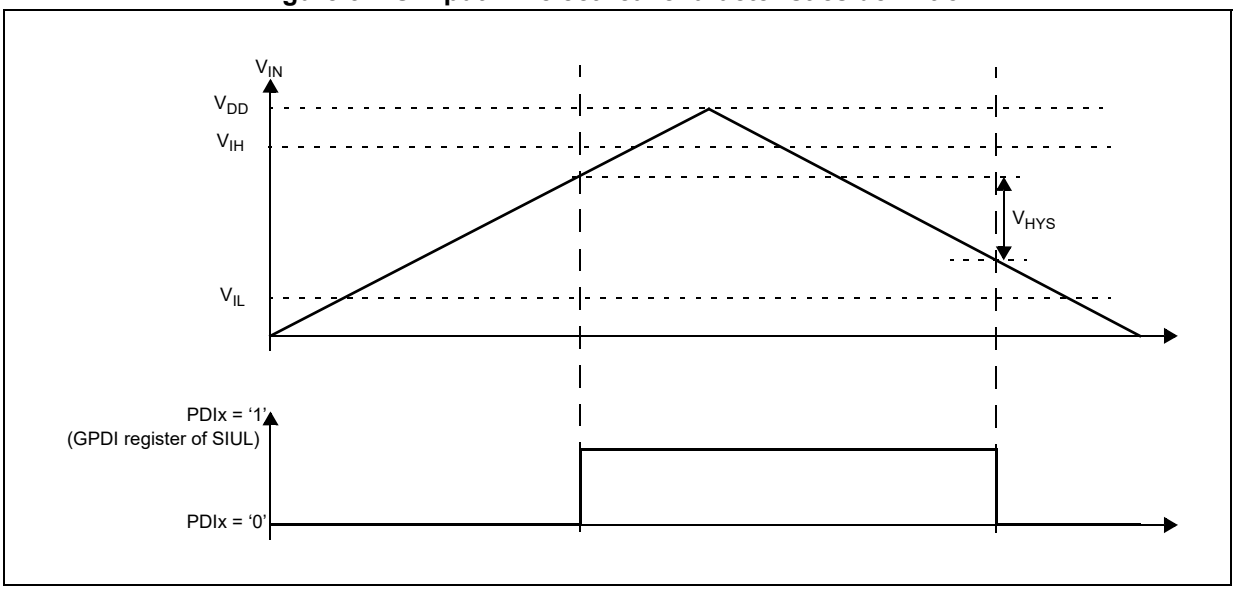


Table 12. I/O input DC electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
TTL							
V_{IH}	SR	P	Input high level TTL	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	2.0(1)	—	—	V
V_{IL}	SR	P	Input low level TTL	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	0.8	
V_{HYST}	—	C	Input hysteresis TTL	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.3(2)	—	—	
CMOS								
V_{IHCMOS_H}(3)	SR	P	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.65 × $V_{DD_HV_IO}$	—	$V_{DD_HV_IO}$ + 0.3	V
V_{IHCMOS}(3)	SR	P	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.6 × $V_{DD_HV_IO}$	—	$V_{DD_HV_IO}$ + 0.3	V
V_{ILCMOS_H}(3)	SR	P	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	-0.3	—	0.35 × $V_{DD_HV_IO}$	V

Table 12. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ILCMOS}(3)	SR	P	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	-0.3	—	0.4 × $V_{DD_HV_IO}$	V
$V_{HYSCMOS}$	—	C	Input hysteresis CMOS	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.1 × $V_{DD_HV_IO}$	—	—	V
Automotive								
V_{IH}(3)	SR	P	Input high level Automotive	4.5 V < $V_{DD_HV_IO}$ < 5.5 V	3.8	—	$V_{DD_HV_IO}$ + 0.3	V
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V	0.75× $V_{DD_HV_IO}$	—	$V_{DD_HV_IO}$ + 0.3	
V_{IL}	SR	P	Input low level Automotive	4.5 V < $V_{DD_HV_IO}$ < 5.5 V	-0.3	—	2.2	V
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V	-0.3	—	0.35 × $V_{DD_HV_IO}$	
V_{HYST}	—	C	Input hysteresis Automotive	4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.5	—	—	V
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V	0.11 × $V_{DD_HV_IO}$	—	—	
Input Characteristics								
I_{LKG}	CC	P	Digital input leakage	—	—	—	1	µA
C_{IN}	C	D	Digital input capacitance	GPIO input pins	—	—	10	pF

1. At 5.5 V and -40 °C, V_{IH} for PA[0], PA[1], and PA[2] is 2.11 V.
2. Minimum hysteresis at 4.0 V
3. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD_HV_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.0 V < $V_{DD_HV_IO}$ < 5.9 V.

Table 13 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 13. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value[1]	$V_{IN} = 0.69 \times V_{DD_HV_IO}$ $4.5\ V < V_{DD_HV_IO} < 5.5\ V$	23	—	—	µA
				$V_{IN} = 0.49 \times V_{DD_HV_IO}$ $4.5\ V < V_{DD_HV_IO} < 5.5\ V$	—	—	82	
				$V_{IN} > V_{IL} = 1.1\ V$ (TTL) $4.5\ V < V_{DD_HV_IO} < 5.5\ V$	—	—	130	
	CC	T		$V_{IN} = 0.75 \times V_{DD_HV_IO}$ $3.0\ V < V_{DD_HV_IO} < 3.6\ V$	10	—	—	
				$V_{IN} = 0.35 \times V_{DD_HV_IO}$ $3.0\ V < V_{DD_HV_IO} < 3.6\ V$	—	—	70	
				$V_{IN} > V_{IL} = 1.1\ V$ (TTL) $3.0\ V < V_{DD_HV_IO} < 3.6\ V$	—	—	75	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = 0.69 \times V_{DD_HV_IO}$ $4.5\ V < V_{DD_HV_IO} < 5.5\ V$	—	—	130	µA
				$V_{IN} = 0.49 \times V_{DD_HV_IO}$ $4.5\ V < V_{DD_HV_IO} < 5.5\ V$	40	—	—	
				$V_{IN} > V_{IL} = 0.9\ V$ (TTL) $4.5\ V < V_{DD_HV_IO} < 5.5\ V$	16	—	—	
	CC	T		$V_{IN} = 0.75 \times V_{DD_HV_IO}$ $3.0\ V < V_{DD_HV_IO} < 3.6\ V$	—	—	92	
				$V_{IN} = 0.35 \times V_{DD_HV_IO}$ $3.0\ V < V_{DD_HV_IO} < 3.6\ V$	19	—	—	
				$V_{IN} > V_{IL} = 0.9\ V$ (TTL) $3.0\ V < V_{DD_HV_IO} < 3.6\ V$	16	—	—	

1. Weak pull-up is enabled within $t_{WK_PU} = 1$ µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.

3.9.3 I/O output DC characteristics

Table 14: Slow configuration I/O output DC characteristics provides DC characteristics for bidirectional pads in the following configurations:

- Slow
- Medium
- Fast
- Very Fast

Table 14. Slow configuration I/O output DC characteristics(1)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{OH_S}	PMOS output impedance slow configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 0.5 mA	560	800	1040	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	560	800	1040	
R_{OL_S}	NMOS output impedance slow configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	560	800	1040	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	560	800	1040	
f_{max_S}	Output frequency slow configuration	C_L = 25 pF	—	—	2	MHz
		C_L = 50 pF	—	—	1	
t_{TR_S}	Transition time output pin slow configuration	C_L = 25 pF	—	—	120	ns
		C_L = 50 pF	—	—	240	
t_{SKEW_S}	Difference between rise time and fall time	—	—	—	28	%

1. The above mentioned values are different for pads PAD[4], PAD[9], PAD[11], PAD[16], PAD[47], PAD[55], PAD[56], PAD[62] and PAD_FCCU_F1E. Please refer to *Table 18* for these pads' values.

Table 15. Medium configuration I/O output DC characteristics(1)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{OH_M}	PMOS output impedance medium configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 2 mA	140	200	260	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 2 mA	140	200	260	
R_{OL_M}	NMOS output impedance medium configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 2 mA	140	200	260	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 2 mA	140	200	260	
f_{max_M}	Output frequency medium configuration	C_L = 25 pF	—	—	12	MHz
		C_L = 50 pF	—	—	6	
t_{TR_M}	Transition time output pin medium configuration	C_L = 25 pF	—	—	35	ns
		C_L = 50 pF	—	—	70	
t_{SKEW_M}	Difference between rise time and fall time	—	—	—	28	%

1. The above mentioned values are different for pads PAD[4], PAD[9], PAD[11], PAD[16], PAD[47], PAD[55], PAD[56], PAD[62] and PAD_FCCU_F1E. Please refer to *Table 18* for these pads' values.

Table 16. Fast configuration I/O output DC characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{OH_F}	PMOS output impedance fast configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 6 mA	44	—	90	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	35	50	65	
R_{OL_F}	NMOS output impedance fast configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL}< 6 mA	44	—	90	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	35	50	65	
f_{max_F}	Output frequency fast configuration	C_L = 25 pF	—	—	50	MHz
		C_L = 50 pF	—	—	25	
t_{TR_F}	Transition time output pin fast configuration	C_L = 25 pF	—	—	12	ns
		C_L = 50 pF	—	—	20	
t_{SKEW_F}	Difference between rise time and fall time	—	—	—	28	%

Table 17. Very Fast configuration I/O output DC characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{OH_V}	PMOS output impedance very fast configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 7 mA	44	—	85	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 9 mA	20	—	60	
R_{OL_V}	NMOS output impedance very fast configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 7 mA	44	—	85	Ω
		4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 9 mA	20	—	60	
f_{max_V}	Output frequency very fast configuration	C_L = 25 pF	—	—	50	MHz
		C_L = 50 pF	—	—	25	
t_{TR_V}	Transition time output pin very fast configuration	C_L = 25 pF	—	—	9	ns
		C_L = 50 pF	—	—	15	
t_{SKEW_V}	Difference between rise time and fall time	—	—	—	28	%

For PAD[4], PAD[9], PAD[11], PAD[16], PAD[47], PAD[55], PAD[56], PAD[62] and PAD_FCCU_F1E, the following values hold true.

Table 18. I/O output DC characteristics for PAD[4], PAD[9], PAD[11], PAD[16], PAD[47], PAD[55], PAD[56], PAD[62] and PAD_FCCU_F1E

Functionality	Symbol	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Slow	R_{OH_S}	PMOS output impedance slow configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 0.5 mA	539	—	1600	Ω
	R_{OL_S}	NMOS output impedance slow configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	534	—	1896	Ω
	f_{max_S}	Output frequency slow configuration	C_L = 25 pF	—	—	2	MHz
			C_L = 50 pF	—	—	1	
	t_{TR_S}	Transition time output pin slow configuration	C_L = 25 pF	—	—	152	ns
			C_L = 50 pF	—	—	279	
	t_{SKEW_S}	Difference between rise time and fall time	—	—	—	50	%
Medium	R_{OH_M}	PMOS output impedance slow configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 0.5 mA	135	—	405	Ω
	R_{OL_M}	NMOS output impedance slow configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	131	—	495	Ω
	f_{max_M}	Output frequency slow configuration	C_L = 25 pF	—	—	12	MHz
			C_L = 50 pF	—	—	6	
	t_{TR_M}	Transition time output pin slow configuration	C_L = 25 pF	—	—	45	ns
			C_L = 50 pF	—	—	77	
	t_{SKEW_M}	Difference between rise time and fall time	—	—	—	46	%

3.10 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

Note: $\overline{PORST}$ pin does not require active control. It is possible to implement an external pull-up to ensure the correct reset exit sequence. The recommended value is 4.7 Kohm.

Figure 4. Start-up reset requirements

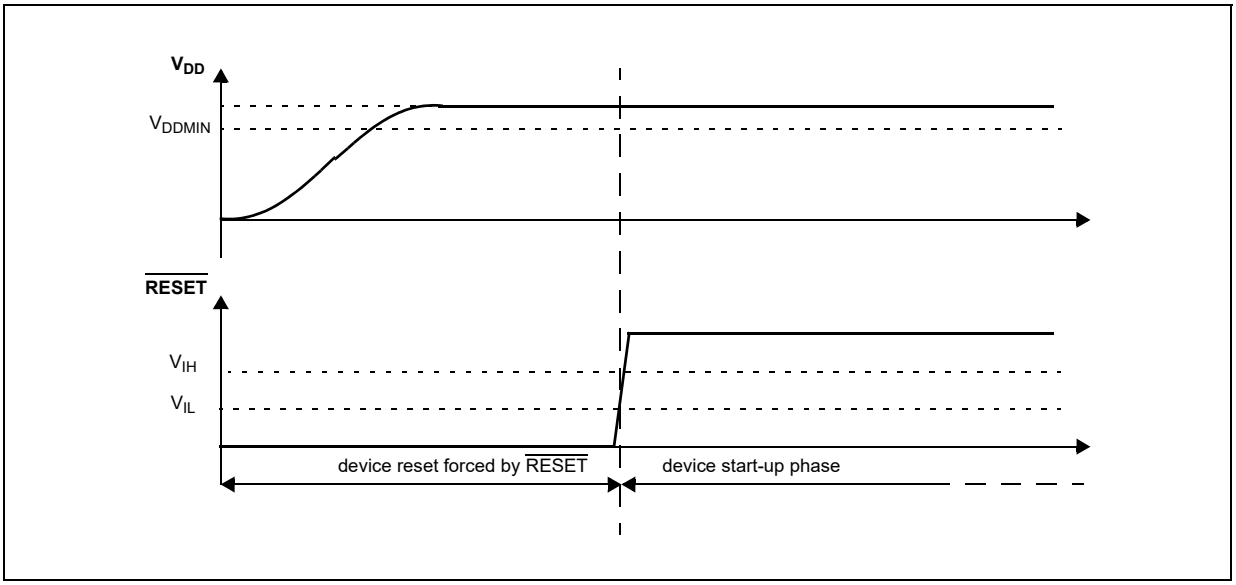


Figure 5 describes the device behavior depending on the supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ does not go low enough: it is filtered by input buffer hysteresis. The device remains in the current state.
2. $\overline{\text{PORST}}$ goes low enough, but not for long enough: it is filtered by a low pass filter. The device remains in the current state.
3. The $\overline{\text{PORST}}$ generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown. It may either be reset or remains in current state depending on extra condition (PVT — process, voltage, temperature).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. The device is under hardware reset.

Figure 5. Noise filtering on reset signal

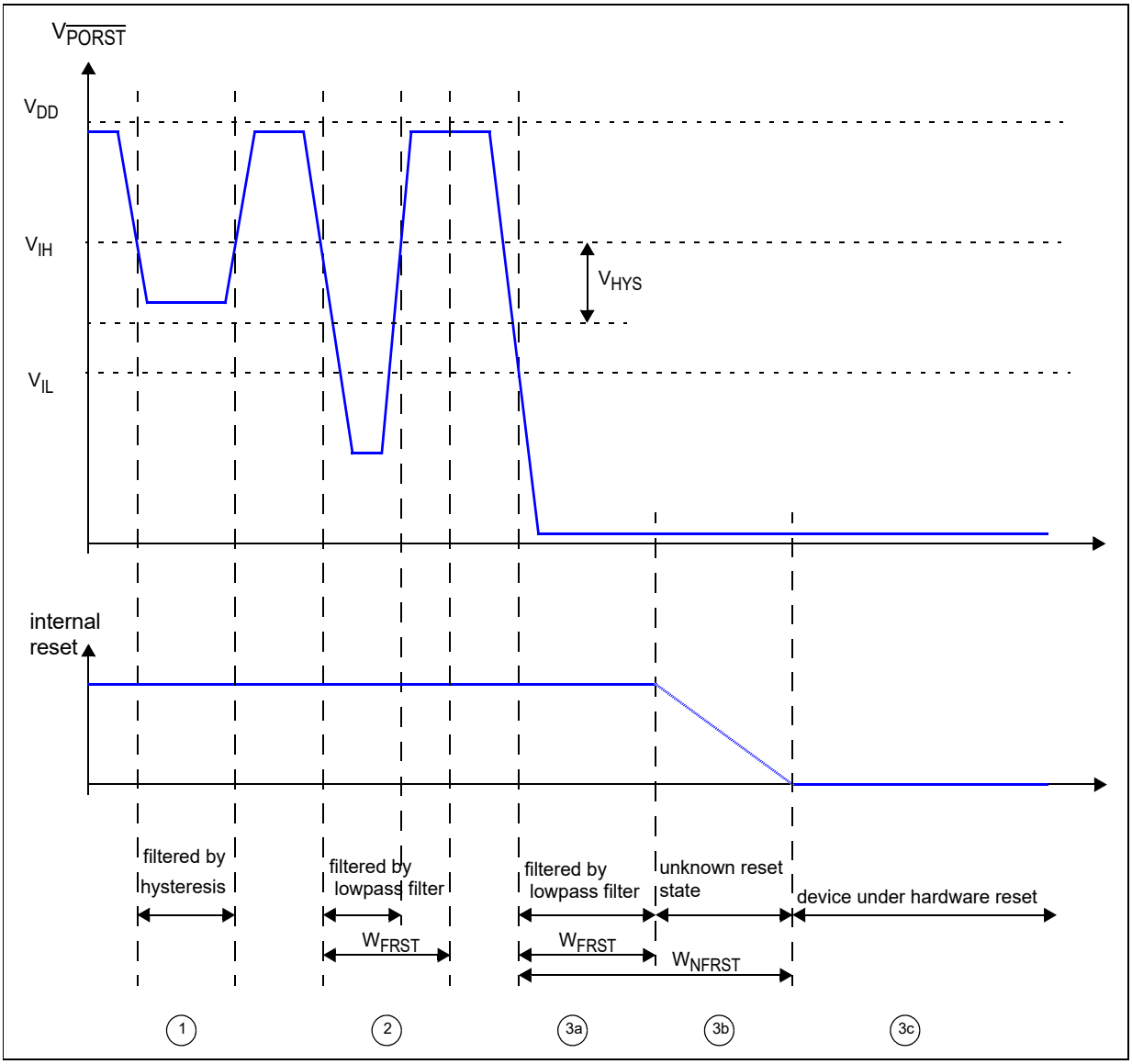


Table 19. Reset electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level TTL (Schmitt trigger)	—	2.0	—	—	V
V_{IL}	SR	P	Input low level TTL (Schmitt trigger)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V	—	—	0.6	V
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	0.8	
V_{HYS}	CC	C	Input hysteresis TTL (Schmitt trigger)	—	300	—	—	mV

Table 19. Reset electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD_POR}	CC	C	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	CC	P	Strong pull-down current	Device under power-on reset $3.0V<V_{DD_HV_IO} < 5.5$ V, $V_{OL} > 1.0V$	0.2	—	—	mA
				Device under power-on reset $V_{DD_HV_IO} = 4.0$ V, $V_{OL} = V_{IL}$	12	—	—	mA
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$\overline{ESR0}$ pin $V_{IN} = 0.69 \times V_{DD_HV_IO}$	23	—	—	µA
				$\overline{ESR0}$ pin $V_{IN} = 0.49 \times V_{DD_HV_IO}$	—	—	82	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$\overline{PORST}$ pin $V_{IN} = 0.69 \times V_{DD_HV_IO}$	—	—	130	µA
				$\overline{PORST}$ pin $V_{IN} = 0.49 \times V_{DD_HV_IO}$	40	—	—	
W_{FRST}	SR	P	$\overline{PORST}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	P	$\overline{PORST}$ input not filtered pulse	—	2000	—	—	ns

3.11 Power management

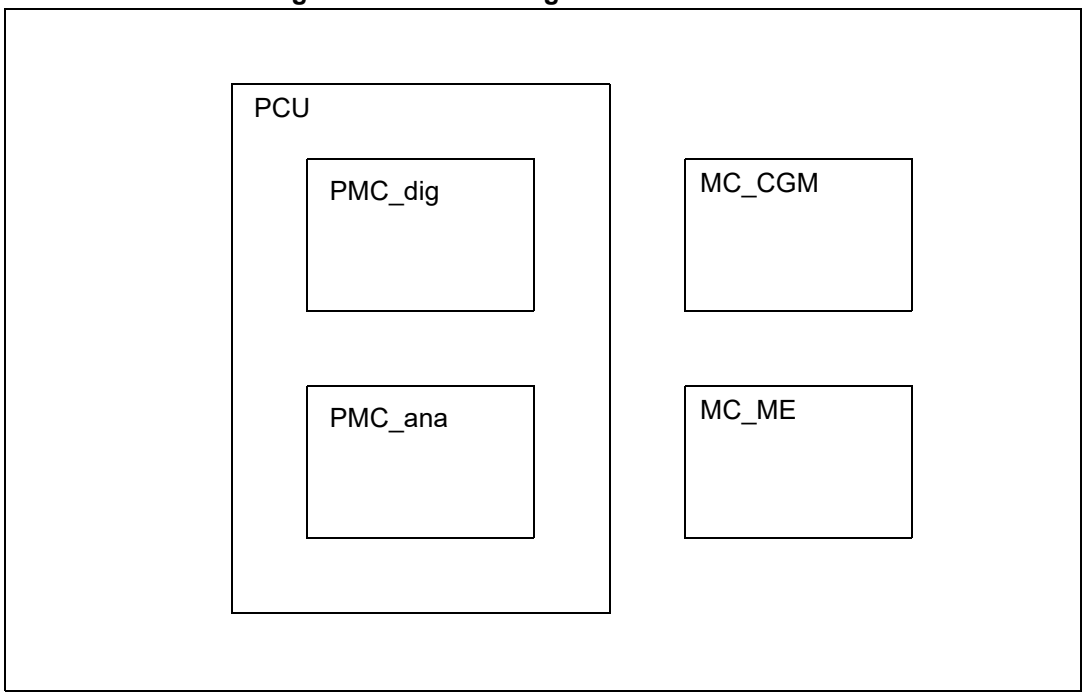
3.11.1 Overview

Figure 6 shows an overview of the power management infrastructure. It consists of:

- a power control unit (PCU) consists of:
  - the digital submodules PMC_dig
  - the analogue submodules PMC_ana
- a clock generation module (MC_CGM)
- a mode entry module (MC_ME)

Note: For detailed information on these modules please refer to the respective chapters of the reference manual.

Figure 6. Power management infrastructure



3.11.2 Voltage regulator electrical characteristics

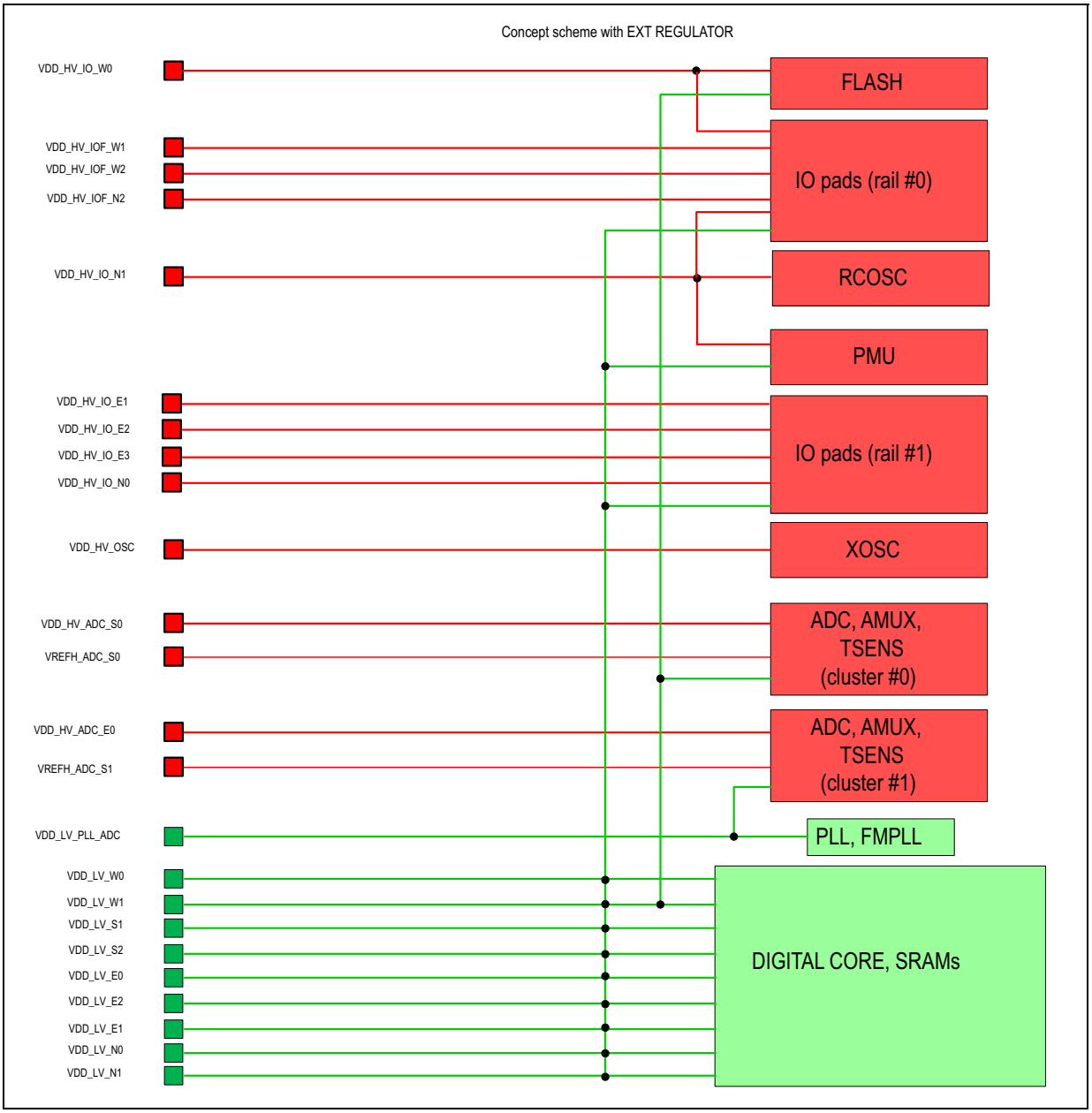
The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply $V_{DD_HV_IO}$. The regulator itself is supplied by $V_{DD_HV_IO}$.

The following supplies are involved:

- HV—High voltage external power supply for the voltage regulator module. This must be provided externally through the $V_{DD_HV_OSC}$ power pin.
- BV—High voltage external power supply for the internal ballast module. This must be provided externally through the $V_{DD_HV_IO}$ power pins. Voltage values should be aligned with $V_{DD_HV_OSC}$.
- LV—Low voltage internal power supply for the core, PLL0 and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is split into three further domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply for PLL1 through double bonding.
  - LV_FLA—Low voltage supply for the code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for PLL1. It is shorted to LV_COR through double bonding.

The concept scheme of the power connections is shown below in *Figure 7*.

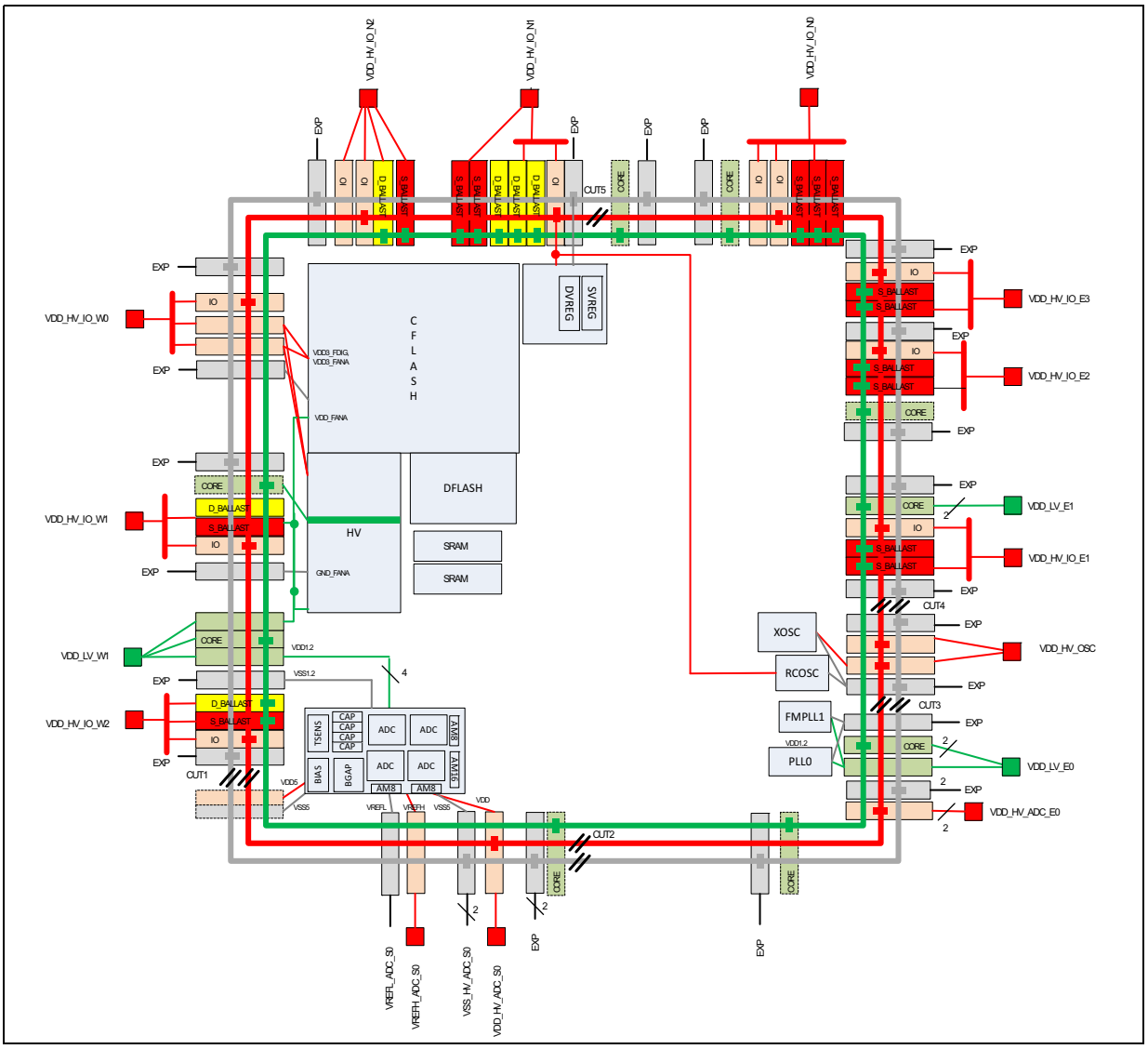
Figure 7. Concept scheme of the power connections



3.11.3 Power Schemes

The power scheme for the eTQFP100 package is shown in *Figure 8*.

Figure 8. Power supply scheme for eTQFP100



The HV ring is divided into 5 different physical domains:

- ADC group #0 and Temperature Sensor
- ADC group #1
- IO rail #0, Flash, PMU and RCOSC
- IO rail #1
- XOSC

Table 20. HV supply schemes

Internal regulator	Number of HV supplies	HV supply domains	Number of LV supplies
Mandatory	2	ADC group #0 IO rail #0 + XOSC + PMU + Flash + IO rail #1	NA

The LV voltage is organized as one single domain. The LV can be generated internally (with internal ballast) or externally, depending on a pin setting. The exposed pad is used to connect the ground ring.

The ballasts are circuits placed in the padring, similarly as other pad circuits (supply or input/output functions).

The S_BALLASTs are controlled by the digital regulator to source the static current. Total current capability for the S_BALLAST on the LV domain is 325mA.

The D_BALLASTs are controlled by the linear regulator to source the dynamic current to support the transient load response. Total current capability for all the D_BALLAST on the LV domain is 100mA.

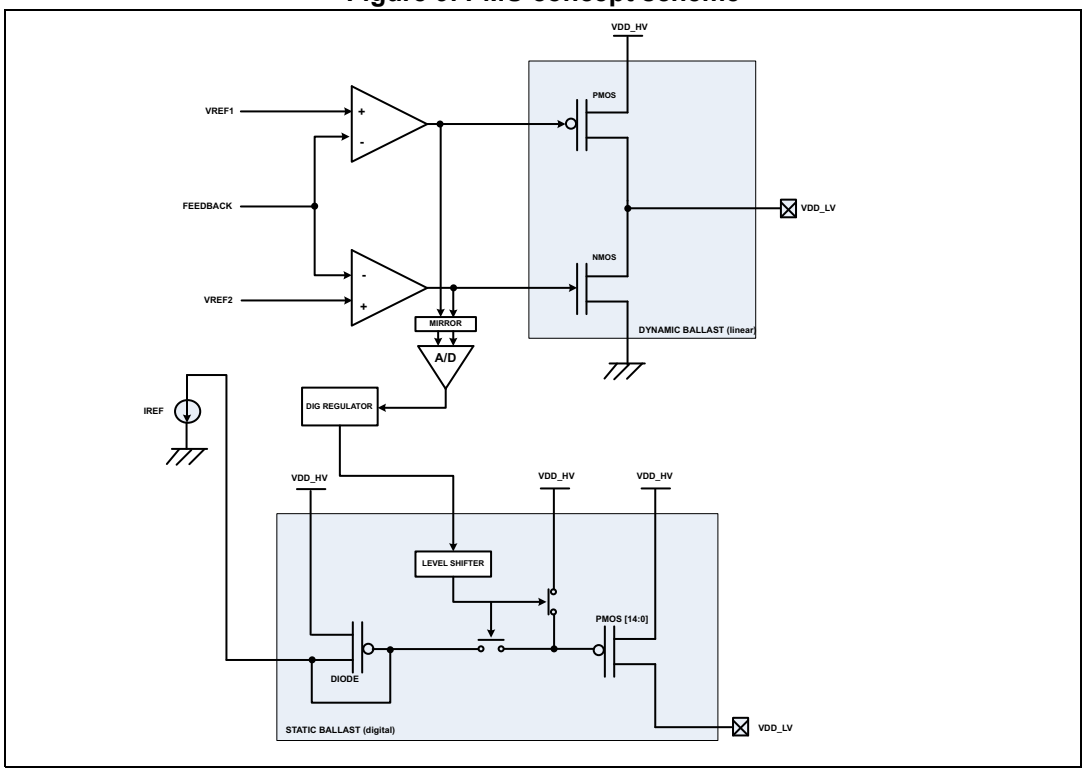
Transient time for the dynamic regulation is 20 µs for maximum 100mA on the LV.

The S_BALLASTs are enabled only in INTERNAL regulator mode (PWMODE = 1).

The D_BALLASTs are always enabled in INTERNAL regulator mode (PWMODE = 1).

The D_BALLASTs are enabled in EXTERNAL regulator mode (PWMODE = 0) only if the LV supply is out of specs (+/- 5%) as tentative to avoid the device reset.

Figure 9. PMU concept scheme



3.11.4 Decoupling capacitors

Table 21. eTQFP100 HV/LV supply decoupling capacitances

Ballast	PAD	Pin	Minimum (Internal Regulation)	Minimum (External Regulation)	Suggested Configuration	Note
—	VDD_LV_W0	—	—	—	—	—
—	VDD_LV_W1	19	2.2 µF + 100 nF	2.2 µF + 100 nF	2.2 µF + 100 nF + 10 nF	LV Buffer capacitance + EMC protection
—	VDD_LV_S1	—	—	—	—	—
—	VDD_LV_S2	—	—	—	—	—
—	VDD_LV_PLL_ADC	52	—	—	—	—
—	VDD_LV_E0	52	100 nF	100 nF	100 nF + 10 nF	LV Buffer capacitance + EMC protection
—	VDD_LV_E2	—	—	—	—	—
—	VDD_LV_E1	68	100 nF	100 nF	100 nF	LV Buffer capacitance
—	VDD_LV_N0	—	—	—	—	—
—	VDD_LV_N1	—	—	—	—	—
—	VDD_HV_IO_W0	20	—	—	—	—
Dynamic Ballast	VDD_HV_IO_W1	20	—	—	—	—
Dynamic Ballast	VDD_HV_IO_W2	20	2.2 µF	2.2 µF	2.2 µF + 4.7 µF + 10 nF NM(1)	HV Buffer capacitance + EMC protection
—	VDD_HV_OSC	55	100 nF	100 nF	100 nF	HV Buffer capacitance
Static Ballast	VDD_HV_IO_E1	51	—	—	—	—
Static Ballast	VDD_HV_IO_E2	51	—	—	—	—
Static Ballast	VDD_HV_IO_E3	51	—	—	—	—
Static Ballast	VDD_HV_IO_N0	85	—	—	—	—
Dynamic Ballast	VDD_HV_IO_N1	85	100 nF	—	100 nF + 10 nF NM(1)	HV Buffer capacitance + EMC protection
Dynamic Ballast	VDD_HV_IO_N2	95	100 nF	—	100 nF + 10 nF NM(1)	HV Buffer capacitance + EMC protection

1. NM = not mounted

Figure 10. ADC decoupling capacitance/resistance scheme

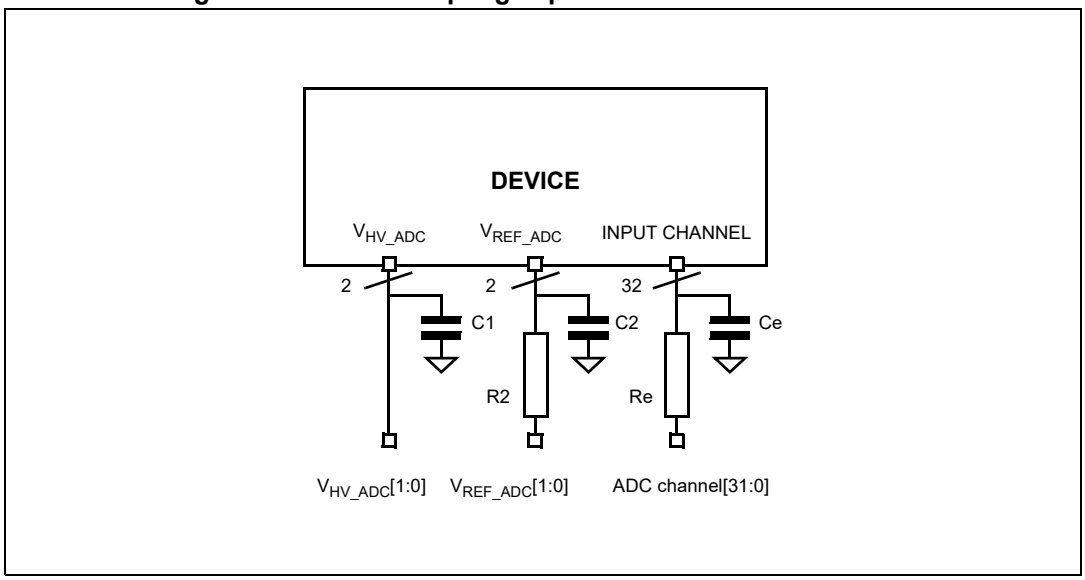


Table 22. ADC decoupling capacitance/resistance values

Label	Instances	Value	Recommended commercial components based on PVT/aging degradation
C1	2	470 nF	min 1 µF
R2	2	5 to 8 Ω	max 8 Ω
C2	2	1 µF	min 2.2 µF
Ce	32	$\geq 8192^{(1)} \times Cs^{(2)} \times 2^{(3)}$ = 115 nF	min 200 nF
Re	32	$<= 1/(8192^{(1)} \times Fs \times Cs^{(2)} \times 2^{(3)})$ = 13 Ω	max 10 Ω

1. Factor depending on the ADC 12 bits
2. Input capacitance Cs = 7 pF
3. Factor for 2 ADCs on the same physical channel

Table 23. Package ADC supply decoupling capacitance

PAD	eTQFP100 package
VREFH_ADC_S0	36
VDD_HV_ADC_S0	39
VREFH_ADC_S1	—
VDD_HV_ADC_E0	51

Note: All 1.2V pins should be shorted externally on board with minimum resistance and minimum inductance. It is recommended to use a 1.2V plane on which all 1.2V pins are shorted to keep resistance and inductance negligible. Recommended capacitors should be placed very close to the device pins such that parasitic resistance can be reduced. Connection from VDD_LV pin to capacitor top plate should not exceed more than 5mohm in resistance and 0.5nH in inductance. Similarly connection from bottom plate of capacitor to PCB ground should not have more than 5mohm resistance and 0.5nH inductance.

3.11.5 Power management electrical characteristics

Table 24. Voltage regulator electrical characteristics[1]

Symbol		Parameter	Conditions[2]	Value[3]			Unit
				Min	Typ	Max	
C_{REG}	SR	Internal voltage regulator stability external capacitance	—	1.1	2.2[4]	2.97	µF
$R_{DECREGn}$	SR	Stability capacitor equivalent serial resistance	Total resistance including board track	1	—	50	mΩ
C_{V1V2}	SR	EMC cap to be placed on every 1.2 V pin	V_{DD}/V_{SS} pair	50	100	135	nF
C_{DECBV}	SR	Decoupling capacitance ballast	V_{DD_BV}/V_{SS_LV} pair	1.1	2.2[4]	2.97	µF
V_{MREG}	CC	Main regulator output voltage	Before trimming	1.21	1.27	1.32[5]	V
			After trimming	1.22	1.25	1.28	
IDD_{MREG}	SR	Main regulator current provided to V_{DD_LV} domain	—	—	—	300	mA
ΔIDD_{MREG}	SR	Main regulator current variation	20 µs observation window	-100	—	100	mA

1. All 1.2V pins should be shorted externally on board with minimum resistance and minimum inductance. It is recommended to use a 1.2V plane on which all 1.2V pins are shorted to keep resistance and inductance negligible. Recommended capacitors should be placed very close to the device pins such that parasitic resistance can be reduced. Connection from VDD_LV pin to capacitor top plate should not exceed more than 5mohm in resistance and 0.5nH in inductance. Similarly connection from bottom plate of capacitor to PCB ground should not have more than 5mohm resistance and 0.5nH inductance.
2. V_{DD} = 5.0 V ± 10%, T_A = -40 / 125 °C, unless otherwise specified.
3. All values need to be confirmed during device validation.
4. Recommended X7R or X5R ceramic -43% / +35% variation, 20% tolerance and 12.5% temperature.
5. At power-up condition before trimming.

3.12 PMU monitor specifications

3.12.1 Nomenclature

- **POR** stands for Power On Reset. The POR circuit manages the reset from very low voltage up to its threshold. Cannot be disabled.
- **MVD** stands for Minimum Voltage Detector. It cannot be disabled by the user and generate a destructive Reset.
- **LVD** stands for Low Voltage Detector. It can be disabled by the user.
- **HVD** stands for High Voltage Detector. It can be disabled by the user.
- **UVD** stands for Upper Voltage Detector. It cannot be disabled by the user and generate a destructive reset.

Table 25. Trimmed (PVT) values

Domain monitor	Voltage	Name	Segment	Lower limit	Upper limit
1.2 V	Power On Reset	POR041	Core	0.39 V	0.95 V
	Low	MVD098	Core	1.045 V	1.095 V
			Flash	1.045 V	1.095 V
		LVD108	Core	1.125 V	1.175 V
	High	HVD140	Core	1.355 V	1.405 V
		UVD145	Core	1.395 V	1.445 V
			Flash	1.395 V	1.445 V
3.3 V	Power On Reset	POR200	Core	1.820 V	2.400 V
	Low	MVD270	Core	2.694 V	2.826 V
			Flash	2.694 V	2.826 V
		LVD290	Core	2.881 V	2.999 V
			Flash	2.881 V	2.999 V
			ADC	2.881 V	2.999 V
	High	HVD400	Core	3.660 V	3.840 V
5 V	Low	LVD400	ADC	4.128 V	4.332 V
	High	UVD600	Core	5.698 V	5.942 V

3.12.2 Power up/down sequencing

For proper device functioning please adhere to the following power sequence:

$V_{DD_HV_ADC_TSENS}$ supply should always be greater than or equal to V_{REFH_ADC} supply.

During power-up, all functional terminals are maintained in a known state as described in the following table.

Table 26. Functional terminals state during power-up and reset

TERMINAL type(1)	POWER-UP(2) pad state	RESET pad state	DEFAULT pad state(3)	Comments
PORST	Strong pull-down(4)	Weak pull-down	Weak pull-down	Power-on reset pad
ESR0(5)	Strong pull-down	Strong pull-down	Weak pull-up	Functional reset pad
ESR1	Weak pull-up	Weak pull-up	Weak pull-up	—
TEST_MODE	Weak pull-down	Weak pull-down(6)	Weak pull-down(6)	—
GPIO	High impedance	High impedance	High impedance	—
ANALOG	High impedance	High impedance	High impedance	—
ERROR[0]	High impedance	High impedance	High impedance	During functional reset, pad state can be overridden by FCCU
TRST	High impedance	Weak pull-down	Weak pull-down	—
TCK	High impedance	Weak pull-down	Weak pull-down	—

Table 26. Functional terminals state during power-up and reset (continued)

TERMINAL type(1)	POWER-UP(2) pad state	RESET pad state	DEFAULT pad state(3)	Comments
TMS	Weak pull-up	Weak pull-up	Weak pull-up	—
TDI	Weak pull-up	Weak pull-up	Weak pull-up	—
TDO	High impedance	High impedance	High impedance	—

1. Refer to pinout information for terminal type
2. POWER-UP state is guaranteed from $V_{DD_HV_IO}$ > V_{DD_POR} and maintained until supply crosses the power-on reset thresholds V_{PORUP_LV} for LV supply and V_{PORUP_HV} for high voltage supply.
3. Before software configuration
4. Pull-down and pull-up strengths are provided in *Table 13: I/O pull-up/pull-down DC electrical characteristics*
5. Unlike ESR0, ESR1 is provided as a normal GPIO and implements weak pull-up during power-up.
6. An internal pull-down is implemented on the TESTMODE pin to prevent the device from entering test mode if the package TESTMODE pin is not connected. It is recommended to connect the TESTMODE pin to $V_{SS_HV_IO}$ on the board for maximum robustness, but not required. The value of TESTMODE is latched at the negation of reset and has no affect afterward. The device will not exit functional reset with the TESTMODE pin asserted during power-up. The TESTMODE pin can be connected externally directly to ground without any other components.

3.13 Platform Flash controller configuration

Table 27. Wait states versus system clock frequency(1)

Read Wait State Control (RWSC)	System clock frequency (MHz)(2)
0b00000	0 - 30 MHz
0b00001	30 - 60 MHz
0b00010	60 - 90 MHz
0b00011	90 - 121 MHz
0b00100	121 - 140 MHz

1. RWSC is a field in the Flash memory of the PFCR register used to specify the wait states for address pipelining and read/write accesses.
2. Values to be confirmed by silicon validation.

3.14 Flash memory electrical characteristics

Table 28 shows the program and erase characteristics.

Table 28. Flash memory program and erase specifications

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 100 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time [Packaged part]	43	C	130	—	—	140	500		C	µs
$t_{pprogram}$	Page (256 bits) program time	72	C	240	—	—	240	1000		C	µs
$t_{pprogrameep}$	Page (256 bits) program time Data Flash - EEPROM (partition 1) [Packaged part]	83	C	264	—	—	276	1000		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	263	C	1040	1200	P	850	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time Data Flash - EEPROM (partition 1) [Packaged part]	285	C	1140	1320	P	978	2000		C	µs
$t_{16kpperase}$	16 KB block pre-program and erase time	150	C	1000	1000	P	190	2000	—	C	ms
$t_{32kpperase}$	32 KB block pre-program and erase time	200	C	1000	1000	P	230	2000	—	C	ms
$t_{64kpperase}$	64 KB block pre-program and erase time	300	C	1000	1000	P	420	2000	—	C	ms
$t_{256kpperase}$	256 KB block pre-program and erase time	900	C	2000	3000	P	1600	5000	—	C	ms
$t_{16kprogram}$	16 KB block program time	34	C	45	50	P	40	1000	—	C	ms
$t_{32kprogram}$	32 KB block program time	67	C	90	100	P	75	2000	—	C	ms
$t_{64kprogram}$	64 KB block program time	135	C	175	200	P	150	3000	—	C	ms
$t_{256kprogram}$	256 KB block program time	540	C	700	850	P	590	4000	—	C	ms
$t_{16kprogrameep}$	Program 16 KB Data Flash - EEPROM (partition 1) [Packaged part]	39	C	52	58	P	64	1000		C	ms
$t_{16keraseeep}$	Erase 16 KB Data Flash - EEPROM (partition 1) [Packaged part]	160	C	1000	1000	P	400	5000		C	ms
t_{tr}	Program rate[8]	2.2	C	2.8	3.40	C	2.4	—		C	s/MB
t_{pr}	Erase rate[8]	3.5	C	8.0	12.0	C	6.4	—		C	s/MB
$t_{ffprogram}$	Full flash programming time[9]	3.3	C	4.2	5.2	P	3.0	16	—	C	s
$t_{fferase}$	Full flash erasing time[9]	6.0	C	15.0	19.0	P	6.8	20	—	C	s

Table 28. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1][2]	Value								Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 100 K cycles		
t_{ESRT}	Erase suspend request rate[10]	500	T	—	—	—	—	—		—	µs
t_{PSRT}	Program suspend request rate[10]	30	T	—	—	—	—	—		—	µs
t_{AMRT}	Array Integrity Check - Margin Read suspend request rate	15	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency[11]	—	—	—	—	—	—	15		T	µs
t_{ESUS}	Erase suspend latency[11]	—	—	—	—	—	—	30		T	µs
t_{AIC0S}	Array Integrity Check (1.5 MB, sequential)[12]	15	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array Integrity Check (256 KB, sequential)[12]	2.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (1.5 MB, proprietary)[12]	2.0	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (1.5 MB, sequential)[12]	75	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin Read (256 KB, sequential)[12]	12.5	T	—	—	—	—	—	—	—	ms

1. Characteristics are valid both for Data Flash and Code Flash, unless specified in the characteristics column.
2. Actual hardware programming times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 20 °C < TJ < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < TJ < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
8. Rate computed based on 256 KB sectors.
9. Only code sectors, not including EEPROM.
10. Time between suspend resume and next suspend. Value stated actually represents Min value specification.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependent on system frequency and number of wait states. Timing in the table is calculated at max frequency.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 29. Flash memory Life Specification

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	Kcycles
N_{DER16K}	16 KB EEPROM Flash endurance	100	—		—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—		—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	15	—		—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—		—	Years

1. Program and erase cycles supported across specified temperature specs.

3.15 PLL0/PLL1 electrical characteristics

The device provides a phase-locked loop (PLL0) as well as a frequency-modulated phase-locked loop (PLL1) module to generate a fast system clock from the main oscillator driver.

Table 30. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	PLL1 reference clock[2]	—	37.5	—	78.125	MHz
Δ_{PLLIN}	SR	—	PLL1 reference clock duty cycle[2]	—	35	—	65	%
f_{PLLOUT}	CC	D	PLL1 output clock frequency	—	4.762	—	625	MHz
f_{VCO}[3]	CC	P	VCO frequency	—	600	—	1250	MHz
t_{LOCK}	CC	P	PLL1 lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	50	µs
Δt_{STJIT}	CC	T	PLL1 short term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz	—	—	1.8	ns
I_{PLL}	CC	C	PLL1 consumption	T_A = 25 °C	—	—	5	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3. Frequency modulation is considered ±2%.

Table 31. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	PLL0 reference clock[2]	—	8	—	56	MHz
Δ_{PLLIN}	SR	—	PLL0 reference clock duty cycle[2]	—	30	—	70	%
f_{PLLOUT}	CC	D	PLL0 output clock frequency	—	4.762	—	625	MHz
f_{VCO}	CC	P	VCO frequency	—	600	—	1250	MHz
t_{LOCK}	CC	P	PLL0 lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	100	µs
Δt_{STJIT}	CC	T	PLL0 short term jitter	f_{sys} maximum	–150	—	150	ps
Δt_{LTJIT}	CC	T	PLL0 long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz	–1	—	1	ns
I_{PLL}	CC	C	PLL0 consumption	T_A = 25 °C	—	—	5	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

3.16 External oscillator (XOSC) electrical characteristics

Table 32. External Oscillator electrical specifications[1]

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range[2]	—	4	8	MHz
				—	>8	20	
				—	>20	40	
t_{cst}	CC	T	Crystal start-up time [3],[4]	T_J = 150 °C	—	5	ms
t_{rec}	CC	—	Crystal recovery time[5]	—	—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage (External Reference)	$V_{REF} = 0.28 \times V_{DD_HV_IO}$	V_{REF} + 0.6	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage[6],[7]	$V_{REF} = 0.28 \times V_{DD_HV_IO}$	—	V_{REF} - 0.6	V
C_{S_EXTAL}	CC	T	Total on-chip stray capacitance on EXTAL pin[8]	QFP	6.0	8.0	pF
C_{S_XTAL}	CC	T	Total on-chip stray capacitance on XTAL pin[8]	QFP	6.0	8.0	pF

Table 32. External Oscillator electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions		Value		Unit
						Min	Max	
g_m	CC	P	Oscillator Transconductance (3.3 V)	T_J = -40 °C to 150 °C	$f_{XTAL} \leq 8$ MHz	2.2	12.1	mA/V
		D			$f_{XTAL} \leq 20$ MHz	7	28.6	
		D			$f_{XTAL} \leq 40$ MHz	9.7	37.4	
	CC	P	Oscillator Transconductance (5 V)	T_J = -40 °C to 150 °C	$f_{XTAL} \leq 8$ MHz	2.6	11.0	mA/V
		D			$f_{XTAL} \leq 20$ MHz	7.9	26.0	
		D			$f_{XTAL} \leq 40$ MHz	10.4	34.0	
V_{EXTAL}	CC	D	Oscillation Amplitude on the EXTAL pin after startup[9]	T_J = –40 °C to 150 °C		0.5	1.6	V
V_{HYS}	CC	D	Comparator Hysteresis	T_J = 150 °C		0.1	1.0	V
I_{XTAL}	CC	D	XTAL current[10]	T_J = 150 °C		—	14	mA

1. All oscillator specifications are valid for $V_{DD_HV_IO}$ = 3.0 V – 5.5 V.
2. The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40MHZ.
3. This value is determined by the crystal manufacturer and board design.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
6. This parameter is guaranteed by design rather than 100% tested.
7. Applies to an external clock input and not to crystal mode.
8. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
9. Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
10. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2-3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in *Figure 12*. The ALC block is the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid overdriving the crystal.

Figure 11. Crystal/Resonator Connections

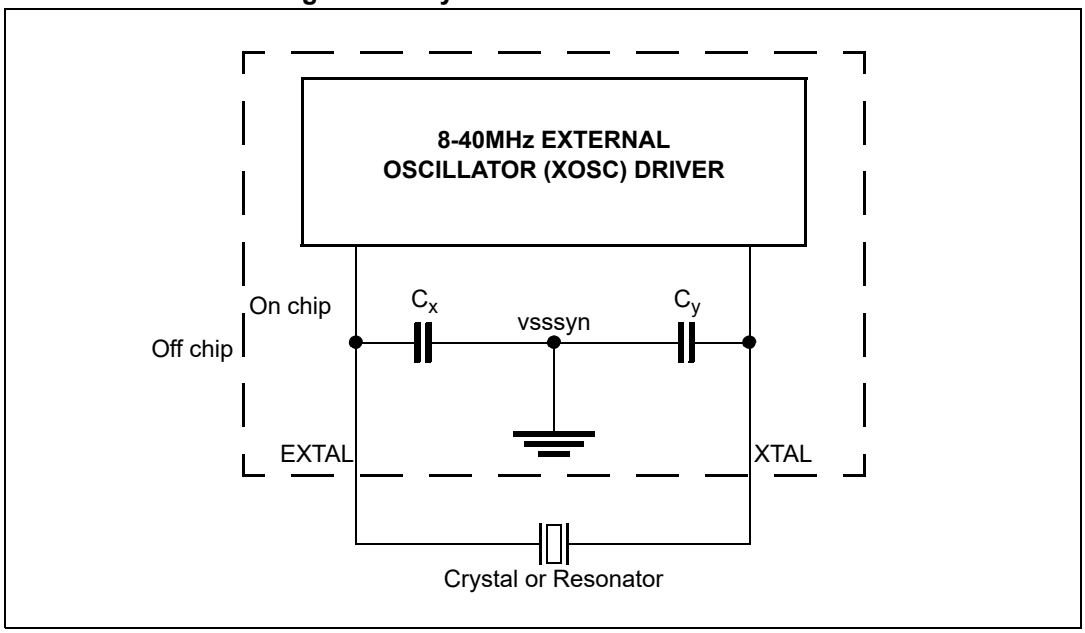
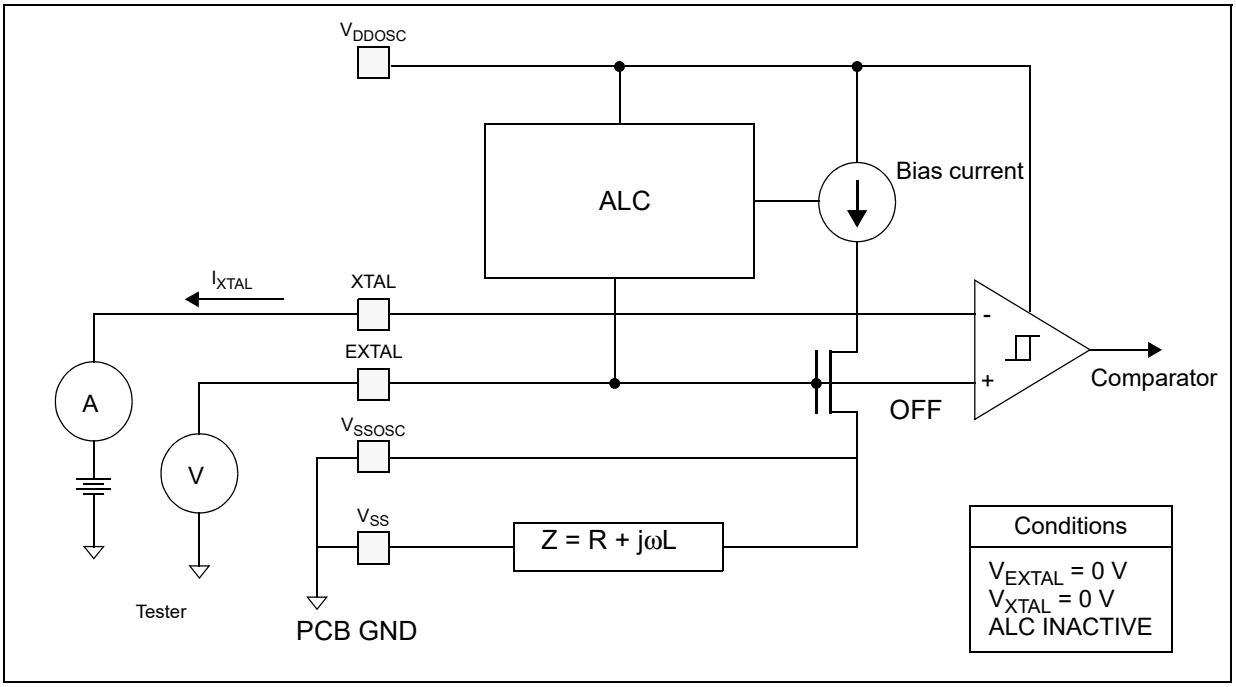


Table 33. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance offered on EXTAL/XTAL (Cx and Cy)(1) (pF)
00000	1.032
00001	1.976
00010	2.898
00011	3.823
00100	4.751
00101	5.679
00110	6.605
00111	7.536
01000	8.460
01001	9.390
01010	10.317
01011	11.245
01100	12.173
01101	13.101
01110	14.029
01111	14.957

1. Values are determined from simulation with a tolerance of ±15%.

Figure 12. Test circuit



3.17 Internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 34. Internal RC oscillator electrical specifications

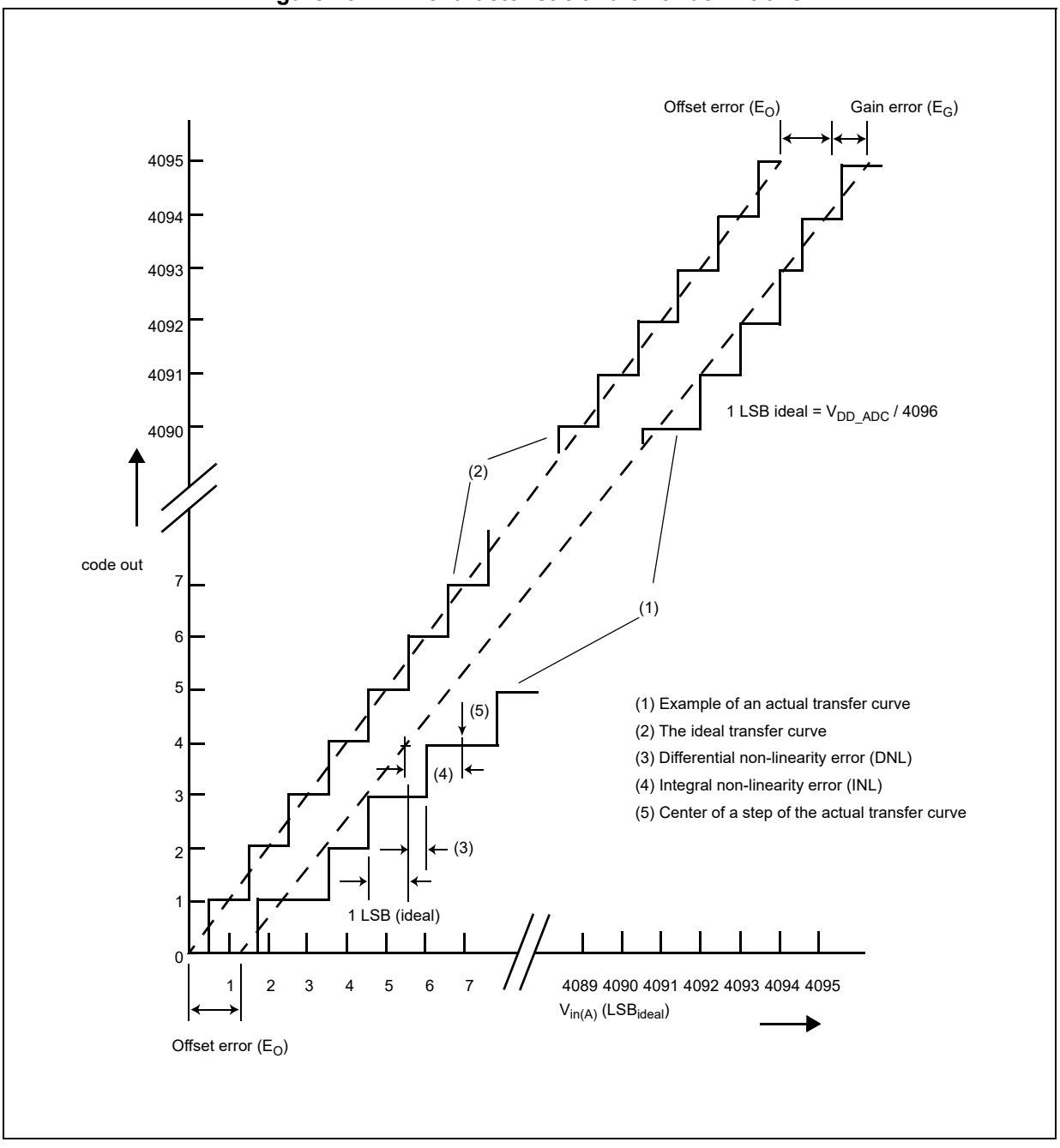
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	—	–8	—	+8	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T_J < 150 °C	–2	—	+2	%
δf_{var_SW}	—	T	IRC software trimming accuracy	Trimming temperature	–1	—	+1	%
t_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs
t_{start_T}	CC	T	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs
I_{AVDD5}	CC	T	Current consumption on 5 V power supply	After t_{start_T}	—	—	400	µA
I_{DVDD12}	CC	T	Current consumption on 1.2 V power supply	After t_{start_T}	—	—	175	µA

3.18 ADC electrical characteristics

3.18.1 Introduction

The device provides a 12-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 13. ADC characteristic and error definitions



3.18.2 ADC electrical characteristics

Table 35. ADC input leakage current

Symbol		Parameter	Conditions		Value		Unit
					Min	Max	
I_{LKG}	CC	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_J < 40 °C	No current injection on adjacent pin	—	70	nA
			T_J < 150 °C		—	220	

Table 36. ADC conversion characteristics

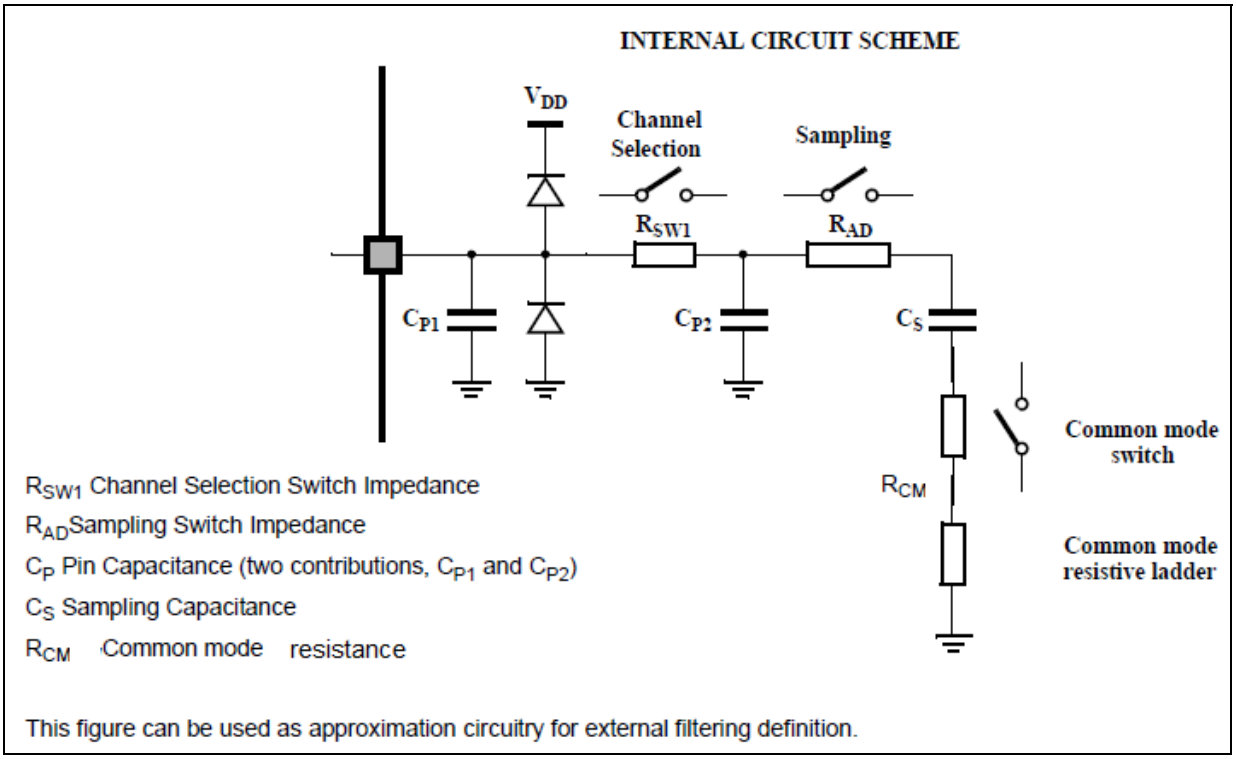
Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{IN}	SR		ADC input signal	$0 < V_{IN} < V_{DD_HV_IO}$	$V_{SS_HV_ADR}$(1)	V_{REFH_ADC}	V
f_{ADCK}	SR	P	Clock frequency	—	7.5	12	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	—	83	—	ns
V_{PRECH}	SR	D	Precharge voltage	—	—	0.25	V
ΔV_{INTREF}	CC		Internal reference voltage precision	Applies to all internal reference points ($V_{SS_HV_ADR}$, $1/3 \times V_{REFH_ADC}$, $2/3 \times V_{REFH_ADC}$, V_{REFH_ADC})	-0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time	SAR – 12-bit configuration	0.5	—	µs
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (12 clock cycles)	1.000	—	µs
		D		10-bit configuration (10 clock cycles)	0.833	—	
$I_{ADCREFH}$(2)	CC	C	ADC high reference current (average across all codes)	Run mode	—	15	µA
				Power Down mode	—	1	
	CC	P	VDD_HV_ADC_TSENS power supply current	Run mode	—	4.0	mA
				Power Down mode	—	0.03	
TUE_{12}	CC	T	Total unadjusted error in 12-bit configuration	$V_{REFH_ADC} > 3$ V	-6	6	LSB (12b)

Table 36. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{12}	CC	D	TUE degradation due to V_{REFH_ADC} offset with respect to $V_{DD_HV_ADC_TSENS}$	$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [0:25 mV]	—	±1	LSB (12b)
		D		$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [25:50 mV]	—	±2.0	
		D		$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [50:75 mV]	—	±3.5	
		D		$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [75:100 mV]	—	±6.0	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [0:25 mV]	—	±2.5	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [25:50 mV]	—	±4.0	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [50:75 mV]	—	±7.0	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [75:100 mV]	—	±12.0	
DNL	CC	P	Differential non-linearity	—	-1	2	LSB (12b)

1. $V_{SS_HV_ADR}$ is connected to exposed pad for the device.
2. The consumption values are given after power-up when steady state is reached. Extra consumption of up to 2 mA can be required during internal circuitry setup.

Figure 14. ADC analog input circuit



C_{P1} Pad capacitance -10 pF

C_{P2} Internal routing capacitance SARn channels 2 pF

C_S SAR ADC sampling capacitance - 3 pF

R_{SW1} Analog switches resistance SARn channels 1.8 kΩ

R_{AD} ADC input analog switches resistance - 800 Ω

R_{CM} Common mode resistance - 8 kΩ

3.19 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 37. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{SENS}	CC	P	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	P	Accuracy	$T_J < 150$ °C	–3	—	3	°C
I_{TEMP_SENS}	CC	C	$V_{DD_HV_ADC_TSENS}$ power supply current	—	—	—	700	µA

3.20 JTAG interface timings

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDC}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%-70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	5	—	ns
6	t_{DOV}	D	TCK low to TDO data valid	—	—	30	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	30	ns
9	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 15. JTAG test clock input timing

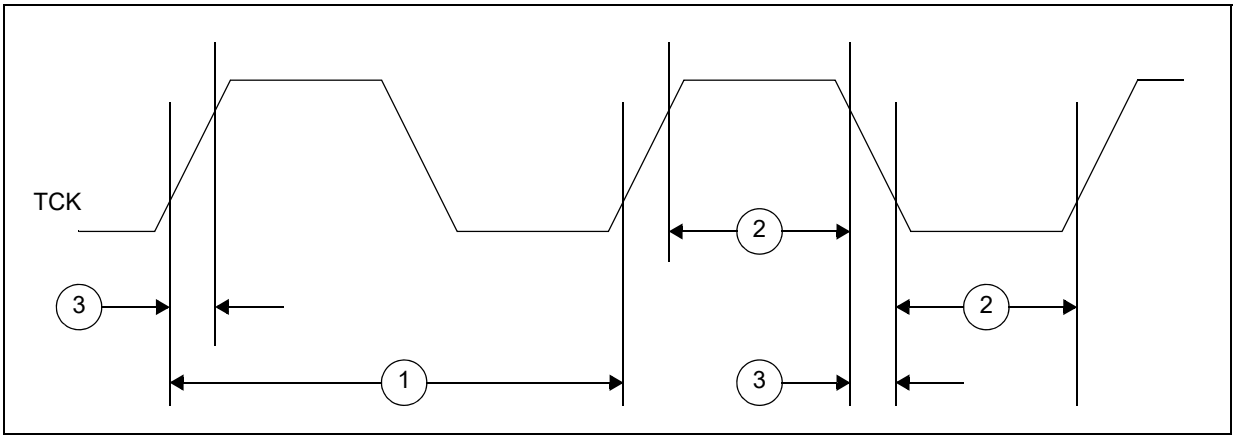


Figure 16. JTAG test access port timing

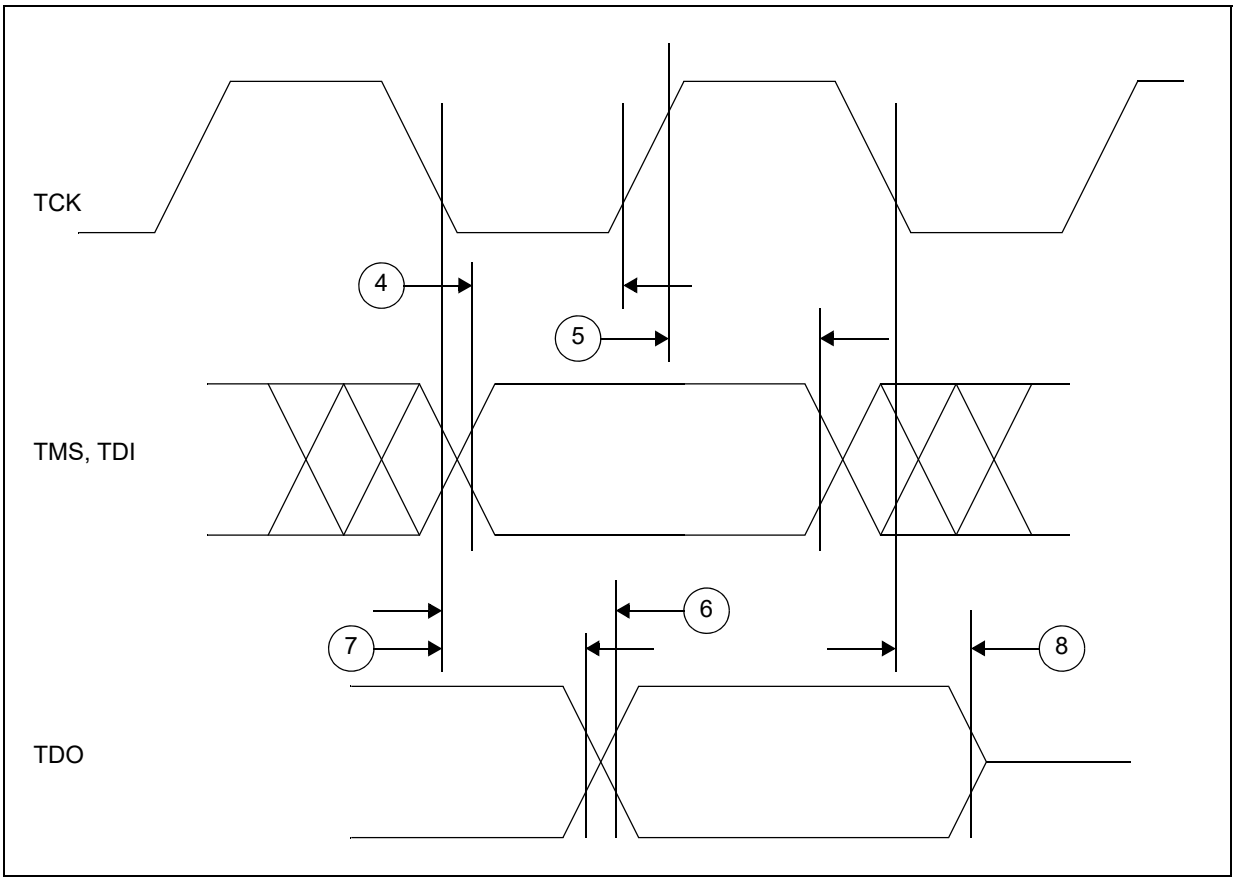
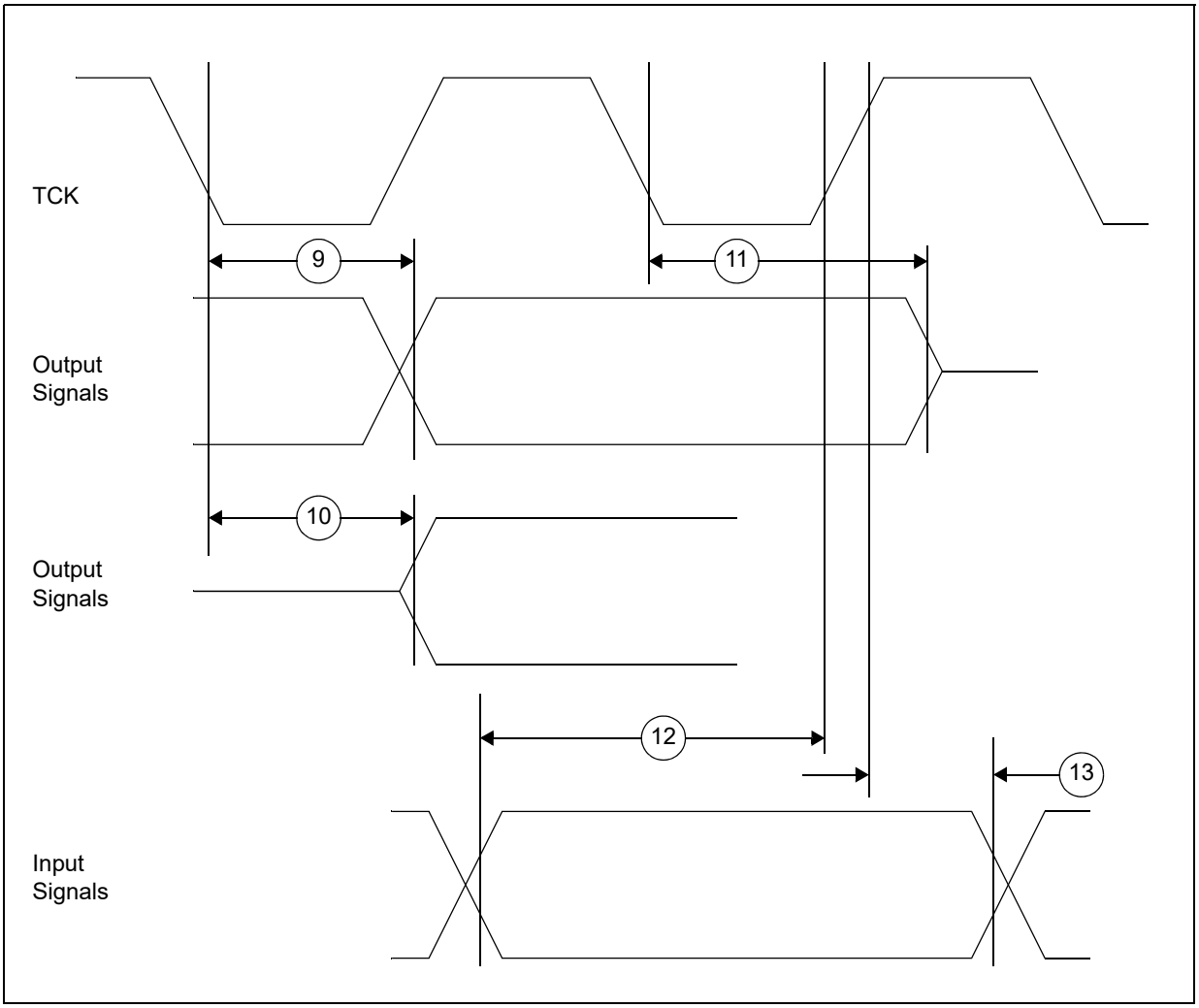


Figure 17. JTAG boundary scan timing



3.21 Nexus interface timing

Table 39. Nexus debug port timing[1]

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
7	t_{EVTIPW}	CC	P	$\overline{EVTI}$ pulse width	4	—	t_{CYC}[2]
8	t_{EVTOPW}	CC	P	$\overline{EVTO}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2[3],[4]	—	t_{CYC}[2]
11	t_{NTDIS}	CC	D	TDI data setup time	5	—	ns
12	t_{NTDIH}	CC	D	TDI data hold time	5	—	ns
13	t_{NTMSS}	CC	D	TMS data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS data hold time	5	—	ns

Table 39. Nexus debug port timing(1) (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
15	—	CC	D	TDO propagation delay from falling edge of TCK(5)	—	16	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD_HV_IO_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

Figure 18. Nexus event trigger and test clock timings

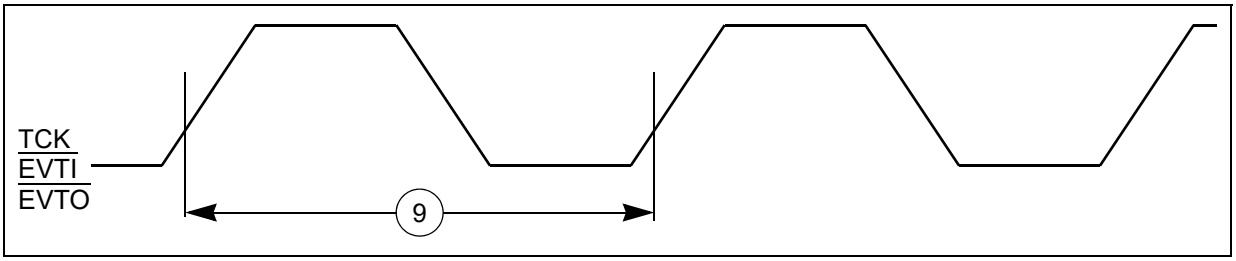
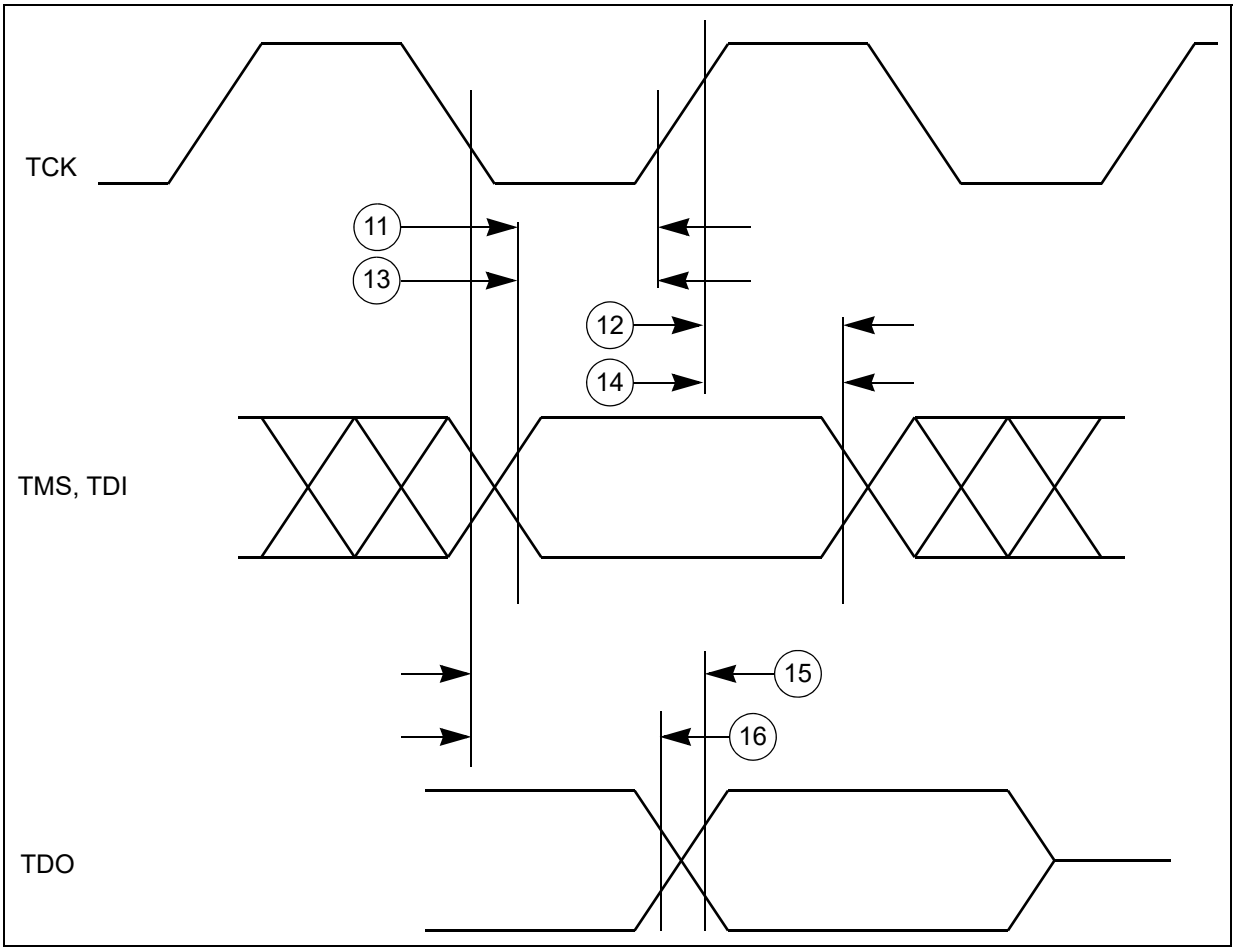


Figure 19. Nexus TDI, TMS, TDO timing



3.22 DSPI CMOS master mode timing

3.22.1 Classic timing

Table 40. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0[1]

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	75	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	50	—	ns
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	53	—	ns

Table 40. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
4	t_{SDC}	CC	D	SCK duty cycle[4]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[5]	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[5]	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK[6]	SCK drive strength				
					Very strong	25 pF	32	—	ns
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK[6]	SCK drive strength				
					Very strong	0 pF	0	—	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK[7]	SOUT and SCK drive strength				
					Very strong	25 pF	—	5	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK[7]	SOUT and SCK drive strength				
					Very strong	25 pF	2	—	ns

1. Protocol clock is 40 MHz and all pads are configured as very strong.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. PCSx and PCSS using same pad configuration.
6. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 20. DSPI CMOS master mode – classic timing, CPHA = 0

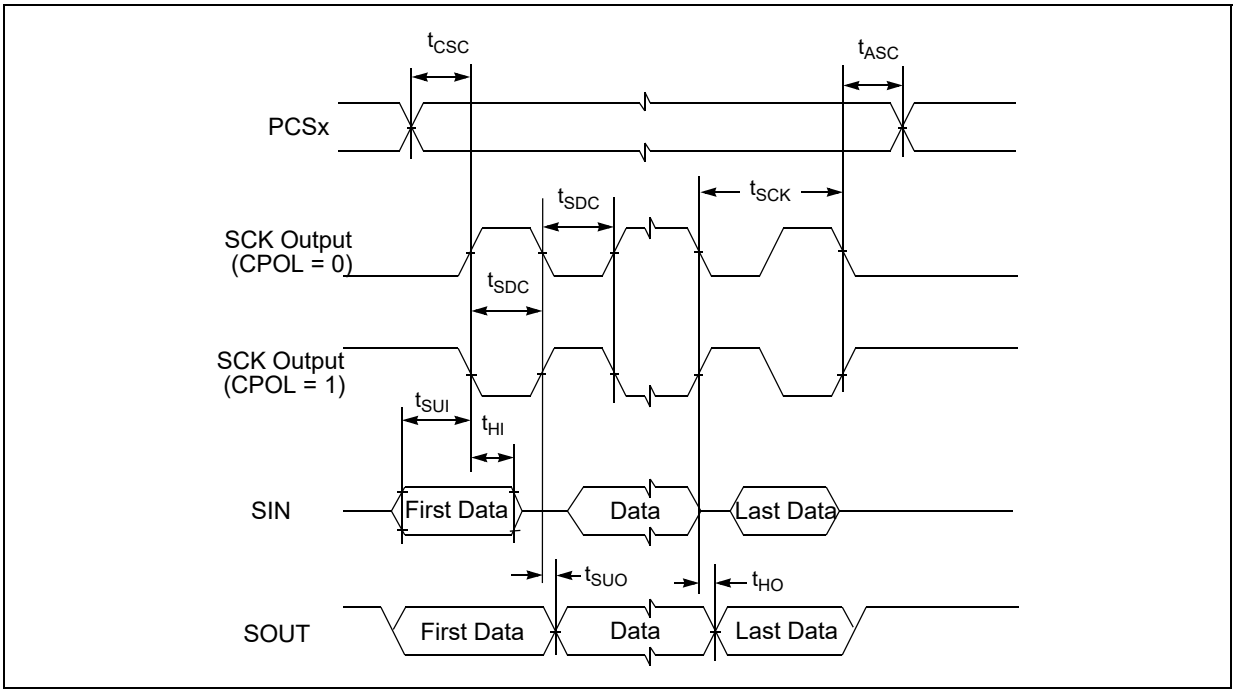


Figure 21. DSPI CMOS master mode – classic timing, CPHA = 1

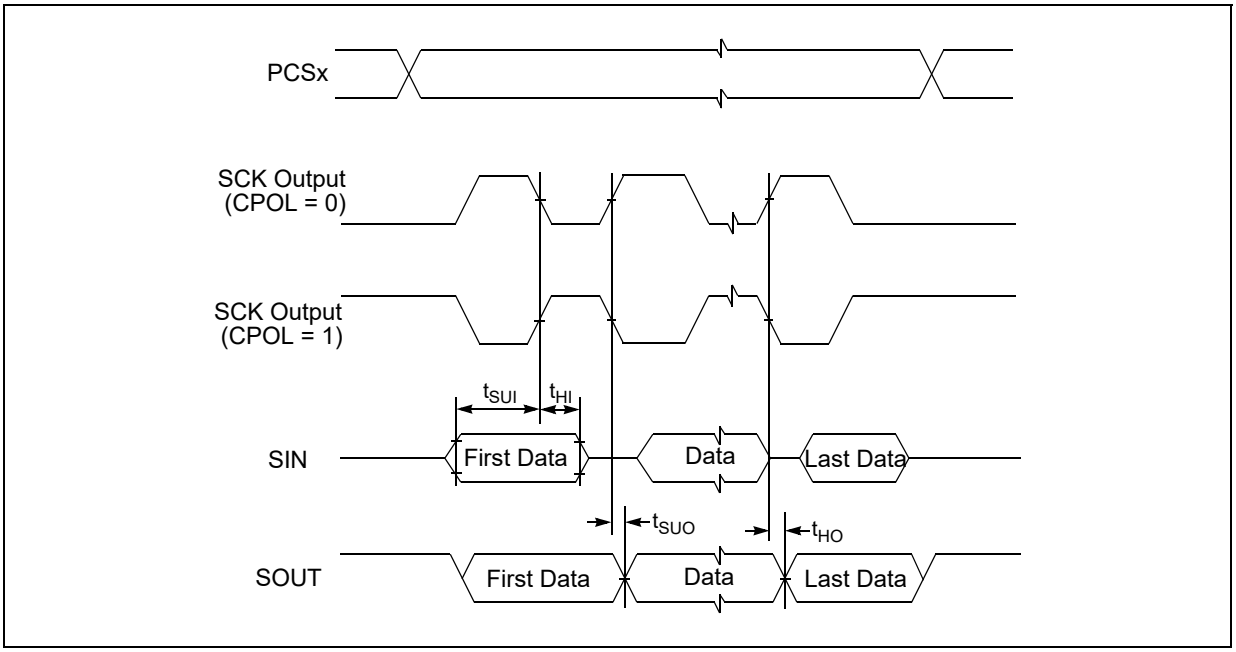
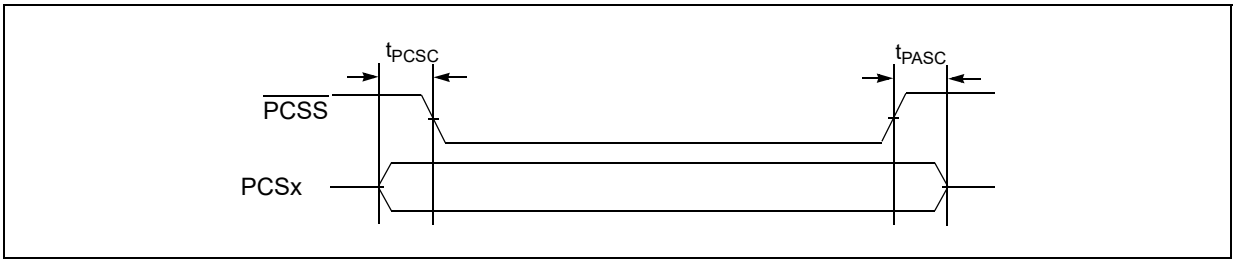


Figure 22. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.22.2 Modified timing

Table 41. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1[1]

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	50	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	50	—	ns
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	53	—	ns
4	t_{SDC}	CC	D	SCK duty cycle[4]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[5]	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[5]	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK	SCK drive strength				
					Very strong	25 pF	20	—	ns
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK	SCK drive strength				
					Very strong	0 pF	0	—	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK	SOUT and SCK drive strength				
					Very strong	25 pF	—	6	ns

Table 41. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1[1] (continued)

#	Symbol	C	Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK	SOUT and SCK drive strength			
					Very strong	25 pF	2	—	ns

1. Protocol clock is 40 MHz and all pads are configured as very strong.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. PCSx and PCSS using same pad configuration.

Figure 23. DSPI CMOS master mode – modified timing, CPHA = 0

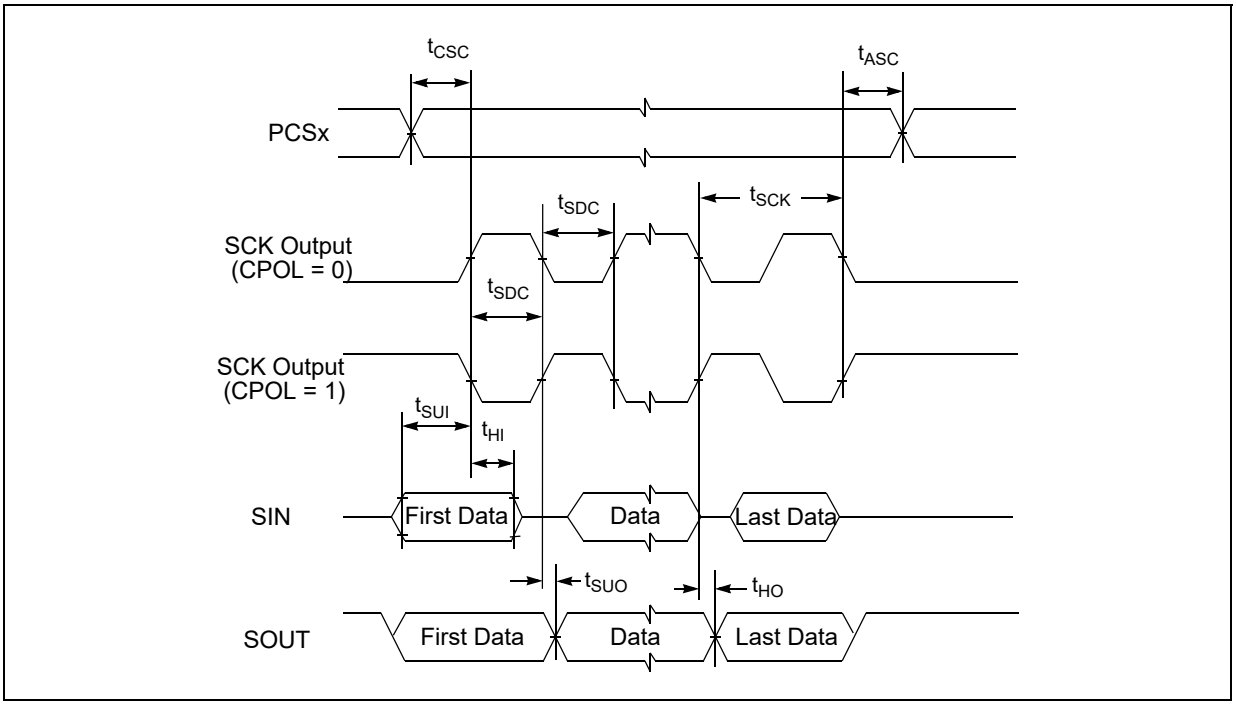


Figure 24. DSPI CMOS master mode – modified timing, CPHA = 1

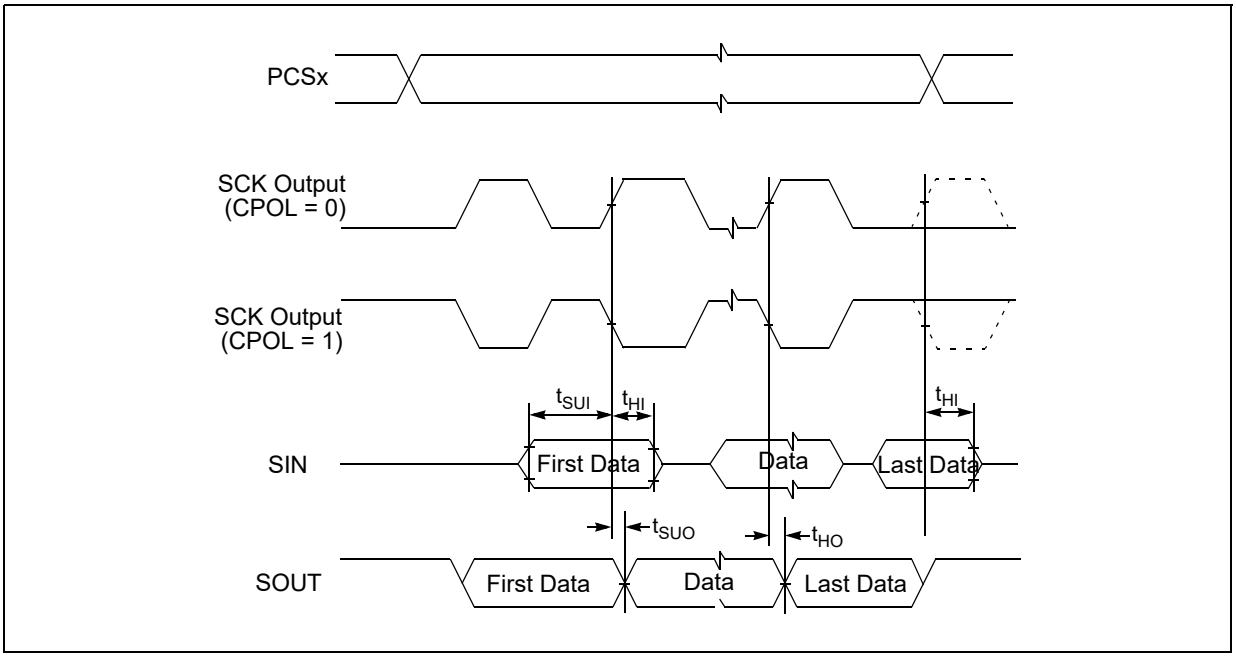
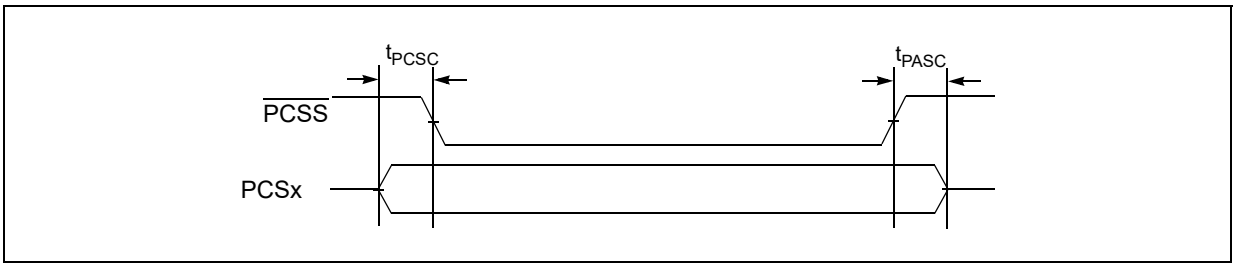


Figure 25. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

4.1 eTQFP100 package information

Figure 26. eTQFP100 package outline

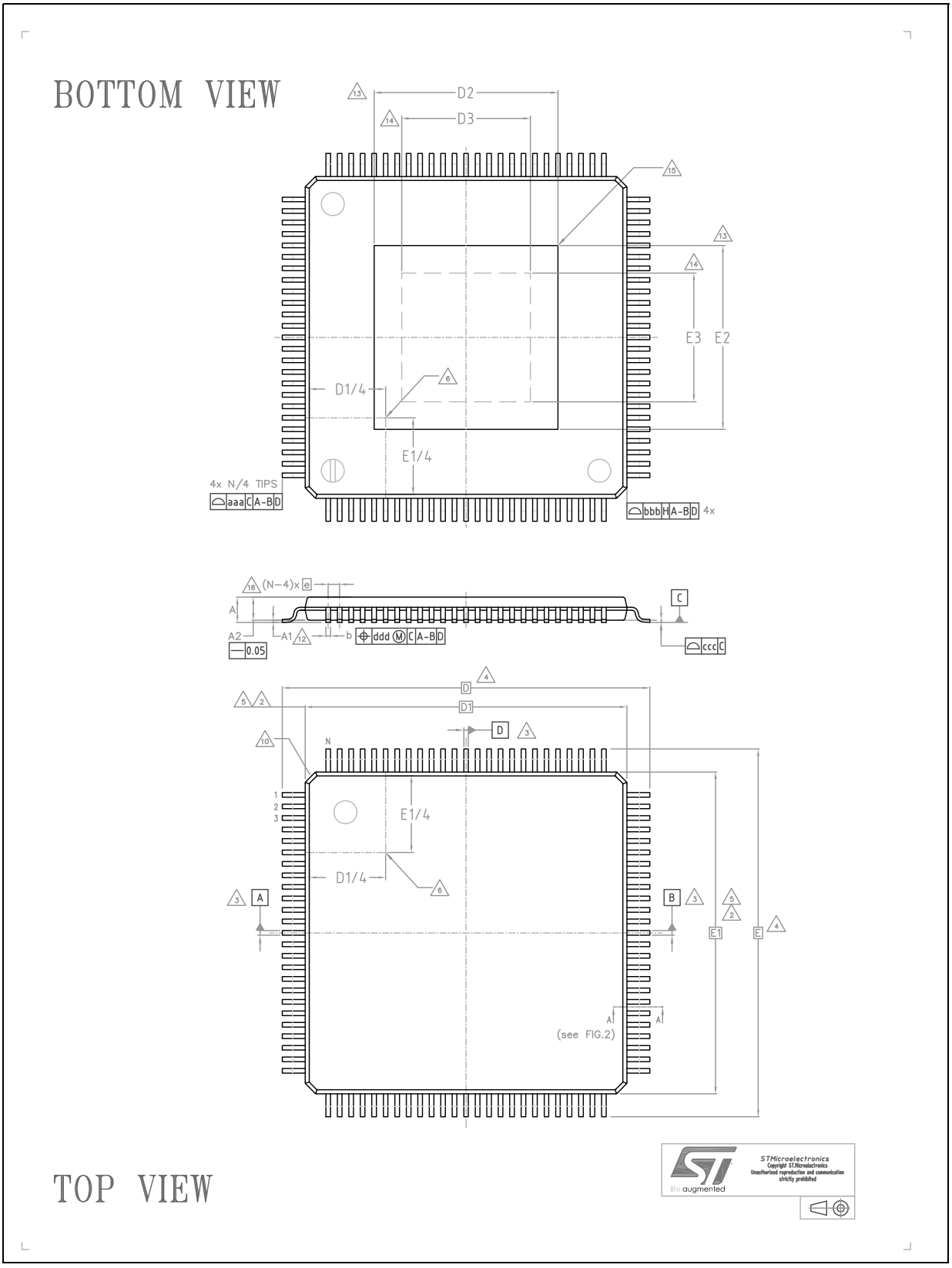


Table 42. eTQFP100 mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
A[2]	—	—	1.20	—	—	0.0472
A1[3]	0.05	—	0.15	0.0020	—	0.0059
A2[2]	0.95	1.00	1.05	0.0374	0.0394	0.0413
b[4],[5]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[5]	0.17	0.20	0.23	0.0067	0.0078	0.0091
c[5]	0.09	—	0.20	0.0035	—	0.0079
c1[5]	0.09	—	0.16	0.0035	—	0.0063
D[6]	16.00			0.6299		
D1[7],[8]	14.00			0.5512		
D2[9]	—	—	6.57	—	—	0.259
D3[10]	4.9	—	—	0.193	—	—
e	0.50			0.0197		
E[6]	16.00			0.6299		
E1[7],[8]	14.00			0.5512		
E2[9]	—	—	6.57	—	—	0.259
E3[10]	4.9	—	—	0.193	—	—
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00			0.0394		
N[11]	100			3.937		
R1	0.08	—	—	0.0031	—	—
R2	0.08	—	—	0.0031	—	—
S	0.20	—	—	0.0079	—	—
aaa[12],[13],[14]	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

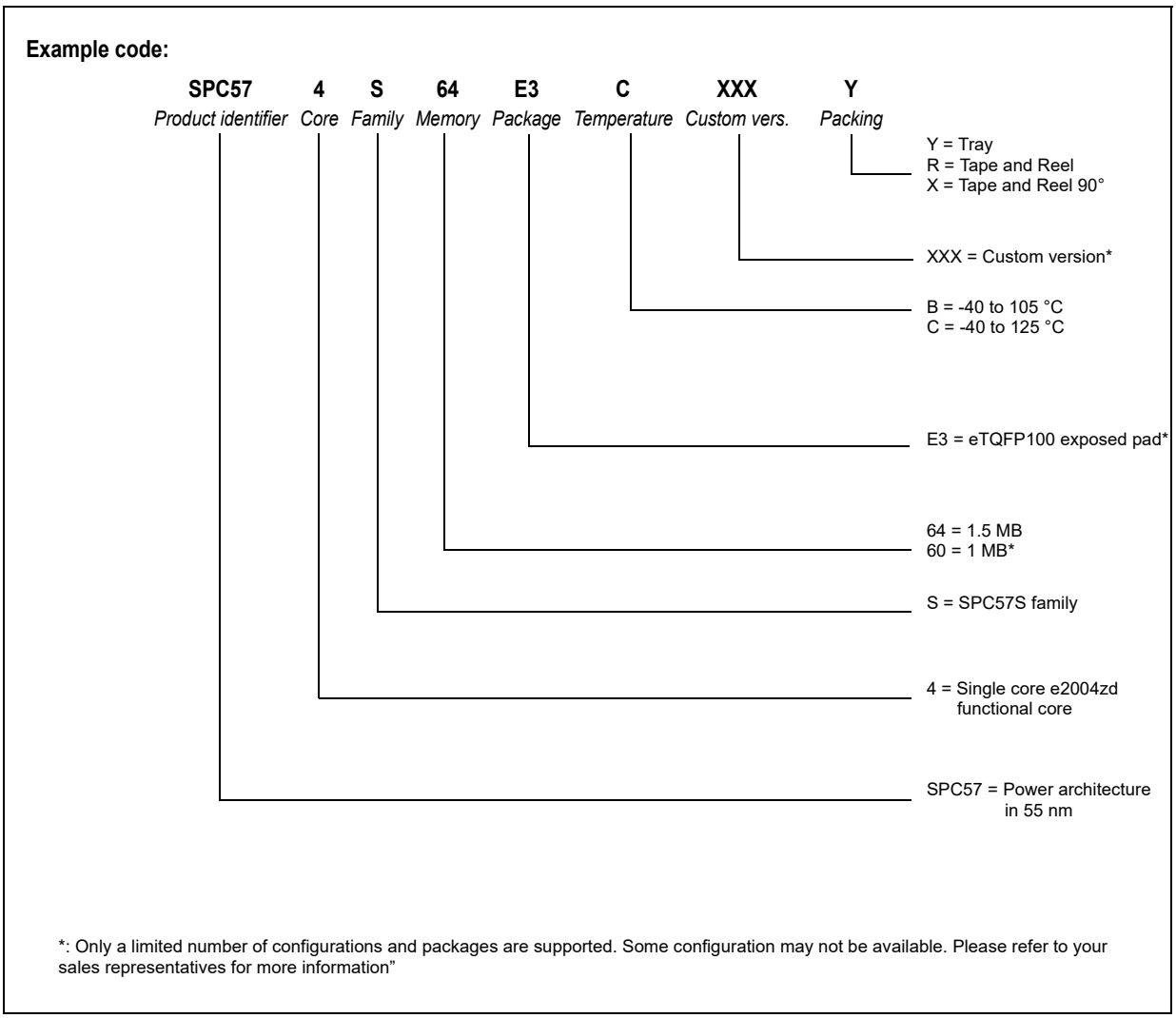
1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.

3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. To be determined at seating datum plane C.
7. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
8. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
9. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
10. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
11. “N” is the number of terminal positions for the specified body size.
12. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
13. All Dimensions are in millimeters.
14. For Symbols, Recommended Values and Tolerances see Table below:

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5 Ordering information

Figure 27. Ordering information scheme



6 Revision history

Table 43. Document revision history

Date	Revision	Changes
22-Sep-2014	1	Initial release
13-Apr-2015	2	Throughout the document: – Editorial and formatting updates – Changed device name from SPC574S60xx, to SPC574Sx – Replaced all occurrences of PLL by PLL0 and FMPLL by PLL1 – Renamed $V_{DD_HV_PMC_OSC}$ and $V_{DD_HV_OSC_PMC}$ as $V_{DD_HV_OSC}$ – Renamed $V_{DD_HV_ADV}$ and $V_{DD_ADC_TSENS}$ as $V_{DD_HV_ADC_TSENS}$ – Renamed $V_{DD_HV_IO_MAIN}$ and $V_{DD_HV_IO_JTAG}$ as $V_{DD_HV_IO}$ – Renamed $V_{DD_HV_ADR}$ as V_{REFH_ADC} – Renamed $V_{SS_HV_IO}$ as V_{SS} Added *Figure 3: 244-ball BGA pinout (top view)* and the LFBGA 244 column to *Table 3: Cross-mapping between pads and package pins* *Table 1: SPC574S60Ex, SPC574S60C2 device feature summary (superset configuration)* – For SMPU, description updated to “Yes (8 Regions)” – Footnote 1 “SMPU with process ID support extension” removed *Table 3: SPC574Sx series block summary* – Updated function description for *Cross triggering unit (CTU)* Added footnote *1* to *Table 3: Cross-mapping between pads and package pins* *Table 6: Absolute maximum ratings* – Added: $V_{DD_HV_OSC}$, $V_{DD_HV_ADC_TSENS}$, V_{REFH_ADC} – Removed T_J – Changed I_{MAXSEG} to I_{MAXSEG} *(IO rail #0)* and I_{MAXSEG} *(IO rail #1)* – Updated values of: *Cycle*, V_{SS}, V_{DD_LV}, $V_{DD_HV_IO}$, V_{IN}, I_{MAXD}, T_{SDR}, T_{XRAY} – Updated footnote *1.* and added footnote *2.* – Updated parameter descriptions for $V_{DD_HV_IO}$, $V_{DD_HV_OSC}$, I_{INJD} and I_{INJA} *Table 8: Device operating conditions*: – Added: V_{DD_LV}, $V_{DD_HV_XOSC}^{(6),(7)}$, V_{REFH_ADC} - $V_{DD_HV_ADC_TSENS}$, V_{IN} – Added footnotes *3.*, *4.*, *5.* and *8.* Updated “Very fast configuration” description in *Table 11: I/O pad specification descriptions* Added *Input Characteristics* section to *Table 12: I/O input DC electrical characteristics* Renamed *Table 18: I/O output DC characteristics for PAD[4], PAD[9], PAD[11], PAD[16], PAD[47], PAD[55], PAD[56], PAD[62] and PAD_FCCU_F1E* to include the pad numbers Removed CMOS parameters from *Table 19: Reset electrical characteristics* Added *Table 20: HV supply schemes* Added *Table 21: eTQFP100 HV/LV supply decoupling capacitances* Added *Table 25: eTQFP144 HV/LV supply decoupling capacitances* Added *Table 26: BGA244 HV/LV supply decoupling capacitances* Added *Table 28: Package ADC supply decoupling capacitance* Changed values of df_{var_T} in *Table 34: Internal RC oscillator electrical specifications*

Table 43. Document revision history (continued)

Date	Revision	Changes
13-Apr-2015	2	Updated *Table 35: ADC input leakage current* *Table 36: ADC conversion characteristics* – Changed values for I_{ADCVDD}*IADV_S* – Added footnotes for $V_{SS_HV_ADR}$ and $I_{ADCREFH}$ Removed $I_{ADCREFL}$, TUE_{10} Renamed *Figure 10* to include BGA244 Added *Figure 10: ADC decoupling capacitance/resistance scheme* Added *Section :* Removed subsections of *Section 2.2: Pin descriptions* with referral to the “Signal description” chapter in the devices’ reference manual Added *Section 3.4: Electromagnetic compatibility (EMC)* Added *Section 3.5: Electrostatic discharge (ESD)* Updated the tables in *Section 3.7: Thermal characteristics* Updated *Section 3.11: Power management* Added *Section 3.12: PMU monitor specifications* Added *Section 3.16: External oscillator (XOSC) electrical characteristics* Added *Section 3.19: Temperature sensor* Added *Section 3.20: JTAG interface timings* Added *Section 3.21: Nexus interface timing*
11-Jan-2016	3	*Figure 1: Block diagram*: added missing CMU4 block. *Figure 3: 244-ball BGA pinout (top view)*: updated pin names for A10, A11, A13, B12, B16, C18, D4, D15, D18, E18, F18, and K18 *Table 21: eTQFP100 HV/LV supply decoupling capacitances*, *Table 25: eTQFP144 HV/LV supply decoupling capacitances* and *Table 26: BGA244 HV/LV supply decoupling capacitances*: correction for VDD_LV_S2 pad name *Table 30: Flash memory program and erase specifications* and *Table 29: Flash memory Life Specification*: removed the mention “(pending silicon Qualification)” *Figure 42: eTQFP100 mechanical data* and *Figure 49: eTQFP144 mechanical data*: updated D2 and E2 values

Table 43. Document revision history (continued)

Date	Revision	Changes
11-Oct-2017	4	Updated RPNs on the cover page to “SPC574S60E3, SPC574S60E5, SPC574S64E3, SPC574S64E5” Removed references of package “BGA244” throughout the document. Number of LinFlexD instances updated from 2 to 4 *Table 1: SPC574S60Ex, SPC574S60C2 device feature summary (superset configuration)*: – System SRAM updated from “64 KB” to “96 KB” – Code flash memory updated from “1 MB” to “1.5 MB” Updated *Section :* Updated *Figure 1: Block diagram* Updated *Table 3: SPC574Sx series block summary*: – “PLL0” updated to “Frequency-modulated phase-locked loop (PLL0)” – “AIPS” updated to “PBRIDGE” – For Flash memory, “1M” updated to “1.5M” – For WKPU, external sources updated from “18” to “4” Updated *Figure 2: eTQFP 100-pin configuration*: – Pin 29 updated from “VREFH_ADC” to “PC[0]” – Pin 30 updated from “PB[9]” to “PC[1]” – Pin 37 updated from “PC[0]” to “VREFH_ADC” – Pin 38 updated from “PC[1]” to “VREFL_ADC” Updated *Figure 2.2: Pin descriptions*: – Pin 6 updated from “VREFH_ADC” to “PC[0]” – Pin 7 updated from “PB[9]” to “PC[1]” – Pin 16 updated from “PC[0]” to “VREFH_ADC” – Pin 17 updated from “PC[1]” to “VREFL_ADC” – Pin 18 updated from “VDD_HV_ADC_TSENS” to “VDD_HV_ADC_TSENS_0” – Pin 28 updated from “PG[9]” to “PH[0]” – Pin 29 updated from “VREFH_ADC” to “PH[1]” – Pin 36 updated from “PH[0]” to “VREFH_ADC_1” – Pin 37 updated from “PH[1]” to “VREFL_ADC_1” – Pin 38 updated from “VDD_HV_ADC_TSENS” to “VDD_HV_ADC_TSENS_1” Removed figure “244-ball BGA pinout (top view)” Updated *Table 4: Cross-mapping between pads and package pins*: – Removed PAD[116] – Added PAD[115] – For PAD[105], pin value for eTQFP144 updated from “28” to “-” Updated *Figure 8: Power supply scheme for eTQFP100*

Table 43. Document revision history (continued)

Date	Revision	Changes
11-Oct-2017	4 (cont'd)	*Section 3.11.3: Power Schemes*: "QFP100" and "QFP144" updated to "eTQFP100" and "eTQFP144" respectively. *Table 10: Current consumption*: – Updated IDD_LV and IDD_HV values for use case "Full function". – Added footnote "Values as seen on ... result are available." – Updated IDD_LV and IDD_HV values for Self test parallel and semi-parallel *Table 23: Package ADC supply decoupling capacitance*: – Value for Pad "VREFH_ADC_S0" for package "eTQFP100" updated from "29" to "36" – Value for Pad "VREFH_ADC_S0" for package "eTQFP144" updated from "6" to "16" – Value for Pad "VREFH_ADC_S1" for package "eTQFP144" updated from "29" to "36" *Table 24: Voltage regulator electrical characteristics*: Added footnote "All 1.2V pins...0.5nH inductance" *Table 26: Functional terminals state during power-up and reset*: For "GPIO", all "Weak pull-up" values changed to "High impedance". Updated *Table 28: Flash memory program and erase specifications* Added *Figure 14: ADC analog input circuit* *Table 42: eTQFP100 mechanical data*, – D2 and D3 value updated to "6.57" – E2 and E3 value updated to "4.9" *Table 49: eTQFP144 mechanical data*: Min value of D2 and E2 updated to 5.0 *Figure 27: Ordering information scheme*: – Memory "60" updated to "64" – Package "E4" updated to "E3" – In temperature classification , removed "D = 4 to 140 ^{o}C – Removed package LFBGA244 – Memory updated from "60 = 1MB" to "64 = 1.5MB and 60 = 1MB"

Table 43. Document revision history (continued)

Date	Revision	Changes
25-Jul-2018	5	Following are the changes in this release of the document: Updated the cover page. *Table 1: SPC574Sx device feature summary (superset configuration)*: Updated the table. *Table 2: SPC574S60Ex, SPC574S64Ex device configuration differences*: Added this table. *Section 1.3: Feature overview*: Updated the list. *Figure 2.2: Pin descriptions*: Updated the figure. *Table 6: Absolute maximum ratings*: Updated the table. *Table 8: Device operating conditions*: Updated the table. *Table 12: I/O input DC electrical characteristics*: Added a note to minimum value of V_{IH}. *Table 10: Current consumption*: Updated the table. *Table 13: I/O pull-up/pull-down DC electrical characteristics*: Updated the table. *Table 19: Reset electrical characteristics*: Removed note from below the table. *Section 3.4: Electromagnetic compatibility (EMC)*: Updated this section. *Section 3.22: DSPI CMOS master mode timing*: Added this section. *Figure 27: Ordering information scheme*: Updated the figure. *Table 25: Trimmed (PVT) values*: Lower limit for POR200 is updated to 1.820 V.
14-Feb-2020	6	Changes from rev 5 to rev 6 are listed below: Deleted all data related to eTQFP144 package including RPN SPC574S60E5 and SPC574S64E5. Removed MCAN2 throughout the document. *Table 8: Device operating conditions*: Updated conditions and values for VREFH_ADC symbol *Table 12: I/O input DC electrical characteristics*: Updated conditions to be compliant with production tests. *Table 14: Slow configuration I/O output DC characteristics*: updated condition from 4.0 V < VDD_HV_IO < 5.5 V to 4.5 V < VDD_HV_IO < 5.5 V for R_{OH_S} and R_{OL_S} *Table 15: Medium configuration I/O output DC characteristics*: updated condition from 4.0 V < VDD_HV_IO < 5.5 V to 4.5 V < VDD_HV_IO < 5.5 V for R_{OH_M} and R_{OL_M} *Table 16: Fast configuration I/O output DC characteristics*: updated condition from 4.0 V < VDD_HV_IO < 5.5 V to 4.5 V < VDD_HV_IO < 5.5 V for R_{OH_F} and R_{OL_F} *Table 17: Very Fast configuration I/O output DC characteristics*: updated condition from 4.0 V < VDD_HV_IO < 5.5 V to 4.5 V < VDD_HV_IO < 5.5 V for R_{OH_V} and R_{OL_V} *Table 19: Reset electrical characteristics*: – Updated conditions to 3.0V < VDD_HV_IO < 3.6 V and to 4.5 V < VDD_HV_IO < 5.5 V for V_{IL} – Updated condition to 3.0V<VDD_HV_IO < 5.5 V, VOL > 1.0V and value to 0.2 for IOL_R 1st condition and updated value to 12 for IOL_R 2nd condition. *Table 23: Package ADC supply decoupling capacitance*: Removed the table footnote and added its content under the table since it provides general information. *Table 32: External Oscillator electrical specifications*: updated the ”C” column for g_m

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