IP3088CX5; IP3088CX10; IP3088CX15; IP3088CX20

Integrated 2, 4, 6 and 8-channel passive LC-filter network with ESD protection to IEC 61000-4-2 level 4

Rev. 01 — 12 February 2010 Product data sheet

1. Product profile

1.1 General description

IP3088CX5, IP3088CX10, IP3088CX15 and IP3088CX20 is a 2, 4, 6 and 8-channel LC low-pass filter array family which is designed to provide filtering of undesired RF signals on the I/O ports of portable communication or computing devices. In addition, IP3088CX5, IP3088CX10, IP3088CX15 and IP3088CX20 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±15 kV according IEC 61000-4-2 level 4.

The devices are fabricated using monolithic silicon technology and integrate and incorporate up to 16 coils and 24 diodes in a 0.5 mm pitch Wafer-Level Chip-Scale Package (WLCSP).

1.2 Features and benefits

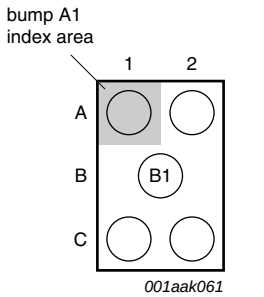
- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Integrated 2, 4, 6 and 8-channel π-type LC-filter network
- 18 Ω channel series resistance; ≤ 45 pF (at 2.5 V DC) channel capacitance
- Integrated ESD protection withstanding ±15 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- ESD protection to ±30 kV contact discharge, per MIL-STD-883D, Method 3015
- WLCSP with 0.5 mm pitch

1.3 Applications

- Cellular and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems and PDAs

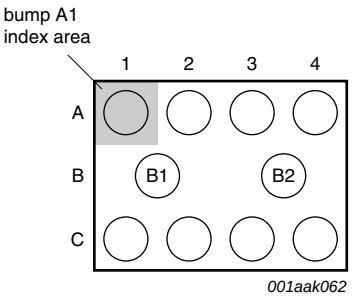
2. Pinning information

2.1 Pinning



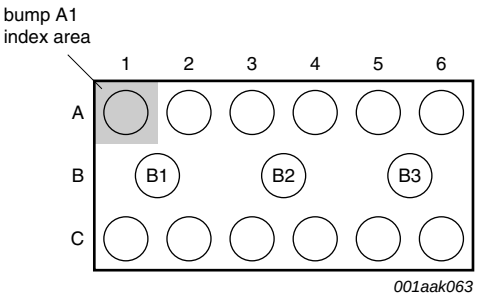
transparent top view,
solder balls facing down

Fig 1. Pin configuration IP3088CX5



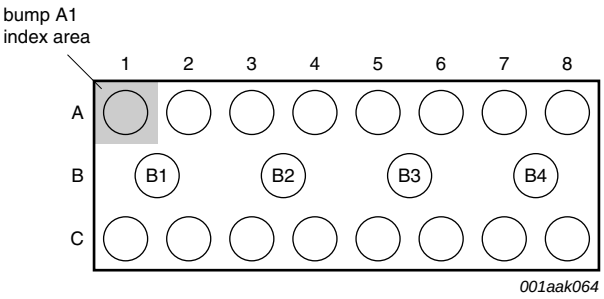
transparent top view,
solder balls facing down

Fig 2. Pin configuration IP3088CX10



transparent top view,
solder balls facing down

Fig 3. Pin configuration IP3088CX15



transparent top view,
solder balls facing down

Fig 4. Pin configuration IP3088CX20

2.2 Pin description

Table 1. Pinning

Pin				Description
IP3088CX5	**IP3088CX10**	**IP3088CX15**	**IP3088CX20**	
A1 and C1	A1 and C1	A1 and C1	A1 and C1	filter channel 1
A2 and C2	A2 and C2	A2 and C2	A2 and C2	filter channel 2
-	A3 and C3	A3 and C3	A3 and C3	filter channel 3
-	A4 and C4	A4 and C4	A4 and C4	filter channel 4
-	-	A5 and C5	A5 and C5	filter channel 5
-	-	A6 and C6	A6 and C6	filter channel 6
-	-	-	A7 and C7	filter channel 7
-	-	-	A8 and C8	filter channel 8
B1	B1 and B2	B1, B2 and B3	B1, B2, B3 and B4	ground

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3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP3088CX5	WLCSP5	wafer level chip-size package; 5 bumps; 0.96 × 1.28 × 0.65 mm	IP3088CX5
IP3088CX10	WLCSP10	wafer level chip-size package; 10 bumps; 1.96 × 1.28 × 0.65 mm	IP3088CX10
IP3088CX15	WLCSP15	wafer level chip-size package; 15 bumps; 2.96 × 1.28 × 0.65 mm	IP3088CX15
IP3088CX20	WLCSP20	wafer level chip-size package; 20 bumps; 3.96 × 1.28 × 0.65 mm	IP3088CX20

4. Functional diagram

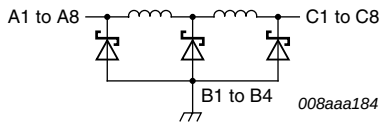


Fig 5. Schematic diagram IP3088CX5; IP3088CX10; IP3088CX15; IP3088CX20

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+5.6	V
V_{ESD}	electrostatic discharge voltage	all pins to ground				
		contact discharge	[1]	−15	+15	kV
		air discharge	[1]	−15	+15	kV
		IEC 61000-4-2 level 4; all pins to ground				
		contact discharge		−8	+8	kV
		air discharge		−15	+15	kV
		MIL-STD-883D (method 3015) HBM contact discharge		−30	+30	kV
I_{ch}	channel current (DC)	per inductor; T_{amb} = 85 °C		-	30	mA
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

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6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance			-	18	-	Ω
$L_{s(ch)}$	channel series inductance			-	40	-	nH
C_{ch}	channel capacitance	$V_{bias(DC)}$ = 0 V; f = 100 kHz	[1]	-	65	-	pF
		$V_{bias(DC)}$ = 2.5 V; f = 100 kHz	[1]	-	42	-	pF
V_{BR}	breakdown voltage	positive clamp; I_{test} = 1 mA		5.8	-	10	V
V_F	forward voltage	negative clamp; I_F = −1 mA		−1.5	-	−0.4	V
I_{LR}	reverse leakage current	per channel; V_I = 3.5 V		-	-	0.1	μA

[1] Guaranteed by design.

Table 5. Frequency characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	R_{gen} = 50 Ω; R_L = 50 Ω				
		800 MHz < f < 1.5 GHz	-	40	-	dB
		1.5 GHz < f < 3.0 GHz	-	33	-	dB
f_{-3dB}	cut-off frequency	R_{gen} = 50 Ω; R_L = 50 Ω; $V_{bias(DC)}$ = 0 V; α_{il} at 1 MHz − 3 dB	-	175	-	MHz

7. Application information

7.1 Insertion loss

IP3088CX5, IP3088CX10, IP3088CX15 and IP3088CX20 is mainly designed as an ElectroMagnetic Interference (EMI) and Radio Frequency Interference (RFI) filter for Subscriber Identity Module (SIM) card interfaces.

The setup for measuring insertion loss in a 50 Ω system is shown in Figure 6.

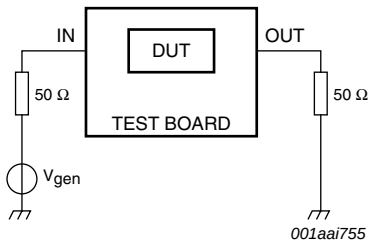
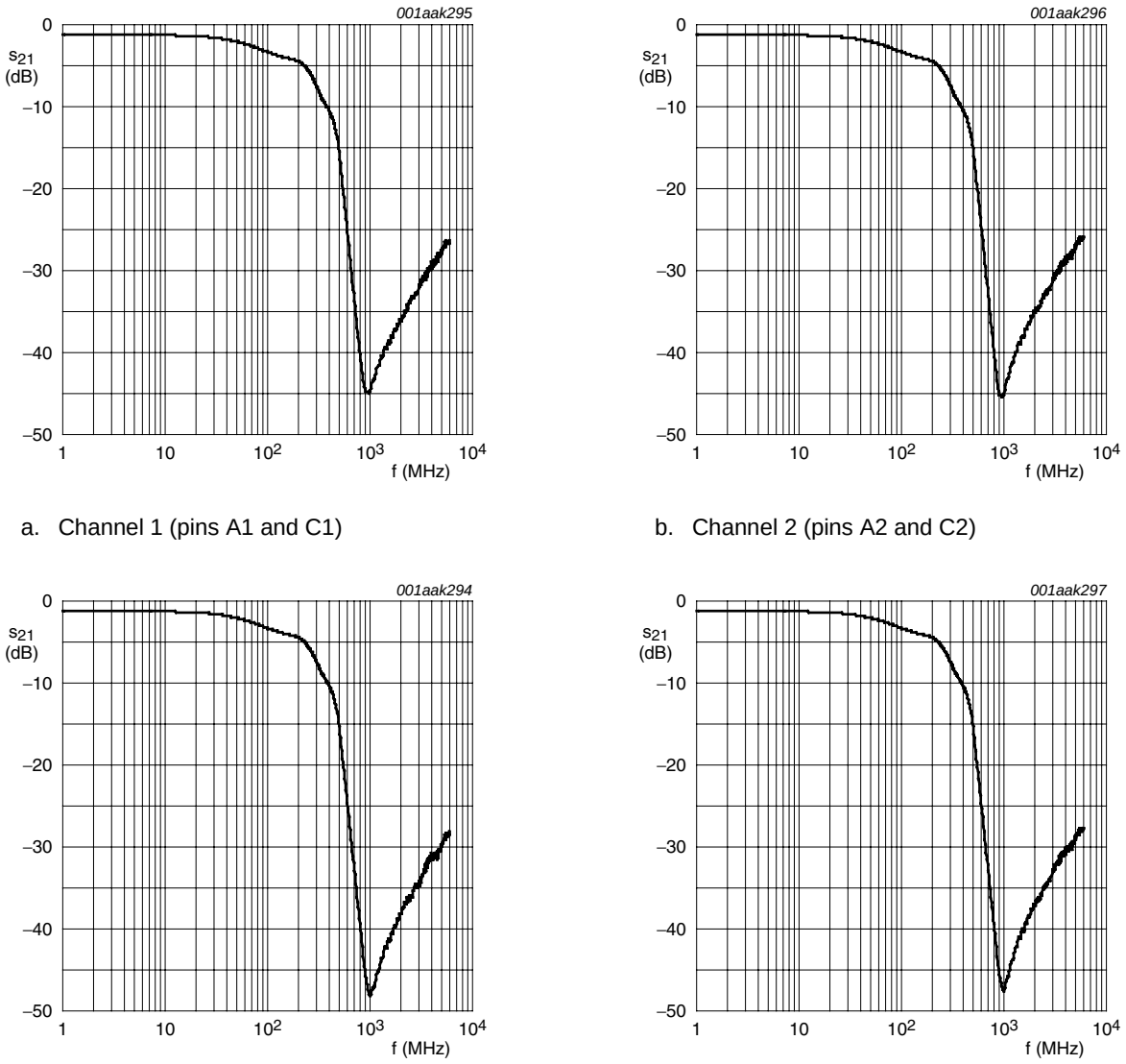


Fig 6. Frequency response measurement configuration

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As an example, the measured insertion loss magnitude for all channels of the IP3088CX10 are shown in Figure 7.



a. Channel 1 (pins A1 and C1)

b. Channel 2 (pins A2 and C2)

c. Channel 3 (pins A3 and C3)

d. Channel 4 (pins A4 and C4)

Fig 7. Measured insertion loss magnitude

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8. Package outline

WLCSP20: wafer level chip-size package; 20 bumps (8-4-8)

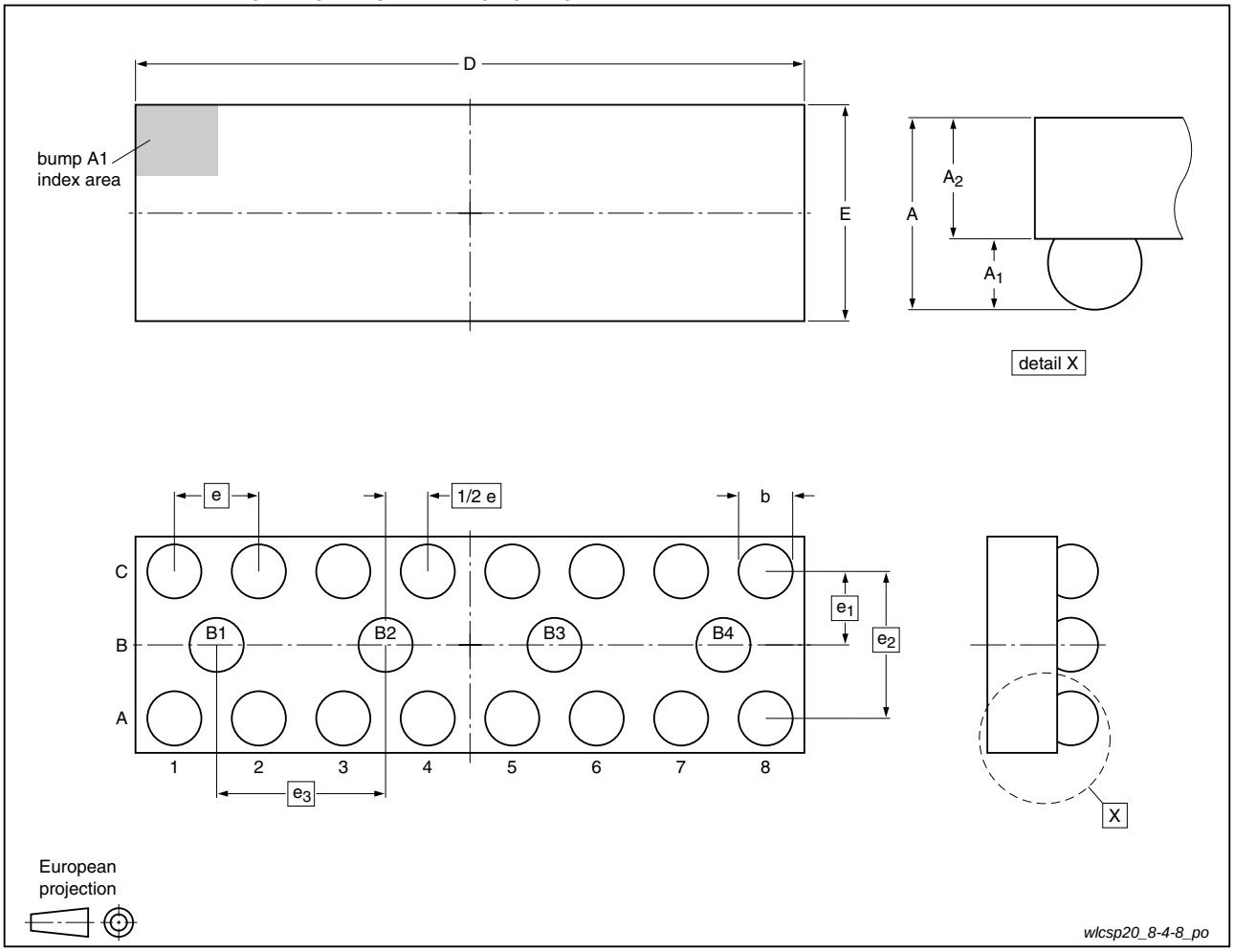


Fig 8. Package outline IP3088CX20 (WLCSP20)

Table 6. Dimensions for Figure 8

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	3.91	3.96	4.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.435	-	mm
e_2	-	0.87	-	mm
e_3	-	1.0	-	mm

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WLCSP15: wafer level chip-size package; 15 bumps (6-3-6)

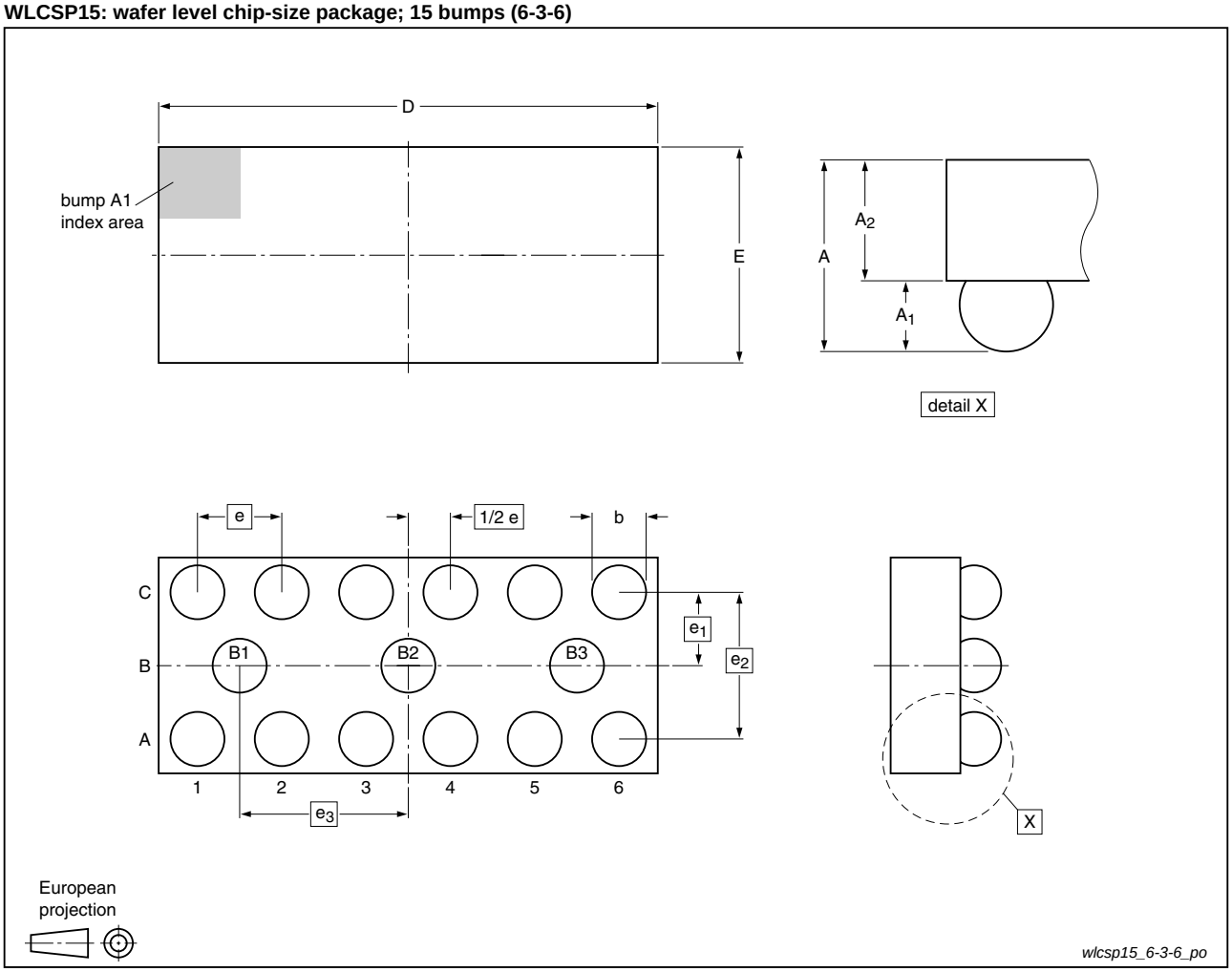


Fig 9. Package outline IP3088CX15 (WLCSP15)

Table 7. Dimensions for Figure 9

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	2.91	2.96	3.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.435	-	mm
e_2	-	0.87	-	mm
e_3	-	1.0	-	mm

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WLCSP10: wafer level chip-size package; 10 bumps (4-2-4)

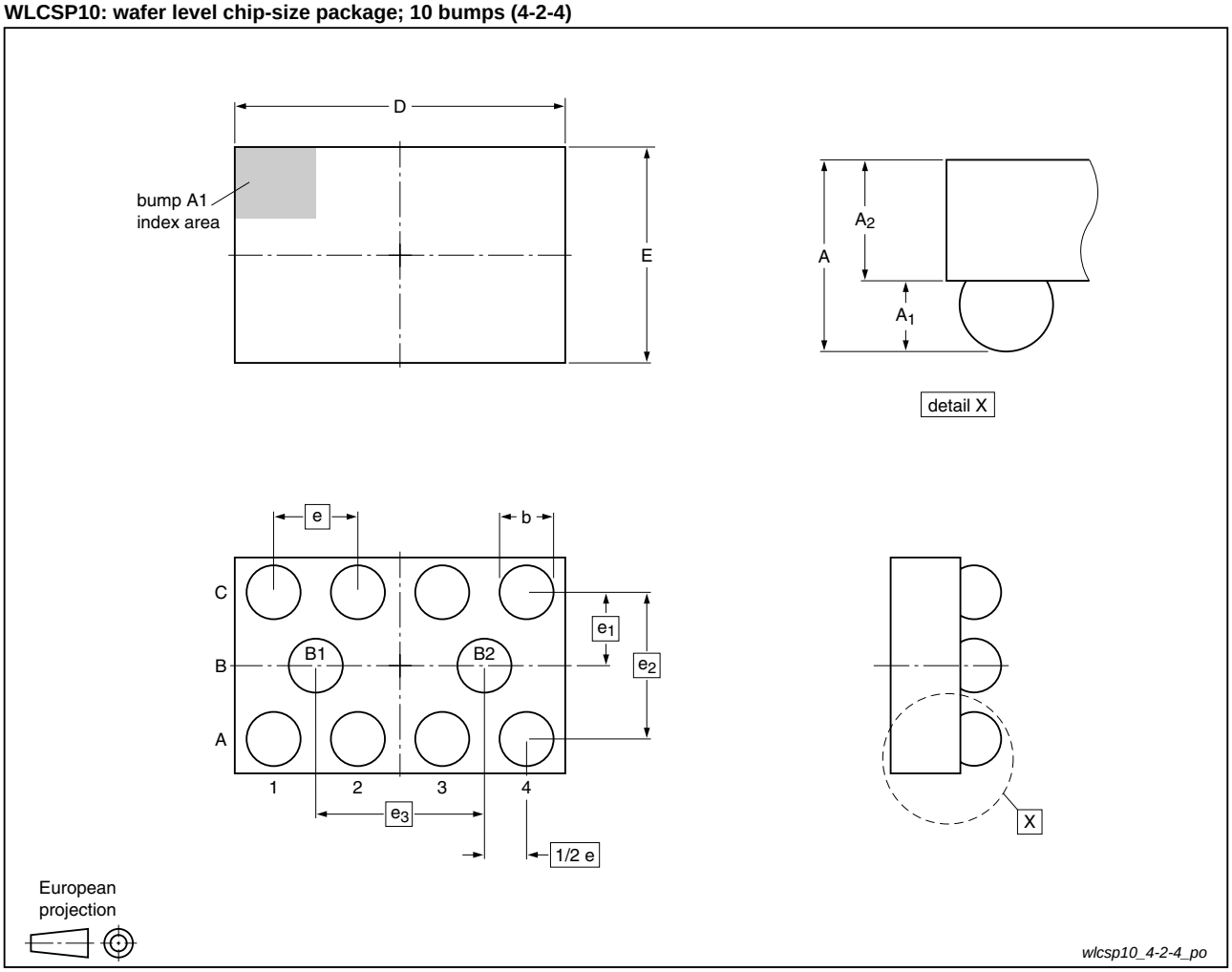


Fig 10. Package outline IP3088CX10 (WLCSP10)

Table 8. Dimensions for Figure 10

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	1.91	1.96	2.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.435	-	mm
e_2	-	0.87	-	mm
e_3	-	1.0	-	mm

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WLCSP5: wafer level chip-size package; 5 bumps (2-1-2)

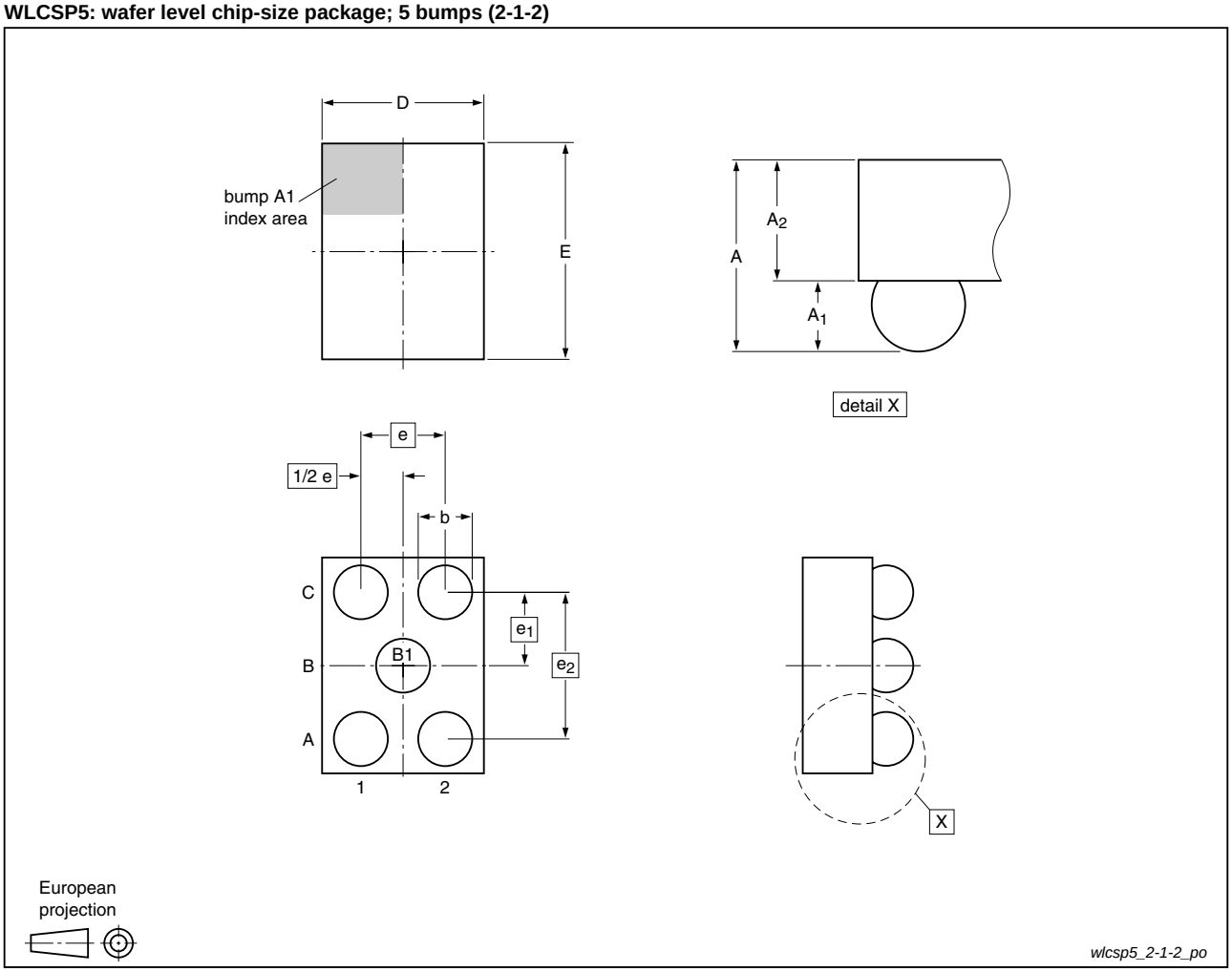


Fig 11. Package outline IP3088CX5 (WLCSP5)

Table 9. Dimensions for Figure 11

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	0.91	0.96	1.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.435	-	mm
e_2	-	0.87	-	mm

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9. Soldering of WLCSP packages

9.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

9.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

9.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10.

Table 10. Lead-free process (from J-STD-020C)

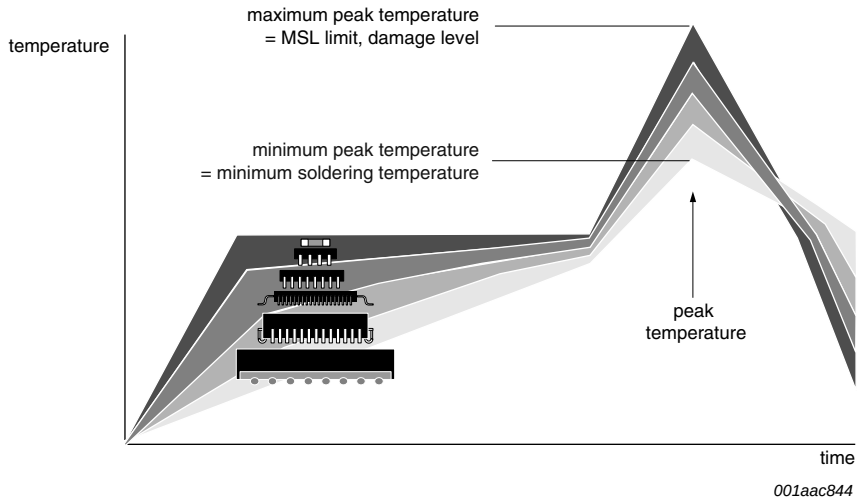
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.

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MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

9.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

9.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

9.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

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Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

9.3.4 Cleaning

Cleaning can be done after reflow soldering.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
LAN	Local Area Network
PCB	Printed-Circuit Board
PCS	Personal Communication System
PDA	Personal Digital Assistant
RFI	Radio Frequency Interference
RoHS	Restriction of Hazardous Substances
SIM	Subscriber Identity Module
WAN	Wide Area Network
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3088CX5_CX10_CX15_CX20_1	20100212	Product data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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