Features

- Transparent RF Receiver ICs for 315 MHz (ATA8201) and 433.92 MHz (ATA8202) With High Receiving Sensitivity
- Fully Integrated PLL With Low Phase Noise VCO, PLL, and Loop Filter
- High FSK/ASK Sensitivity:–105 dBm (ATA8201, FSK, 9.6 Kbits/s, Manchester, BER 10^{-3})
  –114 dBm (ATA8201, ASK, 2.4 Kbits/s, Manchester, BER 10^{-3})
  –104 dBm (ATA8202, FSK, 9.6 Kbits/s, Manchester, BER 10^{-3})
  –113 dBm (ATA8202, ASK, 2.4 Kbits/s, Manchester, BER 10^{-3})
- Supply Current: 6.5 mA in Active Mode (3V, 25°C, ASK Mode)
- Data Rate: 1 Kbit/s to 10 Kbits/s Manchester ASK, 1 Kbit/s to 20 Kbits/s Manchester FSK With Four Programmable Bit Rate Ranges
- Switching Between Modulation Types ASK/FSK and Different Data Rates Possible in ≤ 1 ms Typically, Without Hardware Modification on Board to Allow Different Modulation Schemes
- Low Standby Current: 50 µA at 3V, 25°C
- ASK/FSK Receiver Uses a Low-IF Architecture With High Selectivity, Blocking, and Low Intermodulation (Typical 3-dB Blocking 68.0 dBC at ±3 MHz/74.0 dBC at ±20.0 MHz, System I1dBCP = –31 dBm/System IIP3 = –24 dBm)
- Telegram Pause Up to 52 ms Supported in ASK Mode
- Wide Bandwidth AGC to Handle Large Out-of-band Blockers above the System I1dBCP
- 440-kHz IF Frequency With 30-dB Image Rejection and 420-kHz IF Bandwidth to Support PLL Transmitters With Standard Crystals or SAW-based Transmitters
- RSSI (Received Signal Strength Indicator) With Output Signal Dynamic Range of 65 dB
- Low In-band Sensitivity Change of Typically ±2.0 dB Within ±160-kHz Center Frequency Change in the Complete Temperature and Supply Voltage Range
- Sophisticated Threshold Control and Quasi-peak Detector Circuit in the Data Slicer
- Fast and Stable XTO Start-up Circuit (> –1.4 kΩ Worst-case Start Impedance)
- Clock Generation for Microcontroller
- ESD Protection at all Pins (±4 kV HBM, ±200V MM, ±500V FCDM)
- Dual Supply Voltage Range: 2.7V to 3.3V or 4.5V to 5.5V
- Temperature Range: –40°C to +85°C
- Small 5 mm × 5 mm QFN24 Package

Applications

- Industrial/Aftermarket Keyless Entry and Tire Pressure Monitoring Systems
- Alarm, Telemetering and Energy Metering Systems
- Remote Conrol Systems for Consumer and Industrial Markets
- Access Control Systems
- Home Automation
- Home Entertainment
- Toys

UHF ASK/FSK Receiver

ATA8201
ATA8202

4971A–IND–01/07

Benefits

- **Supports Header and Blanking Periods of Protocols Common in RKE and TPM Systems (Up to 52 ms in ASK Mode)**
- **All RF Relevant Functions are Integrated. The Single-ended RF Input is Suited for Easy Adaptation to λ / 4 or Printed-loop Antennas**
- **Allows a Low-cost Application With Only 8 Passive Components**
- **Optimal Bandwidth Maximizes Sensitivity while Maintaining SAW Transmitter Compatibility**
- **Clock Output Provides an External Microcontroller Crystal-precision Time Reference**
- **Well Suited for Use With PLL Transmitter ATA5756/ATA5757**

1. General Description

The ATA8201/ATA8202 is a UHF ASK/FSK transparent receiver IC with low power consumption supplied in a small QFN24 package (body 5 mm × 5 mm, pitch 0.65 mm). ATA8202 is used in the 433 MHz to 435 MHz band of operation, and ATA8201 in 313 MHz to 317 MHz.

For improved image rejection and selectivity, the IF frequency is fixed to 440 kHz. The IF block uses an 8th-order band pass yielding a receive bandwidth of 420 kHz. This enables the use of the receiver in both SAW- and PLL-based transmitter systems utilizing various types of data-bit encoding such as pulse width modulation, Manchester modulation, variable pulse modulation, pulse position modulation, and NRZ. Prevailing encryption protocols such as Keeloq® are easily supported due to the receiver's ability to hold the current data slicer threshold for up to 52 ms when incoming RF telegrams contain a blanking interval. This feature eliminates erroneous noise from appearing on the demodulated data output pin, and simplifies software decoding algorithms. The decoding of the data stream must be carried out by a connected microcontroller device. Because of the highly integrated design, the only required RF components are for the purpose of receiver antenna matching.

ATA8201 and ATA8202 support Manchester bit rates of 1 Kbit/s to 10 Kbits/s in ASK and 1 Kbit/s to 20 Kbits/s in FSK mode. The four discrete bit rate passbands are selectable and cover 1.0 Kbit/s to 2.5 Kbits/s, 2.0 Kbits/s to 5.0 Kbits/s, 4.0 Kbits/s to 10.0 Kbits/s, and 8.0 Kbits/s to 10.0 Kbits/s or 20.0 Kbits/s (for ASK or FSK, respectively). The receiver contains an RSSI output to provide an indication of received signal strength and a SENSE input to allow the customer to select a threshold below which the DATA signal is gated off. ASK/FSK and bit rate ranges are selected by the connected microcontroller device via pins ASK_NFSK, BR0, and BR1.

Figure 1-1. System Block Diagram

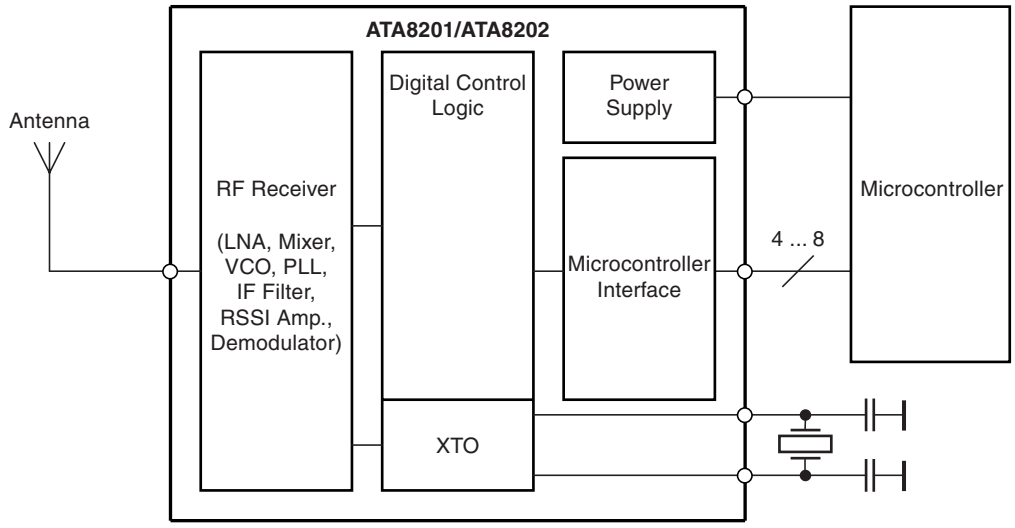


Figure 1-2. Pinning QFN24

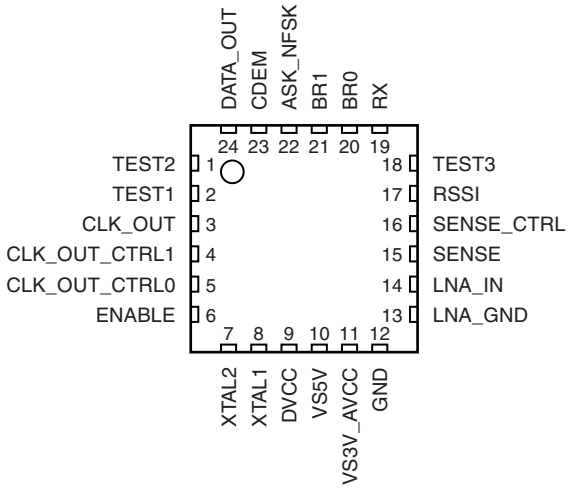
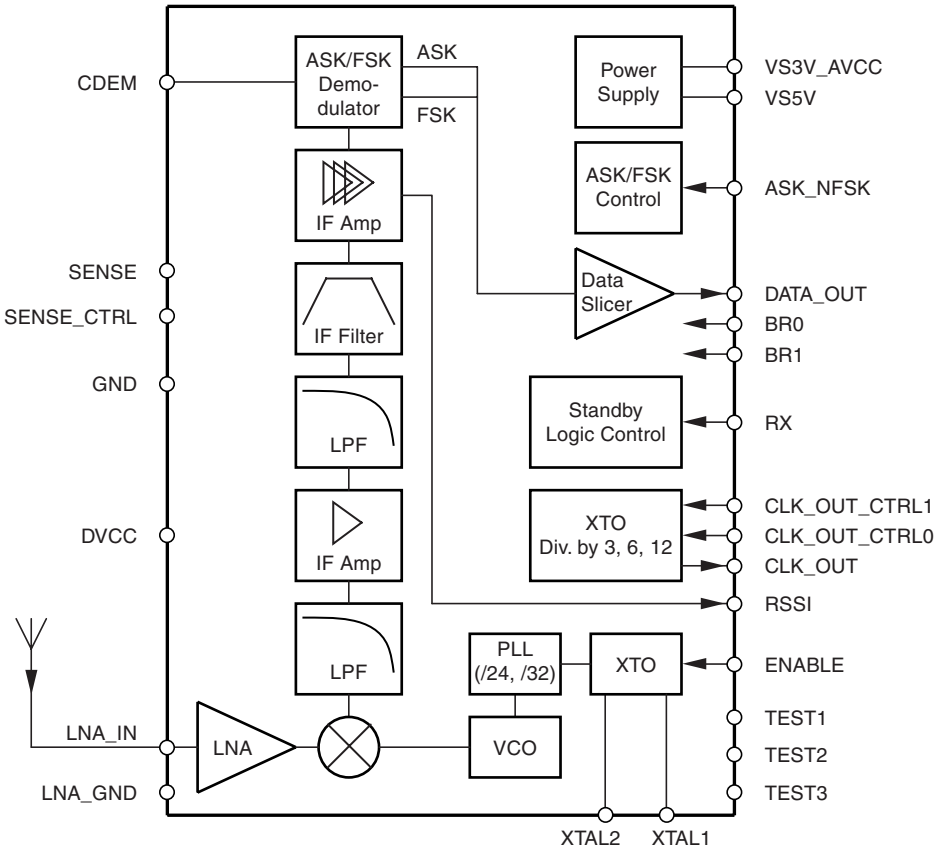


Table 1-1. Pin Description

Pin	Symbol	Function
1	TEST2	Test pin, during operation at GND
2	TEST1	Test pin, during operation at GND
3	CLK_OUT	Output to clock a connected microcontroller
4	CLK_OUT_CTRL1	Input to control CLK_OUT (MSB)
5	CLK_OUT_CTRL0	Input to control CLK_OUT (LSB)
6	ENABLE	Input to enable the XTO
7	XTAL2	Reference crystal
8	XTAL1	Reference crystal
9	DVCC	Digital voltage supply blocking
10	VS5V	Power supply input for voltage range 4.5V to 5.5V
11	VS3V_AVCC	Power supply input for voltage range 2.7V to 3.3V
12	GND	Ground
13	LNA_GND	RF ground
14	LNA_IN	RF input
15	SENSE	Sensitivity control resistor
16	SENSE_CTRL	Sensitivity selection Low: Normal sensitivity, High: Reduced sensitivity
17	RSSI	Output of the RSSI amplifier
18	TEST3	Test pin, during operation at GND
19	RX	Input to activate the receiver
20	BR0	Bit rate selection, LSB
21	BR1	Bit rate selection, MSB
22	ASK_NFSK	FSK/ASK selection Low: FSK, High: ASK
23	CDEM	Capacitor to adjust the lower cut-off frequency data filter
24	DATA_OUT	Data output
	GND	Ground/backplane (exposed die pad)

Figure 1-3. Block Diagram



2. RF Receiver

As seen in Figure 1-3 on page 5, the RF receiver consists of a low-noise amplifier (LNA), a local oscillator, and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter, and data slicer.

In receive mode, the LNA pre-amplifies the received signal which is converted down to a 440-kHz intermediate frequency (IF), then filtered and amplified before it is fed into an FSK/ASK demodulator, data filter, and data slicer. The received signal strength indicator (RSSI) signal is available at the pin RSSI.

2.1 Low-IF Receiver

The receive path consists of a fully integrated low-IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage, and supply current specification needed to design, e.g., an industrial/aftermarket integrated receiver for RKE and TPM systems. A benefit of the integrated receive filter is that no external components needed.

At 315 MHz, the ATA8201 receiver (433.92 MHz for the ATA8202 receiver) has a typical system noise figure of 6.0 dB (7.0 dB), a system I1dBCP of –31 dBm (–30 dBm), and a system IIP3 of –24 dBm (–23 dBm). The signal path is linear for out-of-band disturbers up to the I1dBCP and hence there is no AGC or switching of the LNA needed, and a better blocking performance is achieved. This receiver uses an IF (intermediate frequency) of 440 kHz, the typical image rejection is 30 dB and the typical 3-dB IF filter bandwidth is 420 kHz (f_{IF} = 440 kHz ± 210 kHz, f_{lo_IF} = 230 kHz and f_{hi_IF} = 650 kHz). The demodulator needs a signal-to-noise ratio of 8.5 dB for 10 Kbits/s Manchester with ±38 kHz frequency deviation in FSK mode, thus, the resulting sensitivity at 315 MHz (433.92 MHz) is typically –105 dBm (–104 dBm).

Due to the low phase noise and spurs of the synthesizer together with the 8th-order integrated IF filter, the receiver has a better selectivity and blocking performance than more complex double superhet receivers, without using external components and without numerous spurious receiving frequencies.

A low-IF architecture is also less sensitive to second-order intermodulation (IIP2) than direct conversion receivers where every pulse or amplitude modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second-order non-linearities.

2.2 Input Matching at LNA_IN

The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in Table 2-1. The highest sensitivity is achieved with power matching of these impedances to the source impedance.

Table 2-1. Measured Input Impedances of the LNA_IN Pin

f_{RF} [MHz]	Z_{In}(RF_IN) [Ω]	R_{In_p}//C_{In_p} [pF]
315	(72.4 – j298)	1300Ω//1.60
433.92	(55 – j216)	900Ω//1.60

The matching of the LNA input to 50Ω is done using the circuit shown in Figure 2-1 and the values of the matching elements given in Table 2-2. The reflection coefficients were always ≤–10 dB. Note that value changes of C1 and L1 may be necessary to compensate individual board layout parasitics. The measured typical FSK and ASK Manchester-code sensitivities with a bit error rate (BER) of 10^{-3} are shown in Table 2-3 and Table 2-4 on page 8. These measurements were done with wire-wound inductors having quality factors reported in Table 2-2, resulting in estimated matching losses of 0.8 dB at 315 MHz and 433.92 MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with $R_{loss} = 2 \times \pi \times f \times L \times Q_L$ and the matching loss with $10 \log(1+R_{In\_p} / R_{loss})$.

Figure 2-1. Input Matching to 50Ω

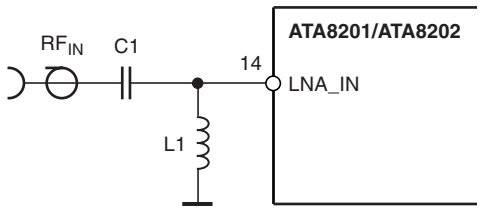


Table 2-2. Input Matching to 50Ω

f_{RF} [MHz]	C_1 [pF]	L_1 [nH]	Q_{L1}
315	2.2	68	20
433.92	2.2	36	15

Table 2-3. Measured Typical Sensitivity FSK, ±38 kHz, Manchester, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0 Kbit/s	BR_Range_0 2.5 Kbits/s	BR_Range_1 5 Kbits/s	BR_Range_2 10 Kbits/s	BR_Range_3 10 Kbits/s	BR_Range_3 20 Kbits/s
315 MHz	–108 dBm	–108 dBm	–107 dBm	–105 dBm	–104 dBm	–104 dBm
433.92 MHz	–107 dBm	–107 dBm	–106 dBm	–104 dBm	–103 dBm	–103 dBm

Table 2-4. Measured Typical Sensitivity 100% ASK, Manchester, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0 Kbit/s	BR_Range_0 2.5 Kbits/s	BR_Range_1 5 Kbits/s	BR_Range_2 10 Kbits/s	BR_Range_3 10 Kbits/s
315 MHz	–114 dBm	–114 dBm	–113 dBm	–111 dBm	–109 dBm
433.92 MHz	–113 dBm	–113 dBm	–112 dBm	–110 dBm	–108 dBm

Conditions for the sensitivity measurement:

The given sensitivity values are valid for Manchester-modulated signals. For the sensitivity measurement the distance from edge to edge must be evaluated. As can be seen in Figure 6-1 on page 25, in a Manchester-modulated data stream, the time segments T_{EE} and $2 \times T_{EE}$ occur.

To reach the specified sensitivity for the evaluation of T_{EE} and $2 \times T_{EE}$ in the data stream, the following limits should be used (T_{EE} min, T_{EE} max, $2 \times T_{EE}$ min, $2 \times T_{EE}$ max).

Table 2-5. Limits for Sensitivity Measurements

Bit Rate	T_{EE} Min	T_{EE} Typ	T_{EE} Max	$2 \times T_{EE}$ Min	$2 \times T_{EE}$ Typ	$2 \times T_{EE}$ Max
1.0 Kbit/s	260 µs	500 µs	790 µs	800 µs	1000 µs	1340 µs
2.4 Kbits/s	110 µs	208 µs	310 µs	320 µs	416 µs	525 µs
5.0 Kbits/s	55 µs	100 µs	155 µs	160 µs	200 µs	260 µs
9.6 Kbits/s	27 µs	52 µs	78 µs	81 µs	104 µs	131 µs

2.3 Sensitivity Versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system, it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure, and IF-filter bandwidth of the receiver. Figure 2-2 and Figure 2-3 on page 9 show the typical sensitivity at 315 MHz, ASK, 2.4 Kbits/s and 9.6 Kbits/s, Manchester, Figure 2-4 and Figure 2-5 on page 10 show a typical sensitivity at 315 MHz, FSK, 2.4 Kbits/s and 9.6 Kbits/s, ±38 kHz, Manchester versus the frequency offset between transmitter and receiver at T_{amb} = +25°C and supply voltage VS = VS3V_AVCC = VS5V = 3.0V.

Figure 2-2. Measured Sensitivity (315 MHz, ASK, 2.4 Kbits/s, Manchester) Versus Frequency Offset

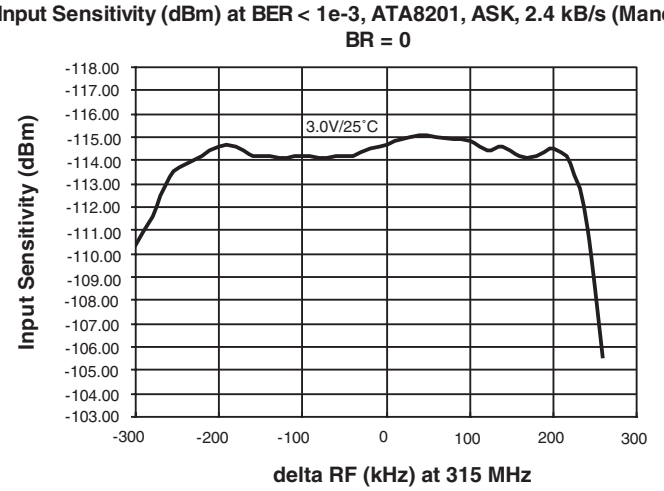


Figure 2-3. Measured Sensitivity (315 MHz, ASK, 9.6 Kbits/s, Manchester) Versus Frequency Offset

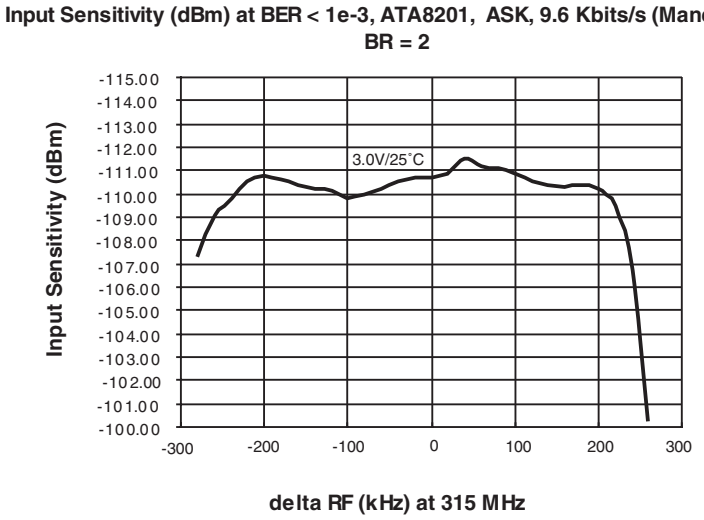


Figure 2-4. Measured Sensitivity (315 MHz, FSK, 2.4 Kbits/s, ±38 kHz, Manchester) Versus Frequency Offset

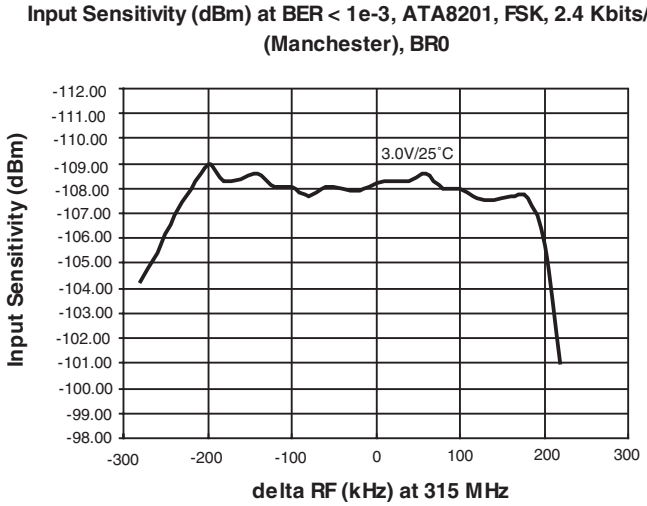
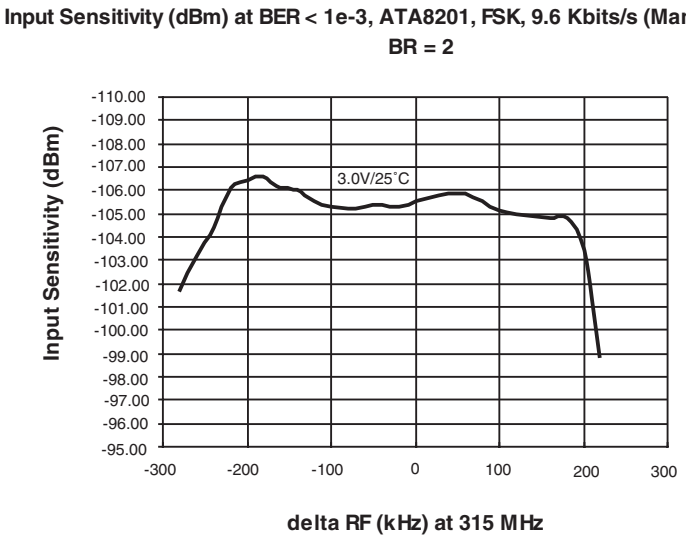


Figure 2-5. Measured Sensitivity (315 MHz, FSK, 9.6 Kbits/s, ±38 kHz, Manchester) Versus Frequency Offset



As can be seen in Figure 2-5 on page 10, the supply voltage has almost no influence. The temperature has an influence of about ±1.0 dB, and a frequency offset of ±160 kHz also influences by about ±1 dB. All these influences, combined with the sensitivity of a typical IC (–105 dB), are then within a range of –103.0 dBm and –107.0 dBm over temperature, supply voltage, and frequency offset. The integrated IF filter has an additional production tolerance of ±10 kHz, hence, a frequency offset between the receiver and the transmitter of ±160 kHz can be accepted for XTAL and XTO tolerances.

Note: For the demodulator used in the ATA8201/ATA8202, the tolerable frequency offset does not change with the data frequency. Hence, the value of ±160 kHz is valid for 1 Kbit/s to 10 Kbits/s.

This small sensitivity change over supply voltage, frequency offset, and temperature is very unusual in such a receiver. It is achieved by an internal, very fast, and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly. If, however, the input frequency makes a larger step (for example, if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to Standby mode and then again to Active mode (pin RX 1 →0 →1) or by generating a positive pulse on pin ASK_NFSK (0 →1 →0).

2.4 RX Supply Current Versus Temperature and Supply Voltage

Table 2-7 shows the typical supply current of the receiver in Active mode versus supply voltage and temperature with VS = VS3V_AVCC = VS5V.

Table 2-6. Measured Current in Active Mode ASK

VS = VS3V_AVCC = VS5V	3.0V
T_{amb} = 25°C	6.5 mA

Table 2-7. Measured Current in Active Mode FSK

VS = VS3V_AVCC = VS5V	3.0V
T_{amb} = 25°C	6.7 mA

2.5 Blocking, Selectivity

As can be seen in Figure 2-6 on page 12, and Figure 2-7 and Figure 2-8 on page 13, the receiver can receive signals 3 dB higher than the sensitivity level in the presence of large blockers of –34.5 dBm or –28 dBm with small frequency offsets of ±3 MHz or ±20 MHz.

Figure 2-6, and Figure 2-7 on page 12 show the narrow-band blocking, and Figure 2-8 on page 13 shows the wide-band blocking characteristic. The measurements were done with a useful signal of 315 MHz, FSK, 10 Kbits/s, ±38 kHz, Manchester, BR_Range2 with a level of –105 dBm + 3 dB = –102 dBm, which is 3 dB above the sensitivity level. The figures show how much larger than –102 dBm a continuous wave signal can be, until the BER is higher than 10^{-3}. The measurements were done at the 50Ω input shown in Figure 2-1 on page 7. At 3 MHz, for example, the blocker can be 67.5 dBC higher than –102 dBm, or –102 dBm + 67.5 dBC = –34.5 dBm.

Figure 2-6. Close-in 3-dB Blocking Characteristic and Image Response at 315 MHz

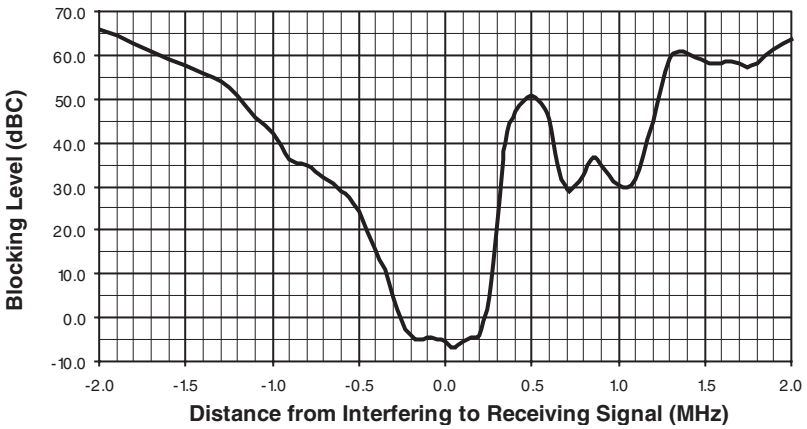


Figure 2-7. Narrow-band 3-dB Blocking Characteristic at 315 MHz

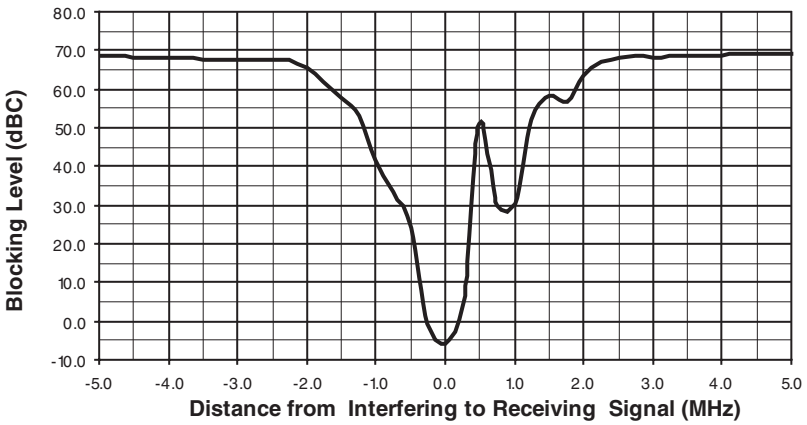


Figure 2-8. Wide-band 3-dB Blocking Characteristic at 315 MHz

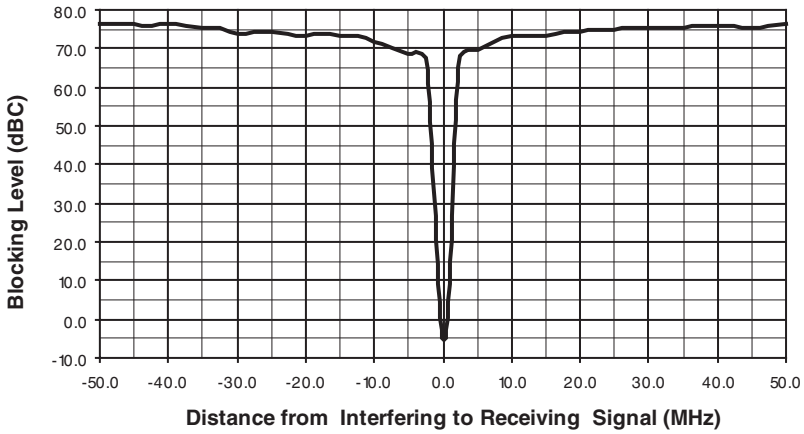


Table 2-8 shows the blocking performance measured relative to –102 dBm for some frequencies. Note that sometimes the blocking is measured relative to the sensitivity level 104 dBm (denoted dBS), instead of the carrier –102 dBm (denoted dBC)

Table 2-8. Blocking 3 dB Above Sensitivity Level With BER < 10^{-3}

Frequency Offset	Blocking Level	Blocking
+1.5 MHz	–44.5 dBm	57.5 dBC, 60.5 dBS
–1.5 MHz	–44.5 dBm	57.5 dBC, 60.5 dBS
+2 MHz	–39.0 dBm	63 dBC, 66 dBS
–2 MHz	–36.0 dBm	66 dBC, 69 dBS
+3 MHz	–34.5 dBm	67.5 dBC, 70.5 dBS
–3 MHz	–34.5 dBm	67.5 dBC, 70.5 dBS
+20 MHz	–28.0 dBm	74 dBC, 77 dBS
–20 MHz	–28.0 dBm	74 dBC, 77 dBS

The ATA8201/ATA8202 can also receive FSK and ASK modulated signals if they are much higher than the I1dBCP. It can typically receive useful signals at –10 dBm. This is often referred to as the nonlinear dynamic range (that is, the maximum to minimum receiving signal), and is 95 dB for 10 Kbits/s Manchester (FSK). This value is useful if the transmitter and receiver are very close to each other.

2.6 In-band Disturbers, Data Filter, Quasi-peak Detector, Data Slicer

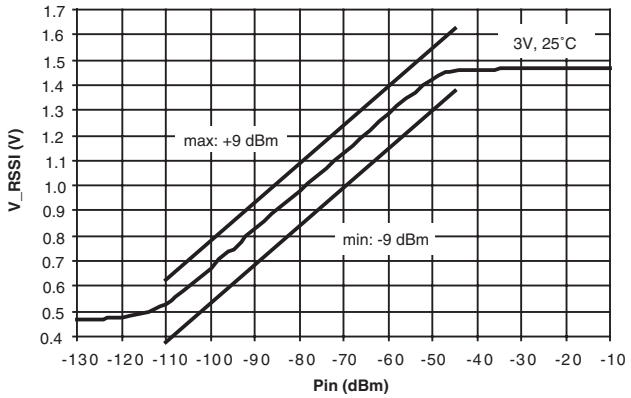
If a disturbing signal falls into the received band, or if a blocker is not a continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. Hence, the demodulator, data filter, and data slicer are important.

The data filter of the ATA8201/ATA8202 functions also as a quasi-peak detector. This results in a good suppression of above mentioned disturbers and exhibits a good carrier-to-noise performance. The required useful-signal-to-disturbing-signal ratio, at a BER of $10^{-3,}$ is less than 14 dB in ASK mode and less than 3 dB (BR_Range_0 to BR_Range_2) and 6 dB (BR_Range_3) in FSK mode. Due to the many different possible waveforms, these numbers are measured for the signal, as well as for disturbers, with peak amplitude values. Note that these values are worst-case values and are valid for any type of modulation and modulating frequency of the disturbing signal, as well as for the receiving signal. For many combinations, lower carrier-to-disturbing-signal ratios are needed.

2.7 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 65 dB, the input power range $P(RF_{IN})$ is –110 dBm to –45 dBm, and the gain is 15 mV/dB. Figure 2-9 shows the RSSI characteristic of a typical device at 315 MHz with VS3V_AVCC = VS5V = 3V and T_{amb} = 25°C with a matched input as shown in Table 2-2 and Figure 2-1 on page 7. At 433.92 MHz, 1 dB more signal level is needed for the same RSSI results.

Figure 2-9. Typical RSSI Characteristic at 315 MHz Versus Temperature and Supply Voltage



As can be seen in Figure 2-9 on page 14, for single devices there is a variance over temperature and supply voltage range of ±3 dB. The total variance over production, temperature, and supply voltage range is ±9 dB.

2.8 Frequency Synthesizer

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency f_{XTO}. The VCO (voltage-controlled oscillator) generates the drive voltage frequency f_{LO} for the mixer. f_{LO} is divided by the factor 24 (ATA8201) or 32 (ATA8202). The divided frequency is compared to f_{XTO} by the phase frequency detector. The current output of the phase frequency detector is connected to the fully integrated loop filter, and thereby generates the control voltage for the VCO. By means of that configuration, the VCO is controlled in a way, such that f_{LO} / 24 (f_{LO} / 32) is equal to f_{XTO}. If f_{LO} is determined, f_{XTO} can be calculated using the following formula: $f_{XTO} = f_{LO} / 24$ ($f_{XTO} = f_{LO} / 32$). The synthesizer has a phase noise of –130 dBC/Hz at 3 MHz and spurs of –75 dBC.

Care must be taken with the harmonics of the CLK output signal, as well as with the harmonics produced by a microprocessor clocked using the signal, as these harmonics can disturb the reception of signals.

3. XTO

The XTO is an amplitude-regulated Pierce oscillator type with external load capacitances (2×16 pF). Due to additional internal and board parasitics (C_P) of approximately 2 pF on each side, the load capacitance amounts to 2×18 pF (9 pF total).

The XTO oscillation frequency f_{XTO} is the reference frequency for the integer-N synthesizer. When designing the system in terms of receiving and transmitting frequency offset, the accuracy of the crystal and XTO have to be considered.

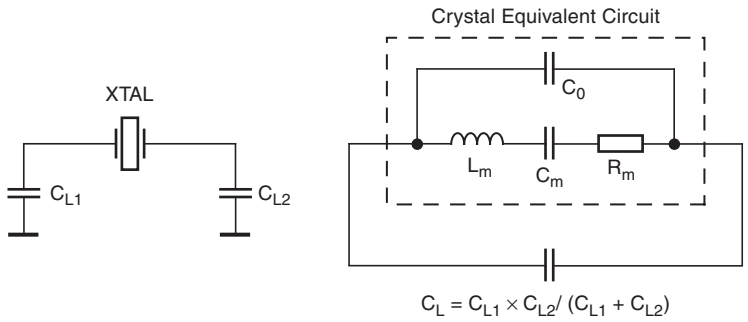
The XTO's additional pulling (including the R_M tolerance) is only ±5 ppm. The XTAL versus temperature, aging, and tolerances is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances $C_{L1,2}$ at pin XTAL1 and XTAL2. The pulling (p) of f_{XTO} from the nominal f_{XTAL} is calculated using the following formula:

$$p = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_O + C_{LN}) \times (C_O + C_L)} \times 10^{-6} \text{ppm}$$

C_m, the crystal's motional capacitance; C_0, the shunt capacitance; and C_{LN}, the nominal load capacitance of the XTAL, are found in the datasheet. C_L is the total actual load capacitance of the crystal in the circuit, and consists of C_{L1} and C_{L2} connected in series.

Figure 3-1. Crystal Equivalent Circuit



With $C_m \leq 10$ fF, $C_0 \geq 1.0$ pF, $C_{LN} = 9$ pF and $C_{L1,2} = 16$ pF ±1%, the pulling amounts to $P \leq \pm 1$ ppm.

The C_0 of the XTAL has to be lower than $C_{Lmin} / 2 = 7.9$ pF for a Pierce oscillator type in order to not enter the steep region of pulling versus load capacitance where there is risk of an unstable oscillation.

To ensure proper start-up behavior, the small signal gain and the negative resistance provided by this XTO at start is very large. For example, oscillation starts up even in the worst case with a crystal series resistance of 1.5 kΩ at $C_0 \leq 2.2$ pF with this XTO. The negative resistance is approximately given by

$$\mathrm{Re}\{Zxtocore\} = \mathrm{Re}\left\{\frac{Z_1 \times Z_3 + Z_2 \times Z_3 + Z_1 \times Z_3 \times gm}{Z_1 + Z_2 + Z_3 + Z_1 \times Z_2 \times gm}\right\}$$

with Z_1 and Z_2 as complex impedances at pins XTAL1 and XTAL2, hence
$Z_1 = -j / (2 \times p \times f_{XTO} \times C_{L1}) + 5\Omega$ and $Z_2 = -j / (2 \times p \times f_{XTO} \times C_{L2}) + 5\Omega$
Z_3 consists of crystal C_0 in parallel with an internal 110-kΩ resistor, hence
$Z_3 = -j / (2 \times p \times f_{XTO} \times C_0) / 110$ kΩ, gm is the internal transconductance between XTAL1 and XTAL2, with typically 20 mS at 25°C.

With $f_{XTO} = 13.5$ MHz, gm = 20 mS, $C_L = 9$ pF, and $C_0 = 2.2$ pF, this results in a negative resistance of about 2 kΩ. The worst case for technology, supply voltage, and temperature variations is then always higher than 1.4 kΩ for $C_0 \leq 2.2$ pF.

Due to the large gain at start, the XTO is able to meet a very low start-up time. The oscillation start-up time can be estimated with the time constant τ.

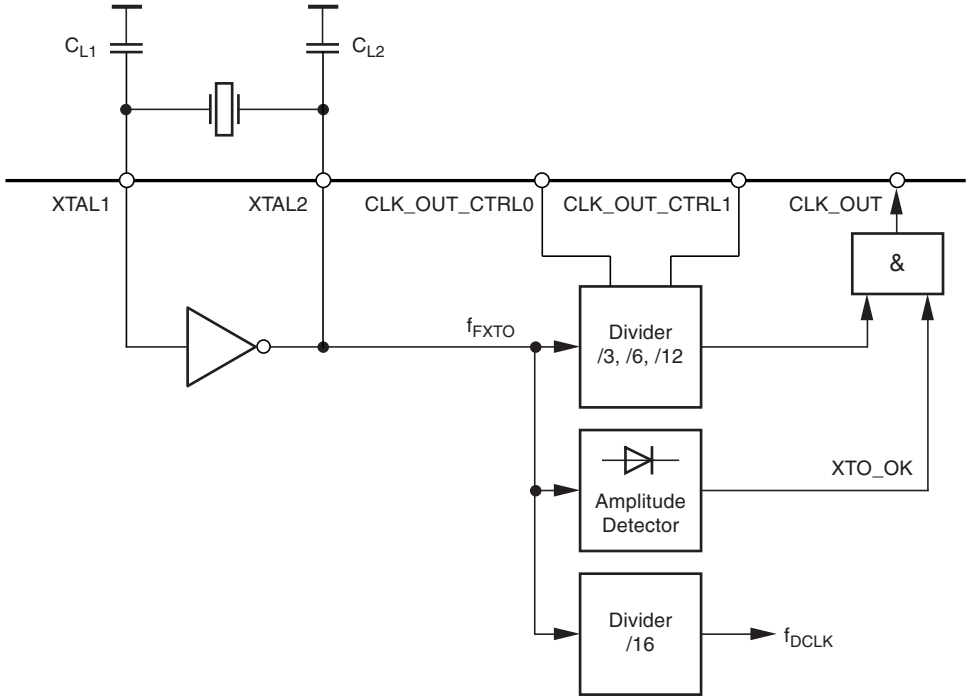
$$\tau = \frac{2}{4 \times \pi^2 \times f_{XTAL}^2 \times C_m \times (\mathrm{Re}(Z_{xtocore}) + R_m)}$$

After 10τ to 20τ, an amplitude detector detects the oscillation amplitude and sets XTO_OK to High if the amplitude is large enough; this activates the CLK_OUT output if it is enabled via the pins CLK_OUT_CTRL0 and CLK_OUT_CTRL1. Note that the necessary conditions of the DVCC voltage also have to be fulfilled.

It is recommended to use a crystal with $C_m = 3.0$ fF to 10 fF, $C_{LN} = 9$ pF, $R_m < 120\Omega$ and $C_0 = 1.0$ pF to 2.2 pF.

Lower values of C_m can be used, slightly increasing the start-up time. Lower values of C_0 or higher values of C_m (up to 15 fF) can also be used, with only little influence on pulling.

Figure 3-2. XTO Block Diagram



The relationship between f_{XTO} and the f_{RF} is shown in Table 3-1.

Table 3-1. Calculation of f_{RF}

Frequency [MHz]	f_{XTO} [MHz]	f_{RF}
433.92 (ATA8202)	13.57375	$f_{XTO} \times$ 32 – 440 kHz
315.0 (ATA8201)	13.1433	$f_{XTO} \times$ 24 – 440 kHz

Attention must be paid to the harmonics of the CLK_OUT output signal f_{CLK_OUT} as well as to the harmonics produced by an microprocessor clocked with it, since these harmonics can disturb the reception of signals if they get to the RF input. If the CLK_OUT signal is used, it must be carefully laid out on the application PCB. The supply voltage of the microcontroller must also be carefully blocked.

3.1 Pin CLK_OUT

Pin CLK_OUT is an output to clock a connected microcontroller. The clock is available in Standby and Active modes. The frequency f_{CLK_OUT} can be adjusted via the pins CLK_OUT_CTRL0 and CLK_OUT_CTRL1, and is calculated as follows:

Table 3-2. Setting of f_{CLK_OUT}

CLK_OUT_CTRL1	CLK_OUT_CTRL0	Function
0	0	Clock on pin CLK_OUT is switched off (Low level on pin CLK_OUT)
0	1	$f_{CLK\_OUT} = f_{XTO} / 3$
1	0	$f_{CLK\_OUT} = f_{XTO} / 6$
1	1	$f_{CLK\_OUT} = f_{XTO} / 12$

The signal at CLK_OUT output has a nominal 50% duty cycle. To save current, it is recommended that CLK_OUT be switched off during Standby mode.

3.2 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry is derived from one clock. As seen in Figure 3-2 on page 17, this clock cycle, T_{DCLK}, is derived from the crystal oscillator (XTO) in combination with a divider.

$$f_{DCLK} = \frac{f_{XTO}}{16}$$

T_{DCLK} controls the following application relevant parameters:

- Debouncing of the data signal stream

- Start-up time of the RX signal path

The start-up time and the debounce characteristic depend on the selected bit rate range (BR_Range) which is defined by pins BR0 and BR1. The clock cycle T_{XDCLK} is defined by the following formulas for further reference:

BR_Range ⇒

BR_Range 0: $T_{XDCLK} = 8 \times T_{DCLK}$
BR_Range 1: $T_{XDCLK} = 4 \times T_{DCLK}$
BR_Range 2: $T_{XDCLK} = 2 \times T_{DCLK}$
BR_Range 3: $T_{XDCLK} = 1 \times T_{DCLK}$

4. Sensitivity Reduction

The output voltage of the RSSI amplifier is internally compared to a threshold voltage V_{Th_red}. V_{Th_red} is determined by the value of the external resistor R_{Sense}. R_{Sense} is connected between the pins SENSE and VS3V_AVCC (see Figure 10-1 on page 29). The output of the comparator is fed into the digital control logic. By this means, it is possible to operate the receiver at a lower sensitivity.

If the level on input pin SENSE_CTRL is low, the receiver operates at full sensitivity.

If the level on input pin SENSE_CTRL is high, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sense}, the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in Figure 2-1 on page 7 and exhibits the best possible sensitivity.

If the sensitivity reduction feature is not used, pin SENSE can be left open, pin SENSE_CTRL must be set to GND.

To operate with reduced sensitivity, pin SENSE_CTRL must be set to high before the RX signal path will be enabled by setting pin RX to high (see Figure 4-1 on page 20). As long as the RSSI level is lower than V_{Th_red} (defined by the external resistor R_{Sense}) no data stream is available on pin DATA_OUT (low level on pin DATA_OUT). An internal RS flip-flop will be set to high the first time the RSSI voltage crosses V_{Th_red}, and from then on the data stream will be available on pin DATA_OUT. From then on the receiver also works with full sensitivity. This makes sure that a telegram will not be interrupted if the RSSI level varies during the transmission. The RS flip-flop can be set back, and thus the receiver switched back to reduced sensitivity, by generating a positive pulse on pin ASK_NFSK (see Figure 4-2 on page 20). In FSK mode, operating with reduced sensitivity follows the same way.

Figure 4-1. Reduced Sensitivity Active

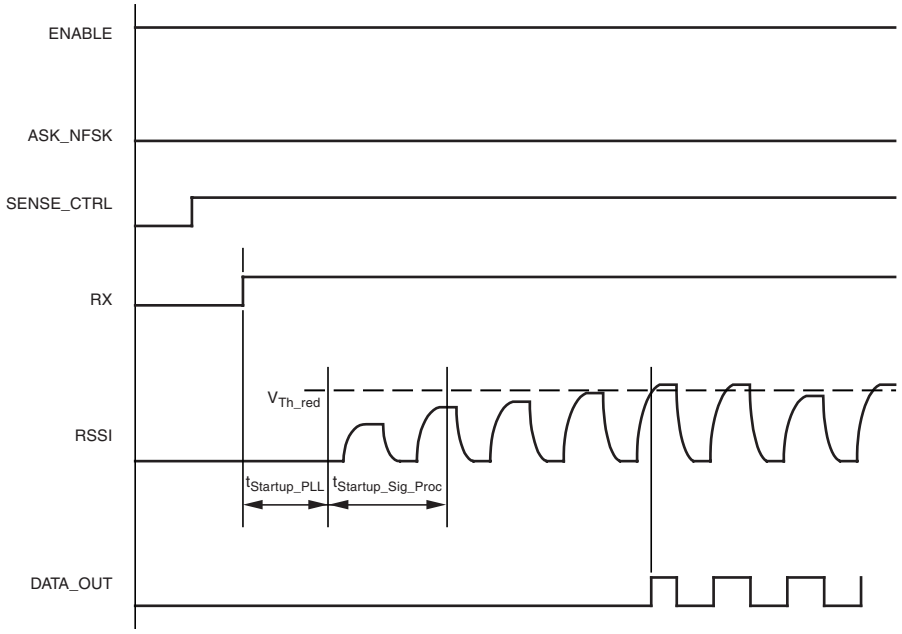
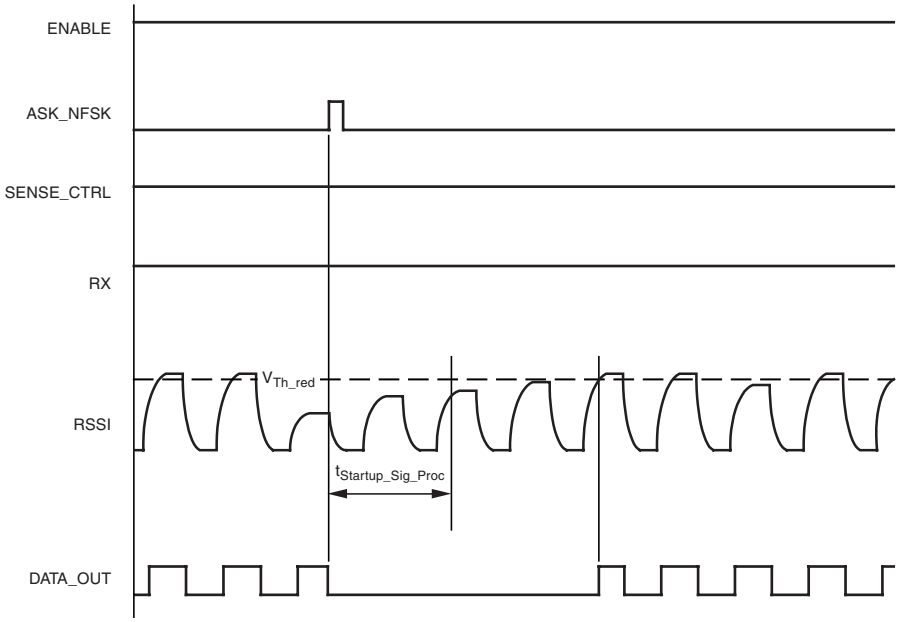
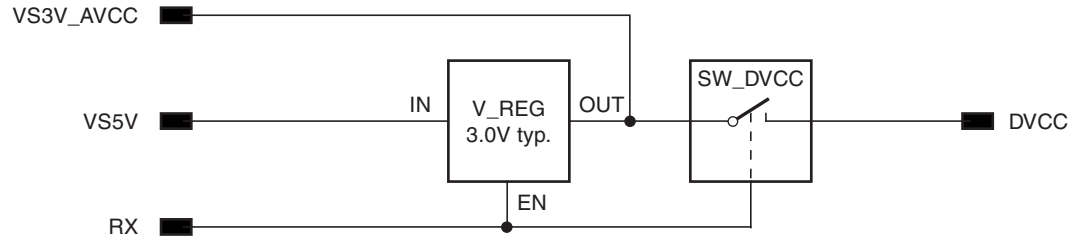


Figure 4-2. Restart Reduced Sensitivity



5. Power Supply

Figure 5-1. Power Supply



The supply voltage range of the ATA8201/ATA8202 is 2.7V to 3.3V or 4.5V to 5.5V.

Pin VS3V_AVCC is the supply voltage input for the range 2.7V to 3.3V, and is used in battery applications using a single lithium 3V cell. Pin VS5V is the voltage input for the range 4.5V to 5.5V (car applications) in this case the voltage regulator V_REG regulates VS3V_AVCC to typically 3.0V. If the voltage regulator is active, a blocking capacitor of 2.2 µF has to be connected to VS3V_AVCC (see Figure 10-1 on page 29).

DVCC is the internal operating voltage of the digital control logic and is fed via the switch SW_DVCC by VS3V_AVCC. DVCC must be blocked on pin DVCC with 68 nF (see Figure 9-1 on page 28 and Figure 10-1 on page 29).

Pin RX is the input to activate the RX signal processing and set the receiver to Active mode.

5.1 OFF Mode

A low level on pin RX and ENABLE will set the receiver to OFF mode (low power mode). In this mode, the crystal oscillator is shut down and no clock is available on pin CLK_OUT. The receiver is not sensitive to a transmitter signal in this mode.

Table 5-1. Standby Mode

RX	ENABLE	Function
0	0	OFF mode

5.2 Standby Mode

The receiver activates the Standby mode if pin ENABLE is set to “1”.

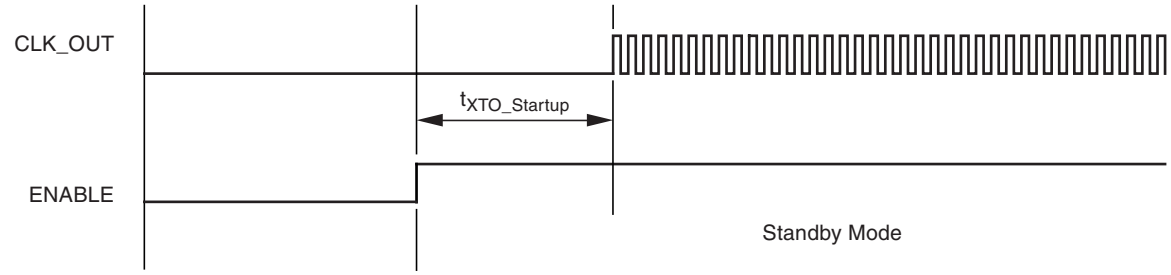
In Standby mode, the XTO is running and the clock on pin CLK_OUT is available after the start-up time of the XTO has elapsed (dependent on pin CLK_OUT_CTRL0 and CLK_OUT_CTRL1). During Standby mode, the receiver is not sensitive to a transmitter signal.

In Standby mode, the RX signal path is disabled and the power consumption $I_{Standby}$ is typically 50 µA (CLK_OUT output off, VS3V_AVCC = VS5V = 3V). The exact value of this current is strongly dependent on the application and the exact operation mode, therefore check the section “Electrical Characteristics: General” on page 30 for the appropriate application case.

Table 5-2. Standby Mode

RX	ENABLE	Function
0	1	Standby mode

Figure 5-2. Standby Mode (CLK_OUT_CTRL0 or CLK_OUT_CTRL1 = 1)



5.3 Active Mode

The Active mode is enabled by setting the level on pin RX to high. In Active mode, the RX signal path is enabled and if a valid signal is present it will be transferred to the connected microcontroller.

Table 5-3. Active Mode

RX	ENABLE	Function
1	1	Active mode

During $T_{Startup\_PLL}$ the PLL is enabled and starts up. If the PLL is locked, the signal processing circuit starts up ($T_{Startup\_Sig\_Proc}$). After the start-up time, all circuits are in stable condition and ready to receive. The duration of the start-up sequence depends on the selected bit rate range.

Figure 5-3. Active Mode

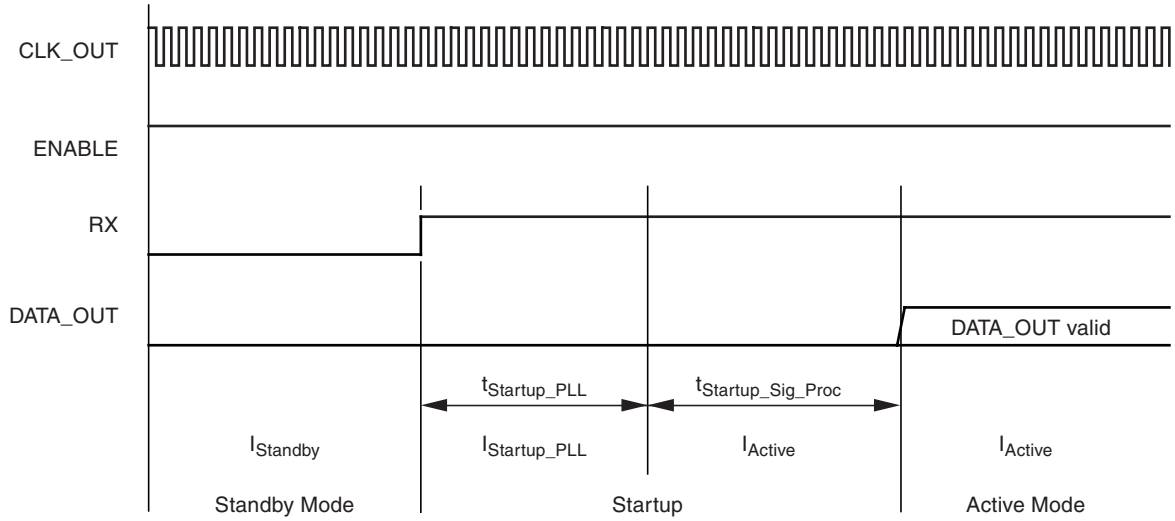


Table 5-4. Start-up Time

BR1	BR0	ATA8202 (433.92 MHz)		ATA8201 (315 MHz)	
		$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$	$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$
0	0	261 µs	1096 µs	269 µs	1132 µs
0	1		644 µs		665 µs
1	0		417 µs		431 µs
1	1		304 µs		324 µs

Table 5-5. Modulation Scheme

ASK_NFSK	RF_{IN} at Pin LNA_IN	Level at Pin DATA_OUT
0	f_{FSK_H}	1
	f_{FSK_L}	0
1	f_{ASK} on	1
	f_{ASK} off	0

6. Bit Rate Ranges

Configuration of the bit rate ranges is carried out via the two pins BR0 and BR1. The microcontroller uses these two interface lines to set the corner frequencies of the band-pass data filter. Switching the bit rate ranges while the RF front end is in Active mode can be done on the fly and will not take longer than 100 µs if done while remaining in either ASK or FSK mode. If the modulation scheme is changed at the same time, the switching time is ($T_{Startup\_Sig\_Proc}$, see Figure 7-1 on page 26). Each BR_Range is defined by a minimum edge-to-edge time. To maintain full sensitivity of the receiver, edge-to-edge transition times of incoming data should not be less than the minimum for the selected BR_Range.

Table 6-1. BR Ranges ASK

BR1	BR0	BR_Range	Recommended Bit Rate (Manchester)(1)	Minimum Edge-to-edge Time Period T_{EE} of the Data Signal(2)	Edge-to-edge Time Period T_{EE} of the Data Signal During the Start-up Period(3)
0	0	BR_Range0	1.0 Kbit/s to 2.5 Kbits/s	200 µs	200 µs to 500 µs
0	1	BR_Range1	2.0 Kbits/s to 5.0 Kbits/s	100 µs	100 µs to 250 µs
1	0	BR_Range2	4.0 Kbits/s to 10.0 Kbits/s	50 µs	50 µs to 125 µs
1	1	BR_Range3	8.0 Kbits/s to 10.0 Kbits/s	50 µs	50 µs to 62.5 µs

Table 6-2. BR Ranges FSK

BR1	BR0	BR_Range	Recommended Bit Rate (Manchester)(1)	Minimum Edge-to-edge Time Period T_{EE} of the Data Signal(2)	Edge-to-edge Time Period T_{EE} of the Data Signal During the Start-up Period(3)
0	0	BR_Range0	1.0 Kbit/s to 2.5 Kbits/s	200 µs	200 µs to 500 µs
0	1	BR_Range1	2.0 Kbits/s to 5.0 Kbits/s	100 µs	100 µs to 250 µs
1	0	BR_Range2	4.0 Kbits/s to 10.0 Kbits/s	50 µs	50 µs to 125 µs
1	1	BR_Range3	8.0 Kbits/s to 20.0 Kbits/s	25 µs	25 µs to 62.5 µs

Note: If during the start-up period ($T_{Startup\_PLL}$ + $T_{Startup\_Sig\_Proc}$) there is no RF signal, the data filter settles to the noise floor, leading to noise on pin DATA_OUT.

Notes:
1. As can be seen, a bit stream of, for example, 2.5 Kbits/s can be received in BR_Range0 and BR_Range1 (overlapping BR_Ranges). To get the full sensitivity, always use the lowest possible BR_Range (here, BR_Range0). The advantage in the next higher BR_Range (BR_Range1) is the shorter start-up period, meaning lower current consumption during Polling mode. Thus, it is a decision between sensitivity and current consumption.
2. The receiver is also capable of receiving non-Manchester-modulated signals, such as PWM, PPM, VPWM, NRZ. In ASK mode, the header and blanking periods occurring in Keeloq-like protocols (up to 52 ms) are supported.
3. To ensure an accurate settling of the data filter during the start-up period ($T_{Startup\_PLL}$ + $T_{Startup\_Sig\_Proc}$), the edge-to-edge time T_{EE} of the data signal (preamble) must be inside the given limits during this period.

Figure 6-1. Examples of Supported Modulation Formats

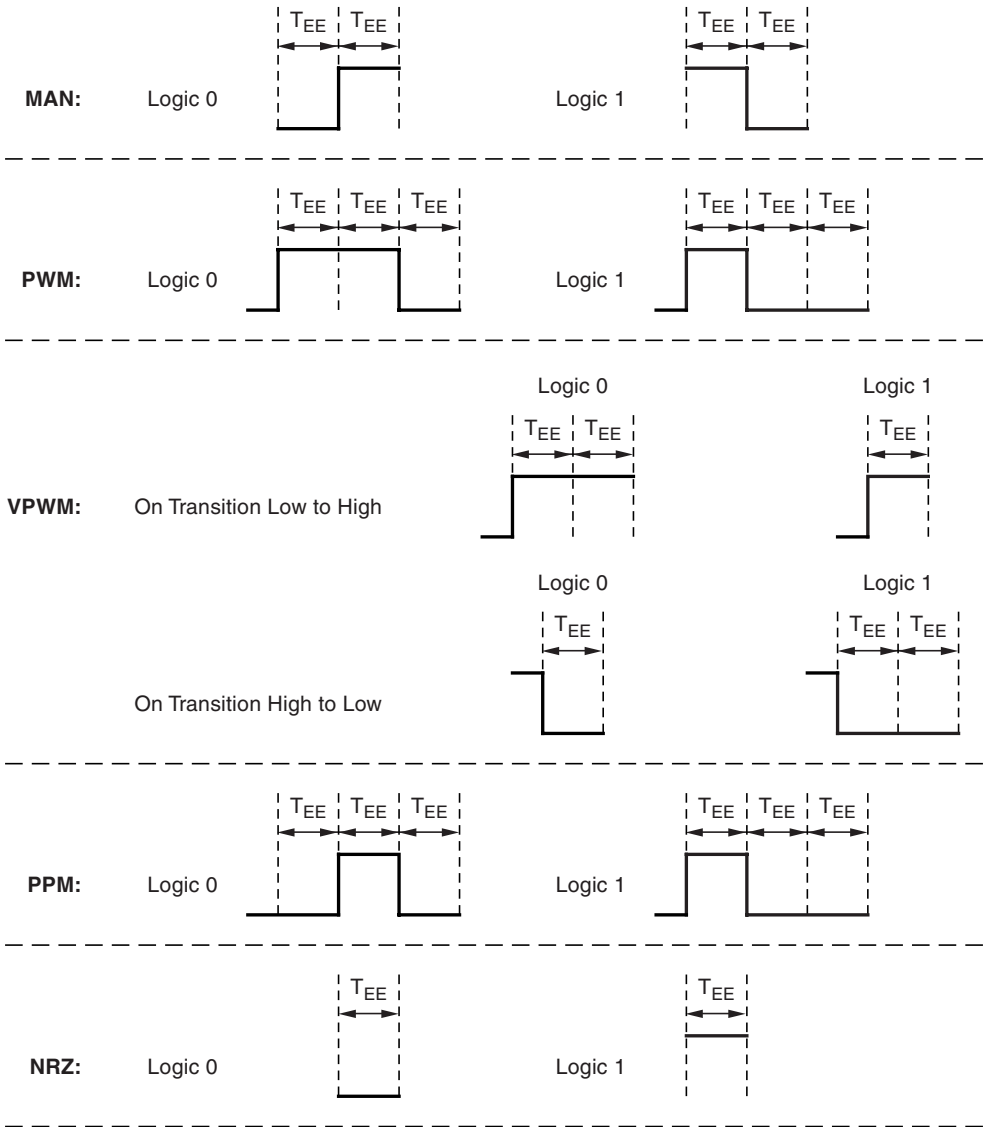
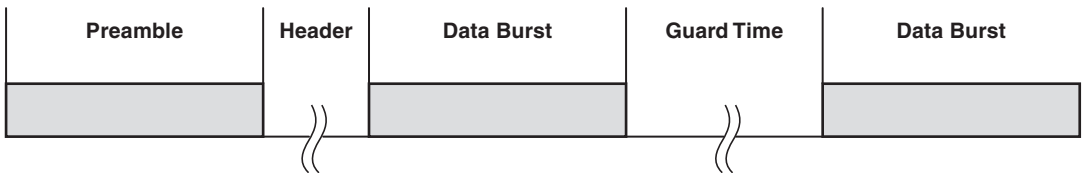


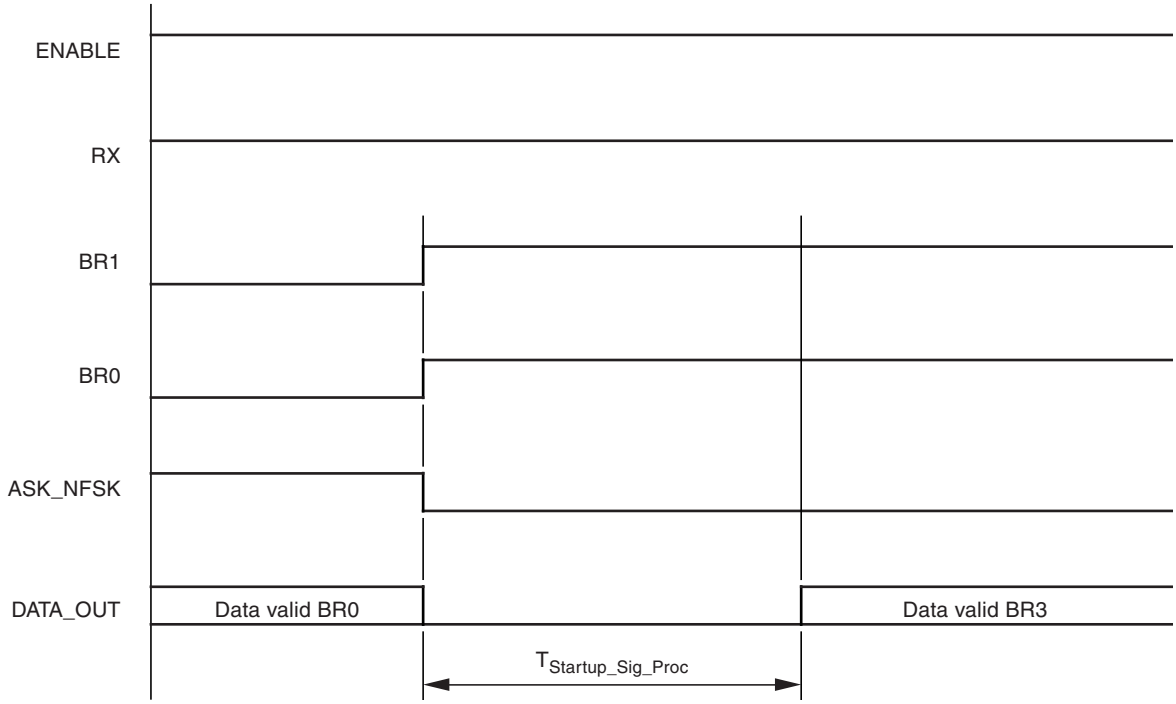
Figure 6-2. Supported Header and Blanking Periods



7. ASK_NFSK

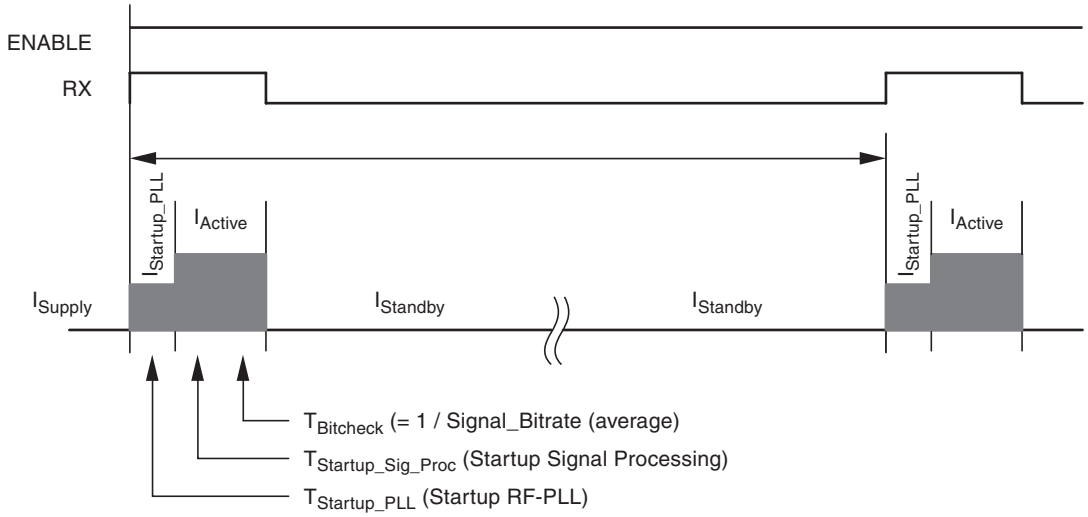
The ASK_NFSK pin allows the microcontroller to rapidly switch the RF front end between demodulation modes. A logic 1 on this pin selects ASK mode, and a logic 0 FSK mode. The time to change modes ($T_{Startup\_Sig\_Proc}$) depends on the bit rate range being selected (not current bit rate range) and is given in Table 5-4 on page 23. This response time is specified for applications that require an ASK preamble followed by FSK data (for typical TPM applications). During $T_{Startup\_Sig\_Proc}$, the level on pin DATA_OUT is low.

Figure 7-1. ASK Preamble 2.4 Kbits/s followed by FSK Data 9.6 Kbits/s



8. Polling Current Calculation

Figure 8-1. Polling Cycle



In an industrial or aftermarket RKE and TPM system, the average chip current in Polling mode, $I_{Polling}$, is an important parameter. The polling period must be controlled by the connected microcontroller via the pins ENABLE and RX. The polling current can be calculated as follows:

$$I_{Polling} = (T_{Startup\_PLL} / T_{Polling\_Period}) \times I_{Startup\_PLL} + (T_{Startup\_Sig\_Proc} / T_{Polling\_Period}) \times I_{Active} + (T_{Bitcheck} / T_{Polling\_Period}) \times I_{Active} + (T_{Polling\_Period} - T_{Startup\_PLL} - T_{Startup\_Sig\_Proc} - T_{Bitcheck}) / T_{Polling\_Period} \times I_{Standby}$$

$T_{Startup\_PLL}$:	depends on 315 MHz/433.92 MHz application.
$T_{Startup\_Sig\_Proc}$:	depends on 315 MHz/433.92 MHz application and the selected bit rate range.
$T_{Bitcheck}$:	depends on the signal bit rate (1 / Signal_Bit_Rate).
$T_{Polling\_Period}$:	depends on the transmitter telegram (preburst).
$I_{Startup\_PLL}$:	depends on 3V or 5V application and the setting of pin CLK_OUT.
I_{Active}:	depends on 3V or 5V application, ASK or FSK mode and the setting of pin CLK_OUT.
$I_{Standby}$:	depends on 3V or 5V application and the setting of pin CLK_OUT.

Example:- 315-MHz application (ATA8201), bit rate: 9.6 Kbits/s, $T_{Polling\_Period}$ = 8 ms

--> $T_{Startup\_PLL}$ = 269 µs

--> $T_{Startup\_Sig\_Proc}$ = 324 µs (Bit Rate Range 3)

--> $T_{Bitcheck}$ = 104 µs

3V application; ASK mode, CLK_OUT disabled

--> $I_{Startup\_PLL}$ = 4.5 mA

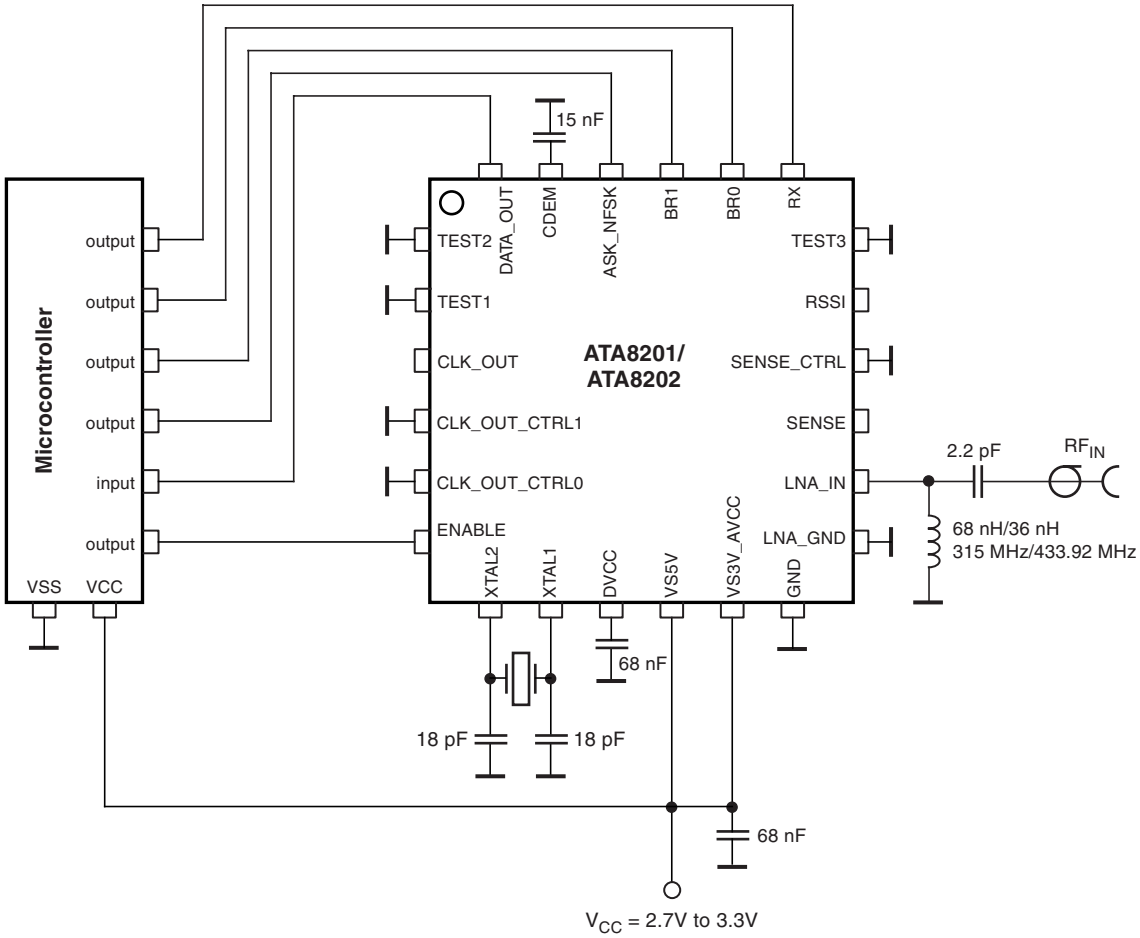
--> I_{Active} = 6.5 mA

--> $I_{Standby}$ = 0.05 mA

--> $I_{Polling}$ = 0.545 mA

9. 3V Application

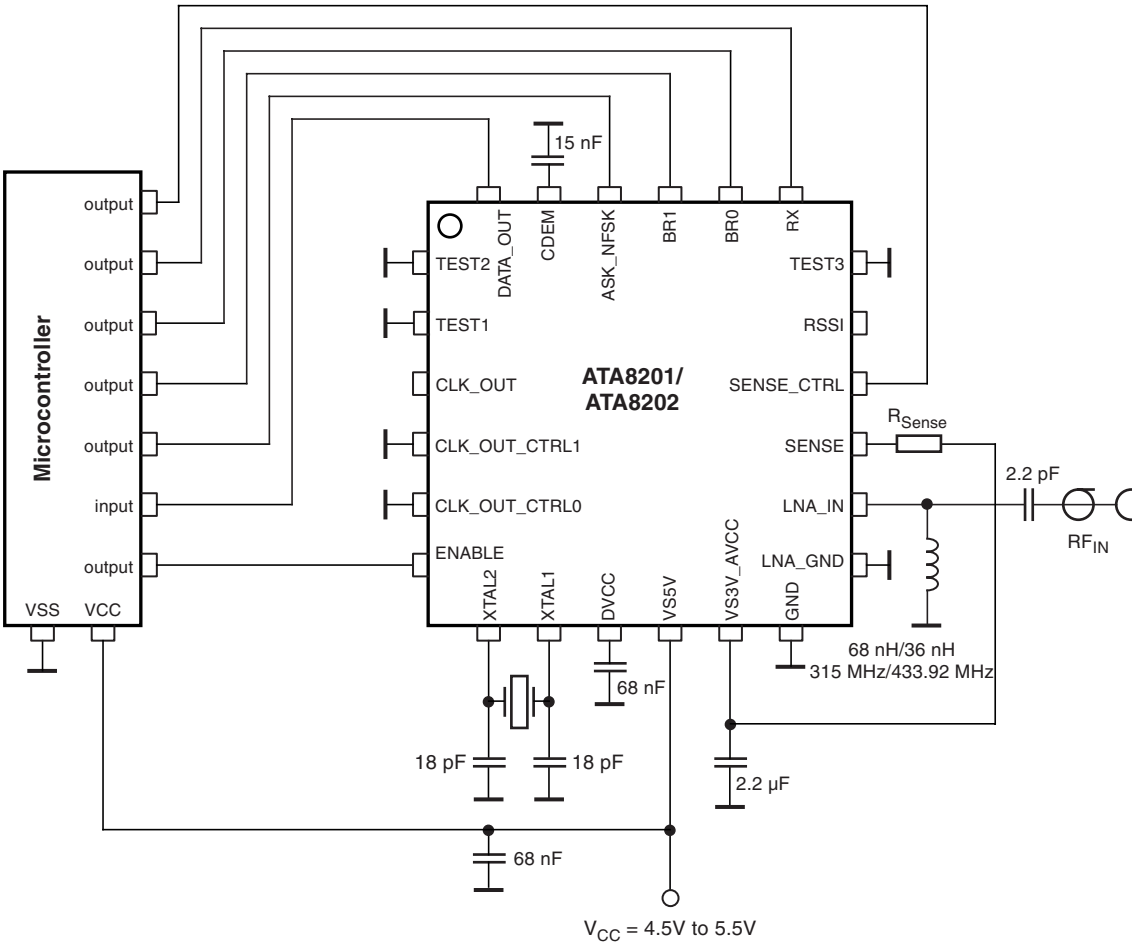
Figure 9-1. 3V Application



Note: Paddle (backplane) must be connected to GND

10. 5V Application

Figure 10-1. 5V Application With Reduced/Full Sensitivity



Note: Paddle (backplane) must be connected to GND

11. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	T_j		+150	°C
Storage temperature	T_{stg}	–55	+125	°C
Ambient temperature	T_{amb}	–40	+85	°C
Supply voltage VS5V	V_S		+6	V
ESD (Human Body Model ESD S 5.1) every pin	HBM	–4	+4	kV
ESD (Machine Model JEDEC A115A) every pin	MM	–200	+200	V
ESD (Field Induced Charge Device Model ESD STM 5.3.1-1999) every pin	FCDM	–500	+500	V
Maximum input level, input matched to 50Ω	P_{in_max}		0	dBm

12. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	25	K/W

13. Electrical Characteristics: General

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 315 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**OFF Mode**								
1.1	Supply current in OFF mode	V_{VS3V_AVCC} = V_{VS5V} ≤ 3V V_{VS5V} = 5V CLK_OUT disabled	10, 11 10	I_{SOFF}			4 4	µA µA	A A
2	**Standby Mode**								
2.1	RF operating frequency range	ATA8201	14	f_{RF}	313		317	MHz	A
		ATA8202	14	f_{RF}	433		435	MHz	A
2.2	Supply current Standby mode	XTO running V_{VS3V_AVCC} = V_{VS5V} ≤ 3V CLK_OUT disabled	10,11	$I_{Standby}$		50	100	µA	A
		XTO running V_{VS5V} = 5V CLK_OUT disabled	10,11	$I_{Standby}$		50	100	µA	A
2.3	System start-up time	XTO startup XTAL: C_m = 5 fF, C_0 = 1.8 pF, R_m = 15Ω		$T_{XTO\_Startup}$		0.3		ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF_IN matched to 50Ω according to Figure 2-1 on page 7 with component values as in Table 2-2 on page 7 (RF_{IN}).

13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 315 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin[1]	Symbol	Min.	Typ.	Max.	Unit	Type*
2.4	Active mode start-up time	From Standby mode to Active mode BR_Range_3 ATA5745 ATA5746		$T_{Startup\_PLL}$ + $T_{Startup\_Sig\_Proc}$			 565 593	 µs µs	A
3	**Active Mode**								
3.1	Supply current Active mode	V_{VS3V_AVCC} = V_{VS5V} = 3V ASK mode CLK_OUT disabled SENSE_CTRL = 0	10,11	I_{Active}		6.5		mA	A
		V_{VS3V_AVCC} = V_{VS5V} = 3V FSK mode CLK_OUT disabled SENSE_CTRL = 0	10,11	I_{Active}		6.7		mA	A
		V_{VS5V} = 5V ASK mode CLK_OUT disabled SENSE_CTRL = 0	10	I_{Active}		6.7		mA	A
		V_{VS5V} = 5V FSK mode CLK_OUT disabled SENSE_CTRL = 0	10	I_{Active}		6.9		mA	A
3.2	Supply current Polling mode	V_{VS3V_AVCC} = V_{VS5V} = 3V $T_{Polling\_Period}$ = 8 ms BR_Range_3, ASK mode, CLK_OUT disabled Data rate = 9.6 Kbits/s	10,11	$I_{Polling}$		545		µA	C
3.3	Input sensitivity FSK f_{RF} = 315 MHz	FSK deviation f_{DEV} = ±38 kHz BER = 10^{-3} T_{amb} = 25°C							
		Bit rate 9.6 Kbits/s BR2	(14)	P_{REF_FSK}	–103	–105	–106.5	dBm	B
		Bit rate 2.4 Kbits/s BR0	(14)	P_{REF_FSK}	–106	–108	–109.5	dBm	B
		FSK deviation ±18 kHz to ±50 kHz							
		Bit rate 9.6 Kbits/s BR2	(14)	P_{REF_FSK}	–101			dBm	B
		Bit rate 2.4 Kbits/s BR0	(14)	P_{REF_FSK}	–104			dBm	B
3.4	Input sensitivity ASK f_{RF} = 315 MHz	ASK 100% level of carrier, BER = 10^{-3} T_{amb} = 25°C							
		Bit rate 9.6 Kbits/s BR2	(14)	P_{REF_ASK}	–109	–111	–112.5	dBm	B
		Bit rate 2.4 Kbits/s BR0	(14)	P_{REF_ASK}	–112	–114	–115.5	dBm	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF_IN matched to 50Ω according to Figure 2-1 on page 7 with component values as in Table 2-2 on page 7 (RF_{IN}).

13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 315 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
3.5	Sensitivity change at f_{RF} = 433.92 MHz compared to f_{RF} = 315 MHz	f_{RF} = 315 MHz to f_{RF} = 433.92 MHz $P = P_{REF\_ASK} + \Delta P_{REF1}$ $P = P_{REF\_FSK} + \Delta P_{REF1}$	(14)	ΔP_{REF1}		+1		dB	B
3.6	Sensitivity change versus temperature, supply voltage and frequency offset	FSK f_{DEV} = ±38 kHz $\Delta f_{OFFSET} \leq \pm 160$ kHz ASK 100% $\Delta f_{OFFSET} \leq \pm 160$ kHz $P = P_{REF\_ASK} + \Delta P_{REF1} + \Delta P_{REF2}$ $P = P_{REF\_FSK} + \Delta P_{REF1} + \Delta P_{REF2}$	(14)	ΔP_{REF2}	+4.5		–1.5		B
3.7	Reduced sensitivity	R_{Sense} connected from pin SENSE to pin VS3V_AVCC		P_{Ref_Red}				dBm (peak level)	
		R_{Sense} = 62 kΩ f_{in} = 433.92 MHz				–76		dBm	C
		R_{Sense} = 82 kΩ f_{in} = 433.92 MHz				–88		dBm	C
		R_{Sense} = 62 kΩ f_{in} = 315 MHz				–76		dBm	C
		R_{Sense} = 82 kΩ f_{in} = 315 MHz				–88		dBm	C
	Reduced sensitivity variation over full operating range	R_{Sense} = 62 kΩ R_{Sense} = 82 kΩ $P_{Red} = P_{Ref\_Red} + P_{\Delta Red}$		ΔP_{Red}	–10		+10	dB	
3.8	Maximum frequency offset in FSK mode	Maximum frequency difference of f_{RF} between receiver and transmitter in FSK mode (f_{RF} is the center frequency of the FSK signal with f_{BIT} = 10 Kbits/s f_{DEV} = ±38 kHz	(14)	Δf_{OFFSET}	–160		+160	kHz	B
3.9	Supported FSK frequency deviation	With up to 2 dB loss of sensitivity. Note that the tolerable frequency offset is 12 kHz lower for f_{DEV} = ±50 kHz than for f_{DEV} = ±38 kHz, hence, $\Delta f_{OFFSET} \leq \pm 148$ kHz	(14)	f_{DEV}	±18	±38	±50	kHz	B
3.10	System noise figure	f_{RF} = 315 MHz	(14)	NF		6.0	9	dB	B
		f_{RF} = 433.92 MHz	(14)	NF		7.0	10	dB	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF_IN matched to 50Ω according to Figure 2-1 on page 7 with component values as in Table 2-2 on page 7 (RF_{IN}).

13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 315 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
3.11	Intermediate frequency	f_{RF} = 433.92 MHz		f_{IF}		440		kHz	A
		f_{RF} = 315 MHz		f_{IF}		440		kHz	A
3.12	System bandwidth	3 dB bandwidth **This value is for information only!** Note that for crystal and system frequency offset calculations, Δf_{OFFSET} must be used.	(14)	SBW		435		kHz	A
3.13	System out-band 3rd-order input intercept point	Δf_{meas1} = 1.8 MHz Δf_{meas2} = 3.6 MHz f_{RF} = 315 MHz	(14)	IIP3		–24		dBm	C
		f_{RF} = 433.92 MHz	(14)	IIP3		–23		dBm	C
3.14	System outband input 1-dB compression point	Δf_{meas1} = 1 MHz f_{RF} = 315 MHz	(14)	I1dBCP		–31	–36	dBm	C
		f_{RF} = 433.92 MHz	(14)	I1dBCP		–30	–35	dBm	C
3.15	LNA input impedance	f_{RF} = 315 MHz	14	Z_{in_LNA}		(72.4 – j298)		Ω	C
		f_{RF} = 433.92 MHz	14	Z_{in_LNA}		(55 – j216)		Ω	C
3.16	Maximum peak RF input level, ASK and FSK	BER < 10^{-3}, ASK: 100%	(14)	P_{IN_max}		+5	–10	dBm	C
		FSK: f_{DEV} = ±38 kHz	(14)	P_{IN_max}		+5	–10	dBm	C
3.17	LO spurs at LNA_IN	f < 1 GHz	(14)				–57	dBm	C
		f >1 GHz	(14)				–47	dBm	C
		f_{LO} = 315.44 MHz 2 × f_{LO} 4 × f_{LO}	(14)			–90 –94 –68		dBm	C
		f_{LO} = 434.36 MHz 2 × f_{LO} 4 × f_{LO}	(14)			–92 –88 –58		dBm	C
3.18	Image rejection	With the complete image band f_{RF} = 315 MHz	(14)		24	30		dB	A
		f_{RF} = 433.92 MHz	(14)		24	30		dB	A
3.19	Useful signal to interferer ratio	Peak level of useful signal to peak level of interferer for BER < 10^{-3} with any modulation scheme of interferer							
		FSK BR_Ranges 0, 1, 2	(14)	SNR_{FSK0-2}		2	3	dB	B
		FSK BR_Range_3	(14)	SNR_{FSK3}		4	6	dB	B
		ASK (P_{RF} < P_{RFIN_High})	(14)	SNR_{ASK}		10	14	dB	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF_IN matched to 50Ω according to Figure 2-1 on page 7 with component values as in Table 2-2 on page 7 (RF_{IN}).

13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 315 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
3.20	RSSI output	Dynamic range	(14),17	D_{RSSI}		65		dB	A
		Lower level of range f_{RF} = 315 MHz f_{RF} = 433.92 MHz	(14),17	P_{RFIN_Low}		–110		dBm	A
		Upper level of range f_{RF} = 315 MHz f_{RF} = 433.92 MHz	(14),17	P_{RFIN_High}		–45		dBm	A
		Gain	(14),17			15		mV/dB	A
		Output voltage range	(14),17	V_{RSSI}	350		1600	mV	A
3.21	Output resistance RSSI pin		17	R_{RSSI}	8	10	12.5	kΩ	C
3.22	Blocking	Sensitivity (BER = 10^{-3}) is reduced by 3 dB if a continuous wave blocking signal at ±Δf is ΔP_{Block} higher than the useful signal level (Bit rate = 10 Kbits/s, FSK, f_{DEV} ± 38 kHz, Manchester code, BR_Range2)							
		f_{RF} = 315 MHz Δf ± 1.5 MHz Δf ± 2 MHz Δf ± 3 MHz Δf ± 10 MHz Δf ± 20 MHz	(14)	ΔP_{Block}		57.5 63.0 67.5 72.0 74.0		dBC	C
		f_{RF} = 433.92 MHz Δf ± 1.5 MHz Δf ± 2 MHz Δf ± 3 MHz Δf ± 10 MHz Δf ± 20 MHz	(14)	ΔP_{Block}		56.5 62.0 66.5 71.0 73.0		dBC	C
3.23	CDEM	Capacitor connected to pin 23 (CDEM)	23		–5%	15	+5%	nF	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF_IN matched to 50Ω according to Figure 2-1 on page 7 with component values as in Table 2-2 on page 7 (RF_{IN}).

13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 315 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
4	**XTO**								
4.1	Transconductance XTO at start	At startup; after startup the amplitude is regulated to V_{PPXTAL}	7,8	$g_{m, XTO}$		20		mS	B
4.2	XTO start-up time	$C_0 \leq 2.2$ pF $C_m < 14$ fF $R_m \leq 120\Omega$	7,8	$T_{XTO\_Startup}$		300		µs	A
4.3	Maximum C_0 of XTAL		7,8	C_{0max}			3.8	pF	D
4.4	Pulling of LO frequency f_{LO} due to XTO, C_{L1} and C_{L2} versus temperature and supply changes	1.0 pF ≤ C_0 ≤ 2.2 pF C_m = 4.0 fF to 7.0 fF $R_m \leq 120\Omega$	3	Δf_{XTO}	–5		+5	ppm	C
4.5	Amplitude XTAL after startup	C_m = 5 fF, C_0 = 1.8 pF $R_m = 15\Omega$							
		V(XTAL1, XTAL2) peak-to-peak value	7,8	V_{PPXTAL}		700		mVpp	C
		V(XTAL1) peak-to-peak value	7,8	V_{PPXTAL}		350		mVpp	C
4.6	Maximum series resistance R_m of XTAL at startup	$C_0 \leq 2.2$ pF, small signal start impedance, this value is important for crystal oscillator startup	7,8	Z_{XTAL12_START}	–1400	–2000		Ω	B
4.7	Maximum series resistance R_m of XTAL after startup	$C_0 \leq 2.2$ pF $C_m < 14$ fF	7,8	R_{m_max}		15	120	Ω	B
4.8	Nominal XTAL load resonant frequency	f_{RF} = 433.92 MHz f_{RF} = 315 MHz	7,8	f_{XTAL}		13.57375 13.1433		MHz	D
4.9	External CLK_OUT frequency	CLK_OUT_CRTL1 = 0 CLK_OUT_CTRL0 = 0 --> CLK_OUT disabled	3	f_{CLK_OUT}	f_{CLK} disabled (low level on pin CLK_OUT)			MHz	A
		CLK_OUT_CRTL1 = 0 CLK_OUT_CTRL0 = 1 --> division ratio = 3			$f_{CLK} = \frac{f_{XTO}}{3}$				
		CLK_OUT_CRTL1 = 1 CLK_OUT_CTRL0 = 0 --> division ratio = 6			$f_{CLK} = \frac{f_{XTO}}{6}$				
		CLK_OUT_CRTL1 = 1 CLK_OUT_CTRL0 = 1 --> division ratio = 12			$f_{CLK} = \frac{f_{XTO}}{12}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF_IN matched to 50Ω according to Figure 2-1 on page 7 with component values as in Table 2-2 on page 7 (RF_{IN}).

13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 315 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
		f_{RF} = 433.92 MHz CLK_OUT division ratio = 3 = 6 = 12 CLK_OUT has nominal 50% duty cycle	3	f_{CLK_OUT}		4.52458 2.26229 1.13114		MHz	D
		f_{RF} = 315 MHz CLK_OUT division ratio = 3 = 6 = 12 CLK_OUT has nominal 50% duty cycle	3	f_{CLK_OUT}		4.3811 2.190 1.0952		MHz	D
4.10	DC voltage after startup	V_{DC} (XTAL1, XTAL2) XTO running (Standby mode, Active mode)	7,8	V_{DCXTO}	–250	–45		mV	C
5	**Synthesizer**								
5.1	Spurs in Active mode	At $\pm f_{CLK\_OUT}$, CLK_OUT enabled (division ratio = 3) f_{RF} = 315 MHz f_{RF} = 433.92 MHz		SP_{RX}		–75	–70	dBC	C
		at $\pm f_{XTO}$ f_{RF} = 315 MHz f_{RF} = 433.92 MHz		SP_{RX}		–75	–70	dBC	A
5.2	Phase noise at 3 MHz Active mode	f_{RF} = 315 MHz f_{RF} = 433.92 MHz		L_{RX3M}		–130	–127	dBC/Hz	A
5.3	Phase noise at 20 MHz Active mode	Noise floor		L_{RX20M}		–135	–132	dBC/Hz	B
6	**Microcontroller Interface**								
6.1	CLK_OUT output rise and fall time	f_{CLK_OUT} < 4.5 MHz C_L = 10 pF C_L = Load capacitance on pin CLK_OUT 2.7V ≤ V_{VS5V} ≤ 3.3V or 4.5V ≤ V_{VS5V} ≤ 5.5V 20% to 80% V_{VS5V}	3	t_{rise} t_{fall}		20 20	30 30	ns ns	B
6.2	Internal equivalent capacitance	Used for current calculation	3	C_{CLK_OUT}		8		pF	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF_IN matched to 50Ω according to Figure 2-1 on page 7 with component values as in Table 2-2 on page 7 (RF_{IN}).

14. Electrical Characteristic: 3V Application

All parameters refer to GND and are valid for T_{amb} = 25°C, $V_{VS3V\_AVCC} = V_{VS5V}$ = 3V and V_{VS5V} = 5V. Typical values are given at f_{RF} = 433.92 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	**3V Application**								
7.1	Supply current in OFF mode	$V_{VS3V\_AVCC} = V_{VS5V} \le 3V$ CLK_OUT disabled	10, 11	I_{SOFF}			2	µA	A
7.2	Supported voltage range	3V application	10, 11	V_{VS3V_AVCC}, V_{VS5V}	2.7		3.3	V	A
7.3	Current in Standby mode (XTO is running)	$V_{VS3V\_AVCC} = V_{VS5V} \le 3V$ external load C on pin CLK_OUT = 12 pF CLK enabled (division ratio 3) CLK enabled (division ratio 6) CLK enabled (division ratio 12) CLK disabled	10, 11	$I_{Standby}$		420 290 220 50		µA	C C C A
7.4	Current during $T_{Startup\_PLL}$	$V_{VS3V\_AVCC} = V_{VS5V} \le 3V$ CLK disabled	10, 11	$I_{Startup\_PLL}$		4.5		mA	C
7.5	Current in Active mode ASK	$V_{VS3V\_AVCC} = V_{VS5V} \le 3V$ CLK disabled SENSE_CTRL = 0	10, 11	I_{Active}		6.5		mA	A
7.6	Current in Active mode FSK	$V_{VS3V\_AVCC} = V_{VS5V} \le 3V$ CLK disabled SENSE_CTRL = 0	10, 11	I_{Active}		6.7		mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics: 5V Application

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V and V_{VS5V} = 5V. Typical values are given at f_{RF} = 433.92 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**5V Application**								
8.1	Supply current in OFF mode	V_{VS5V} = 5V CLK_OUT disabled	10	I_{SOFF}			2	µA	A
8.2	Supported voltage range	5V application	10	V_{VS5V}	4.5		5.5	V	A
8.3	Current in Standby mode (XTO is running)	$V_{VS5V} \leq 5V$ external load C on pin CLK_OUT = 12 pF CLK enabled (division ratio 3) CLK enabled (division ratio 6) CLK enabled (division ratio 12) CLK disabled	10	$I_{Standby}$		700 490 370 50		µA	C C C A
8.4	Current during $T_{Startup\_PLL}$	V_{VS5V} = 5V CLK disabled	10	$I_{Startup\_PLL}$		4.7		mA	C
8.5	Current in Active mode ASK	V_{VS5V} = 5V CLK disabled SENSE_CTRL = 0	10	I_{Active}		6.7		mA	A
8.6	Current in Active mode FSK	V_{VS5V} = 5V CLK disabled SENSE_CTRL = 0	10	I_{Active}		6.9		mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

16. Digital Timing Characteristics

All parameters refer to GND and are valid for T_{amb} = 25°C, $V_{VS3V\_AVCC} = V_{VS5V}$ = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 433.92 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9	**Basic Clock Cycle of the Digital Circuitry**								
9.1	Basic clock cycle			T_{DCLK}	16 / f_{XTO}		16 / f_{XTO}	µs	A
9.2	Extended basic clock cycle	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		T_{XDCLK}	8 4 2 1 × T_{DCLK}		8 4 2 1 × T_{DCLK}	µs	A
10	**Active Mode**								
10.1	Startup PLL			$T_{Startup\_PLL}$			15 µs + 208 × T_{DCLK}	µs	A
10.2	Startup signal processing	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		$T_{Startup\_Sig\_Proc}$	929.5 545.5 353.5 257.5 × T_{DCLK}		929.5 545.5 353.5 257.5 × T_{DCLK}		A
10.3	Bit rate range	ASK BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3 FSK BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3		BR_Range	 1.0 2.0 4.0 8.0 1.0 2.0 4.0 8.0		 2.5 5.0 10.0 10.0 2.5 5.0 10.0 20.0	Kbits/s	A
10.4	Minimum time period between edges at pin DATA_OUT	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3	24	$T_{DATA\_OUT\_min}$	10 × T_{XDCLK}			µs	A
10.5	Edge-to-edge time period of the data signal for full sensitivity in Active mode	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		T_{DATA_OUT}	200 100 50 25		500 250 125 62.5	µs	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

17. Digital Port Characteristics

All parameters refer to GND and are valid for T_{amb} = 25°C, $V_{VS3V\_AVCC} = V_{VS5V}$ = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 433.92 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11	**Digital Ports**								
11.1	ENABLE input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	6	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	6	V_{Ih}	$0.8 \times V_S$			V	A
11.2	RX input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	19	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	19	V_{Ih}	$0.8 \times V_S$			V	A
11.3	BR0 input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	20	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	20	V_{Ih}	$0.8 \times V_S$			V	A
11.4	BR1 input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	21	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	21	V_{Ih}	$0.8 \times V_S$			V	A
11.5	ASK_NFSK input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	22	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	22	V_{Ih}	$0.8 \times V_S$			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

17. Digital Port Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, $V_{VS3V\_AVCC} = V_{VS5V}$ = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 433.92 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.6	SENSE_CTRL input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	16	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	16	V_{Ih}	$0.8 \times V_S$			V	A
11.7	CLK_OUT_CTRL0 input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	5	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	5	V_{Ih}	$0.8 \times V_S$			V	A
11.8	CLK_OUT_CTRL1 input - Low level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	4	V_{Il}			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC}$ = V_{VS5V} = 2.7V to 3.3V $V_S = V_{VS5V}$ = 4.5V to 5.5V	4	V_{Ih}	$0.8 \times V_S$			V	A
11.9	TEST1 input	TEST1 input must always be connected directly to GND	2		0		0	V	D
11.10	TEST2 output	TEST2 output must always be connected directly to GND	1		0		0	V	D
11.11	TEST3 input	TEST3 input must always be connected directly to GND	18		0		0	V	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

17. Digital Port Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS3V_AVCC} = V_{VS5V} = 3V, and V_{VS5V} = 5V. Typical values are given at f_{RF} = 433.92 MHz unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.12	DATA_OUT output - Saturation voltage low	V_S = V_{VS3V_AVCC} = V_{VS5V} = 2.7V to 3.3V V_S = V_{VS5V} = 4.5V to 5.5V I_{DATA_OUT} = 250 µA	24	V_{ol}		0.15	0.4	V	B
	- Saturation voltage high	V_S = V_{VS3V_AVCC} = V_{VS5V} = 2.7V to 3.3V V_S = V_{VS5V} = 4.5V to 5.5V I_{DATA_OUT} = –250 µA	24	V_{oh}	V_{VS} – 0.4	V_{VS} – 0.15		V	B
11.13	CLK_OUT output - Saturation voltage low	V_S = V_{VS3V_AVCC} = V_{VS5V} = 2.7V to 3.3V V_S = V_{VS5V} = 4.5V to 5.5V I_{DATA_OUT} = 100 µA	3	V_{ol}		0.15	0.4	V	B
	- Saturation voltage high	V_S = V_{VS3V_AVCC} = V_{VS5V} = 2.7V to 3.3V V_S = V_{VS5V} = 4.5V to 5.5V I_{DATA_OUT} = –100 µA	3	V_{oh}	V_{VS} – 0.4	V_{VS} – 0.15		V	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

18. Ordering Information

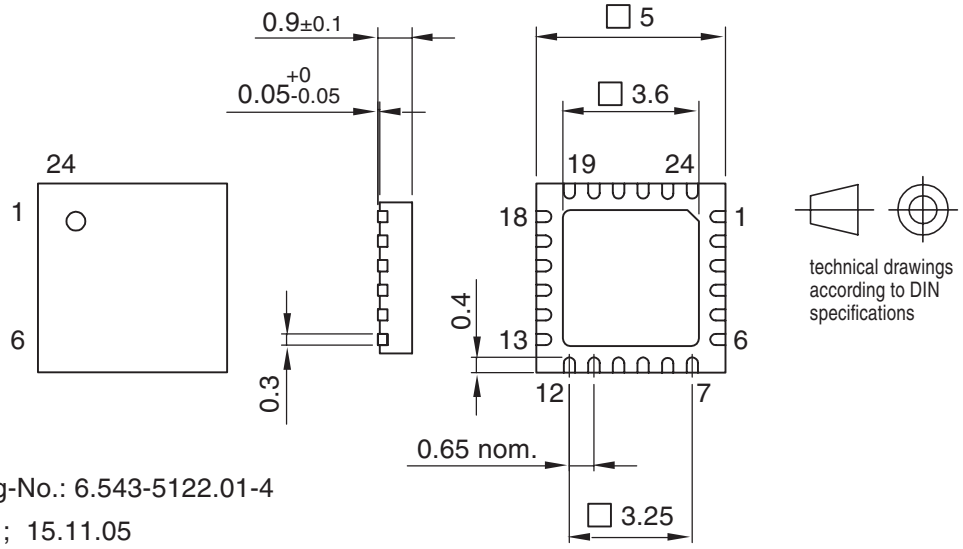
Extended Type Number	Package	MOQ	Remarks
ATA8202-PXQW	QFN24	6000 pcs	5 mm × 5 mm, Pb-free, 433.92 MHz
ATA8201-PXQW	QFN24	6000 pcs	5 mm × 5 mm, Pb-free, 315 MHz

19. Package Information

Package: QFN 24 - 5 x 5
Exposed pad 3.6 x 3.6
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm

Not indicated tolerances ±0.05



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