

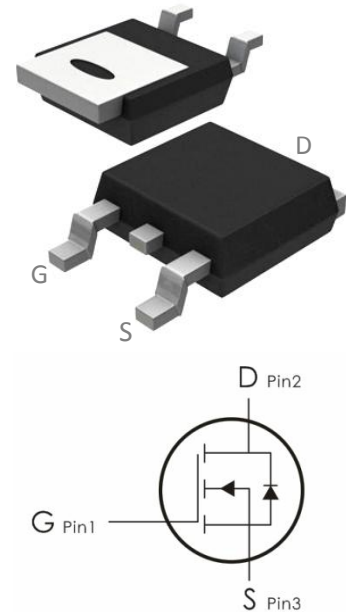
Description:

This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.

Features:

- 1) $V_{DS}=40V, I_D=30A, R_{DS(on)} < 20m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low $R_{DS(on)}$.
- 5) Excellent package for good heat dissipation.



Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current- $T_C=25^\circ C$	30	A
	Continuous Drain Current- $T_C=100^\circ C$	21	
	Continuous Drain Current- $T_A=25^\circ C$	8.4	
	Continuous Drain Current- $T_A=70^\circ C$	6.7	
I_{DM}	Pulsed Drain Current ²	80	A
E_{AS}	Single Pulsed Avalanche Energy ³	31.3	mJ
I_{AS}	Avalanche Current	25	A
P_D	Power Dissipation ⁴ - $T_C=25^\circ C$	31.3	W
	Power Dissipation ⁴ - $T_A=25^\circ C$	2	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case ¹	4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ¹	62	

Electrical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
V _{(BR)DSS}	Drain-Sourtce Breakdown Voltage	V _{GS} =0V,I _D =250 μ A	40	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =32V,T _J = 25℃	---	---	1	μ A
		V _{GS} =0V, V _{DS} =32V,T _J = 55℃	---	---	5	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0A	---	---	± 100	nA
On Characteristics						
V _{GS(th)}	GATE-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	1	---	2.5	V
R _{DS(ON)}	Drain-Source On Resistance ²	V _{GS} =10V,I _D =15A	---	---	20	m Ω
		V _{GS} =4.5V,I _D =10A	---	---	25	m Ω
G _{FS}	Forward Transconductance	V _{DS} =5V, I _D =15A	---	34	---	S
R _g	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz	---	2.1	---	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1010	---	pF
C _{Oss}	Output Capacitance		---	102	---	
C _{rss}	Reverse Transfer Capacitance		---	70	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} =20V,I _D =15A, R _G =3.3Ω,	---	2.8	---	ns
t _r	Rise Time	V _{GS} =10V	---	12.8	---	ns

t_{d(off)}	Turn-Off Delay Time	V _{DD} =20V, I _D =15A, R _G =3.3Ω, V _{GS} =10V	---	21.2	---	ns
t_f	Fall Time		---	6.4	---	ns
Q_g	Total Gate Charge	V _{DS} =32V, V _{GS} =4.5V, I _D =15A	---	10	---	nC
Q_{gs}	Gate-Source Charge		---	2.55	---	nC
Q_{gd}	Gate-Drain Charge		---	4.8	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage ²	I _S =1A, V _{GS} =0V, T _J = 25 °C	---	---	1.2	V
I_S	Continuous Source Current ^{1,5}	V _G =V _D =0V , Force Current	---	---	33	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	80	A
T_{rr}	Reverse Recovery Time	I _F = 15 A, dI _F / dt = 100 A/ μ s	---	10	---	ns
Q_{rr}	Reverse Recovery Charge	T _J = 25 °C	---	3.1	---	nC

Notes:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=25A$
- 4.The power dissipation is limited by $150^\circ C$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics: (T_J=25°C unless otherwise noted)

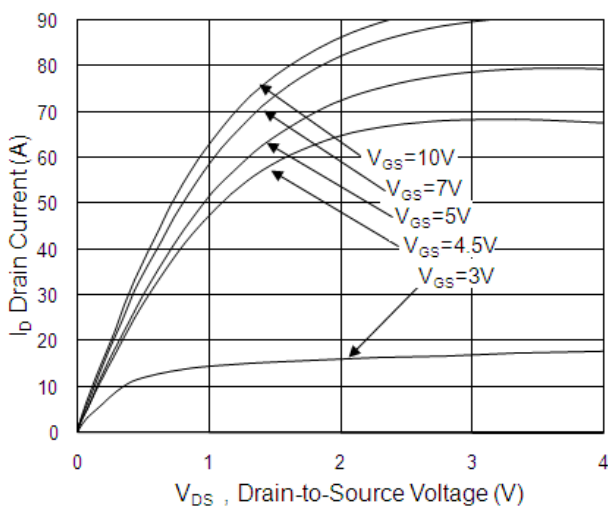


Fig.1 Typical Output Characteristics

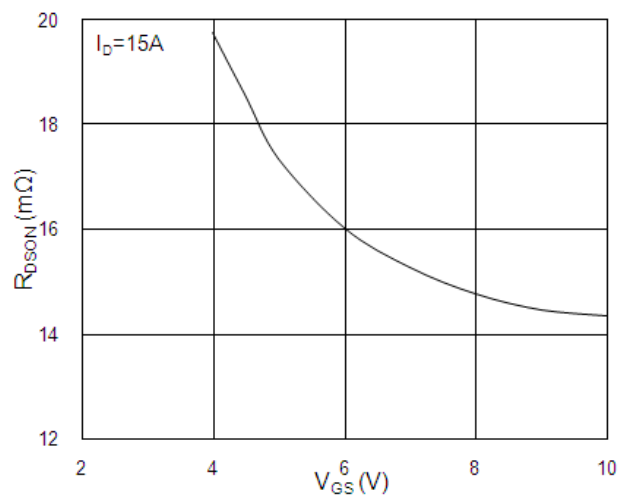


Fig.2 On-Resistance vs. G-S Voltage

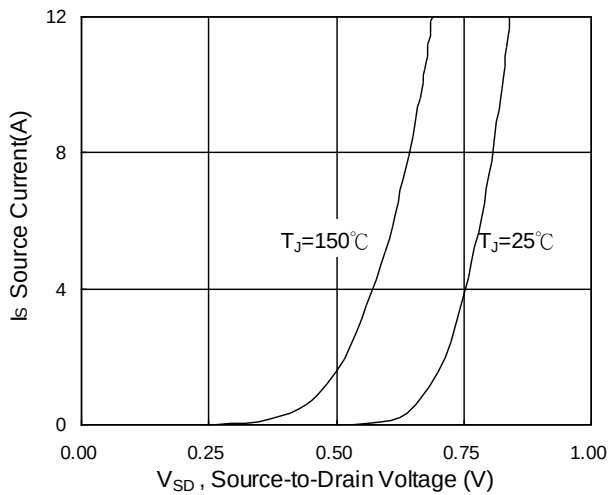


Fig.3 Forward Characteristics Of Reverse

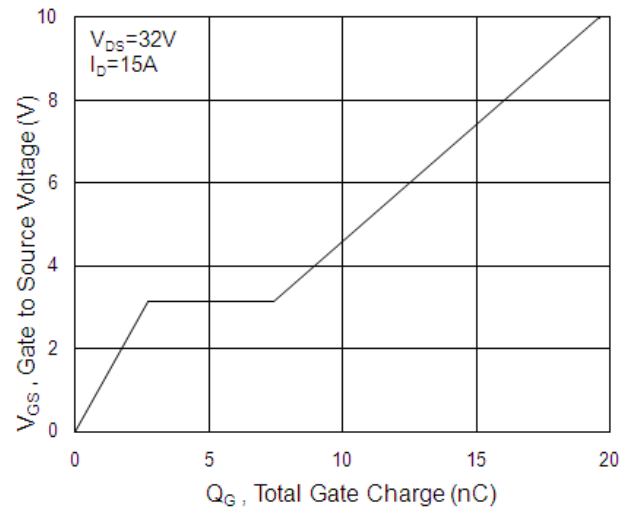


Fig.4 Gate-Charge Characteristics

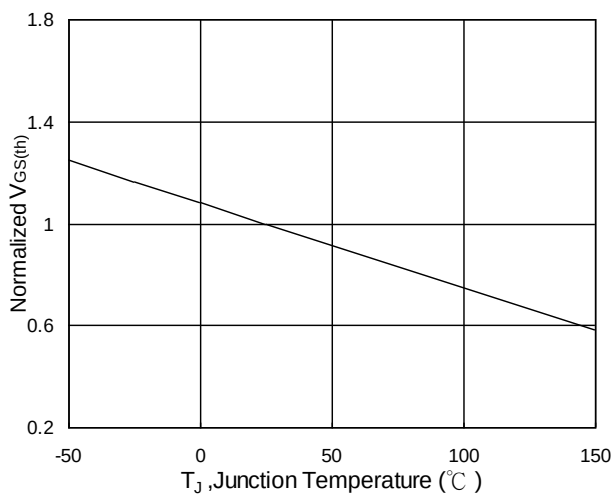


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

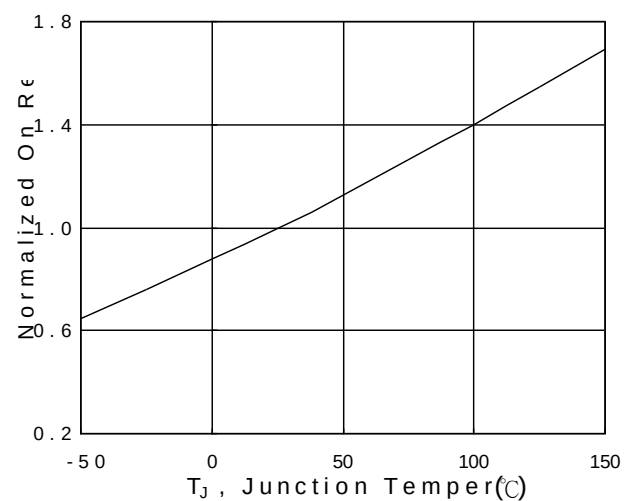


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

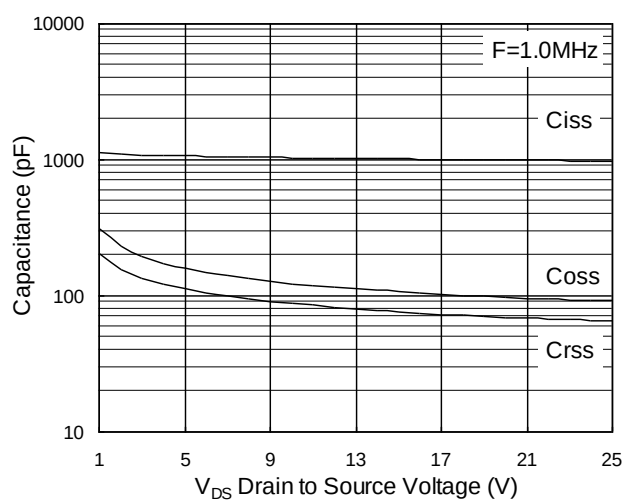


Fig.7 Capacitance

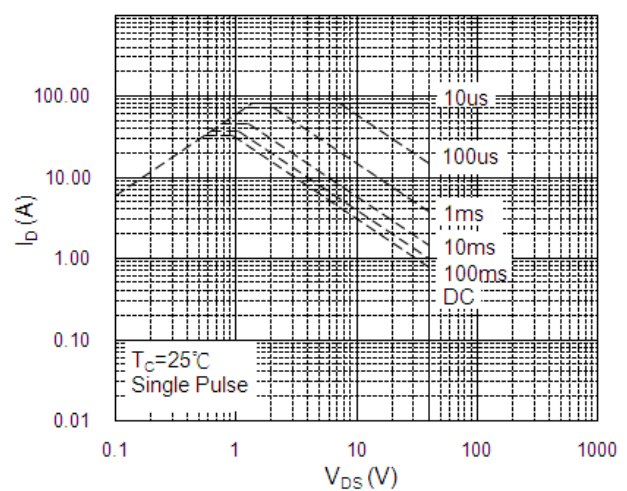


Fig.8 Safe Operating Area

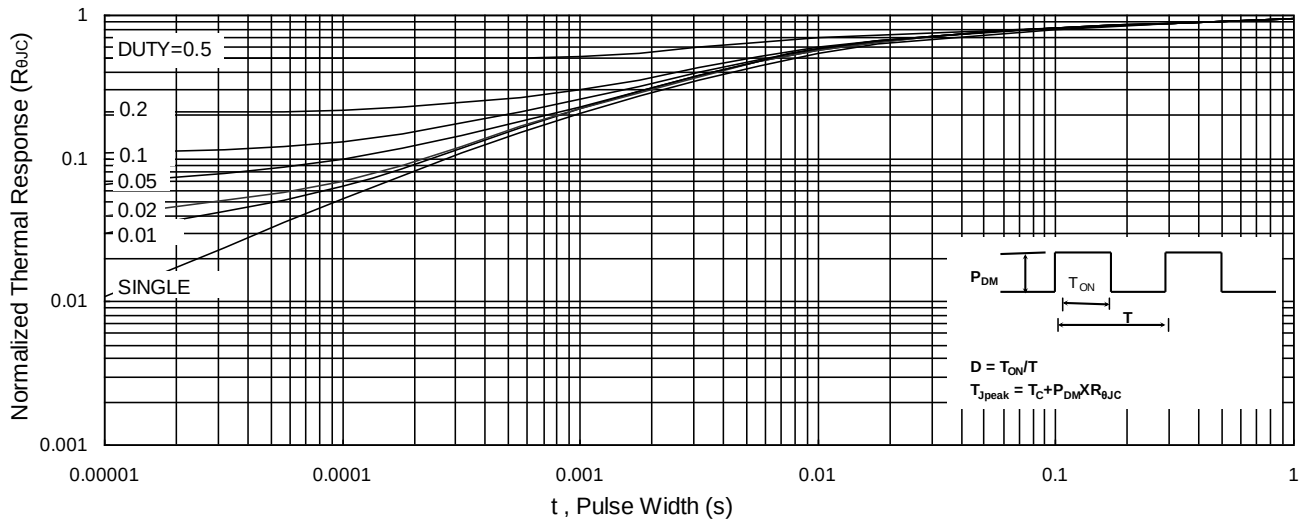


Fig.9 Normalized Maximum Transient Thermal Impedance

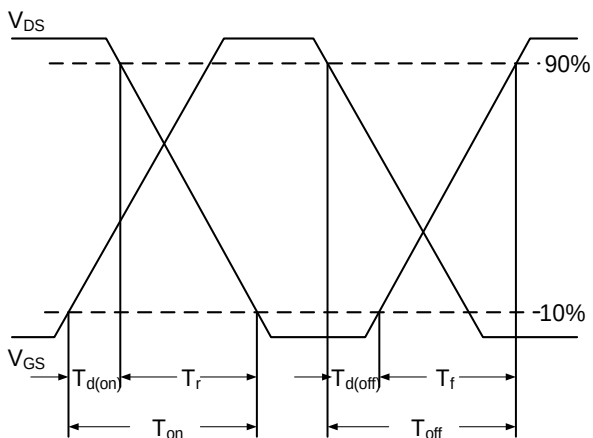


Fig.10 Switching Time Waveform

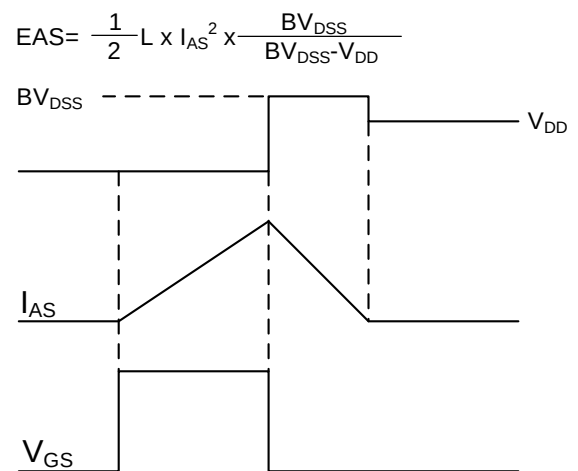


Fig.11 Unclamped Inductive Switching Waveform



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