To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M65664FP

PICTURE-IN-PICTURE
SIGNAL PROCESSING

DESCRIPTION

The M65664FP is a PIP (Picture in Picture) signal processing LSI, whose sub-picture input is composite signal for NTSC, PAL-M, and PAL-N. The built-in field memory (168k-bit RAM) , V-chip data slicer and analog circuitries lead the high quality PIP system low cost and small size.

APPLICATION

NTSC, PAL-M, PAL-N color TV

FEATURES

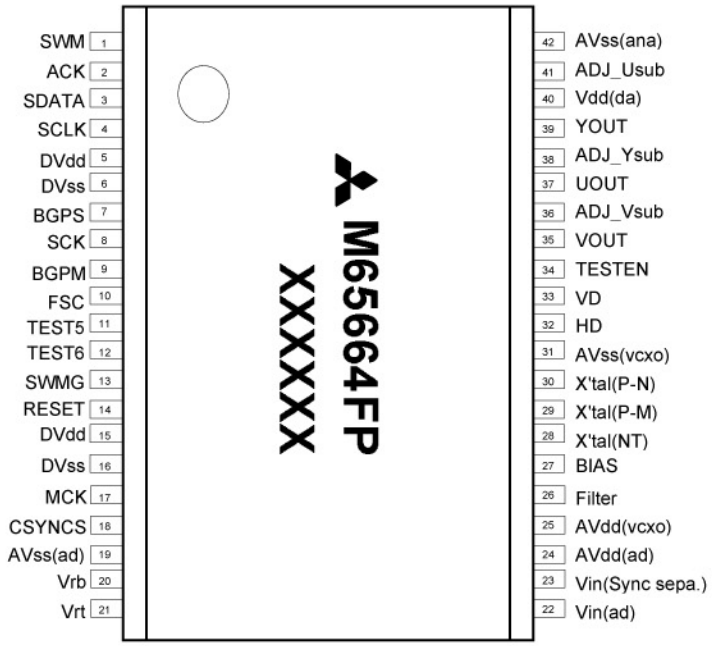
* Internal V-chip data slicer (for sub-picture)
* Vertical filter for sub-picture (Y signal)
* Single sub-picture (selectable picture size : 1/9 , 1/16)
* Sub-picture processing specification (1/9 , 1/16 size) :
  Quantization bits Y, B-Y, R-Y : 7 bits
  Horizontal sampling 229 pixels (Y), 57 pixels (B-Y, R-Y)
  Vertical lines 69/ 52 lines
* Frame (sub-picture) on/off
* Built-in analog circuits :
  One 8-bit A/D converter (for sub-picture signal)
  Three 8-bit D/A converters (for Y, U and V of sub-picture)
  Sync-tip-clamp, VCXO ... etc..
* IIC BUS control (parallel/serial control) :
  PIP on/off , Frame on/off (programmable luma level),
  Sub-picture size (1/9, 1/16),
  PIP position (free position), Picture freeze ,
  Y delay adjustment, Chroma level, Tint, Black level,
  Contrast ...etc..

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ---------- 3.2 ~ 3.5 V
Operating frequency ---------- 14.32 MHz
Operating temperature ---------- 0 ~ 70 deg.
Input voltage (CMOS interface) "H" ----- VDD x 0.7 ~ VDD V
"L" ----- 0 ~ VDD x 0.3 V
Output current (output buffer) ---------- 4 mA (MAX)
Output load capacitance ---------- 20 pF (MAX) *1
Circuit current ---------- - mA

NOTICE: Connect a 0.1□F or larger capacitor between VDD and VSS pins.
*1 : Include pin capacitance (7 pF)

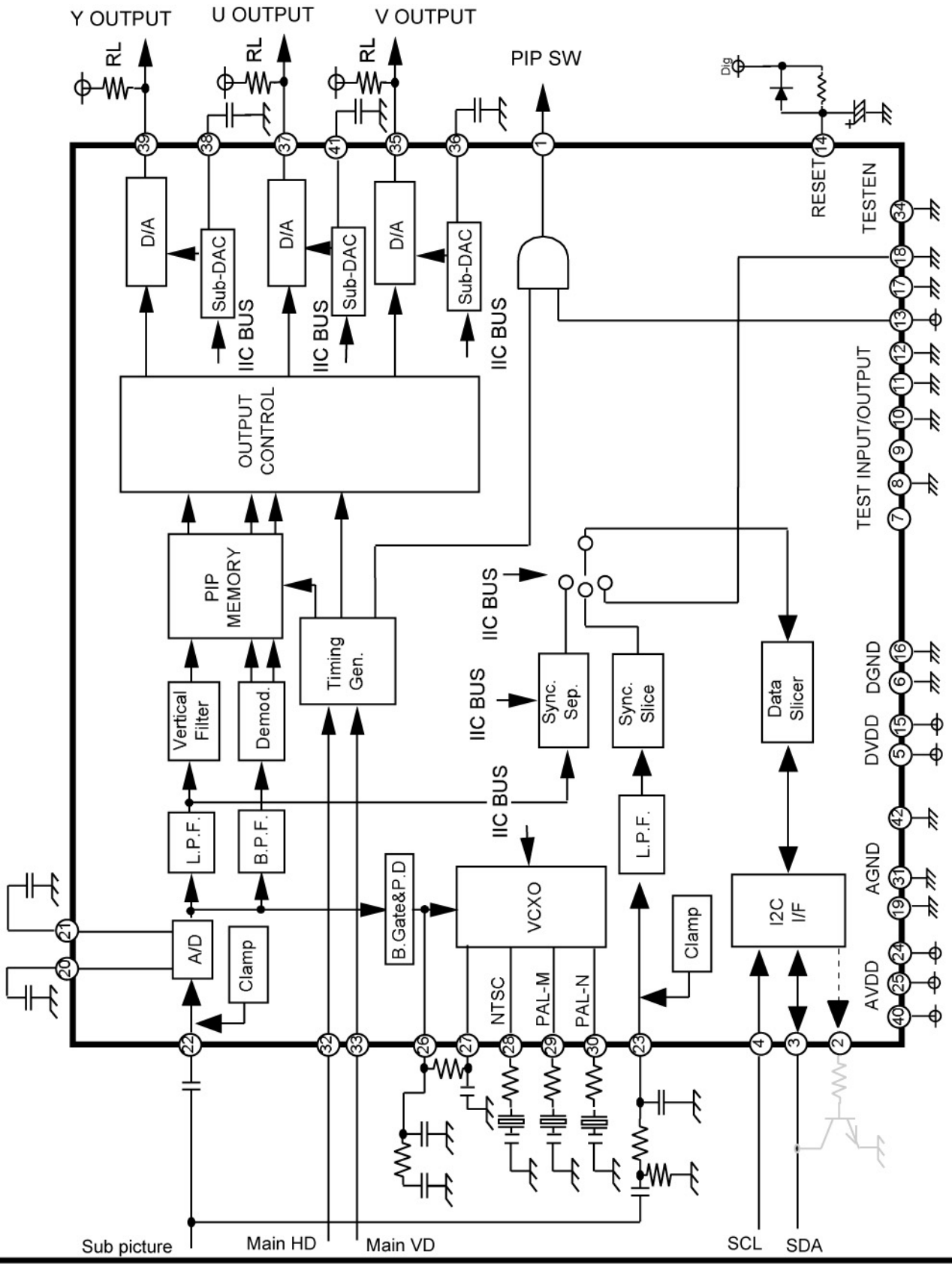
PIN CONFIGURATION (TOP VIEW)



Outline 0.8mm pitch 42 Pin SOP Package

RENESAS

BLOCK DIAGRAM



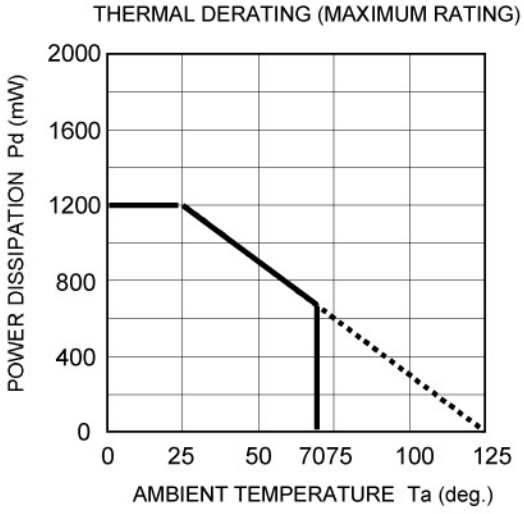
ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
V_{DD3}	Supply voltage (3.3V)		-0.3	4.2	V
V_I	Input voltage(except 5V input)		-0.3	V_{DD3}+0.3	V
V_I	Input voltage(5V input)		-0.3	5.25	V
V_O	Output voltage		-0.3	V_{DD3}+0.3	V
I_O	Output current (*1)		I_{OH} = -4	I_{OL} = 4	mA
P_D	Power dissipation		-	1200	mW
Topr	Operating temperature		-10	70	deg.
Tstg	Storage temperature		-50	125	deg.

(*1) Output current per output terminal. But Pd limits all current.

TYPICAL CHARACTERISTICS



DC CHARACTERISTICS

(Ta = 25 deg. unless otherwise noted) (V_{SS}=0V)

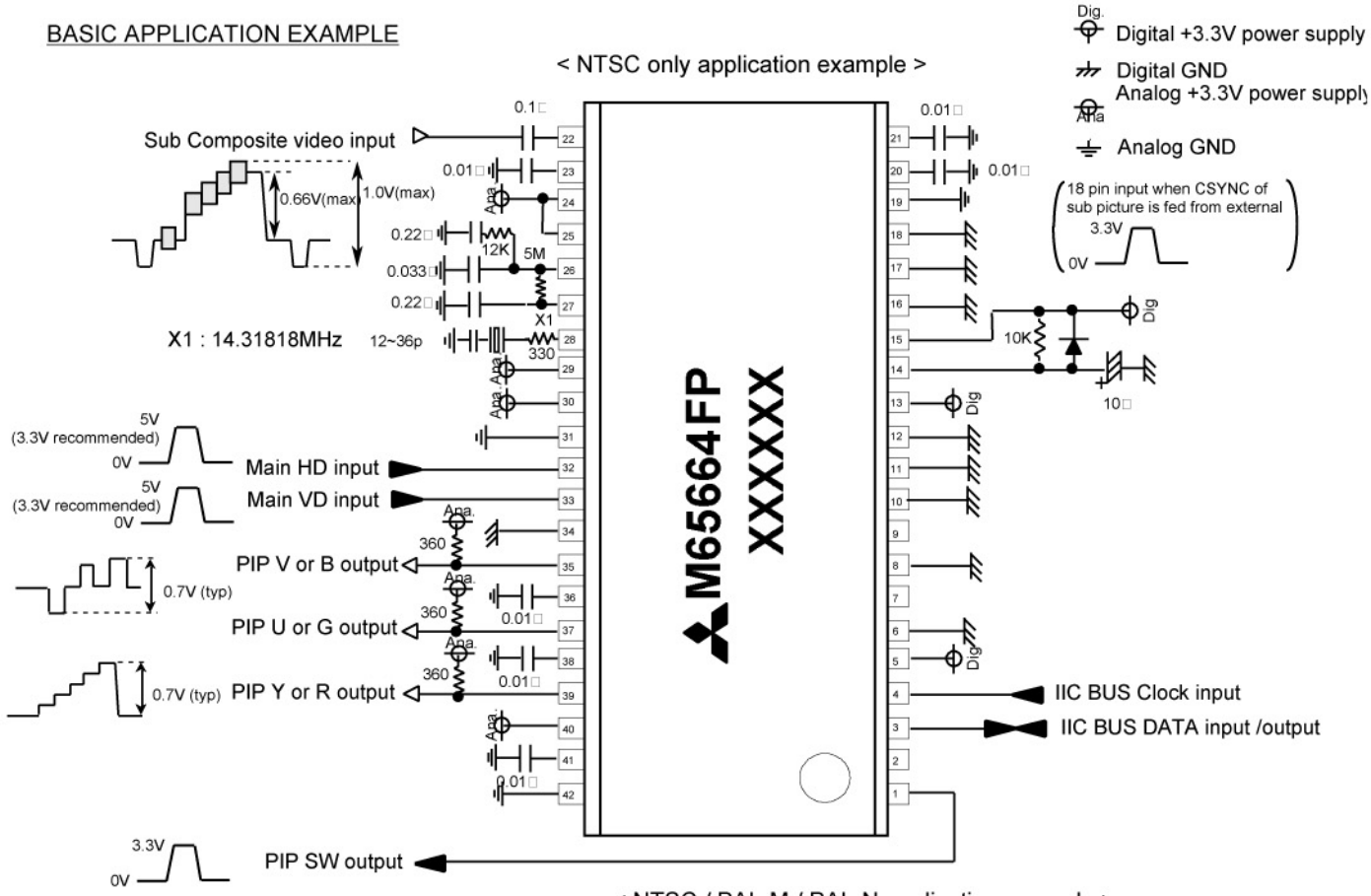
Symbol	Parameter		Condition	Limits			Unit
				Min.	Typ.	Max.	
V_{IL}	Input voltage (3.3V CMOS interface)	L	V_{DD} = 2.7V	0	-	0.81	V
V_{IH}		H	V_{DD} = 3.6V	2.52	-	3.6	
I_{IH}	Input current (3.3V CMOS interface)	L	V_{DD} = 3.6V, V_I = 0V	-10	-	10	□A
I_{IL}		H	V_{DD} = 3.6V, V_I = 3.6V	-10	-	10	
V_{T-}	Input voltage schmitt (5.0V CMOS interface)	-	V_{DD} = 3.3V	0.8	-	1.65	V
V_{T+}		+		1.4	-	2.7	
V_H		Hysteresis		0.3	-	1.2	
I_{IH}	Input current (5.0V CMOS interface)	L	V_{DD} = 3.6V, V_I = 0V	-100	-	10	□A
I_{IL}		H	V_{DD} = 3.6V, V_I = 3.6V	-10	-	10	
V_{OL}	CMOS output voltage	L	V_{DD} = 3.3V, |I_O| = 1□A	-	-	0.05	V
V_{OH}		H		3.25	-	-	
I_{OL}	CMOS output current	L	V_{DD} = 3.0V, V_{OL} = 0.4V	4	-	-	mA
I_{OH}		H	V_{DD} = 3.0V, V_{OH} = 2.6V	-	-	-4	
I_{OZL}	Output leakage current	L	V_{DD} = 3.6V, V_O = 0V	-10	-	10	□A
I_{OZH}		H	V_{DD} = 3.6V, V_O = 3.6V	-10	-	10	
C_I	Input pin capacitance		f = 1MHz, V_{DD} = 0V	-	7	15	pF
C_O	Output pin capacitance			-	7	15	
C_{IO}	Bidirectional pin capacitance			-	7	15	
I_{DD}	Operating current	3.3V supply		-	140	-	mA

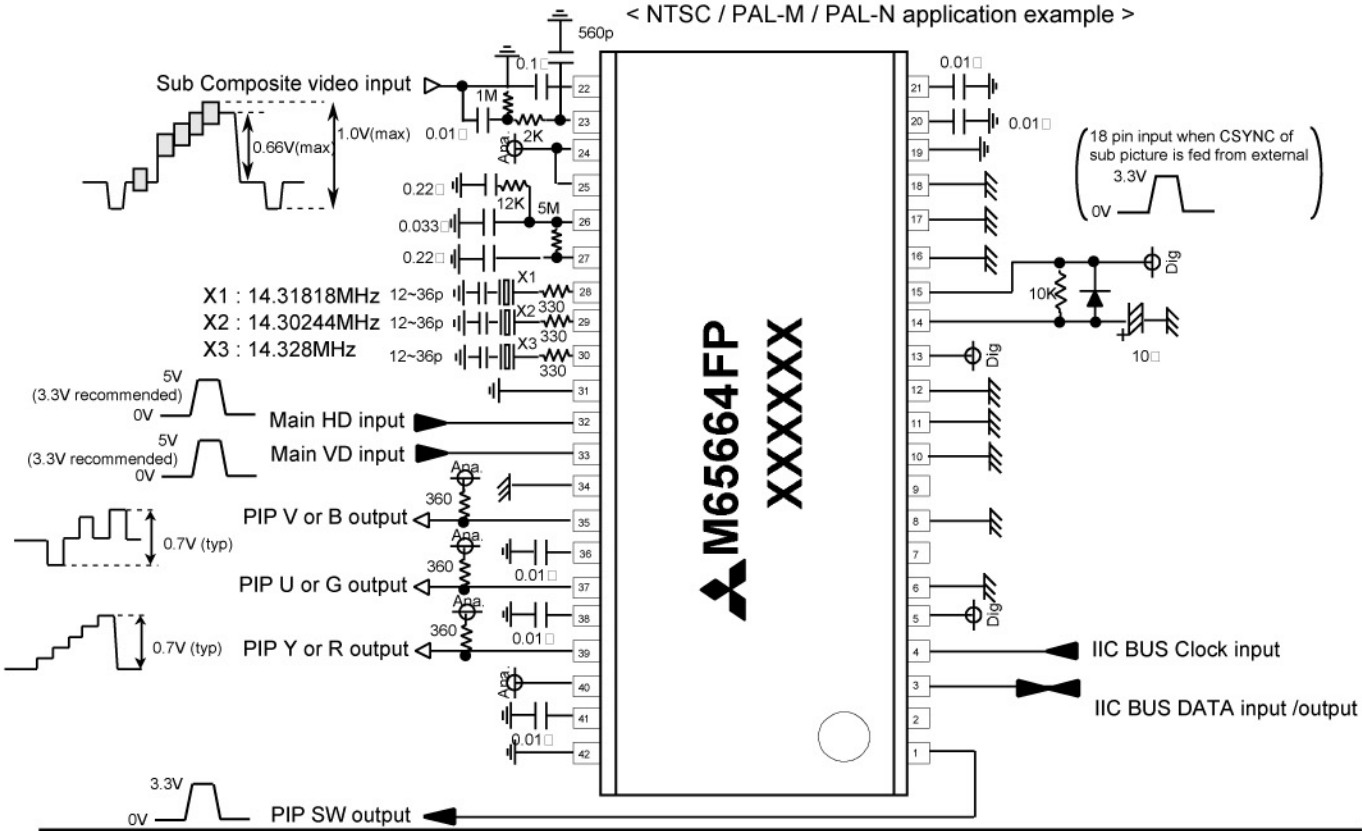
PIN DESCRIPTION

Pin No.	Name	I/O	Function	Remarks
1	SWM	CMOS output	PIP switch output	
2	ACK	CMOS output	I2C SDA output (for high load SDA line use only)	
3	SDATA	CMOS I/O(5V)*1	I2C SDA input/output	
4	SCLK	CMOS input(5V)*1	I2C SCL input	
5	DVdd1	Digital Vdd	Vdd for digital part	
6	DVss1	Digital Vss	Vss for digital part	
7	BGPS	CMOS output	Test output	
8	SCK	CMOS input	Test input	connect to GND
9	BGPM	CMOS output	Test output	
10	FSC	CMOS input	Test input	connect to GND
11	TEST5	CMOS input	Test input	connect to GND
12	TEST6	CMOS input	Test input	connect to GND
13	SWMG	CMOS input		connect to Vdd
14	RESET	CMOS input	Power on reset input	
15	DVdd2	Digital Vdd	Vdd for digital part	
16	DVss2	Digital Vss	Vss for digital part	
17	MCK	CMOS input	Test input	connect to GND
18	CSYNCS	CMOS input	Sub picture external C-sync input	
19	AVss (ADC)	Analog Vss	Vss for internal ADC	
20	VRB	Analog	Low level reference voltage output of ADC	
21	VRT	Analog	High level reference voltage output of ADC	
22	VIN (ADC)	Analog	Sub picture input of ADC	
23	VIN (Sync Sep.)	Analog	Sub picture input of sync sep. for sub picture	
24	AVdd (ADC)	Analog Vdd	Vdd for internal ADC	
25	AVdd (VCXO)	Analog Vdd	Vdd for VCXO	
26	FILTER	Analog	VCXO filter voltage connection	
27	BIAS	Analog	VXCO bias voltage connection	
28	X'tal (NTSC)	Analog	X'tal of NTSC connection	
29	X'tal (PAL-M)	Analog	X'tal of PAL-M connection	
30	X'tal (PAL-N)	Analog	X'tal of PAL-N connection	
31	AVss (VCXO)	Analog Vss	Vss for VCXO	
32	HD	CMOS input(5V)*1	Main picture HD input	
33	VD	CMOS input(5V)*1	MAIN picture VD input	
34	TESTEN	CMOS input	Test input	connect to GND
35	VOUT	Analog	Sub picture V or B output	
36	ADJ_Vsub	Analog	Referece voltage connection of DAC of V	
37	UOUT	Analog	Sub picture U or G output	
38	ADJ_Ysub	Analog	Referece voltage connection of DAC of Y	
39	YOUT	Analog	Sub picture Y or R output	
40	AVdd (DAC)	Analog Vdd	Vdd for DAC	
41	ADJ_Usub	Analog	Referece voltage connection of DAC of U	
42	AVss (sub)	Analog Vss	Vss for substrate	

*1) (5V)means 5V I/F torelant

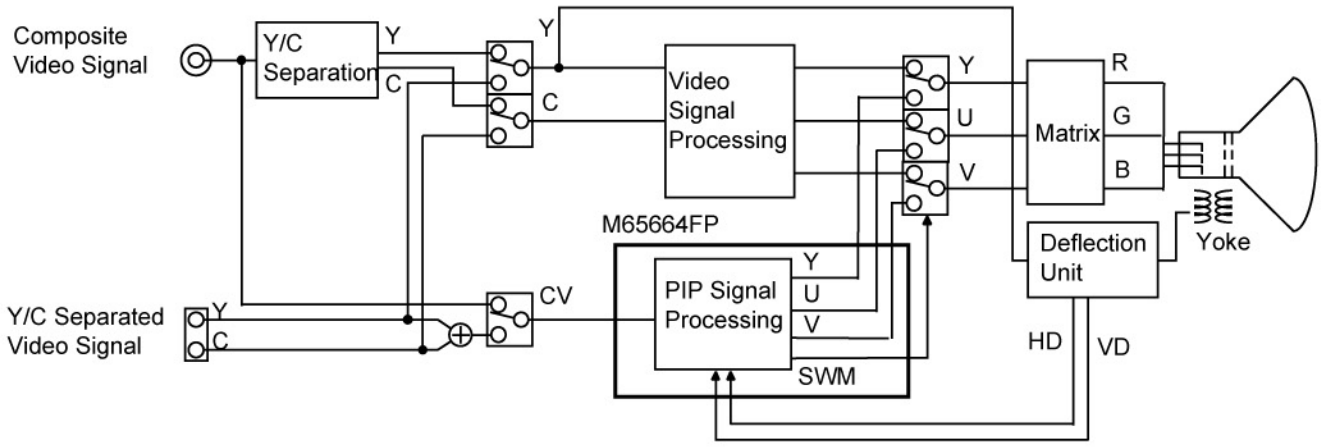
BASIC APPLICATION EXAMPLE

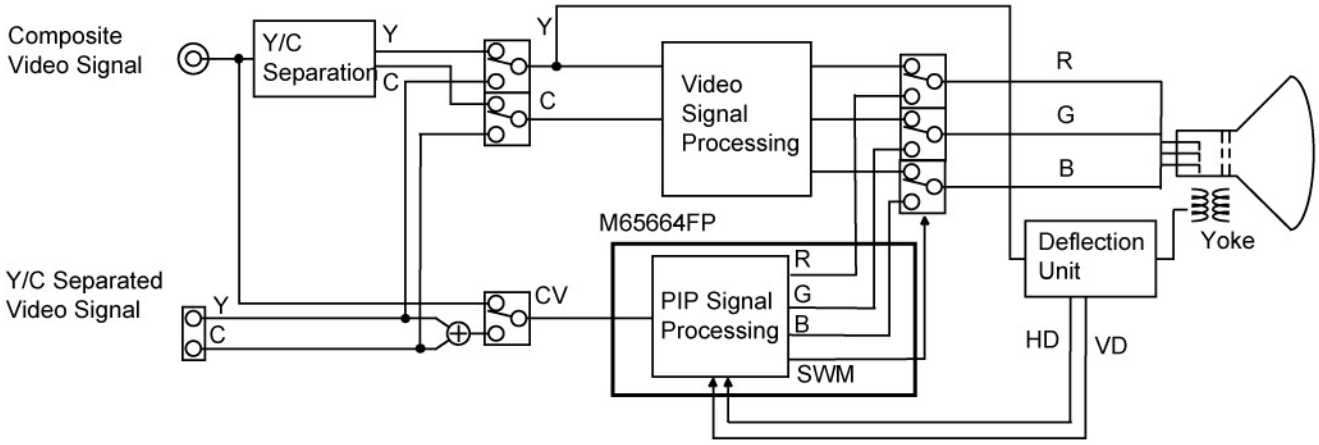




M65664FP TV SYSTEM BLOCK DIARGRAM

<BASIC >





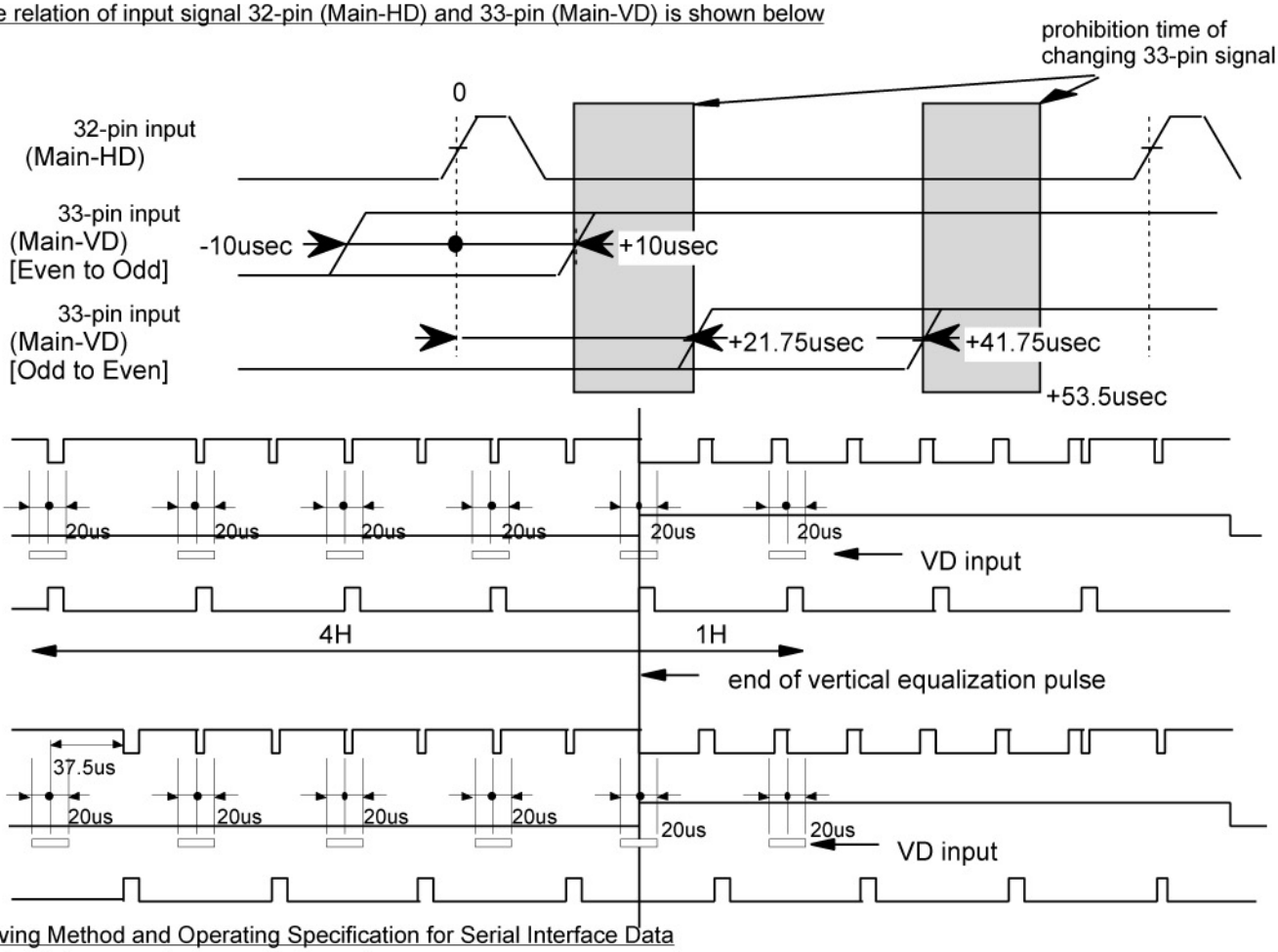
Internal register information

address	bit	symbol	Reset val	1/9 ex.	remarks
00h	<7>	DISP	0	1	Sub picture display : [0] off, [1] on
	<6>	SIZE_V	0	0	Sub picture vertical size : [0] 1/9, [1] 1/16
	<5>	SIZE_H	0	0	Sub picture horizontal size : [0] 1/9, [1] 1/16
	<4>	WEN	0	1	Sub picture : [0] Still, [1] Moving
	<3>	BGC	0	0	Back ground display : [0] off, [1] on
	<2>	BGCS	0	0	Sub picture mute : [0] off, [1] on
	<1>	FREE_RUN		0	VCXO ocsilation : [0] Lock, [1] Free run
	<0>	RVS	0	0	HD/VD input synchronous mode selection : [0] sync., [1] async.
01h	<7:0>	VXA<7:0>		20h	Sub picture vertical position
02h	<7:0>	HXA<7:0>		20h	Sub picture horizontal position
03h	<7>	DECODE	0	0	Sub picture color decoder reset : [1] reset
	<6:0>	CONTRAST<6:0>		32h	Sub picture Y or R DAC output amplitude control
04h	<7>	KILLER	0	0	Sub picture color killer : [0] enable, [1] disable
	<6:0>	U_DAC<6:0>		32h	Sub picture U or G DAC output amplitude control
05h	<7>	GRC		1	Frame display : [0] off, [1] on
	<6>	YUVN_RGB_SEL	0	0	PIP output mode selection : [0] YUV, [1] RGB
	<5:0>	TINT<5:0>	00h	00h	Sub picture tint control
06h	<7:6>	EXT_SC_SEL<1:0>	0h	0h	Sub picture C-Sync sep. input selection : [0] Digital, [1] 23 pin input, [2] external (18 pin), [3] Int. analog
	<5>	HIMPRV	0	0	H jitter improvement circuit : [0] off, [1] on
	<4>	SUBINPUT	0	0	Sub picture input level : [0] 33% bigger : [0] same with M65669
	<3:0>	HT<3:0>		Ah	Sub picture display timing adjust
07h	<7:6>	EXPORT<1:0>		2h	Ext. port (7 pin) : [0or1] Sub BGP, [2]"0" output, [3]"1" output
	<5:0>	BG_START<5:0>		0Eh	Sub picture BGP position setting
08h	<7:4>	ADJ<3:0>		2h	Main/Sub switch delay control
	<3:0>	YDL<3:0>		5h	Sub picture Y/C delay adjust
09h	<7:5>	BGBY<2:0>	0h	0h	Back ground U level setting
	<4:0>	Y_OFFSET<4:0>		0Fh	Sub picture Y bright control
0Ah	<7>	VCHIP_ONLY	0	0	V-chip decode mode : [0] off, [1] on
	<6:4>	BGRY<2:0>	0h	0h	Back ground V level setting
	<3:0>	BGY<3:0>		Ch	Back ground Y level setting
0Bh	<7:4>	PEDESTV<3:0>	0h	0h	Sub picture V pedestal level (2's comp)
	<3:0>	PEDESTU<3:0>	0h	0h	Sub picture U pedestal level (2's comp)
0Ch	<7>	UV_FILTER_OFF	0	0	Sub picture U, V output filter : [0]on, [1]off
	<6>	SET_ACC	0	0	Address 0Dh, 0Eh setting mode : [0]default, [1] enable to set
	<5:4>	SYSTEM_MODE<1:0>	0h	0h	System : [0]NTSC , [1]PAL-M, [2]PAL-N, [3] N.A.
	<3>	SET_SIZE	0	0	Address 11h - 14h setting mode : [0]default, [1] enable to set
	<2>	SET_VCHIP	0	0	Address 15h - 17h setting mode : [0]default , [1] enable to set
	<1>	INV_UV	0	0	Invert U, V output value : [0] normal, [1] invert
	<0>	CROSS_SEL	0	0	Sub picture read mode : [0] pixel based, [1] H based
0Dh	<7:6>	SYNC_DELAY<1:0>	0h	0h	Sub picture sync.delay control
	<5:4>	DCONT<1:0>	0h	0h	Sub picture digital sync sep.threshold setting
	<3>	C_GAIN_SEL	0	0	Sub picture chroma : [0] x1, [1] x2
	<2>	AUTOAFC	0h	0h	for test : 0 set only
	<1>	SUBINPUTB	0h	0h	for test : 0 set only
	<0>	CVF	0h	0h	Internal chroma comb filter : [0] on : [0] off
0Eh	<7>	BITSEL	0	0	Sub picture Y clamp time constant : [0] x2, [1] x1
	<6>	AFCBITSEL	0	0	Sub picture AFC time constant : [0] x2, [1] x1
	<5:0>	ACC_LEVEL<5:0>		15h	Sub picture color decoder amplitude
0Fh	<7>	AUTO_ENABLE	0	0	System automatic judgment : [0] off, [1] on
	<6>	BURST_CLOCK_MODE	0	0	VCXO mode selection : [0] 1H based, [1] 2H based
	<5>	PALN_ENABLE	0	0	Main picture PAL-N : [0] enable, [1] disable
	<4>	INV_WFF	0	0	Invert sub picture field definition : [0] normal, [1] invert
	<3>	INV_RFF	0	0	Invert main picture field definition : [0] normal, [1] invert
	<2>	ERRSEL	0	0	for test : 0 set only
	<1>	RFF_FIX	0	0	Main picture field fix : [0] not fix, [1]fix
	<0>	AUTO_RFF_FIX	0	1	Automatic 50/60Hz Judgement : [0] enable, [1] disable

Internal register information (continuing)

address	bit	symbol	Reset val	1/9 ex.	remarks
10h	<7>	INVDECODE	0	0	Sub picture decoder mode : [0] NTSC, [1] PAL
	<6>	AVERAGE	0	0	Sub picture decoder mode : [0] 1H based, [1] 2H based
	<5:0>	PALRY<5:0>	00h	00h	Threshold control of ident judgment of sub picture decoder
11h	<7>	WDOF_KILLER_ON	0	0	Sub picture killer on when its vert. sync lost : [0] on, [1] off
	<6:0>	HYA<6:0>		37h	Sub picture horizontal display pixel
12h	<7:0>	VYA<7:0>		44h	Sub picture vertical display line number
13h	<7:2>	HX<5:0>		1Eh	Sub picture horizontal capture position (coarse)
	<1:0>	HP<1:0>	0h	0h	Sub picture horizontal capture position (fine)
14h	<7:6>	MVC<1:0>	0h	0h	Sub picture C-sync input mask period : 0] 48us, [1] 44us, [2] 53us, [3] off
	<5:0>	VXS<5:0>		29h	Sub picture sample start line
15h	<7>	-	0	0	for test : 0 set only
	<6>	PLUS	0	0	for test : 0 set only
	<5>	-	0	0	for test : 0 set only
	<4:0>	LINE_NUM<4:0>		11h	Data slicer line selection
16h	<7:0>	STB_DLY<7:0>		40h	Data slicer start bit detection parameter
17h	<7:0>	L_LEVEL<7:0>		82h	Data slicer data slice parameter
18h	<7>	EDGE_ON	0	0	Frame data independent control : [0] disable, [1] enable
	<6:4>	BGBY_EDGE<2:0>	0h	0h	Frame data independent B-Y data setting
	<3:0>	BGY_EDGE<3:0>		0h	Frame data independent Y data setting
19h	<7:5>	BGRY_EDGE<2:0>	0h	0h	Frame data independent R-Y data setting
	<4>	HPFOFF	0	0	Sub picture Y output HPF : [0]on, [1]off
	<3:0>	FREE_RUN_ADJ<3:0>	0h	0h	Frequency adjustment control when free run mode (2's comp)
1Ah	<7:0>	SUB_PALM_JDGE<7:0>	0h	0h	Parameter setting for PAL-M judgment
1Bh	<7:6>	NO_BST_LEVEL	0h	0h	for test
	<5:4>	BW_DET_LEVEL	0h	0h	for test
	<3:0>	HADJ<3:0>	0h	0h	Parameter setting for PAL-M judgment
1Ch	<7>	PINOE	0	0	for test
	<6:0>	V_DAC<6:0>	0h	32h	Sub picture V or B DAC output amplitude control
1Dh	<7:0>	PINOE<7:0>		E6h	for test
1Eh	<7:0>	-			No assignment
1Fh	<7:6>	SYSTEM_STATE<1:0>			Color state : [0] NTSC, [1] PAL-M, [2] PAL-N, [3]N.A.(Read only)
	<5>	MAIN_PALN			Main is : [0] not PAL-N, [1] PAL-N (Read only)
	<4>	SUB_UNLOCK			VCXO is : [0] Lock, [1] Unlock (Read only)
	<3>	SUB_PALN			Sub is : [0] not PAL-N, [1] PAL-N (Read only)
	<2>	RDOF			Main picture V sync is : [0] present, [1] not present (Read only)
	<1>	MAIN_BW			Test use (Read only)
	<0>	WDOF			Sub picture V sync is : [0] present, [1] not present (Read only)
20h	<7:6>	NOISE<1:0>			Test use (Read only)
	<5>	WDOF			Sub picture vertical sync detection (Read only)
	<4>	EDS_ACK2			EDS data flag of even field : [0] no EDS, [1] EDS (Read only)
	<3>	EDS_ACK1			EDS data flag of odd field : [0] no EDS, [1] EDS (Read only)
	<2>	SIGNAL_OK			Test use (Read only)
	<1>	READ_REQB			Read request of even field : [0] no, [1] requesting (Read only)
	<0>	READ_REQA			Read request of odd field : [0] no, [1] requesting (Read only)
21h	<7:0>	PDB<15:8>			Even field Sliced data upper 8 bit (Read only)
22h	<7:0>	PDB<7:0>			Even field Sliced data lower 8 bit (Read only)
23h	<7:0>	PDA<15:8>			Odd field Sliced data upper 8 bit (Read only)
24h	<7:0>	PDA<7:0>			Odd field Sliced data lower 8 bit (Read only)

The relation of input signal 32-pin (Main-HD) and 33-pin (Main-VD) is shown below



Driving Method and Operating Specification for Serial Interface Data

(1) Serial data transmission completion and start

A low-to-high transition of the DATA (serial data) line while the CLK (serial clock) is high, that completes the serial transmission and makes the bus free.

A high-to-low transition of the DATA line while the CLK is high, that starts the serial transmission and waits for the following CLK and DATA inputs.

(2) Serial data transmission

The data are transmitted in the most significant bit (MSB) first by one-byte unit on the DATA line successively. One-byte data transmission is completed by 9 clock cycles, the former 8 cycles are for address/data and the latter one is for acknowledge detection. (In reading state, ACK is 'H' under these two conditions ; 1) the coincidence of two address data for the address data transmission, 2) the completion of 8-bit setting data transfer. In writing state, ACK is 'H' with the address coincidence and ACK is 'L' for detecting acknowledge input from the master (micro processor) after sending 8-bit setting data.)

For address/data transmission, DATA must change while CLK is 'L'. (The data change while CLK is 'H' or the simultaneous change of CLK and DATA, that will be a false operation because of undistinguished condition from the completion/start of serial data transfer).

After the beginning of serial data transmission, the total number of data bytes that can be transferred are not limited.

(3) The byte format of data transmission (The sequence of data transmission)

a. The byte format during data setting to M65664FP are shown as follows.

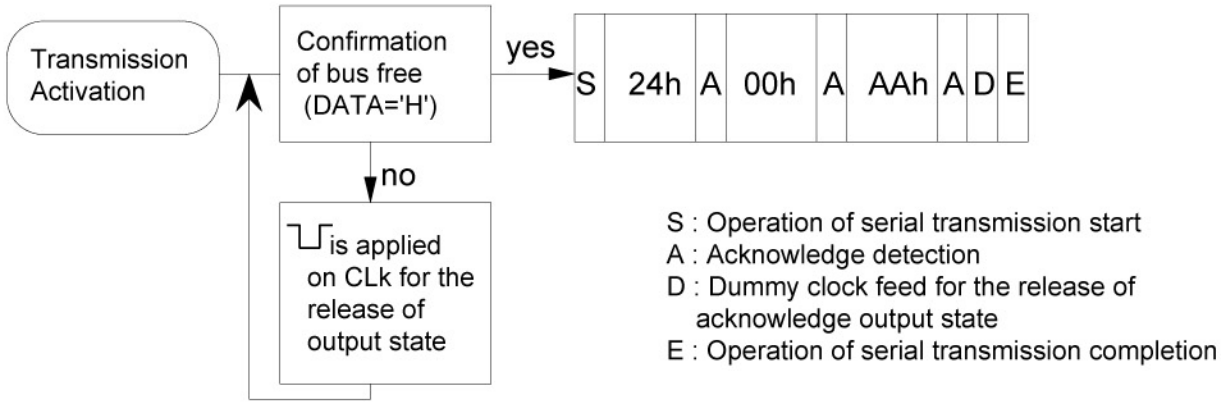
In right after the forming of serial data transmitting state, the slave address 24h (00100100b) is transferred. Afterwards, the internal register address (1 byte) and setting data (by 1 byte unit) are transferred successively. Several bytes of setting data can be handled in the one transmission. In this operation, the setting data are written into the address register whose address is increased one in initially transferred internal register address.

b. The byte format during data reading from M65664FP are shown as follows.

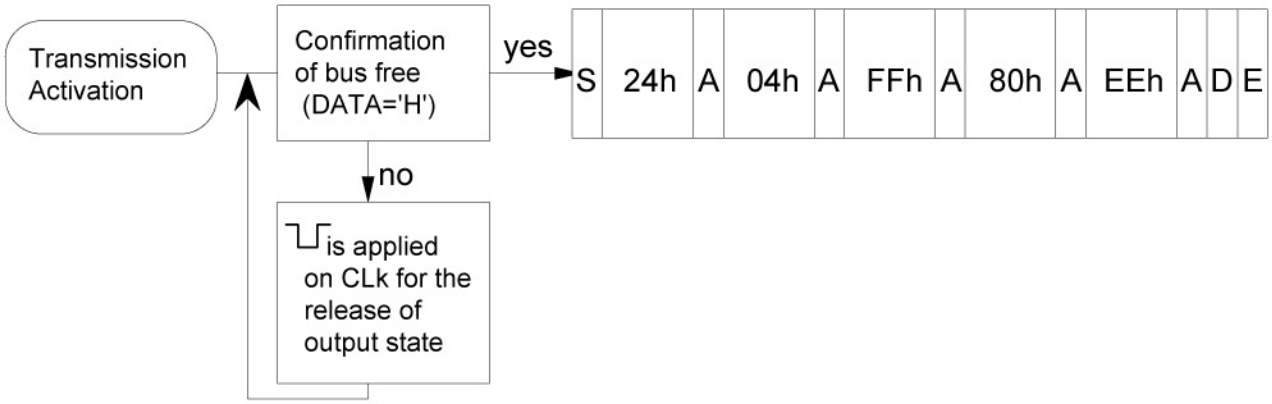
Before data reading from M65664FP, whose internal address need to be set by the data reading/transmitting. After the data reading/transmitting, the operation of "serial data transmission completion and start" (described in (1)) is necessary. Continuously, the slave address 25h (00100101b) is sent, and then the inverted read out data are available on ACK. Several bytes of writing data can be handled in the one transmission, too. In this operation, the setting data also are written into the address register whose address is increased one in initially transferred internal register address.

<The examples of serial byte transmission format>

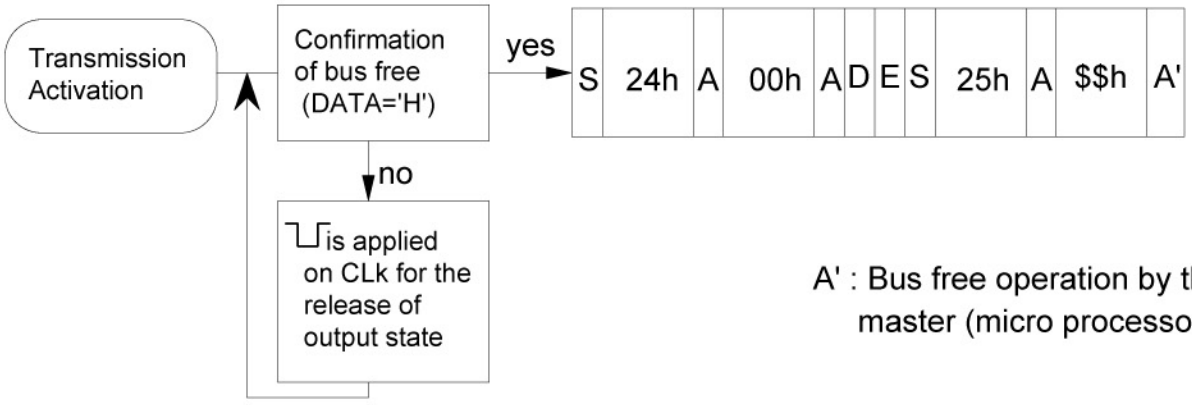
(1) The writing operation of the setting data (AAh) into M65664FP internal address of 00h



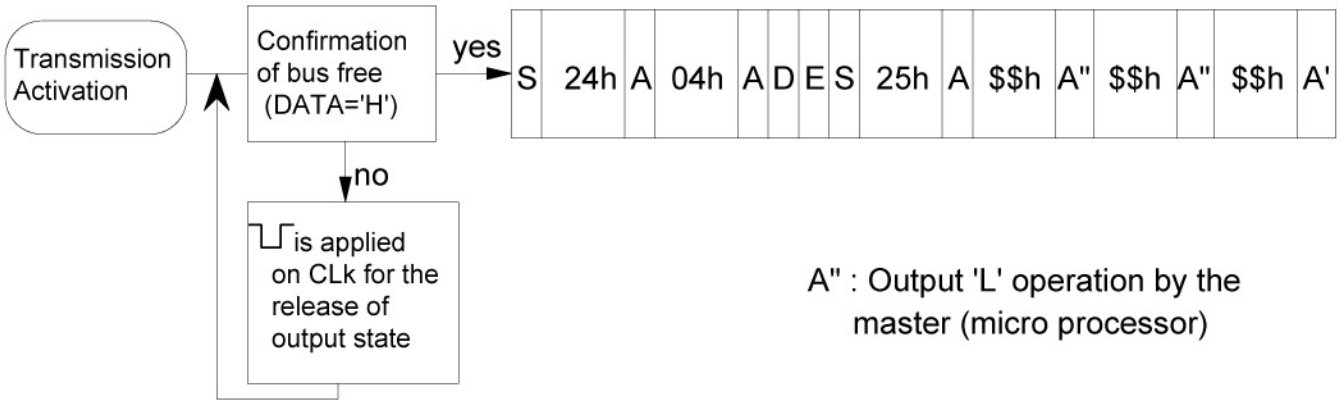
(2) The writing operation of the setting data (FFh, 80h, EEh) into M65664FP internal address of 04h ~ 06h



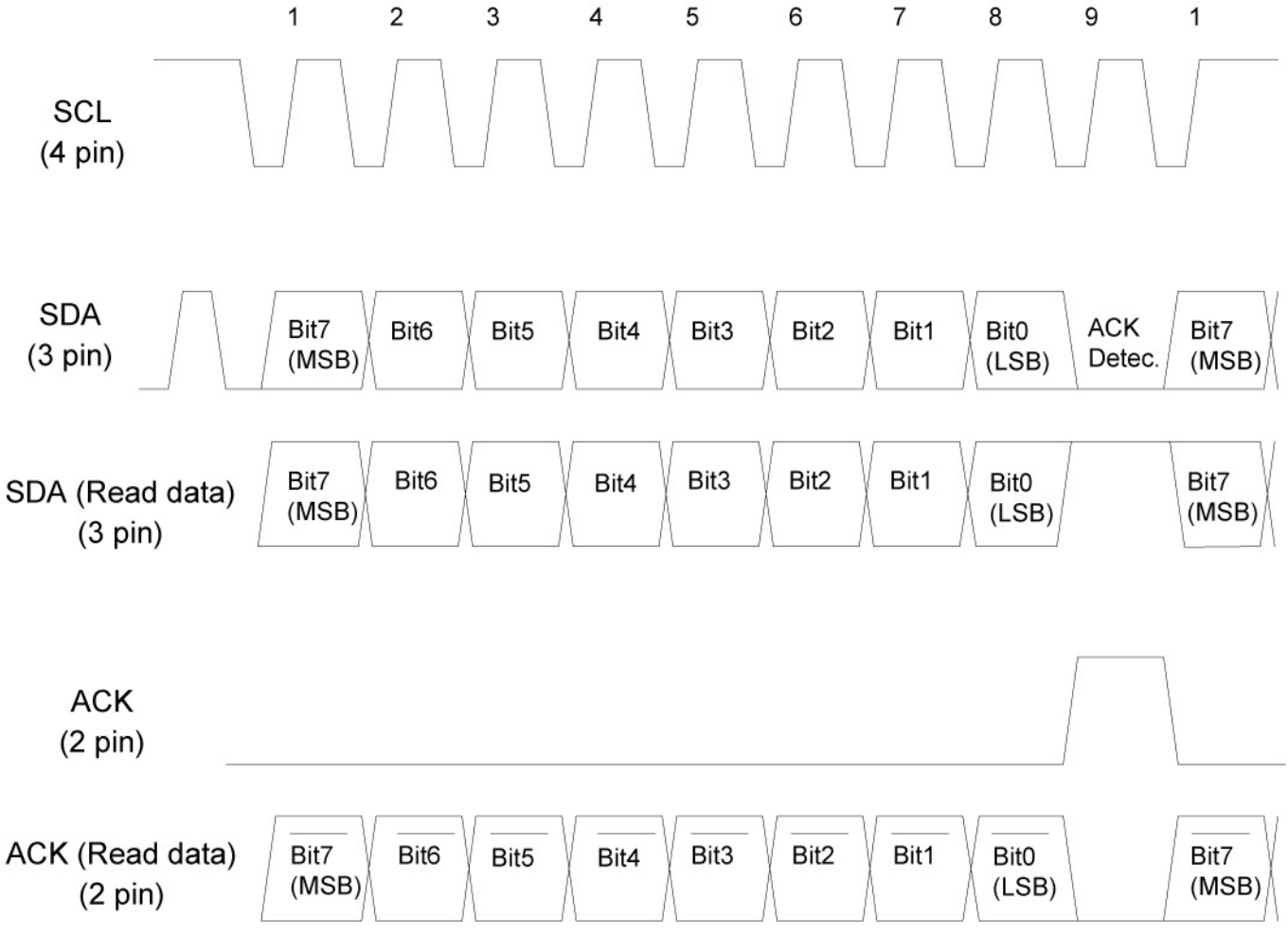
(3) The reading operation of the setting data from M65664FP internal address of 00h



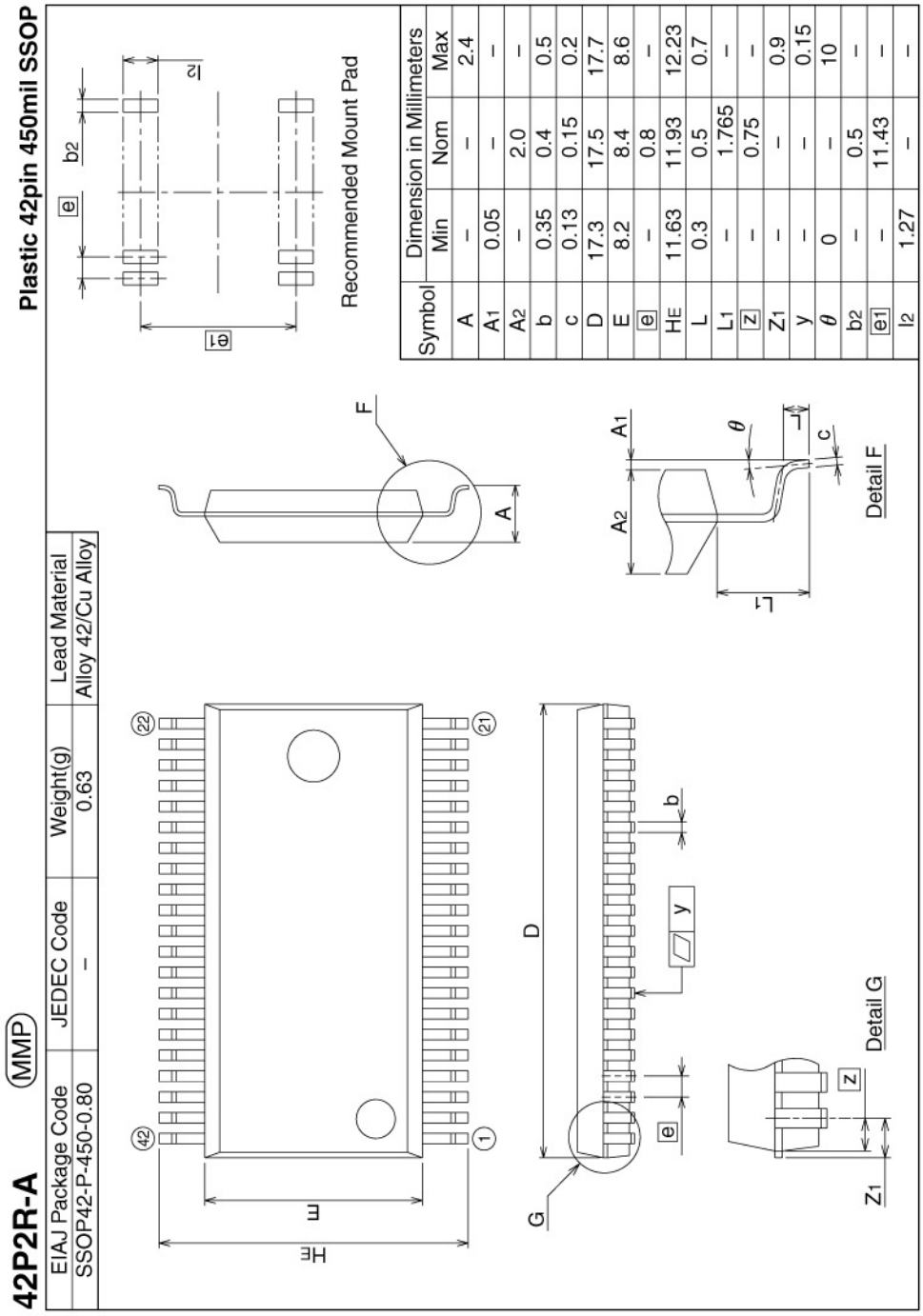
(4) The reading operation of the setting data from M65664FP internal address of 04h ~ 06h



<Timing Diagram>



DETAILED DIAGRAM OF PACKAGE OUTLINE



Keep safety first in your circuit designs!

●Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

●These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.
●Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
●All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (http://www.mitsubishichips.com).
●When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
●Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
●The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.
●If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
●Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.