MN673273

Signal-Processing LSI for Multimedia Camera

■ Overview

The MN673273 is a signal processing LSI for digital cameras inputting to computer. In addition to the basic functions of luminance signal and chrominance signal processing, the MN673273 integrates microcontroller functions (ALC, AWB, and AGC), SSG, and CG on a single chip.

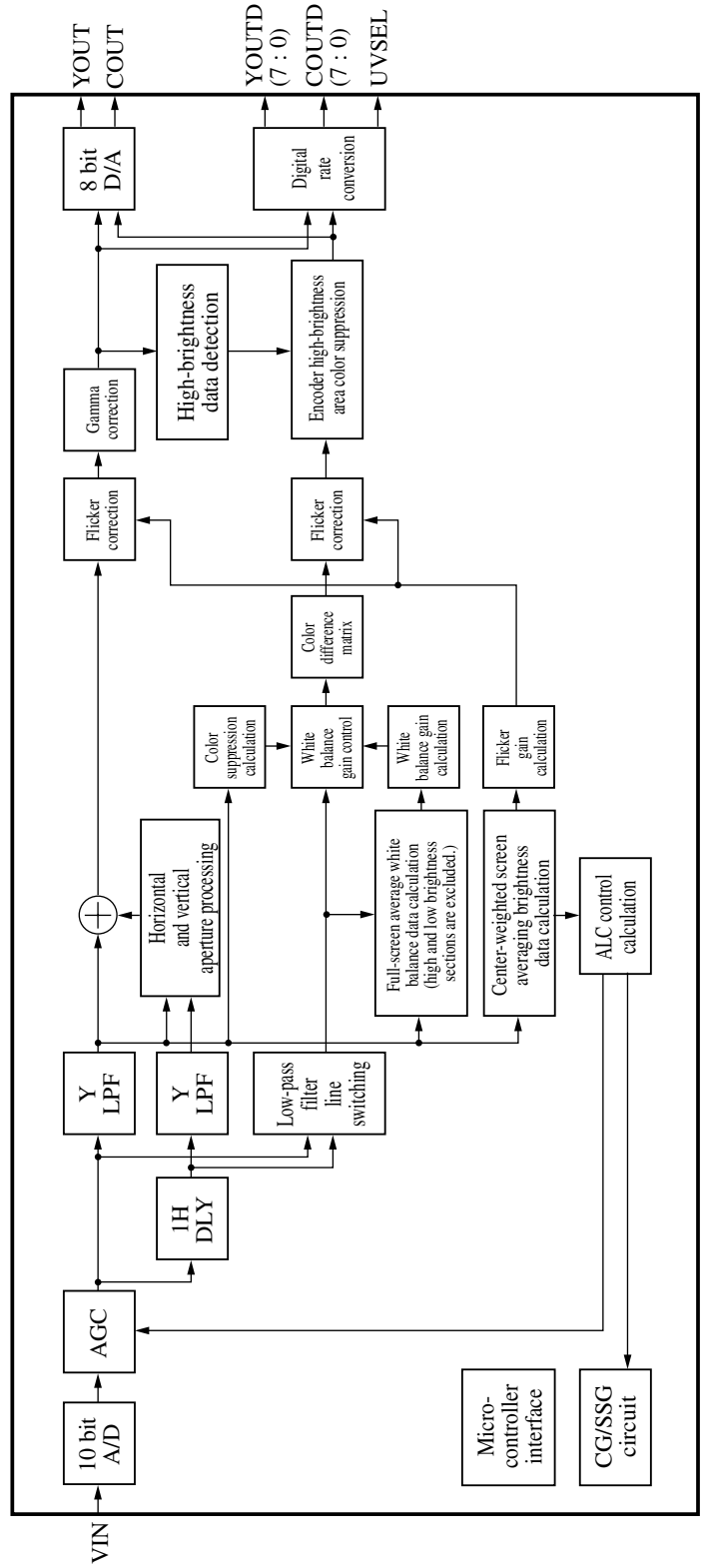
■ Features

- Input: Analog signal (A/D converter input)
- Outputs: Digital outputs
  - 8-bit Y signal
  - 8-bit C signal
  - Analog outputs
  - Y signal
  - C signal
- Operating supply voltage: 3.3 V ±0.3 V
- Operating clock frequency: 9.5 to 20 MHz
- Main functions
  - — 10-bit A/D converter
  - — Two-channel 8-bit D/A converter
  - — Analog Y and C outputs
  - — Digital Y and C outputs
  - — ALC (supports both electronic and mechanical iris), AWB, AGC. Can be used with either a hardware control system or a microcontroller based control system.
  - — 50 Hz fluorescent lamp flicker correction
  - — Supports analog AGC (AN2108)
  - — On-chip CG and SSG
  - — Supports both 510 and 360 horizontal lines (However, 360 horizontal line output is only provided for the digital outputs.)
  - — Supports pseudo-VGA (digital rate conversion)
  - — Supports both NTSC and PAL

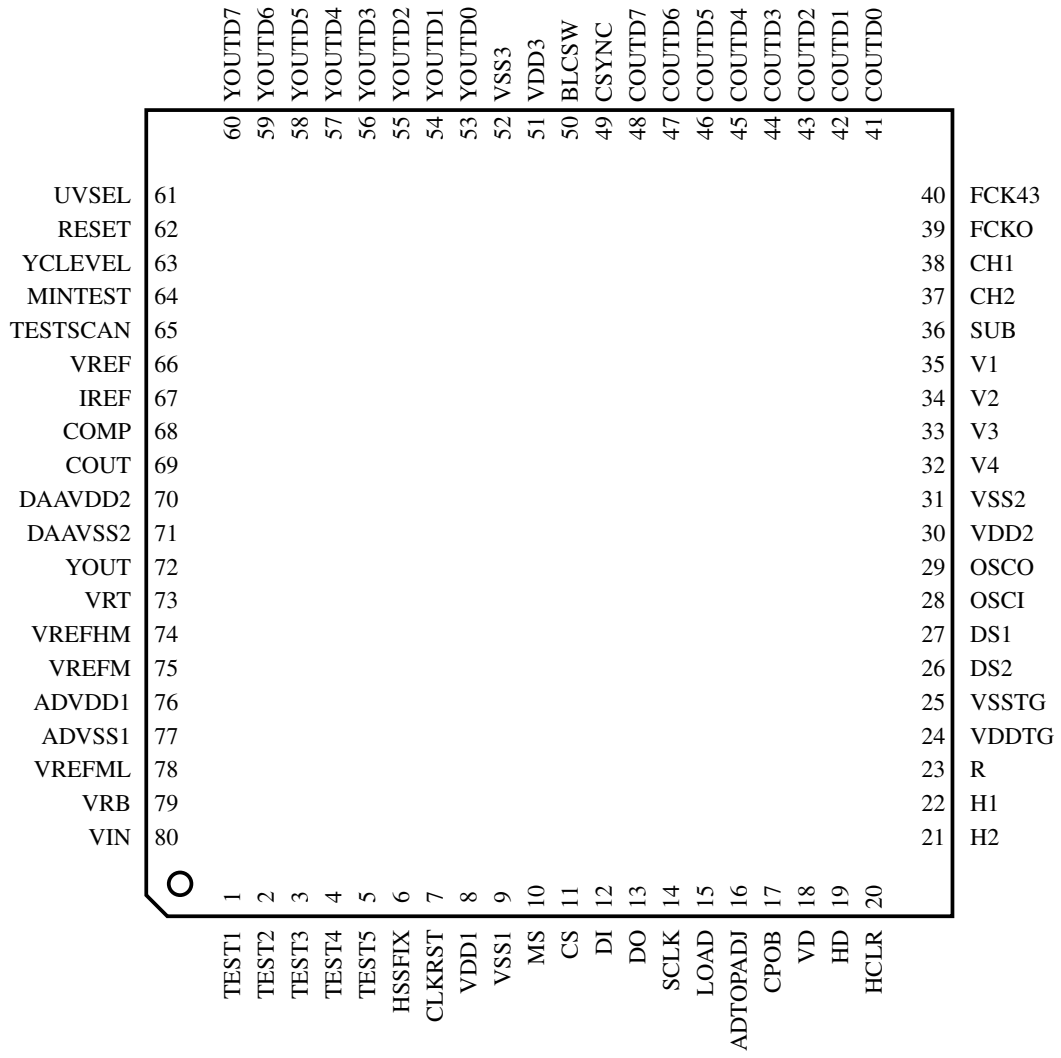
■ Applications

- PC cameras, multimedia cameras

■ Block Diagram



■ Pin Arrangement



(TOP VIEW)

■ Pin Descriptions

Pin No.	Pin Name	I/O	CLOCK	Function
1	TEST1	I		Test pin (Must be hold low during normal operation.)
2	TEST2	I		Test pin (Must be hold low during normal operation.)
3	TEST3	I		Test pin (Must be hold low during normal operation.)
4	TEST4	I		Test pin (Must be hold low during normal operation.)
5	TEST5	I		Test pin (Must be hold low during normal operation.)
6	HSSFIX	I		Shutter lock (1: On, 0: Off)/Flicker correction (1: Off, 0: On)/ External synchronization input
7	CLKRST	I		Clock reset
8	VDD1	VDD		Digital system power supply (3.3 V)
9	VSS1	VSS		Digital system ground
10	MS	I		Master/slave switching
11	CS	I/O	FCK	EPROM chip select
12	DI	I/O	FCK	Serial data input and output
13	DO	I		Serial data input
14	SCLK	I/O	FCK	Serial clock input and output
15	LOAD	O	FCK	Load pulse for AN2108/Analog AGC control signal (PWM)
16	ADTOPADJ	O	FCK	A/D converter input clamp voltage adjustment (PWM)
17	CPOB	O	FCK	A/D converter input clamp pulse or D/A converter output clamp pulse (CP2)
18	VD	O	FCK, 4/3FCK	Vertical drive signal/External synchronization VP
19	HD	O	FCK, 4/3FCK	Horizontal drive signal
20	HCLR	O	FCK, 4/3FCK	Horizontal reference signal/External synchronization output
21	H2	O		ϕH2 transfer pulse
22	HI	O		ϕH1 transfer pulse
23	R	O		ϕR pulse
24	VDDTG	VDD		ϕH power supply (3.3 V)
25	VSSTG	VSS		ϕH ground
26	DS2	O		CDS pulse 2
27	DS1	O		CDS pulse 1
28	OSCI	I		Oscillator input (2FCK)
29	OSCO	O		Oscillator output (2FCK)
30	VDD2	VDD		Digital system power supply (3.3 V)
31	VSS2	VSS		Digital system ground
32	V4	O	FCK	ϕV4 charge pulse
33	V3	O	FCK	ϕV3 charge pulse
34	V2	O	FCK	ϕV2 charge pulse
35	V1	O	FCK	ϕV1 charge pulse
36	SUB	O	FCK	Vertical exclusion pulse

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	CLOCK	Function
37	CH2	O	FCK	V3 charge pulse
38	CH1	O	FCK	V1 charge pulse
39	FCKO	O		FCK output
40	FCK43	O		4/3 FCK output
41	COUTD0	O	FCK, 4/3FCK	Digital chrominance-signal output (LSB)
42	COUTD1	O	FCK, 4/3FCK	Digital chrominance-signal output
43	COUTD2	O	FCK, 4/3FCK	Digital chrominance-signal output
44	COUTD3	O	FCK, 4/3FCK	Digital chrominance-signal output
45	COUTD4	O	FCK, 4/3FCK	Digital chrominance-signal output
46	COUTD5	O	FCK, 4/3FCK	Digital chrominance-signal output
47	COUTD6	O	FCK, 4/3FCK	Digital chrominance-signal output
48	COUTD7	O	FCK, 4/3FCK	Digital chrominance-signal output (MSB)
49	CSYNC	O	FCK, 4/3FCK	Composite sync output
50	BLCSW	I	FCK, 4/3FCK	Backlighting correction switching (1: On, 0: Off)
51	VDD3	VDD		Digital system power supply (3.3 V)
52	VSS3	VSS		Digital system ground
53	YOUTD0	O	FCK, 4/3FCK	Digital luminance-signal output (LSB)
54	YOUTD1	O	FCK, 4/3FCK	Digital luminance-signal output
55	YOUTD2	O	FCK, 4/3FCK	Digital luminance-signal output
56	YOUTD3	O	FCK, 4/3FCK	Digital luminance-signal output
57	YOUTD4	O	FCK, 4/3FCK	Digital luminance-signal output
58	YOUTD5	O	FCK, 4/3FCK	Digital luminance-signal output
59	YOUTD6	O	FCK, 4/3FCK	Digital luminance-signal output
60	YOUTD7	O	FCK, 4/3FCK	Digital luminance-signal output (MSB)
61	UVSEL	O	FCK, 4/3FCK	Color difference discrimination signal (High: R-Y, Low: B-Y)
62	RESET	I	FCK	Power on reset
63	YCLEVEL	O	FCK	D/A converter reference adjustment voltage
64	MINTEST	I		Test pin (Must be hold low during normal operation.)
65	TESTSCAN	I		Test pin (Must be hold low during normal operation.)
66	VREF	I		D/A converter reference voltage input
67	IREF	I		D/A converter bias current setting
68	COMP	I		D/A converter phase compensation capacitor connection
69	COUT	O		Clock signal output
70	DAAVDD2	AVDD		D/A converter power supply
71	DAAVSS2	AVSS		D/A converter ground
72	YOUT	O		Luminance signal output
73	VRT	I		A/D converter high-level reference voltage input

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	CLOCK	Function
74	VREFHM	I		A/D converter intermediate reference voltage
75	VREFM	I		A/D converter intermediate reference voltage
76	ADVDD1	AVDD		A/D converter power supply
77	ADVSS1	AVSS		A/D converter ground
78	VREFML	I		A/D converter intermediate reference voltage
79	VRB	I		A/D converter low-level reference voltage input
80	VIN	I		A/D converter input signal

■ Shared Function Pins

Pin No.	Pin Name	I/O	Function	Switch settings
6	HSSFIX	I	HSSFIX: Electronic shutter speed lock (1: On, 0: Off)	WE34 upper (1) = 0 and WE04 upper (2) = 0
			FLICOFF: Flicker correction (1: Off, 0: On)	WE34 upper (1) = 0 and WE04 upper (2) = 1
			VRSTI: External synchronization vertical reset pulse	WE34 upper (1) = 1
15	LOAD	O	LOAD: AN2108 load pulse	WE3D upper (3) = 0
			ANAGC: Analog AGC control signal	WE3D upper (3) = 1
17	CPOB	O	CPOB: A/D converter input signal clamp pulse	WE3C upper (3) = 0
			CP2: D/A converter output clamp pulse	WE3C upper (3) = 1
18	VD	O	VD: Vertical drive signal	WE34 upper (1) = 0 and WE11 upper (6) = 0
			VP: External synchronization VP signal	WE34 upper (1) = 0 and WE11 upper (6) = 0
20	HCLR	O	HCLR: Horizontal reference signal	WE34 upper (1) = 0
			VRSTM: External synchronization vertical reset mask signal	WE34 upper (1) = 0 and WE34 upper (6) = 0

■ Electrical Characteristics

1. Absoluste Maximum Ratings

Parameter		Symbol	Rating	Unit
Supply voltage(digital)		V_{DD}	− 0.3 to +4.6	V
Supply voltage(analog)		AV_{DD}	− 0.3 to +4.6	V
Input voltage		V_I	− 0.3 to V_{DD}+0.3	V
Output voltage		V_O	− 0.3 to V_{DD}+0.3	V
Average output voltages	1 mA cell	I_O	±3	mA
	2 mA cell		±6	
	4 mA cell		±12	
	16 mA cell		±48	
Operating temperature		T_{opr}	−20 to +85	°C
Storage temperature		T_{stg}	−55 to +150	°C

Notes: 1. The absolute maximum ratings are limiting values under which the chip will not be destroyed. Operation is not guaranteed within these ranges.

2. The VDD1, VDD2, VDD3, VDDTG, ADVDD1, and DAAVDD2 pins must always be held at the same voltage. The VSS1, VSS2, VSS3, VSSTG, ADVSS1, and DAAVSS2 pins must always be held at the same voltage.

2. Operating Conditions $V_{SS} = AV_{SS} = 0$ V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage(digital)	V_{DD}	Digital system power supply	3.0	3.3	3.6	V
Supply voltage(analog)	AV_{DD}	A/D and D/A converter power supply	3.0	3.3	3.6	V
Supply voltage(R, H1, H2)	V_{DDH}	Drive power supply for the R, H1, and H2 output pins	3.0	3.3	3.6	V
Operating frequency	f_{CLK}	duty 50 %	9.5	—	20.0	MHz

3. DC Characteristics

V_{DDH} = 3.0 V to 3.6 V, $V_{DD} = AV_{DD}$ = 3.0 V to 3.6 V, $V_{SS} = AV_{SS}$ = 0 V, T_a = −20 °C to +85 °C

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Operating supply current		I_{DD}	$V_{DD} = AV_{DD} = V_{DDH}$ = 3.6 V, f_{CLK} = 20.0 MHz, T_a = 25 °C	—	100	180	mA
Input pins1-1 TEST5, CLKRST, BLCSW, RESET, MINTEST, TESTSCAN							
Input voltage	High-level	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
	Low-level	V_{IL}		0	—	$V_{DD} \times 0.2$	
Input leakage current		I_{LI}	$V_I = V_{DD}$ or V_{SS}	−5	—	5	µA
Input pins1-2 Pull-down Input pins TEST1 to TEST4, HSSFIX, MS, DO							
Input voltage	High-level	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
	Low-level	V_{IL}		0	—	$V_{DD} \times 0.2$	
Input leakage current		I_{LIPD}	$V_I = V_{SS}$	−10	—	10	µA
Pull-down resistor		R_{PD}	$V_I = V_{DD}$	10	30	90	kΩ

■ Electrical Characteristics (continued)

3. DC Characteristics (continued)

at V_{DDH} = 3.0 V to 3.6 V, V_{DD} = AV_{DD} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 °C to +85 °C

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Output pins1-1 LOAD, ADTOPADJ, CPOB, HCLR, YOUTD0 to YOUTD7, UVSEL, YCLEVEL							
Output voltage	High-level	V_{OH}	I_O = –1 mA	V_{DD} – 0.6	—	—	V
	Low-level	V_{OL}	I_O = 1 mA	—	—	0.4	
Output pins1-2 V4 to V1, SUB, CH2, CH1, COUTD0 to COUTD7, CSYNC							
Output voltage	High-level	V_{OH}	I_O = –2 mA	V_{DD} – 0.6	—	—	V
	Low-level	V_{OL}	I_O = 2 mA	—	—	0.4	
Output pins1-3 VD, HD, DS2, DS1, FCKO, FCK43							
Output voltage	High-level	V_{OH}	I_O = –4 mA	V_{DD} – 0.6	—	—	V
	Low-level	V_{OL}	I_O = 4 mA	—	—	0.4	
Output pins1-4 H2, H1, R							
Output voltage	High-level	V_{OH}	I_O = –16 mA	V_{DD} – 0.6	—	—	V
	Low-level	V_{OL}	I_O = 16 mA	—	—	0.4	
I/O pins 1: CS, DI, and SCLK							
Input/Output voltage	High-level	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
	Low-level	V_{IL}		0	—	$V_{DD} \times 0.2$	
Output voltage	High-level	V_{OH}	I_O = –4 mA	V_{DD} – 0.6	—	—	V
	Low-level	V_{OL}	I_O = 4 mA	—	—	0.4	
Output leakage current		I_{LO}	$V_O = V_{DD}$ or V_{SS}	–5	—	5	µA
Oscillator pins 1: OSCI and OSCO							
Standard oscillator frequency		f_{OSC}	V_{DD} = 3.3 V, Xtal	9.5	—	20.0	MHz
Internal feedback resistors		R_{FB}	V_{DD} = 3.3 V $V_I(X_I) = V_{DD}$ or V_{SS}	313	940	2820	kΩ
Output voltage	High-level	I_{OH}	V_{DD} = 3.3 V $V_I = V_{SS}$, $V_O = V_{SS}$	–11.5	–4.6	–1.84	mA
	Low-level	I_{OL}	V_{DD} = 3.3 V $V_I = V_{DD}$, $V_O = V_{DD}$	1.92	4.8	12	

■ Electrical Characteristics (continued)

4. AC Characteristics

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input pins2-1 OSCI							
Clock waveform	Period	tcyc	See figure 1	50.0	—	105.3	ns
	Clock duty	dclk	See figure 1 dclk = thi/tcyc	48	50	52	%
Input pins2-2 HSSFIX, MS, DO, BLCSW							
Input timing	Setup	tsu	See figure 1	10	—	—	ns
	Hold	thd	See figure 1	15	—	—	
Output pins2 LOAD, ADTOPADJ, CPOB, VD, HD, HCLR, H2, H1, R, DS2, DS1, V4 to V1, SUB, CH2, CH1, FCKO, FCK43, COUTD0 to COUTD7, CSYNC, YOUTD0 to YOUTD7, UVSEL, and YCLEVEL							
Output timing	Delay	tod	Load: 60 pF, output level: 50% See figure 1	—	—	45	ns

5. A/D converter at V_{DD} = AV_{DD} = 3.3 V, V_{SS} = AV_{SS} = 0 V, T_a = +25 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Recommended A/D converter operating conditions VIN, VRT, VRB						
Analog input voltage	V_{AIN}	VIN	VRB	—	VRT	V
Analog input pin capacitance	C_{AI}	VIN	—	15	—	pF
High-level reference voltage	V_{RT}	VRT	—	2.5	—	V
Low-level reference voltage	V_{RB}	VRB	—	0.5	—	V
Reference resistance (VRB−VRT)	R_{REF}		—	440	—	Ω
A/D Converter Characteristics						
Resolution	R_{ES}		—	—	10	Bit
Nonlinearity error	E_L	f_{CLK} = 9.5 MHz, VRT = 2.5 V VRB = 0.5 V, C_{VREFM} = C_{VREFHM} = C_{VREFML} = 10 µF	—	±5.0	±7.5	LSB
Differential nonlinearity error	E_D		—	±2.0	±6.5	
Analog input dynamic range	D_R				VRT−VRB	V[P-P]

■ Electrical Characteristics (continued)

6. Converter at V_{DD} = AV_{DD} = 3.3 V, V_{SS} = AV_{SS} = 0 V, T_a = +25 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Recommended D/A converter operating conditions VREF, IREF, COMP, YOUT, COUT						
Reference voltage	VREF		—	1.38	—	V
External phase compensation capacitor	C_{COMP}	Inserted between the COMP pin and AV_{DD}	—	1.0	—	µF
External output resistor	R_L	Inserted between AVSS and the YOUT and COUT pins, respectively	—	200	—	Ω
External bias current setting resistor	R_{IREF}	Inserted between the IREF pin and AV_{SS}	—	2.2	—	kΩ
D/A Converter Characteristics						
Resolution	R_{ES}		—	—	8	Bit
Nonlinearity error	E_L	f_{CLK} = 20.0 MHz, V_{DD} = 3.3 V	—	—	±2.0	LSB
Differential nonlinearity error	E_D	R_L = 200 Ω, R_{IREF} = 2.2 kΩ, VREF = 1.38 V, C_{COMP} = 1.0 µF	—	—	±2.0	
Full-scale voltage	V_{OFS}		—	1.0	—	V
Zero-scale voltage	V_{OZS}		—	0	—	V

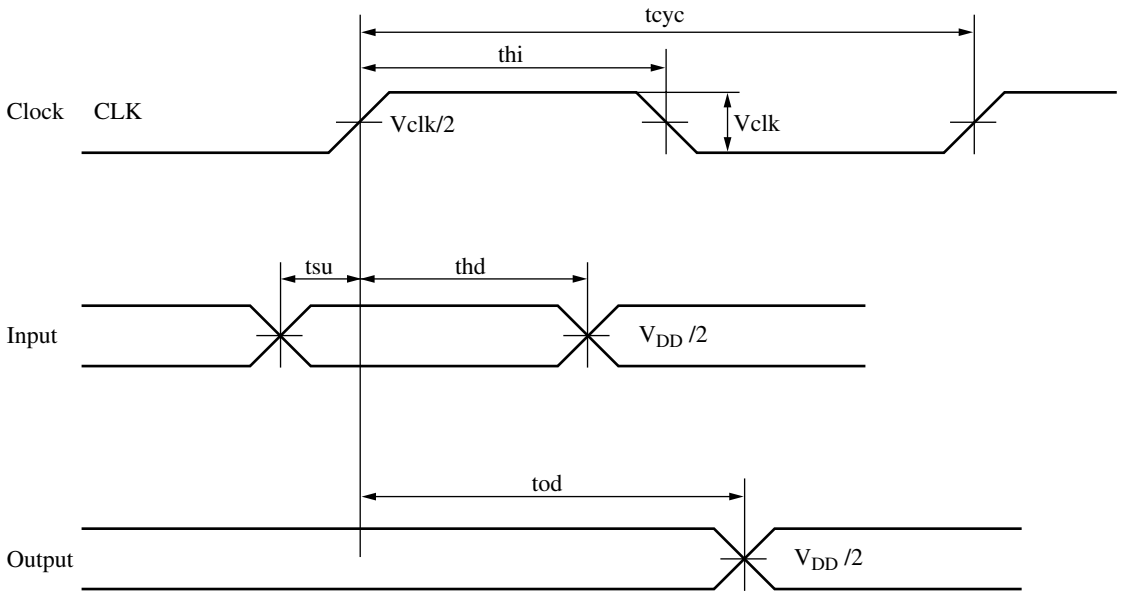
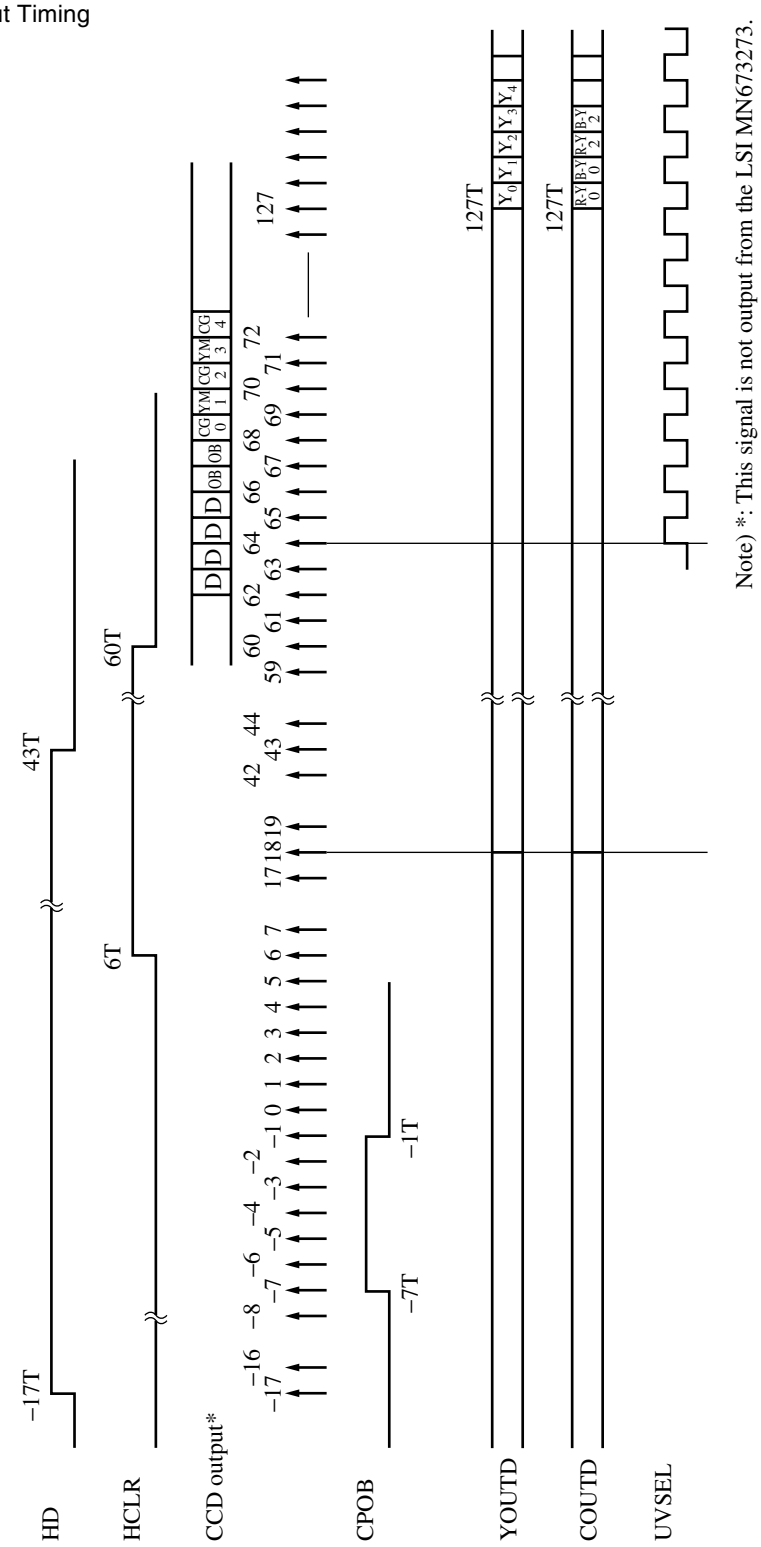


Figure 1. Input and Output Timing

■ Timing Charts

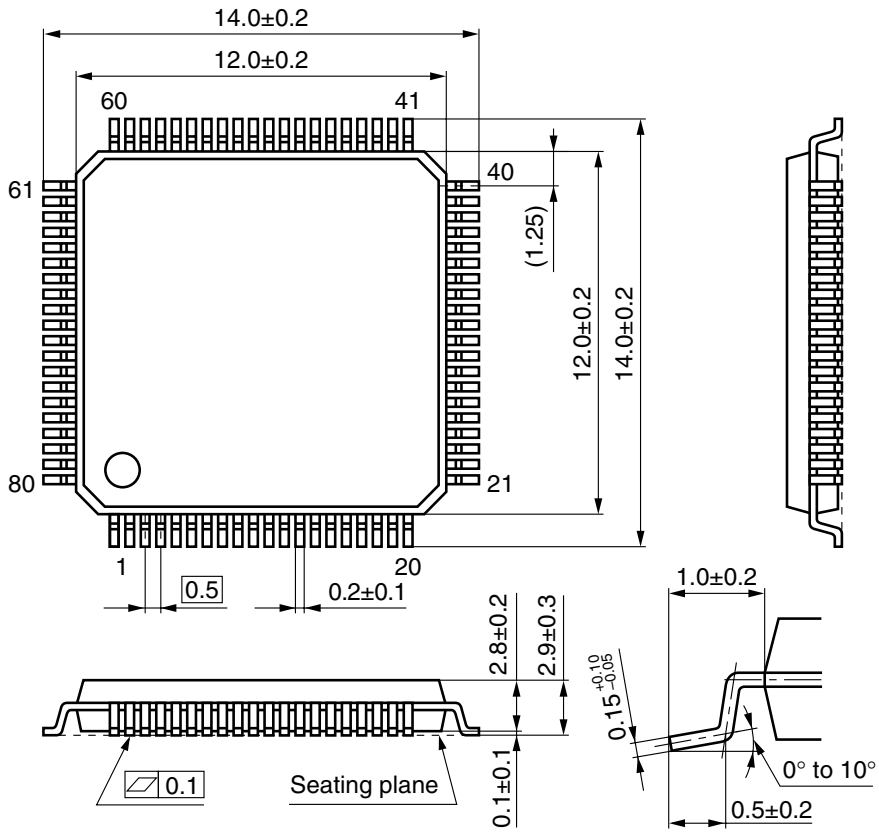
• Input and Output Timing



Note) *: This signal is not output from the LSI MN673273.

■ Package Dimensions (Units: mm)

• QFH080-P-1212



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