DAC8812 Dual, Serial-Input 16-Bit Multiplying Digital-to-Analog Converter

1 Features

- Relative Accuracy: 1 LSB Max
- Differential Nonlinearity: 1 LSB Max
- 2-mA Full-Scale Current ±20%, With V_{REF} = ±10 V
- 0.5-µs Settling Time
- Midscale or Zero-Scale Reset
- Separate 4Q Multiplying Reference Inputs
- Reference Bandwidth: 10 MHz
- Reference Dynamics: –105-dB THD
- SPI™-Compatible 3-Wire Interface: 50 MHz
- Double Buffered Registers to Enable Simultaneous Multichannel Update
- Internal Power-On Reset
- Industry-Standard Pin Configuration

2 Applications

- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration

3 Description

The DAC8812 is a dual, 16-bit, current-output digital-to-analog converter (DAC) designed to operate from a single 2.7-V to 5.5-V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A double-buffered, serial data interface offers high-speed, 3-wire, SPI and microcontroller compatible inputs using serial data in (SDI), clock (CLK), and a chip-select ($\overline{CS}$). A common level-sensitive load DAC strobe ($\overline{LDAC}$) input allows simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power-on reset forces the output voltage to zero at system turnon. An MSB pin allows system reset assertion ($\overline{RS}$) to force all registers to zero code when MSB = 0, or to half-scale code when MSB = 1.

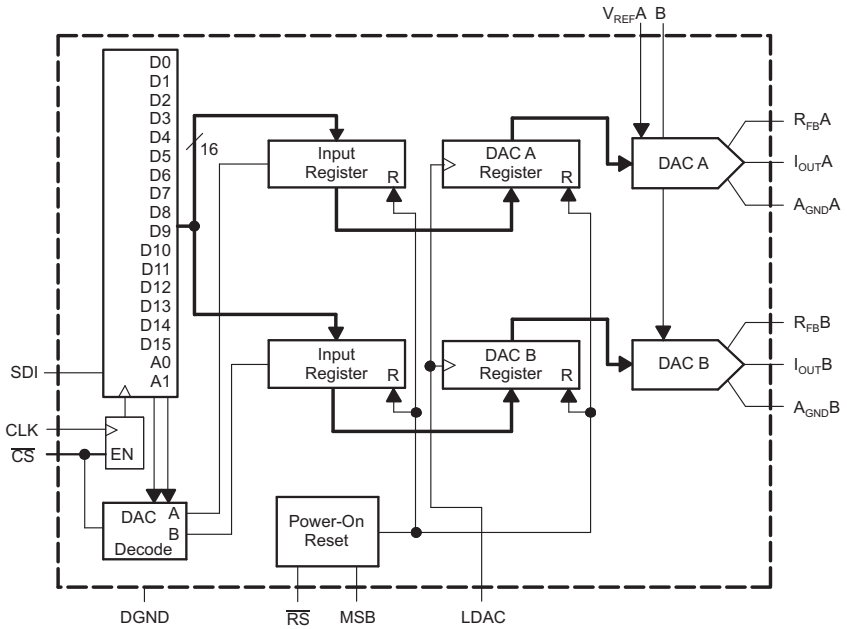
The DAC8812 is available in a TSSOP-16 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8812	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Timing Requirements ... 6
7.7 Switching Characteristics ... 6
7.8 Typical Characteristics ... 8
8 Detailed Description ... 13
8.1 Overview ... 13
8.2 Functional Block Diagram ... 13
8.3 Feature Description ... 13
8.4 Device Functional Modes ... 15
9 Application and Implementation ... 18
9.1 Application Information ... 18
9.2 Typical Application ... 18
10 Power Supply Recommendations ... 19
11 Layout ... 20
11.1 Layout Guidelines ... 20
11.2 Layout Example ... 21
12 Device and Documentation Support ... 22
12.1 Documentation Support ... 22
12.2 Community Resources ... 22
12.3 Trademarks ... 22
12.4 Electrostatic Discharge Caution ... 22
12.5 Glossary ... 22
13 Mechanical, Packaging, and Orderable Information ... 22

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2015) to Revision D	Page
• Changed the *DAC8812 Timing Diagram* image to show the setup and hold time with respect to rising edge	7

Changes from Revision B (February 2007) to Revision C	Page
• Added ESD Ratings table, Timing Requirements and Switching Characteristics tables, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
• Replaced Package/Ordering Information table with Device Comparison table	3
• Added I/O column to Pin Functions table	3

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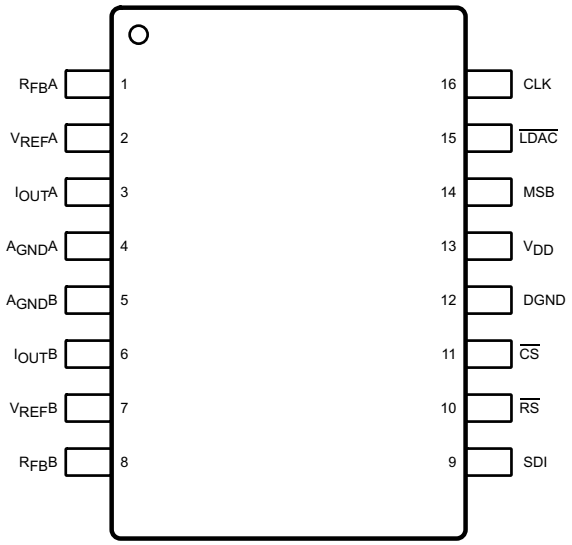
5 Device Comparison Table

DEVICE	MAXIMUM RELATIVE ACCURACY (LSB)
DAC8812C	±1
DAC8812B	±2

6 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$R_{FB}A$	I	Establish voltage output for DAC A by connecting to external amplifier output.
2	$V_{REF}A$	I	DAC A reference voltage input pin. Establishes DAC A full-scale output voltage. Can be tied to V_{DD} pin.
3	$I_{OUT}A$	O	DAC A current output
4	$A_{GND}A$	—	DAC A analog ground
5	$A_{GND}B$	—	DAC B analog ground
6	$I_{OUT}B$	O	DAC B current output
7	$V_{REF}B$	I	DAC B reference voltage input pin. Establishes DAC B full-scale output voltage. Can be tied to V_{DD} pin.
8	$R_{FB}B$	I	Establish voltage output for DAC B by connecting to external amplifier output.
9	SDI	I	Serial data input; data loads directly into the shift register.
10	$\overline{RS}$	I	Reset pin; active-low input. Input registers and DAC registers are set to all 0s or midscale. Register data = 0x0000 when MSB = 0. Register data = 0x8000 when MSB = 1 for DAC8812.
11	$\overline{CS}$	I	Chip-select; active-low input. Disables shift register loading when high. Transfers serial register data to input register when $\overline{CS}$ goes high. Does not affect $\overline{LDAC}$ operation.
12	DGND	—	Digital ground
14	MSB	I	MSB bit sets output to either 0 or midscale during a RESET pulse ($\overline{RS}$) or at system power-on. Output equals zero scale when MSB = 0 and midscale when MSB = 1. MSB pin can be permanently tied to ground or V_{DD}.
13	V_{DD}	I	Positive power-supply input. Specified range of operation 2.7 V to 5.5 V.
15	$\overline{LDAC}$	I	Load DAC register strobe; level-sensitive active-low. Transfers all input register data to the DAC registers. Asynchronous active-low input. See Table 2 for operation.
16	CLK	I	Clock input. Positive edge clocks data into shift register.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
V_{DD} to GND	–0.3	7	V
$V_{REF}x$, $R_{FB}x$ to GND	–18	18	V
Digital logic inputs to GND	–0.3	V_{DD} + 0.3	V
$I_{OUT}x$ to GND	–0.3	V_{DD} + 0.3	V
$A_{GND}x$ to DGND	–0.3	0.3	V
Input current to any pin except supplies	–50	50	mA
Package power dissipation		(150°C – T_A) / $R_{\theta JA}$	W
Maximum junction temperature ($T_J$max)		150	°C
Operating temperature	–40	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage to GND	2.7		5.5	V
T_A	Operating ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		DAC8812 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V, $I_{OUT}X$ = Virtual GND, $A_{GND}X$ = 0 V, $V_{REF}A$, B = 10 V, T_A = full operating temperature range, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
	Resolution				16	Bits
INL	Relative accuracy	DAC8812B			±2	LSB
		DAC8812C			±1	
DNL	Differential nonlinearity				±1	LSB
$I_{OUT}X$	Output leakage current	Data = 0000h, T_A = 25°C			10	nA
		Data = 0000h, T_A = T_A max			20	
G_{FSE}	Full-scale gain error	Data = FFFFh		±0.75	±4	mV
TCV_{FS}	Full-scale temperature coefficient(2)			1		ppm/°C
$R_{FB}X$	Feedback resistor	V_{DD} = 5 V		5		kΩ
REFERENCE INPUT(2)						
$V_{REF}X$	$V_{REF}X$ range		–15		15	V
$R_{REF}X$	Input resistance		4	5	6	kΩ
	Input resistance match			1%		
$C_{REF}X$	Input capacitance			5		pF
ANALOG OUTPUT(2)						
$I_{OUT}X$	Output current	Data = FFFFh	1.6		2.5	mA
$C_{OUT}X$	Output capacitance	Code-dependent		50		pF
LOGIC INPUTS(2)						
V_{IL}	Input low voltage	V_{DD} = 2.7 V			0.6	V
		V_{DD} = 5 V			0.8	
V_{IH}	Input high voltage	V_{DD} = 2.7 V	2.1			V
		V_{DD} = 5 V	2.4			
I_{IL}	Input leakage current				1	µA
C_{IL}	Input capacitance				10	pF

(1) All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OPA277 I-to-V converter amplifier. The DAC8812 R_{FB} pin is tied to the amplifier output. Typical values represent average readings measured at 25°C.
(2) These parameters are not subject to production testing.

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Electrical Characteristics (continued)

V_{DD} = 2.7 V to 5.5 V, $I_{OUT}X$ = Virtual GND, $A_{GND}X$ = 0 V, $V_{REF}A$, B = 10 V, T_A = full operating temperature range, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
$V_{DD\ RANGE}$	Power supply range		2.7		5.5	V
I_{DD}	Positive supply current	Logic inputs = 0 V, V_{DD} = 4.5 V to 5.5 V		2	5	µA
		Logic inputs = 0 V, V_{DD} = 2.7 V to 3.6 V		1	2.5	µA
P_{DISS}	Power dissipation	Logic inputs = 0 V			0.0275	mW
P_{SS}	Power supply sensitivity	ΔV_{DD} = ±5%			0.006%	
AC CHARACTERISTICS(2) (3)						
t_s	Output voltage settling time	To ±0.1% of full-scale, Data = 0000h to FFFFh to 0000h		0.3		µs
		To ±0.0015% of full-scale, Data = 0000h to FFFFh to 0000h		0.5		
Q_G	DAC glitch impulse	$V_{REF}x$ = 10 V, data = 7FFFh to 8000h to 7FFFh		5		nV-s
BW –3 dB	Reference multiplying BW	$V_{REF}x$ = 100 mV_{RMS}, data = FFFFh, C_{FB} = 3 pF		10		MHz
	Feedthrough error	Data = 0000h, $V_{REF}x$ = 100 mV_{RMS}, f = 100 kHz		–70		dB
	Crosstalk error	Data = 0000h, $V_{REF}B$ = 100 mV_{RMS}, Adjacent channel, f = 100 kHz		–100		dB
Q_D	Digital feedthrough	$\overline{CS}$ = 1 and f_{CLK} = 1 MHz		1		nV-s
THD	Total harmonic distortion	V_{REF} = 5 V_{PP}, data = FFFFh, f = 1 kHz		–105		dB
e_n	Output spot noise voltage	f = 1 kHz, BW = 1 Hz		12		nV/√Hz

(3) All ac characteristic tests are performed in a closed-loop system using a THS4011 I-to-V converter amplifier.

7.6 Timing Requirements

See Figure 1

		MIN	NOM	MAX	UNIT
INTERFACE TIMING(1)					
t_{CH}	Clock duration, high	10			ns
t_{CL}	Clock duration, low	10			ns
t_{CSS}	$\overline{CS}$ to clock setup	0			ns
t_{CSH}	Clock to $\overline{CS}$ hold	10			ns
t_{LDAC}	Load DAC pulse duration	20			ns
t_{DS}	Data setup	10			ns
t_{DH}	Data hold	10			ns
t_{LDS}	Load setup	5			ns
t_{LDH}	Load hold	25			ns

(1) All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

7.7 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERFACE TIMING						
t_{PD}	Clock to SDO propagation delay		2		20	ns

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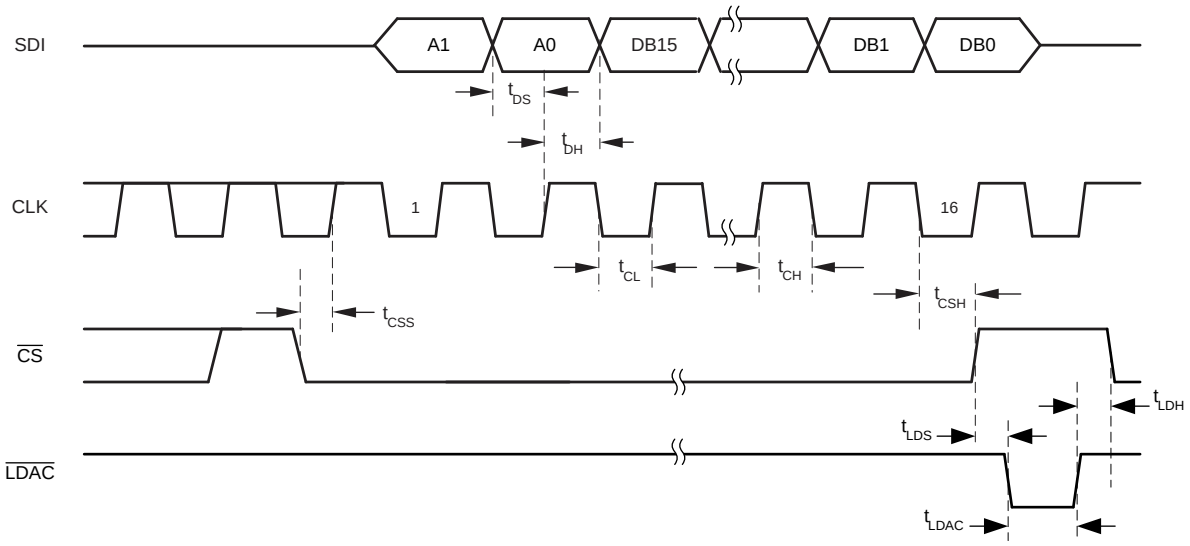

Figure 1. DAC8812 Timing Diagram

7.8 Typical Characteristics

7.8.1 Channel A—5 V

At T_A = 25°C, V_{DD} = 5 V, unless otherwise noted

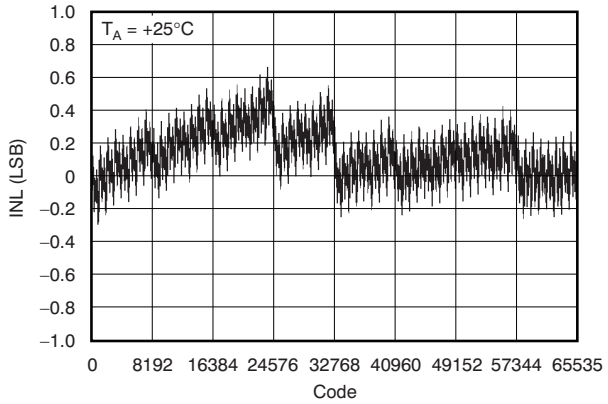

Figure 2. Integral Nonlinearity vs Digital Input Code

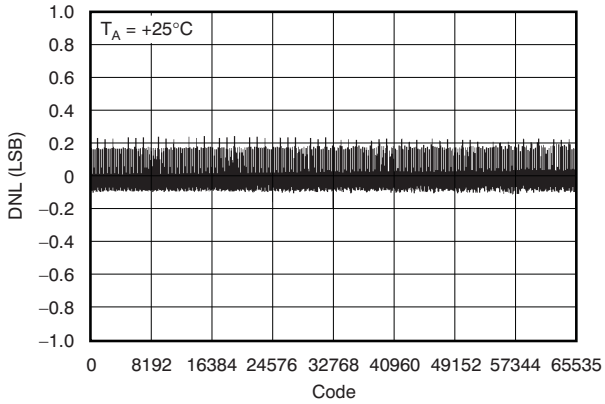

Figure 3. Differential Nonlinearity vs Digital Input Code

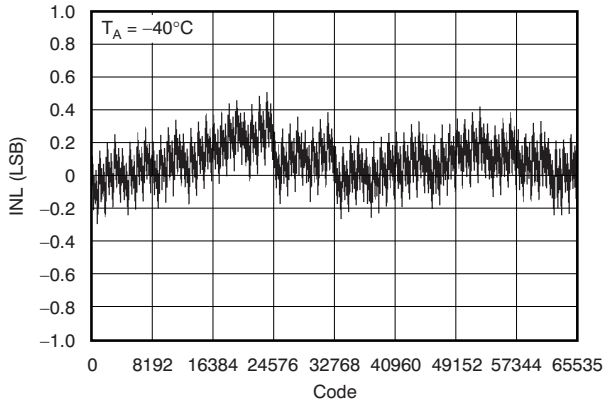

Figure 4. Integral Nonlinearity vs Digital Input Code

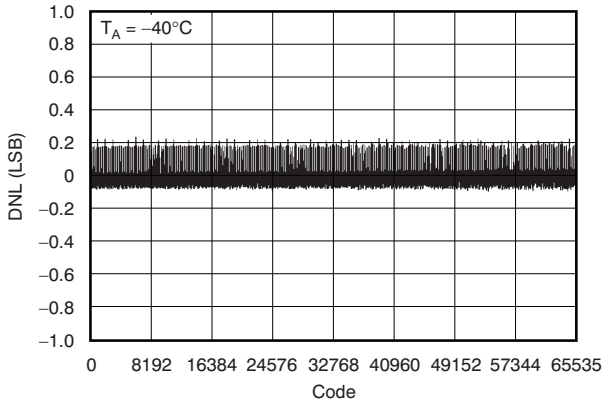

Figure 5. Differential Nonlinearity vs Digital Input Code

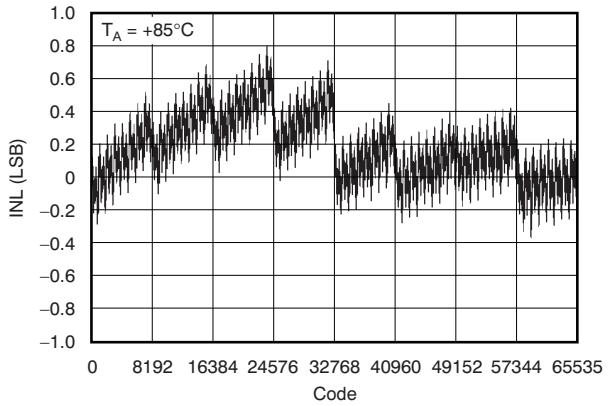

Figure 6. Integral Nonlinearity vs Digital Input Code

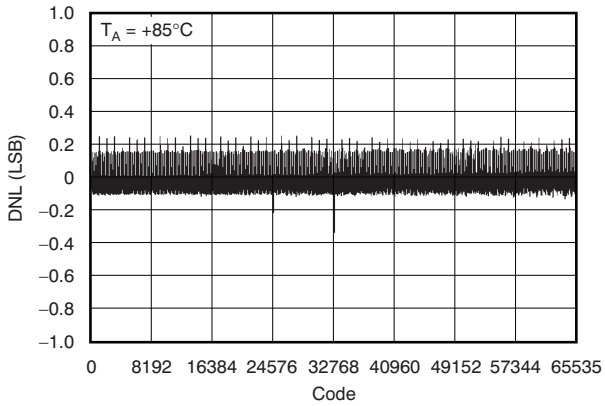

Figure 7. Differential Nonlinearity vs Digital Input Code

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7.8.2 Channel B—5 V

At T_A = 25°C, V_{DD} = 5 V, unless otherwise noted

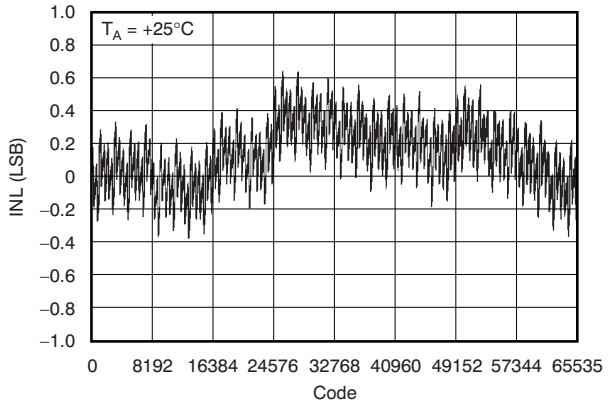

Figure 8. Integral Nonlinearity vs Digital Input Code

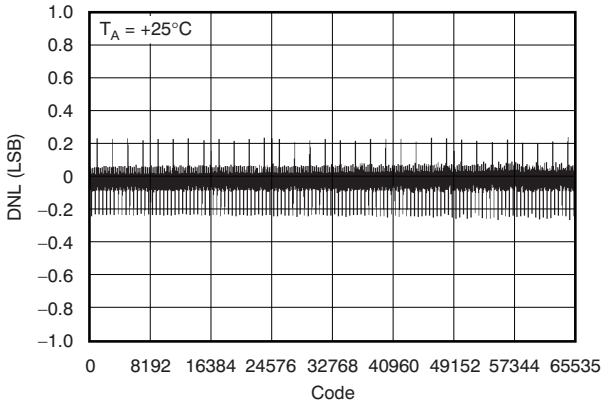

Figure 9. Differential Nonlinearity vs Digital Input Code

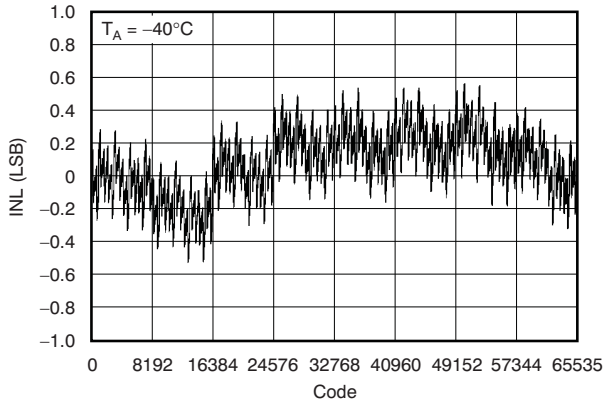

Figure 10. Integral Nonlinearity vs Digital Input Code

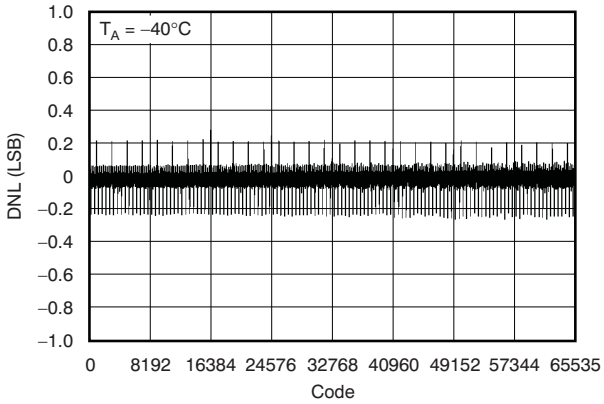

Figure 11. Differential Nonlinearity vs Digital Input Code

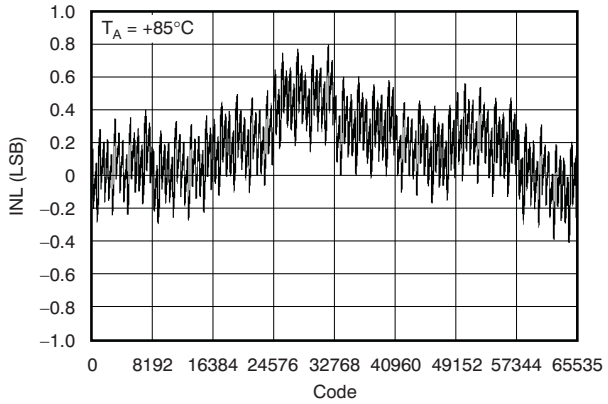

Figure 12. Integral Nonlinearity vs Digital Input Code

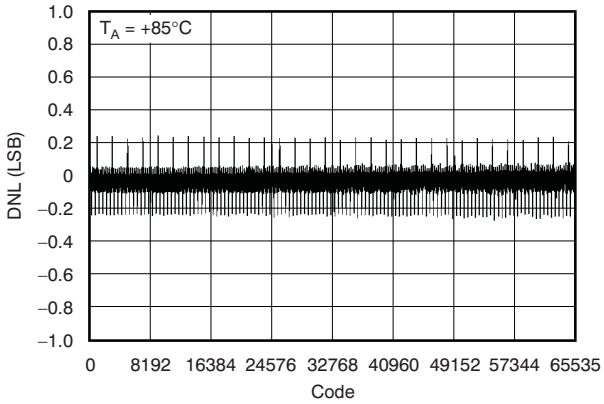

Figure 13. Differential Nonlinearity vs Digital Input Code

Channel B—5 V (continued)

At T_A = 25°C, V_{DD} = 5 V, unless otherwise noted

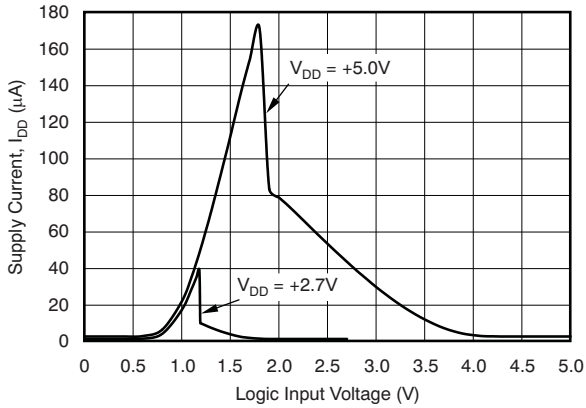

Figure 14. Supply Current vs Logic Input Voltage

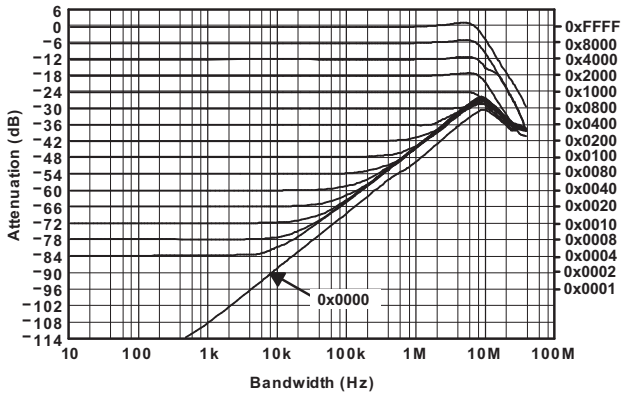

Figure 15. Reference Multiplying Bandwidth

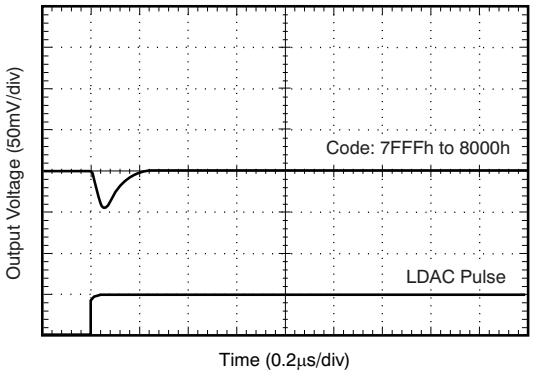

Figure 16. DAC Glitch

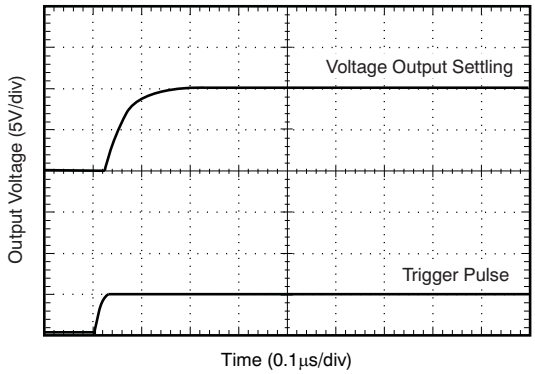

Figure 17. DAC Settling Time

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7.8.3 Channel A—2.7 V

At T_A = 25°C, V_{DD} = 2.7 V, unless otherwise noted

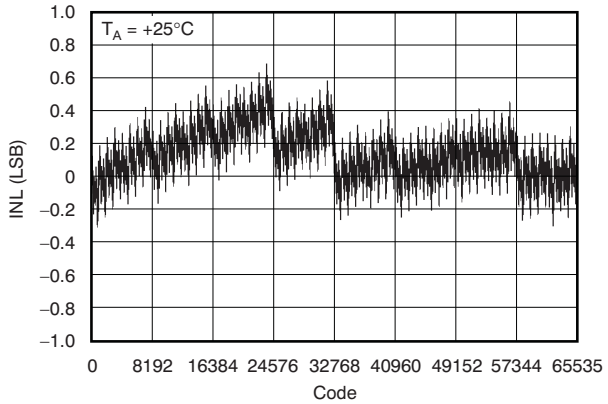

Figure 18. Integral Nonlinearity vs Digital Input Code

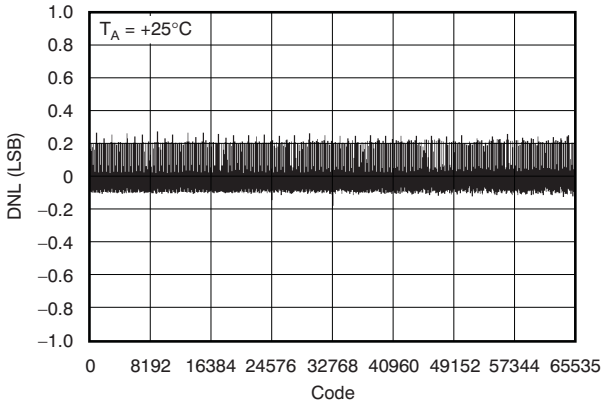

Figure 19. Differential Nonlinearity vs Digital Input Code

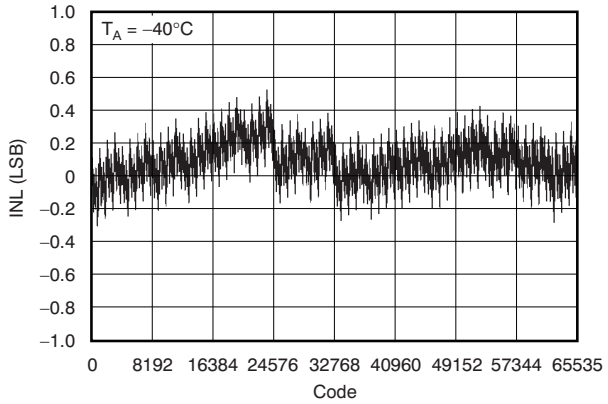

Figure 20. Integral Nonlinearity vs Digital Input Code

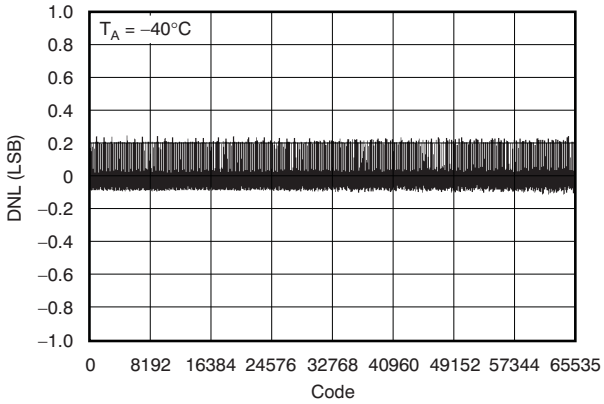

Figure 21. Differential Nonlinearity vs Digital Input Code

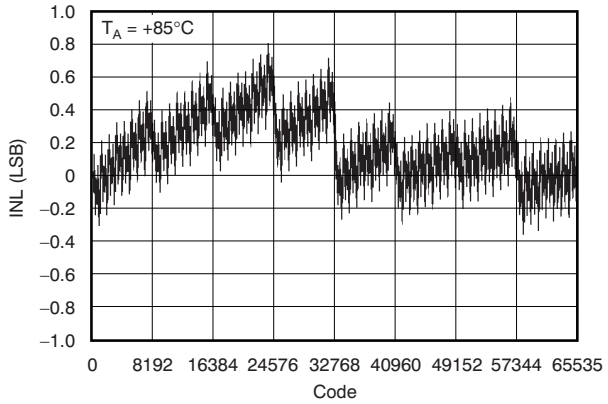

Figure 22. Integral Nonlinearity vs Digital Input Code

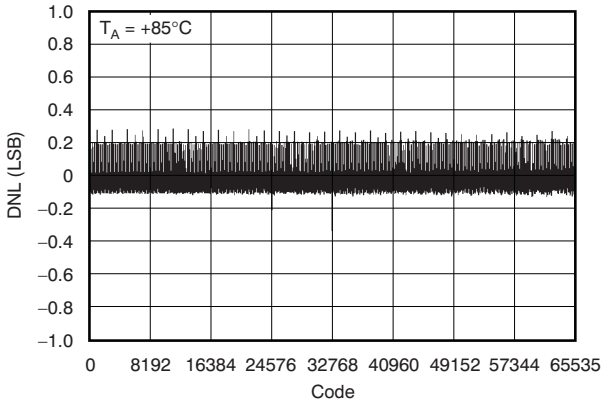

Figure 23. Differential Nonlinearity vs Digital Input Code

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7.8.4 Channel B—2.7 V

At T_A = 25°C, V_{DD} = 2.7 V, unless otherwise noted

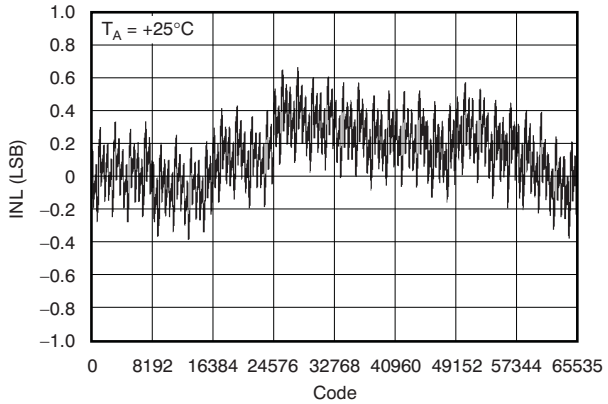

Figure 24. Integral Nonlinearity vs Digital Input Code

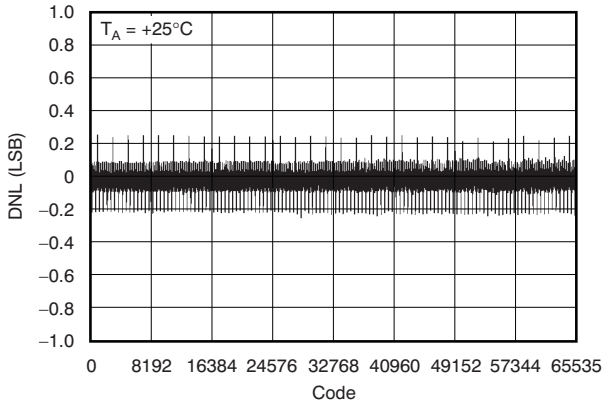

Figure 25. Differential Nonlinearity vs Digital Input Code

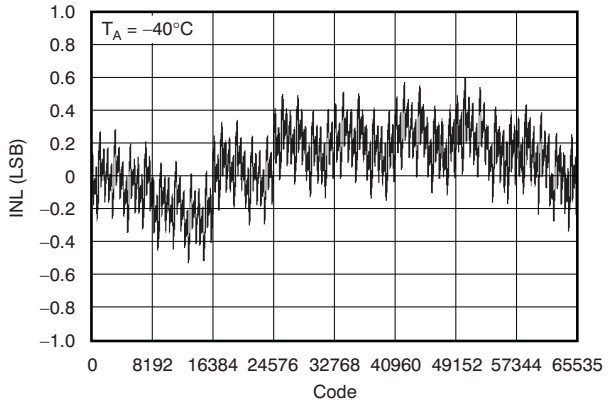

Figure 26. Integral Nonlinearity vs Digital Input Code

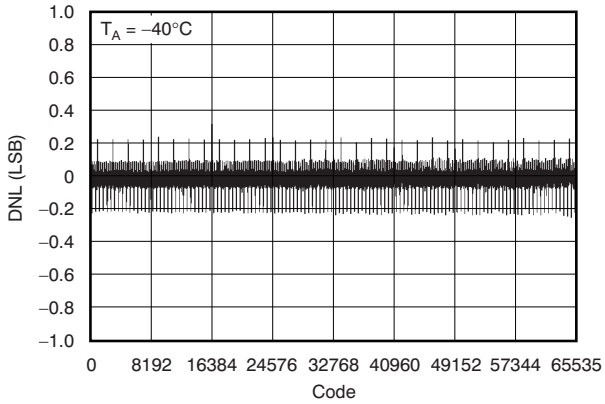

Figure 27. Differential Nonlinearity vs Digital Input Code

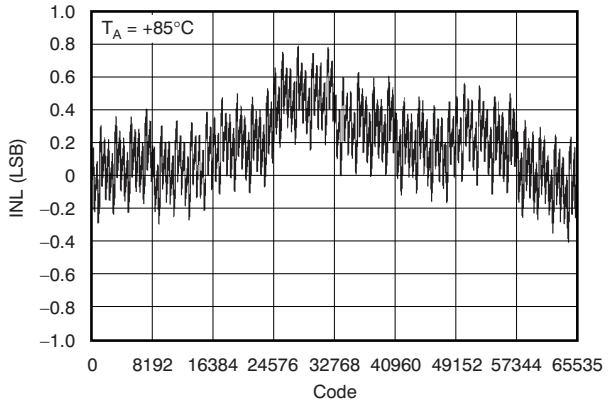

Figure 28. Integral Nonlinearity vs Digital Input Code

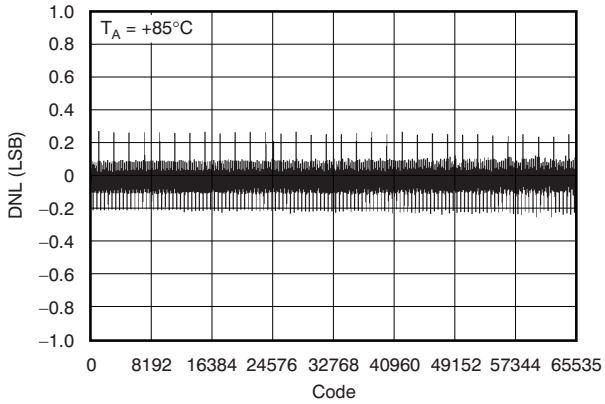

Figure 29. Differential Nonlinearity vs Digital Input Code

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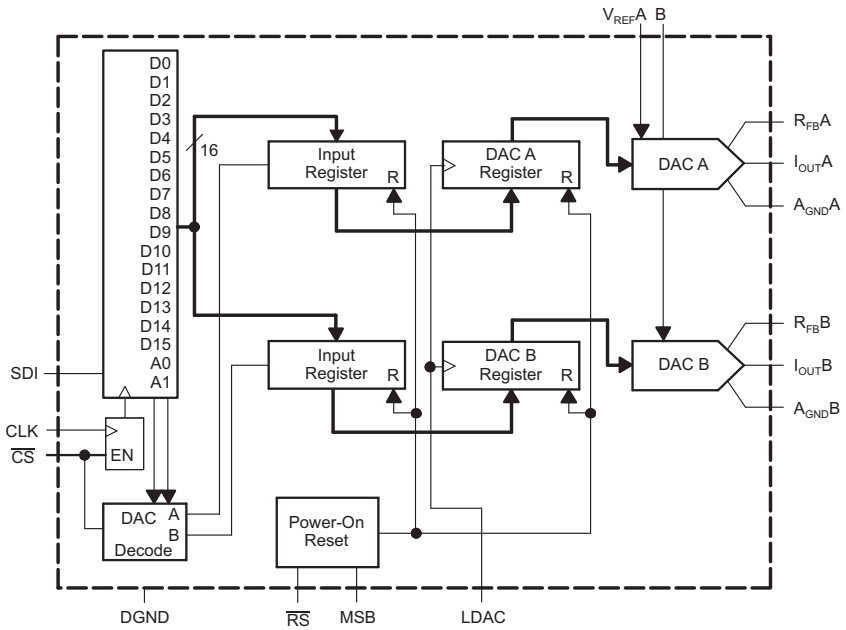
8 Detailed Description

8.1 Overview

The DAC8812 contains two 16-bit, current-output, digital-to-analog converters (DACs). Each DAC has its own independent multiplying reference input. The DAC8812 uses a 3-wire, SPI-compatible serial data interface, with a configurable asynchronous $\overline{RS}$ pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an $\overline{LDAC}$ strobe enables two channel simultaneous updates for hardware synchronized output voltage changes.

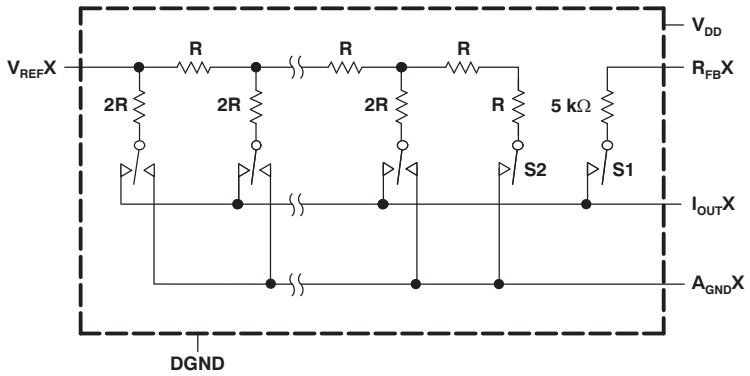
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital-to-Analog Converters

The DAC8812 contains two current-steering R-2R ladder DACs. Figure 30 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The $R_{FB}X$ pin is connected to the output of the external amplifier. The $I_{OUT}X$ pin is connected to the inverting input of the external amplifier. The $A_{GND}X$ pin should be Kelvin-connected to the load point in the circuit requiring the full 16-bit accuracy.



Digital interface connections omitted for clarity.
Switches S1 and S2 are closed, V_{DD} must be powered.

Figure 30. Typical Equivalent DAC Channel

Feature Description (continued)

The DAC is designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users are attempting to measure the value of R_{FB}, power must be applied to V_{DD} in order to achieve continuity. The DAC output voltage is determined by V_{REF} and the digital data (D) according to Equation 1:

$$V_{OUT} = V_{REF} \times \frac{D}{65536} \tag{1}$$

Note that the output polarity is opposite of the V_{REF} polarity for dc reference voltages.

The DAC is also designed to accommodate ac reference input signals. The DAC8812 accommodates input reference voltages in the range of –15 V to 15 V. The reference voltage inputs exhibit a constant nominal input resistance of 5 kΩ, ±20%. On the other hand, DAC outputs I_{OUT}A and B are code-dependent and produce various output resistances and capacitances.

The choice of external amplifier should take into account the variation in impedance generated by the DAC8812 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor, C_{FB} (4 pF to 20 pF typical), may be needed to provide a critically damped output response for step changes in reference input voltages.

Figure 15 shows the gain vs frequency performance at various attenuation settings using a 3 pF external feedback capacitor connected across the I_{OUT}X and R_{FB}X pins. In order to maintain good analog performance, power-supply bypassing of 0.01 µF, in parallel with 1 µF, is recommended. Under these conditions, clean power supply with low ripple voltage capability should be used. Switching power supplies is usually not suitable for this application due to the higher ripple voltage and P_{SS} frequency-dependent characteristics. It is best to derive the DAC8812 5-V supply from the system analog supply voltages (do not use the digital 5-V supply); see Figure 31.

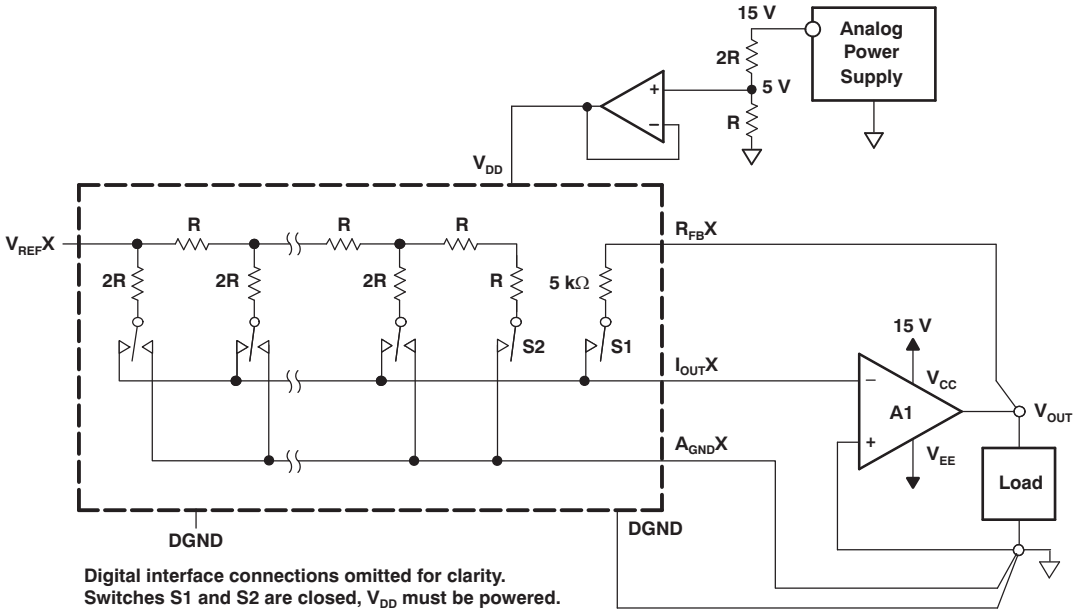


Figure 31. Recommended Kelvin-Sensed Hookup

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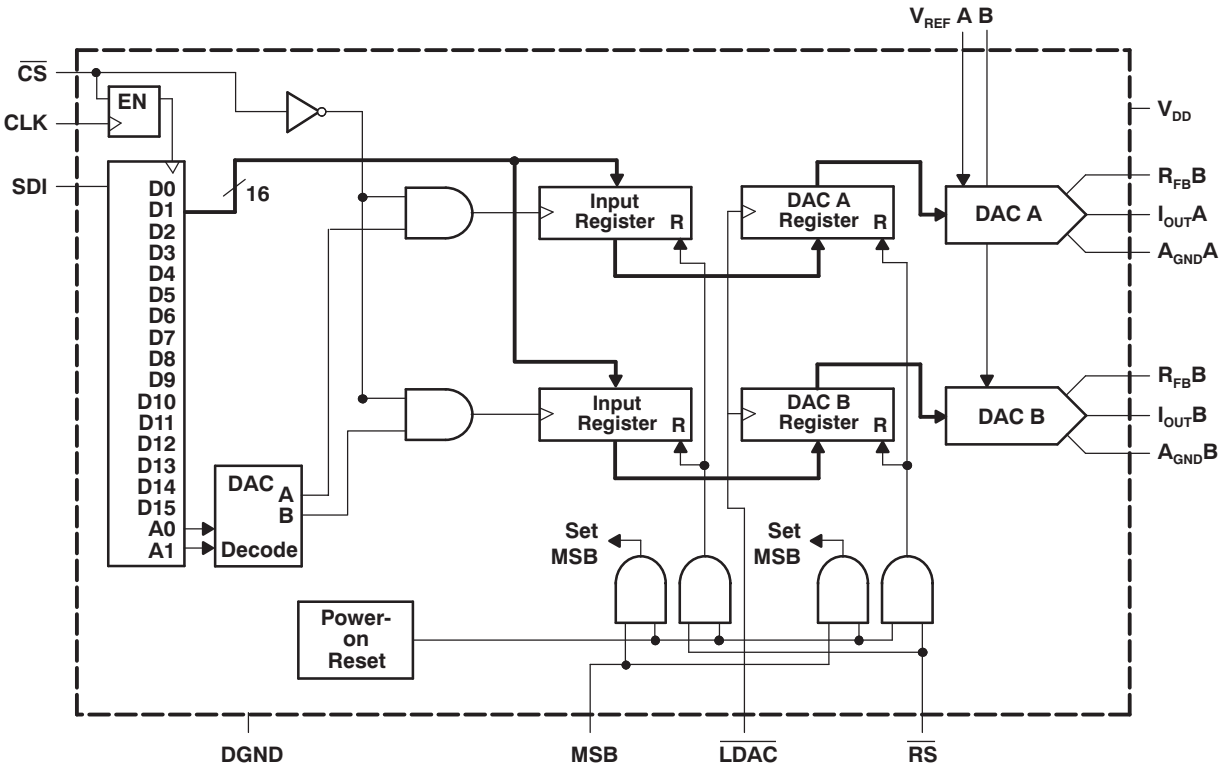

Figure 32. System-Level Digital Interfacing

8.3.2 Power-On Reset

When the V_{DD} power supply is turned on, an internal reset strobe forces all the Input and DAC registers to the zero-code state or half-scale, depending on the MSB pin voltage. The V_{DD} power supply should have a smooth positive ramp without drooping, in order to have consistent results, especially in the region of V_{DD} = 1.5 V to 2.3 V. The DAC register data stays at zero or half-scale setting until a valid serial register data load takes place.

8.3.2.1 ESD Protection Circuits

All logic-input pins contain back-biased ESD protection zener diodes connected to ground (DGND) and V_{DD} as shown in Figure 33.

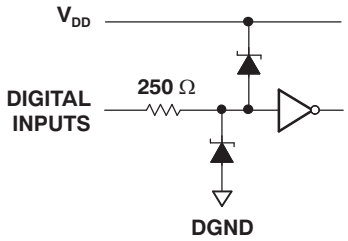

Figure 33. Equivalent ESD Protection Circuits

8.4 Device Functional Modes

8.4.1 Serial Data Interface

The DAC8812 uses a 3-wire ($\overline{CS}$, SDI, CLK) SPI-compatible serial data interface. Serial data of the DAC8812 is clocked into the serial input register in an 18-bit data-word format. MSB bits are loaded first. Table 1 defines the 18 data-word bits for the DAC8812.

Device Functional Modes (continued)

Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the *Interface Timing* specifications of the *Electrical Characteristics*. Data can only be clocked in while the $\overline{CS}$ chip select pin is active low. For the DAC8812, only the last 18 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state.

Since most microcontrollers output serial data in 8-bit bytes, three right-justified data bytes can be written to the DAC8812. Keeping the $\overline{CS}$ line low between the first, second, and third byte transfers will result in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the $\overline{CS}$ initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1 and A0. For the DAC8812, Table 1, Table 2, Table 3, and Figure 1 define the characteristics of the software serial interface.

Table 1. Serial Input Register Data Format, Data Loaded MSB First(1)

Bit	B17 (MSB)	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) Only the last 18 bits of data clocked into the serial register (address + data) are inspected when the $\overline{CS}$ line positive edge returns to logic high. At this point an internally-generated load strobe transfers the serial register data contents (bits D15-D0) to the decoded DAC-input-register address determined by bits A1 and A0. Any extra bits clocked into the DAC8812 shift register are ignored; only the last 18 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 2. Control Logic Truth Table(1)

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	SERIAL SHIFT REGISTER	INPUT REGISTER	DAC REGISTER
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	↑+	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
↑+	L	H	H	X	No effect	Selected DAC updated with current SR contents	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	↑+	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0000h	Latched data = 0000h
H	X	H	L	H	No effect	Latched data = 8000h	Latched data = 8000h

(1) **↑+** = Positive logic transition; **X** = Don't care

Table 3. Address Decode

A1	A0	DAC DECODE
0	0	None
0	1	DAC A
1	0	DAC B
1	1	DAC A and DAC B

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Figure 34 shows the equivalent logic interface for the key digital control pins for the DAC8812.

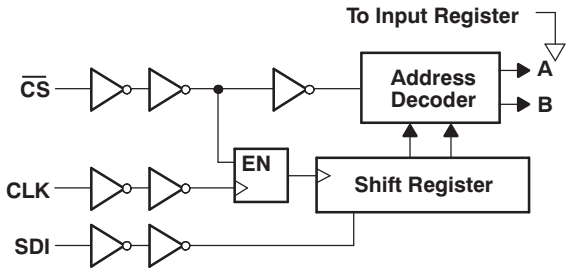

Figure 34. DAC8812 Equivalent Logic Interface

Two additional pins, $\overline{RS}$ and MSB, provide hardware control over the preset function and DAC register loading. If these functions are not needed, the $\overline{RS}$ pin can be tied to logic high. The asynchronous input $\overline{RS}$ pin forces all input and DAC registers to either the zero-code state (MSB = 0), or the half-scale state (MSB = 1).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This design features one channel of the DAC8812 followed by a four-quadrant circuit for multiplying DACs. The circuit conditions the current output of an MDAC into a symmetrical bipolar voltage. The design uses an op amp in a transimpedance configuration to convert the MDAC current into a voltage, followed by an additional amplifier in a summing configuration to apply an offset voltage.

9.2 Typical Application

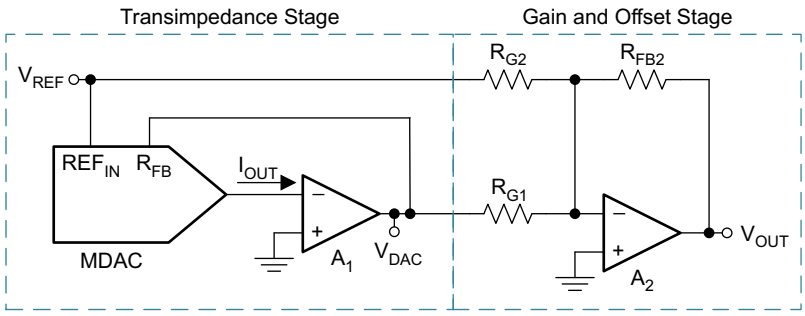

Figure 35. Four-Quadrant Multiplying Application Circuit

9.2.1 Design Requirements

Using a multiplying DAC requires a transimpedance stage using an amplifier with minimal input offset voltage. The tolerance of the external resistors varies depending on the goals of the application, but for optimal performance with the DAC8812 the tolerance should be 0.1 % for all of the external resistors. The summing stage amplifier also requires low input-offset voltage and enough slew rate for the output range desired.

9.2.2 Detailed Design Procedure

The first stage of the design converts the current output of the MDAC (I_{OUT}) to a voltage (V_{OUT}) using an amplifier in a transimpedance configuration. A typical MDAC features an on-chip feedback resistor sized appropriately to match the ratio of the resistor values used in the DAC R-2R ladder. This resistor is available using the input shown in Figure 35 called R_{FB} on the MDAC. The MDAC reference and the output of the transimpedance stage are then connected to the inverting input of the amplifier in the summing stage to produce the output that is defined by Equation 2.

$$V_{OUT}(\text{Code}) = \left(\frac{2_{FB2}}{R_{G1}} \times \frac{V_{REF} \times \text{Code}}{2^{\text{bits}}}\right) - \left(\frac{R_{FB2}}{R_{G2}} \times V_{REF}\right) \tag{2}$$

9.2.3 Application Curves

Figure 36 shows the output voltage vs code of this design, and Figure 37 shows the output error vs code. Notice that the error gets worse as the output code increases because the contribution of the DAC gain error increases with code.

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Typical Application (continued)

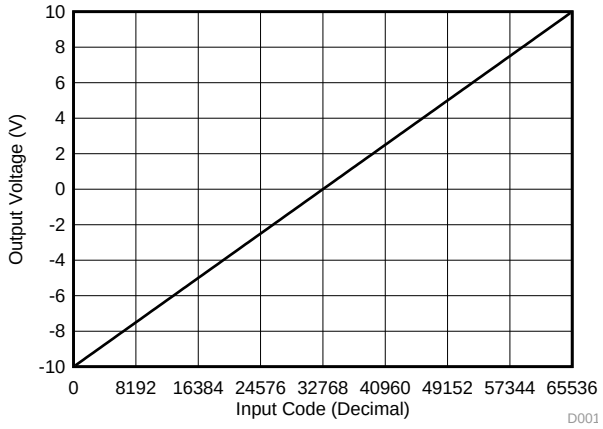

Figure 36. Input Code vs Output Voltage

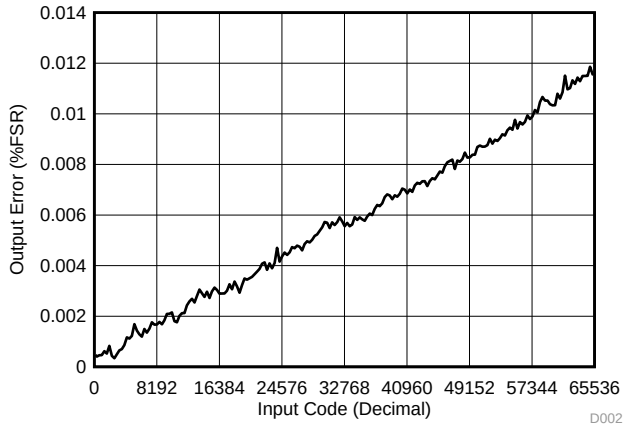

Figure 37. Input Code vs Output Error

10 Power Supply Recommendations

This device can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to V_{DD} should be well-regulated and low-noise. In order to further minimize noise from the power supplies, a strong recommendation is to include a 100-pF to 1-nF capacitor and a 0.1-µF to 1-µF bypass capacitor very close to the V_{DD} pin. The current consumption of the V_{DD} pin, the short-circuit current limit, and the load current for these devices are listed in the *Electrical Characteristics* table. Choose a power supply for these devices to meet the aforementioned current requirements.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC8812 offers single-supply operation, and is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output. This device has three ground pins: two for analog ground ($A_{GND}A$ and $A_{GND}B$) and one for digital ground (DGND), which are pinned out on opposite sides of the device. Ideally, the analog grounds would be connected directly to an analog ground plane, and similarly the digital ground connected to a digital ground plane. These planes would be separated until they were connected at the power-entry point of the system. The power applied to V_{DD} should be well-regulated and low-noise. Switching power supplies and dc-dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. V_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until the analog and digital supplies are connected at the power-entry point. In addition, adding both a 100-pF to 1-nF capacitor and a 0.1-µF to 1-µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a pi filter made up of inductors and capacitors – all designed essentially to provide low-pass filtering for the supply and remove the high-frequency noise.

The compensation capacitors shown on the layout in Figure 38 are not required for normal operation of the DAC. However, overshoot of the amplifier output voltage on large code changes is possible. This can be mitigated by using a compensation capacitor between the IOUTx and RFBx nodes, as shown implemented here.

Performance of the DAC8812 can be compromised by grounding and PCB lead trace resistance. The 16-bit DAC8812 with a 10-V full-scale range has an LSB size of 153 µV. The ladder and associated reference and analog ground currents for a given channel can be as high as 2 mA. With this 2-mA current level, a series wiring and connector resistance of only 76 mΩ causes 1 LSB of voltage drop. The preferred PCB layout for the DAC8812 is to have all AGNDx pins connected directly to an analog ground plane at the device. The noninverting input for the transimpedance amplifier of each channel should also either connect directly to the analog ground plane or have an individual sense trace back to the AGNDx pin connection. The feedback resistor trace to the transimpedance amplifier should also be kept short and have low resistance in order to prevent IR drops from contributing to gain error. Therefore, it is important to place the transimpedance amplifier as close to the DAC as possible. This attention to wiring and placement ensures the optimal performance of the DAC8812.

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11.2 Layout Example

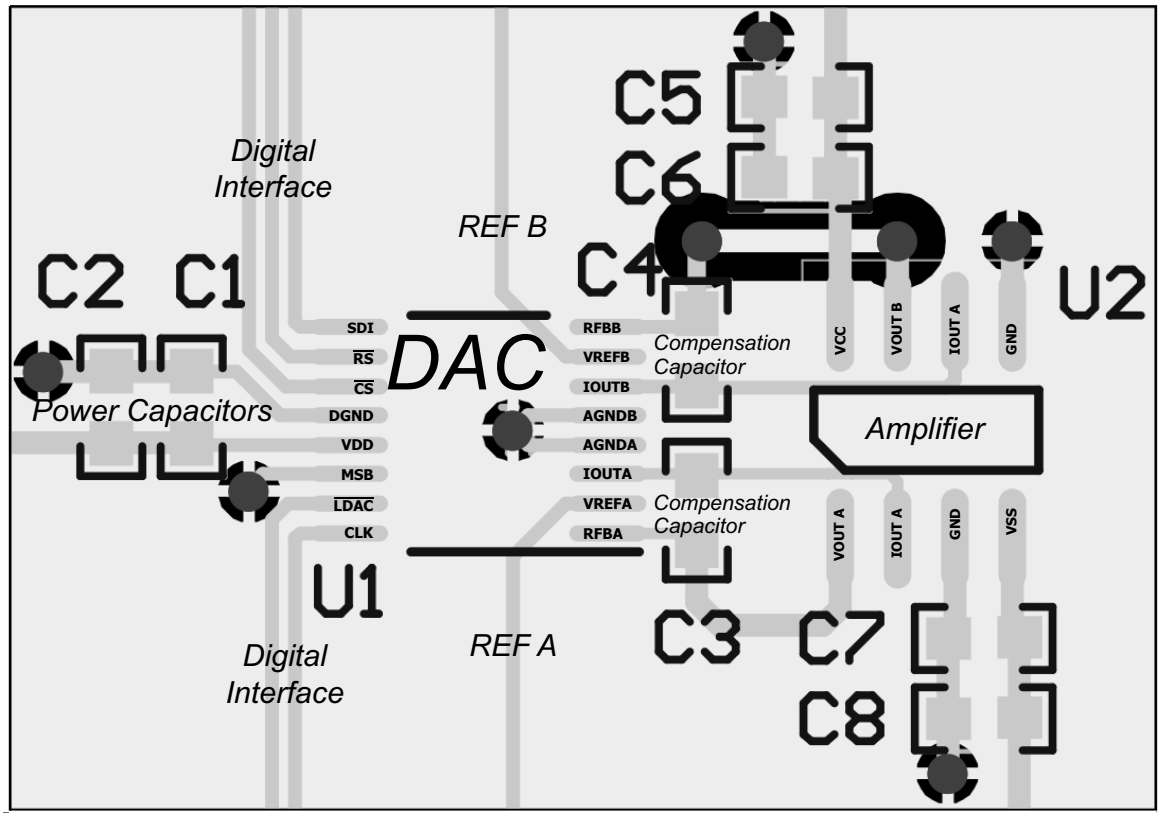

Figure 38. DAC8812 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

DAC8811 16-Bit, Serial Input Multiplying Digital-to-Analog Converter, SLAS411

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8812IBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples
DAC8812IBPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples
DAC8812IBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples
DAC8812IBPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples
DAC8812ICPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples
DAC8812ICPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples
DAC8812ICPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples
DAC8812ICPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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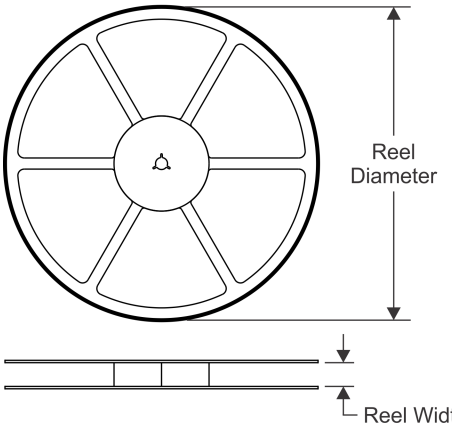
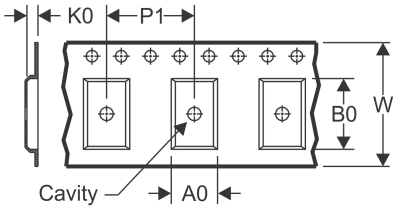
TAPE AND REEL INFORMATION

REEL DIMENSIONS

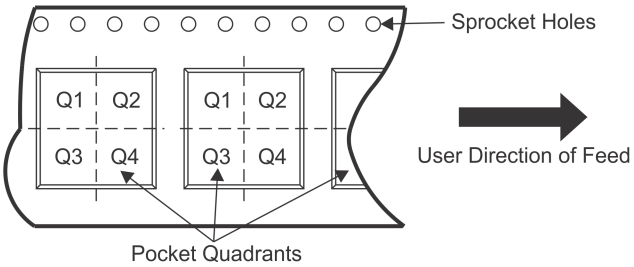


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

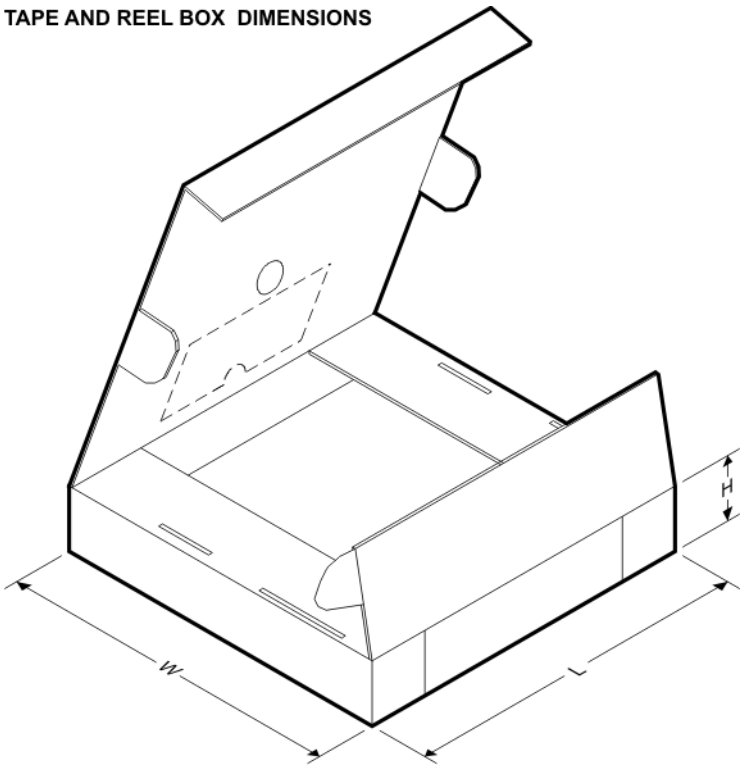
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8812IBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8812ICPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

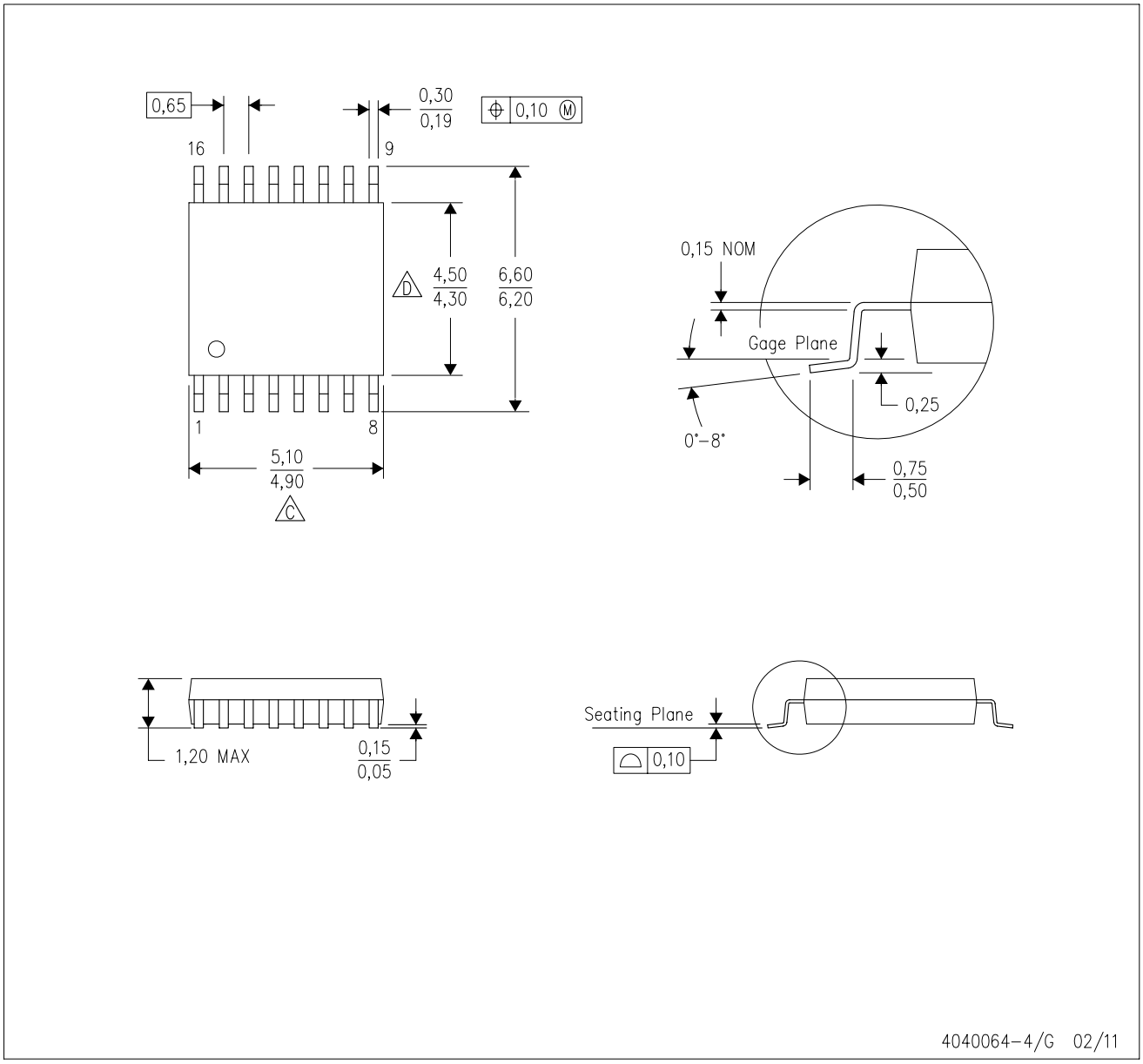
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

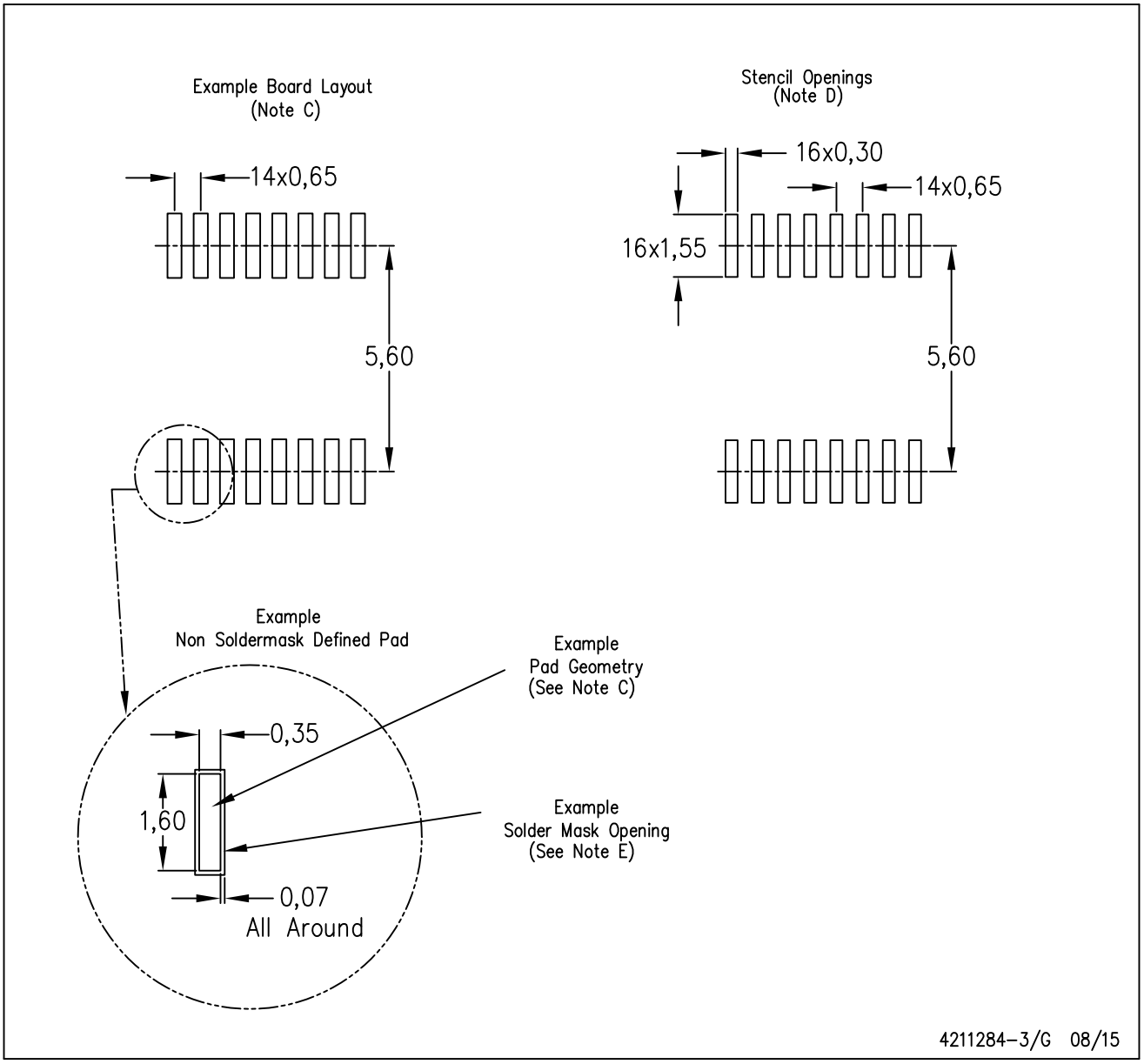
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8812IBPWR	TSSOP	PW	16	2000	367.0	367.0	38.0
DAC8812ICPWR	TSSOP	PW	16	2000	367.0	367.0	38.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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