Central™
Semiconductor Corp.

PROCESS CP753V

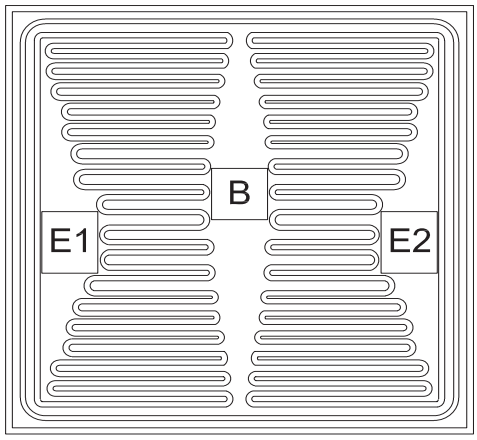
Small Signal Transistors

PNP - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	66 x 66 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	7.9 x 7.9 MILS
Emitter 1 Bonding Pad Area	7.9 x 9.5 MILS
Emitter 2 Bonding Pad Area	7.9 x 9.5 MILS
Top Side Metalization	Al-Si 30,000Å
Back Side Metalization	Au 12,000Å

GEOMETRY



BACKSIDE: COLLECTOR R0

GROSS DIER PER 5 INCH WAFER

3,878

PRINCIPAL DEVICE TYPES

CZT953

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R0 (23- September 2005)