GPS RF Downconverter

ADSST-GPSRF01

FEATURES

Single chip GPS downconverter
GPS L1 band C/A code (1575.42 MHz) receiver
2.7 V to 3.3 V power supply
On-chip LNA
On-chip PLL including complete VCO
On-chip reference oscillator
On-chip NCO for sampling clock
Option to choose 6.144 MHz, or 6.552 MHz, or external sampling clock
60 dB AGC dynamic range
SIGN and MAGN outputs
Low power operation 55 mA
Supports power-down mode

APPLICATIONS

Security applications
Asset tracking
Marine navigation
Portable GPS receiver

GENERAL DESCRIPTION

The ADSST-GPSRF01 is a high performance, fully integrated, RF front-end chip for downconversion and amplification of GPS signals. It has been designed for L1 (1575.42 MHz), C/A GPS band receivers.

The ADSST-GPSRF01 is a dual conversion, superheterodyne receiver with an on-chip low noise amplifier (LNA), local oscillator, two downconversion IF stages (at 24.52 MHz and 8.194 MHz, respectively), an automatic gain controlled amplifier (AGC), and a 2-bit analog-to-digital converter (ADC).

Two selectable, fixed frequency sampling clocks from an on-chip NCO can be used for output sampling (6.144 MHz or 6.552 MHz). In addition, an external sampling clock can be used up to 32 MHz.

The chip can be interfaced with any active/passive GPS antenna.

FUNCTIONAL BLOCK DIAGRAM

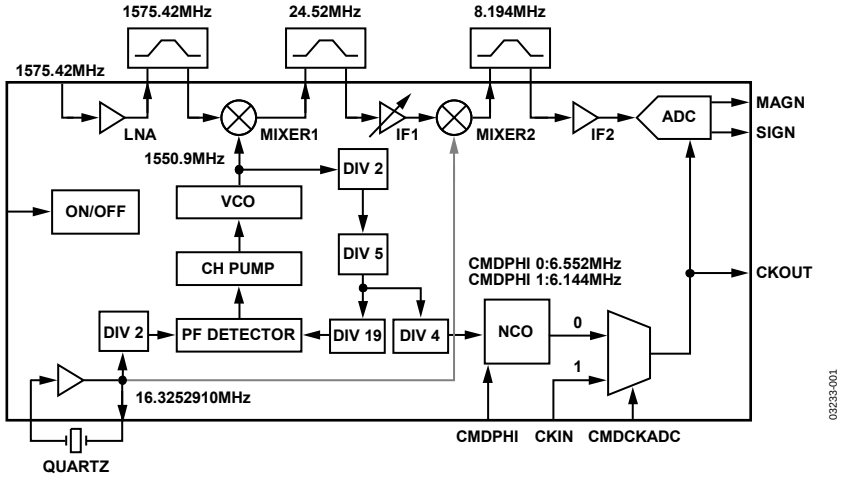

Figure 1.

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REVISION HISTORY

3/07—Revision 0: Initial Version

SPECIFICATIONS

Recommended operating conditions: VCC = 2.7 V to 3.3 V, VEE = 0 V, typical is at VCC = 3 V, and T_A @ 25°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
LNA CHARACTERISTICS	See the LNA Matching Network section				
RF Frequency		1570	1575.42	1580	MHz
Input Impedance	With external matching network		50		Ω
Input VSWR	With external matching network		1	2	
Output Impedance	With external matching network		50		Ω
Output VSWR	With external matching network		1	2	
Gain	With external matching network, typical simulation	17	21	25	dB
	No external matching network	12	16	20	dB
OP1dB			−4		dBm
Noise Figure	Typical simulation			3	dB
MIXER CHARACTERISTICS	See the Mixer Matching Network section				
RF Frequency		1570	1575.42	1580	MHz
LO Frequency	95 times the reference frequency		1550.9		MHz
IF Frequency		24	24.51	25.5	MHz
Input Impedance	With external matching network		50		Ω
Input VSWR	With external matching network		1	2	
Differential Output Impedance	See Mixer Matching Network section		1000		Ω
Conversion Gain	With external matching network	7	12	16	dB
	No external matching network	7	15	17	dB
OP1dB		−16	−12		dBm
SSB Noise Figure	Typical simulation			15	dB
PILOTE CHARACTERISTICS					
Reference Frequency			16.325291		MHz
Input Magnitude Level	On a 50 Ω load		−4	0	dBm
Gain		8	10	13	dB
Output Level High, V_{OH}			VCC		V
Output Level Low, V_{OL}			VCC − 0.8		V
VCO CHARACTERISTICS	See the PLL Filter section				
Nominal Frequency	With the reference frequency	1.45	1.55	1.68	GHz
Phase Noise (Free-Running VCO)	Typical simulations @ 400 kHz		−78		dBc/Hz
Phase Noise (Closed Loop)					
With Proposed Filter (Loop Bandwidth 100 kHz)	Typical simulation @ 100 kHz		−66		dBc/Hz
Nonharmonic Spurious (Closed Loop)	Typical simulations				
@ 8 kHz				−30	dBc
@ 16 kHz				−40	dBc
@ 24 kHz				−50	dBc
VCO Slope	Typical simulations	1.2	2.4	3.5	GHz/V
VTUNE Voltage		0.6		VCC	V
IF1/MIXER CHARACTERISTICS					
Input Frequency	With the reference frequency		24.51		MHz
Output Frequency	With the reference frequency		8.192		MHz
Differential Input Impedance	See the IF Input Network section		1000		Ω
Differential Output Impedance	See the IF Input Network section		1000		Ω

Parameter	Conditions	Min	Typ	Max	Unit
Gain (S21) (IF1 + MIXER2)	Without AGC regulation				
Maximum		+41	+56	+72	dB
Minimum		−29	−26	−20	dB
Noise Figure	Typical simulations				
S21 = +50 dB			6		dB
S21 = +20 dB			15		dB
S21 = −10 dB			45		dB
OP1dB	Typical simulations				
S21 = +50 dB			−15		dBm
S21 = +20 dB			−18		dBm
S21 = −10 dB			−45		dBm
AGC Dynamic Range		65			dB
AGC Slope	Typical simulations for a gain within 20 dB ± 30 dB range	300		2500	dB/V
AGC Voltage Range (on CAMP Pin)	Typical simulations		400		mV
CAMP Pin Maximum Rating Voltage	If externally controlled	1		VCC	V
Magnitude Bit Duty Cycle (Use for AGC Regulation Point)	This rate allows ADSST-GPSRF01 to fix the conversion loss below 0.6 dB	23	33	43	%
AGC Band-Pass	Typical simulations	1	3	10	kHz
LO2 Leakage on MIXER2 Output			−28	−17	dBm
Output Offset	For a gain within 20 dB ± 30 dB range			<100	mV
IF2 CHARACTERISTICS	See the IF Input Network section				
Frequency			8.192		MHz
Differential Input Impedance	See the IF Input Network section		1000		Ω
Gain		31	34	39	dB
OP1dB		−15			dBm
LSB	Typical simulations		100		mV
Output Test Attenuation			−20		dB
Output Test Level	On a 50 Ω load		−40		dBm
INPUT CMOS LEVELS CKIN, CMDCKADC, CMDPHI, POWER ON					
Input CMOS Level High, V_{IH}		VCC × 0.7			V
Input CMOS Level Low, V_{IL}				0.3 × VCC	V
OUTPUT CMOS LEVELS MAGN, SIGN, CKOUT					
Output CMOS Level High, V_{OH}		VCC × 0.85			V
Output CMOS Level Low, V_{OL}				0.15 × VCC	V
Maximum Rating Output Load				15	pF
CKOUT to MAGN/SIGN Skew	Typical simulations			20	ns
POWER CONSUMPTION	Standby measured			0.1	mA
	3 V (min @ −40°C, max @ +85°C)	40	55	65	mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC to VEE[1]	−0.3 V to +5 V
Analog I/O Voltage to VEE	−0.3 V to VCC + 0.3 V
Digital I/O Voltage to VEE	−0.3 V to VCC + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Maximum Junction Temperature	+125°C

[1] VEE = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

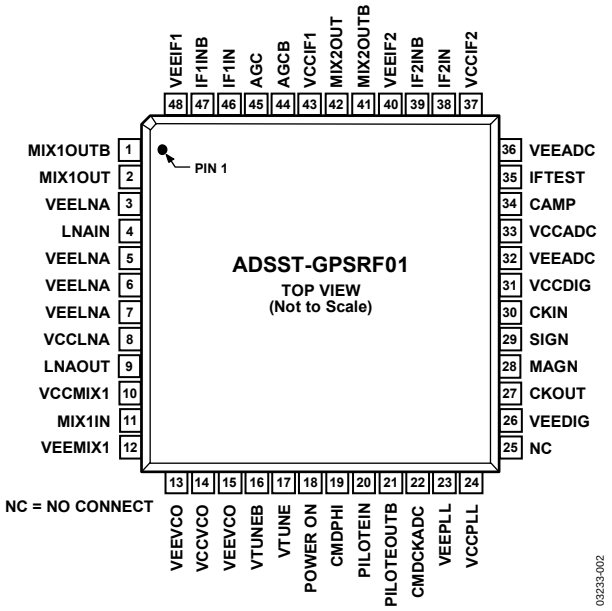

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Pin Type	Description
1	MIX1OUTB	Analog	MIXER1 Output, IF1 Signal, (24.52 MHz).
2	MIX1OUT	Analog	Complementary MIXER1 Output.
3, 5 to 7	VEELNA	Ground	LNA Ground.
4	LNAIN	Analog	LNA RF Input Signal, (1575.42 MHz).
8	VCCLNA	Supply	LNA Supply.
9	LNAOUT	Analog	LNA RF Output Signal, (1575.42 MHz).
10	VCCMIX1	Supply	MIXER1 Supply.
11	MIX1IN	Analog	MIXER1 RF Input Signal, (1575.42 MHz).
12	VEEMIX1	Ground	MIXER1 Ground.
13, 15	VEEVCO	Ground	VCO Ground.
14	VCCVCO	Supply	VCO Supply.
16	VTUNEB	Analog	VCO Input Command. This pin is used for internal decoupling.
17	VTUNE	Analog	External PLL Filter Connection.
18	POWER ON	CMOS	Power-On Input.
19	CMDPHI	CMOS	NCO Frequency Switch Input Control.
20	PILOTEIN	Analog	Reference Clock Input.
21	PILOTEOUTB	Analog	Reference Clock Output with 180° Phase Shift.
22	CMDCKADC	CMOS	NCO/CKIN Switch Input Control.
23	VEEPLL	Ground	PLL Ground.
24	VCCPLL	Supply	PLL Supply.
25	NC		Not Connected.
26	VEEDIG	Ground	Digital Ground.
27	CKOUT	CMOS	Clock Output.
28	MAGN	CMOS	Magnitude Bit Data Output.
29	SIGN	CMOS	Sign Bit Data Output.
30	CKIN	CMOS	External Sampling Clock Input.
31	VCCDIG	Supply	Digital Supply.
32, 36	VEEADC	Ground	ADC Ground.
33	VCCADC	Supply	ADC Supply.
34	CAMP	Analog	Amplitude Bit Capacitor Signal.

Pin No.	Mnemonic	Pin Type	Description
35	IFTEST	Analog	IF Test Output.
37	VCCIF2	Supply	IF2 Supply.
38	IF2IN	Analog	Second Amplifier IF Input, (8.194 MHz).
39	IF2INB	Analog	Complementary Second Amplifier IF Input.
40	VEEIF2	Ground	Substrate Connection to Die Paddle.
41	MIX2OUTB	Analog	MIXER2 Output, IF2 Signal, (8.194 MHz).
42	MIX2OUT	Analog	Complementary MIXER2 Output, IF2 Signal.
43	VCCIF1	Supply	IF1 Supply.
44	AGCB	Analog	AGC Capacitor Signal.
45	AGC	Analog	Complementary AGC Capacitor Signal.
46	IF1IN	Analog	First Amplifier IF Input, (24.52 MHz).
47	IF1INB	Analog	Complementary First Amplifier IF Input.
48	VEEIF1	Ground	IF1 Ground.

THEORY OF OPERATION

POWER SUPPLIES

The ADSST-GPSRF01 uses eight different power supply groups as follows:

a. VCCLNA and VEELNA

b. VCCMIX1 and VEEMIX1

c. VCCVCO and VEEVCO

d. VCCIF1 and VEEIF1

e. VCCIF2 and VEEIF2

f. VCCADC and VEEADC

g. VCCDIG and VEEDIG

h. VCCPLL and VEEPLL

These separate power groups increase isolation between internal components. Each power supply group is externally decoupled by a single low value capacitor for oscillation risk reduction. There should be only one regulated 3 V power supply on the board and only one common ground. If isolation is not high enough, a separate 3 V regulated power supply should be used.

MATCHING NETWORK

The RF input has an unmatched input impedance. The necessary 50 Ω RF external input matching components must be mounted as close to the RF input as possible. Input and output matching networks provide 50 Ω source and load impedance.

LNA MATCHING NETWORK

LNA input is internally biased; therefore, it should be externally ac-coupled.

Tests were made with lumped matching elements, performing maximum power transfer between LNA and input and output. Input matching impedances given in Table 4 are designed for simultaneous input and output matching. Input and output RF signals should be connected to the external devices via a 50 Ω line.

Table 4. External Components Used for LNA Matching

Component Name	Typical Value	Unit
L_{IN}	3.3	nH
C_{IN}	2.7	pF
L_{OUT}	5.6	nH
C_{OUT}	1.2	pF
C_{LINK}	100	pF

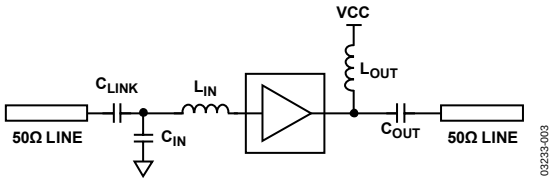

Figure 3. LNA Matching Network Connections

MIXER MATCHING NETWORK

The mixer structure is double-balanced with open-collector outputs. The local oscillator (LO) input and IF output are fully differential. One of the RF differential port inputs is internally decoupled. The other RF input must be externally ac-coupled. The RF inputs have unmatched input impedance. The 50 Ω matching is obtained with external components.

The IF outputs require external dc bias to VCC. This bias is provided through two inductors that also cancel the imaginary part of the output impedance.

RF input requires 50 Ω matching to ensure maximum power transfer.

Due to its high impedance, the IF output is not matched, but external components must be added to provide the filter input with a 1000 Ω load. An external 1000 Ω parallel resistor performs this task and also decreases the sensitivity to component tolerances. This 1000 Ω external resistor must not be confused with the 1000 Ω load that represents the filter input.

Table 5. External Components Used for Mixer Matching

Component Name	Typical Value	Unit
L_{IN}	5.6	nH
C_{IN}	Not connected	pF
C_{LINK}	100	pF
L_{COIL}	10	µH
R_{OUT}	1	kΩ

Note that C_{IN} can be omitted due to the parasitic capacitor displayed by the board.

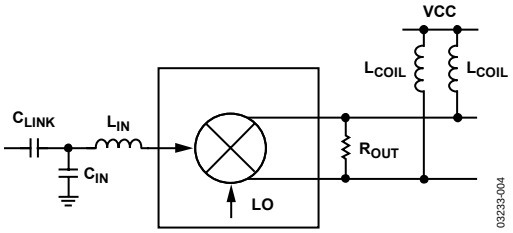

Figure 4. Mixer Matching Network Connections

Table 6.

Mode	Crystal Frequency with an Equivalent C_L Load Capacitance	Equivalent Series Resistances (Typical)	Shunt Capacitance (Typical)	Drive Level (Typical)	C1, C2	C_L
Fundamental	16.3252910 MHz	10 Ω	5.5 pF	50 µW	39 pF	22 pF

REFERENCE CLOCK GENERATION

The PILOTE input/output are internally biased, therefore, they must be externally ac-coupled.

The PILOTE structure allows the ADSST-GPSRF01 to be directly driven by an external reference clock or to be used as an oscillator with an external crystal (see Figure 5 for the circuit connection and Table 6 for the component values).

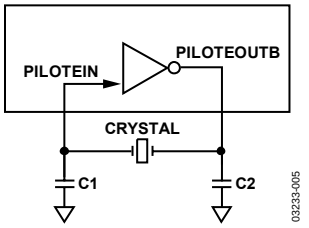

Figure 5. Crystal Connections

PLL FILTER

The PLL generates the local oscillation. It includes a VCO with an on-chip tank circuit, dividers, and a phase detector with external loop filter components. A reference frequency is required for the PLL. The PLL is a second- or a third-order loop, Type 2 for zero frequency error.

This VCO is a monolithic LC voltage controlled oscillator. The loop gain is maintained high enough to ensure oscillations in all process, temperature, and power supply conditions. The voltage control is amplified by a low gain differential amplifier.

The divider chain involves three dividers. The first one is a fast divider by two. The second one is a divider by five. The third one divides by 19. The whole divider divides the local oscillator (LO) frequency by 190 before being compared with the reference clock divided by 2.

The PLL provides a local oscillator frequency divided by a 40 MHz CMOS output clock to an NCO that, in turn, delivers either a 6.144 MHz or 6.552 MHz clock for the DSP serial link. The PILOTE provides a 16.3252910 MHz clock.

The design of the PLL depends on two criteria: the filtering of the reference frequency signal and the phase noise of the output signal of the PLL. The phase noise of the VCO is filtered by the PLL.

The PLL includes a charge-pump active filter to perform a second-order loop. The PLL loop filter components are selected to give a PLL loop bandwidth of approximately 100 kHz to minimize phase noise.

An additional on-chip LPF (R = 10 kΩ and C = 10 pF) is present in series in the VTUNE command and allows better rejection harmonics of the comparison frequency.

The PLL filter is listed in Table 7 and displayed in Figure 6.

Table 7. External Components Used for the PLL Filter

Component Name	Typical Value	Unit
C1	22	nF
C2	1	nF
R2	390	Ω
L2	Shorted	nH

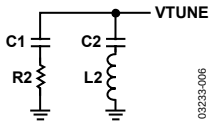

Figure 6. PLL Filter Connections

IF INPUT NETWORK

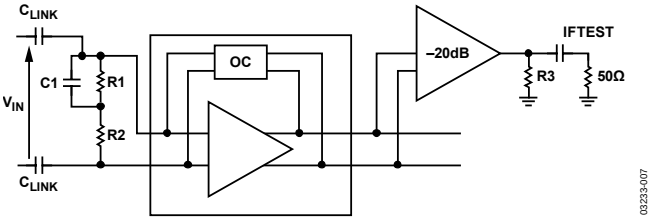

Figure 7. IF Amplifier Connections

Both IF amplifier stages have to display, at minimum, 1000 Ω at dc to get a good offset compensation. Table 8 lists the limit offset values. These stages are internally biased requiring them to be ac-coupled.

The IFTEST output is used for test purposes only; it checks the RF chain gain.

Table 8. External Components Used with IF Amplifiers

Component Name	Typical Value	Unit
R1	3	kΩ
R2	1	kΩ
R3	2	kΩ
C1	1	nF
C_{LINK}	1	nF

MIXER2 OUTPUT NETWORK

The mixer structure is double-balanced with open-collector outputs. The IF1 input, LO input, and IF2 output are fully differential. The IF1 outputs require external dc bias to VCC. This bias is provided through two 500 Ω resistors that fix the differential output impedance to 1000 Ω.

AGC/ADC

To maximize the signal-to-noise ratio (SNR) with a 2-bit ADC, the AGC regulation point is fixed at 1 σ to activate the amplitude bit 33% of the time. This mean time allows the ADSST-GPSRF01 to fix the conversion loss below 0.6 dB.

When the whole chain gain is too high, the CAMP pin is at a high voltage (around 2 V depending on VCC) to reduce the IF1 gain stage. When the whole chain gain is too low, the CAMP pin is at a low voltage (around 1.5 V depending on VCC) to reduce the IF1 gain stage.

In Table 9, IF2 is the signal at the ADC input and the LSB is the magnitude reference level. The data rate of the ADC is dependent on the sampling clock employed in the design.

Table 9. SIGN and MAGN Logic Level vs. IF2 Magnitude Level

IF2 Magnitude Level	SIGN Logic Level	MAGN Logic Level
LSB < IF2	1	1
0 < IF2 < LSB	1	0
–LSB < IF2 < 0	0	0
IF2 < –LSB	0	1

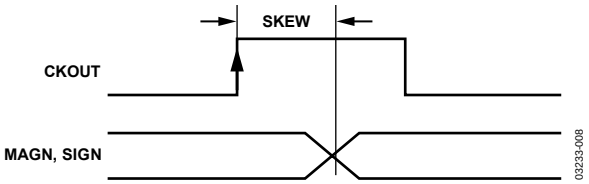

Figure 8. CKOUT to MAGN/SIGN Skew

It is also necessary to stabilize the AGC and to set the AGC band-pass to be less sensitive to external strong spurious noise. Therefore, some passive components are used on CAMP, AGC, and AGCB pins.

Table 10. External Components Used with the AGC

Component Name	Typical Value	Unit
R_{AGC}	2	kΩ
C_{AGC}	20	nF
CAMP	20	nF

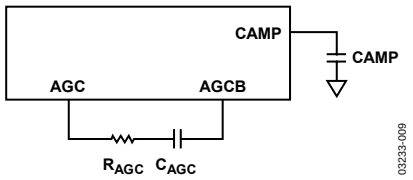

Figure 9. AGC Connections

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

The NCO works with a 38.772 MHz ($F_{CRYSTAL}$ × 19/8) master clock delivered by the PLL. It includes a phase accumulator and delivers a fixed clock that has an average frequency of the NCO clock selected.

Two frequencies are available: 6.144 MHz or 6.552 MHz. This clock has a phase jitter equal to a 38.772 MHz clock period. It is applied to both the ADC and the clock input of the DSP serial link. The clock waveform is shown in Figure 10.

The NCO provides a 6.144 MHz/6.552 MHz clock with an accuracy of less than 2 Hz.

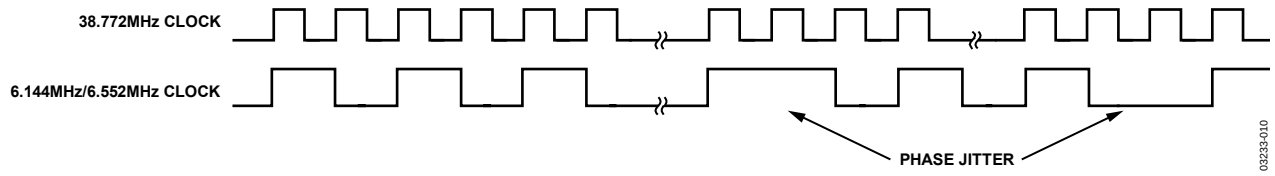

Figure 10. NCO Clock Behavior

POWER ON/STANDBY MODE

One digital input pad permits the ADSST-GPSRF01 circuit to enter standby mode.

Table 11. POWER ON Logic Control Signal

Mode	Logic Level POWER ON
Active	1
Stand By	0

ADC SAMPLING CLOCK SELECTION

Two digital input pins (CMDCKADC and CMDPHI) select the sampling clock. The sampling clock can come from the NCO or from an external clock. This selection is performed by the CMDCKADC pin (see Table 12).

Table 12. CMDCKADC Logic Control Signal

Mode	Logic Level CMDCKADC
NCO Sampling Clock	0
CKIN Sampling Clock	1

Then, the CMDPHI pin selects one of the two available frequencies generated by NCO as listed in Table 13.

Table 13. CMDPHI Logic Control Signal

NCO Frequency	Logic Level CMDPHI
6.552 MHz	0
6.144 MHz	1

OUTLINE DIMENSIONS

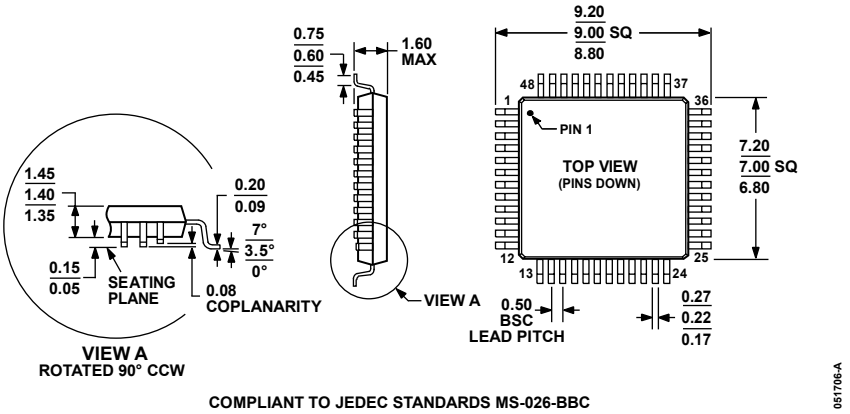

Figure 11. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Operating Voltage	Temperature Range	Package Description	Package Option
ADSST-GPSRF01BSTZ[1]	3 V	−40°C to +85°C	48-Lead LQFP	ST-48

[1] Z = Pb-free part.

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