DATA SHEET

NE56631-XX
Active-LOW system reset

Product data
Supersedes data of 2002 Oct 07

2003 Feb 14

Philips
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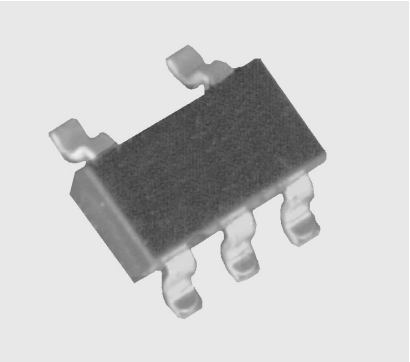
Active-LOW system reset NE56631-XX

GENERAL DESCRIPTION

The NE56631-XX is a family of Active-LOW, power-on resets that offers precision threshold voltage detection within ±3% and super low operating supply current of typically 1.5 μA.

Several detection threshold voltages are available at 1.9 V, 2.0 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.2 V, 4.3 V, 4.4 V, 4.5 V, and 4.6 V. Other thresholds are offered upon request at 100 mV steps from 1.9 V to 4.6 V.

With its ultra low supply current and high precision voltage threshold detection capability, the NE56631-XX is well suited for various battery powered applications such as reset circuits for logic and microprocessors, voltage check, and level detecting.



FEATURES

- High precision threshold detection voltage: V_S ±3%
- Super low operating supply current: I_{CCH}=1.5 μA typ.; I_{CCL}=1.0 μA typ.
- Hysteresis voltage: 50 mV typ.
- Internal Power-On-Reset Delay time: 20 μs typ.
- Detection threshold voltage: 1.9 V, 2.0 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.2 V, 4.3 V, 4.4 V, 4.5 V, and 4.6 V
- Other detection threshold voltages available upon request at 100 mV steps from 1.9 V to 4.6 V
- Large low reset output current: 30 mA typ.
- Reset assertion with V_{CC} down to 0.65 V typ.

APPLICATIONS

- Reset for microprocessor and logic circuits
- Voltage level detection circuit
- Battery voltage check circuit
- Detection circuit for battery backup

SIMPLIFIED SYSTEM DIAGRAM

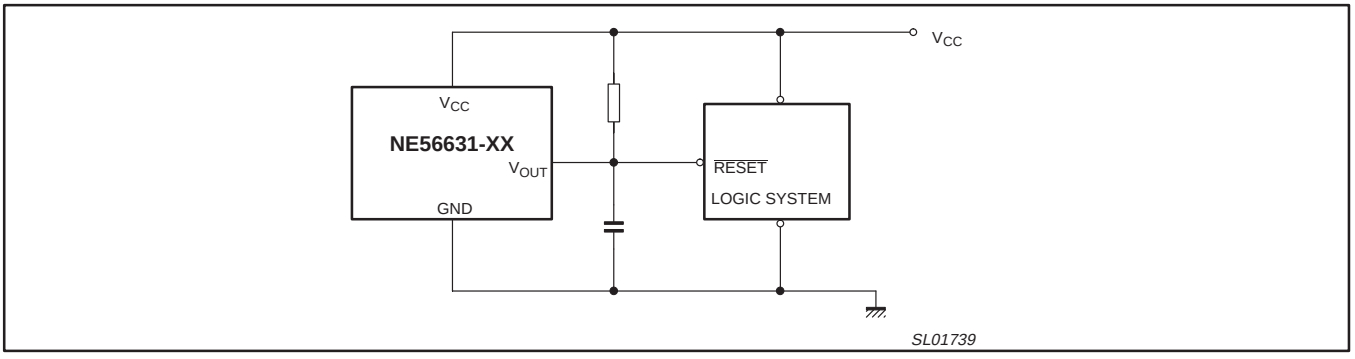


Figure 1. Simplified system diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
NE56631-**XX**D	SOT23-5 / SOT25 (SO5)	plastic small outline package; 5 leads (see dimensional drawing)	–20 to +75 °C

NOTE:
The device has 12 voltage output options, indicated by the XX on the 'Type number'.

XX	VOLTAGE (Typical)
19	1.9 V
20	2.0 V
27	2.7 V
28	2.8 V
29	2.9 V
30	3.0 V
31	3.1 V
42	4.2 V
43	4.3 V
44	4.4 V
45	4.5 V
46	4.6 V

PIN CONFIGURATION

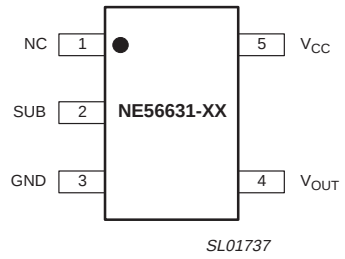


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	NC	No connection.
2	SUB	Substrate. Connect to ground (GND).
3	GND	Ground. Negative supply.
4	V_{OUT}	Reset output ($\overline{RESET}$). Active-LOW, open collector.
5	V_{CC}	Positive supply voltage

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	–0.3	+10	V
T_{amb}	Ambient operating temperature	–20	+75	°C
T_{stg}	Storage temperature	–40	+125	°C
P_D	Power dissipation	–	150	mW

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_S	Detection threshold voltage	R_L = 470 Ω; $V_{OL} \leq$ 0.4 V; V_{CC} = HIGH-to-LOW	0.97 V_S	V_S	1.03 V_S	V
ΔV_S	Hysteresis voltage	R_L = 470 Ω; V_{CC} = LOW-to-HIGH-to-LOW	30	50	100	mV
$V_S/\Delta T$	Detection threshold voltage temperature coefficient	R_L = 470 Ω; T_{amb} = –20 °C to +75 °C	–	±0.01	–	%/°C
V_{OL}	LOW-level output voltage	$V_{CC} = V_{S(min)}$ – 0.05 V; R_L = 470 Ω	–	0.2	0.4	V
I_{LO}	Output leakage current	V_{CC} = 10 V; $V_O = V_{CC}$	–	–	±0.1	V
I_{CCL}	Supply current (LOW Reset)	$V_{CC} = V_{S(min)}$ – 0.05 V; $R_L = \infty$	–	1.0	2.0	µA
I_{CCH}	Supply current (HIGH Reset)	$V_{CC} = V_{S(typ)}$ / 0.85 V; $R_L = \infty$	–	1.5	2.5	µA
t_{PLH}	HIGH-to-LOW delay time	C_L = 100 pF; R_L = 4.7 kΩ	–	20	60	µs
t_{PHL}	LOW–to-HIGH delay time	C_L = 100 pF; R_L = 4.7 kΩ	–	20	60	µs
V_{OPL}	Minimum operating threshold voltage	R_L = 4.7 kΩ; $V_{OL} \leq$ 0.4 V	–	0.65	0.80	V
I_{OL1}	Output current (LOW Reset) 1	V_O = 0.4 V; R_L = 0; $V_{CC} = V_{S(min)}$ – 0.05 V	–	30	–	mA
I_{OL2}	Output current (LOW Reset) 2	V_O = 0.4 V; R_L = 0; $V_{CC} = V_{S(min)}$ – 0.15 V; T_{amb} = –30 °C to +80 °C	–	23	–	mA

TYPICAL PERFORMANCE CURVES

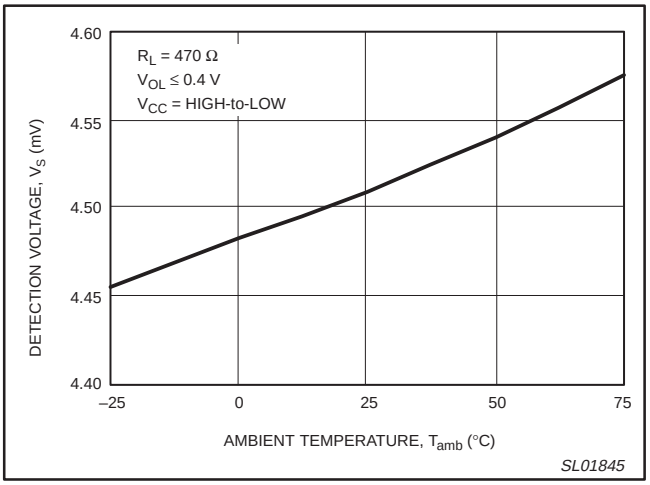


Figure 3. Detection voltage versus ambient temperature.

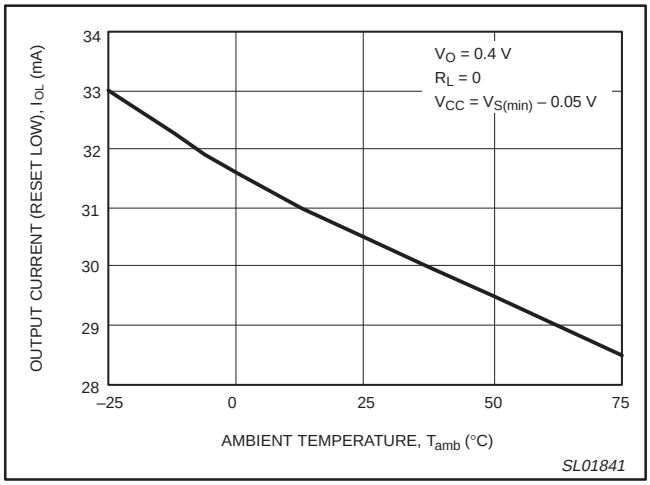


Figure 4. Detection voltage versus ambient temperature.

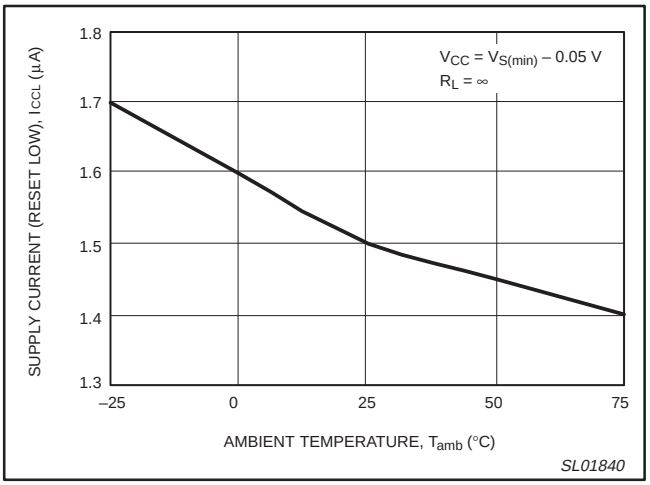


Figure 5. Supply current (Reset LOW) versus ambient temperature.

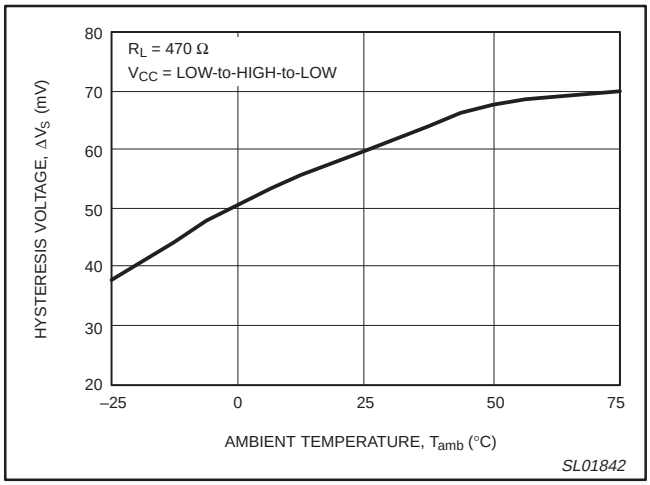


Figure 6. Hysteresis voltage versus ambient temperature.

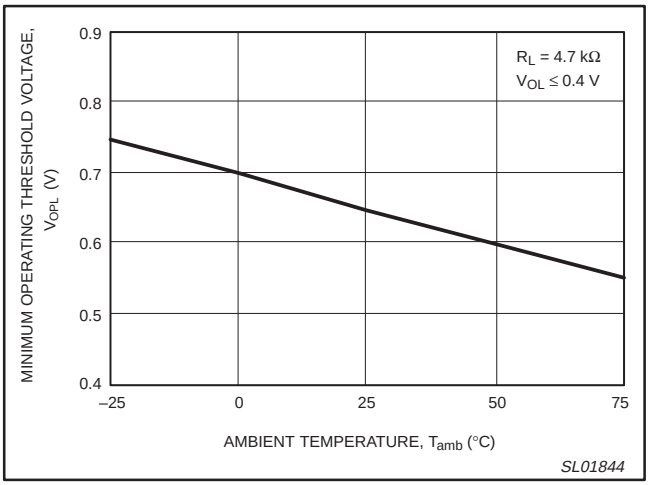


Figure 7. Minimum operating threshold voltage versus ambient temperature.

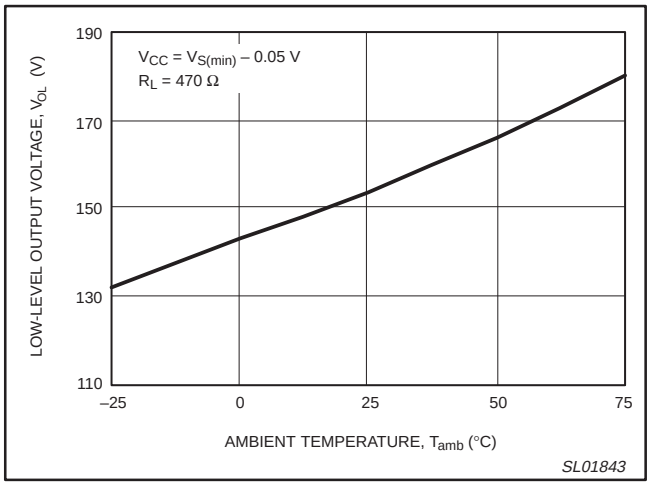


Figure 8. LOW-level output voltage versus ambient temperature.

TECHNICAL DISCUSSION

The NE56631-XX is a Bipolar IC designed to provide power source monitoring and a system reset function in the event the power sags below an acceptable level for the system to operate reliably. The IC is designed to generate a reset signal for a wide range of microprocessor and other logic systems. The NE56631-XX can operate at supply voltage up to 10 volts. The series includes several devices with precision threshold reset voltage values of 1.9, 2.0, 2.7, 2.8, 2.9, 3.0, 3.1, 4.2, 4.3, 4.4, 4.5, 4.6 V. The reset threshold incorporates a typical hysteresis of 50 mV to prevent erratic reasserts from being generated. An internal fixed delay time circuit provides a fixed power-on-reset delay of typically 20 μs with a guaranteed maximum delay of 60 μs.

The output of the NE56631-XX utilizes an open collector topology, which requires an external pull-up resistor to V_{CC}. Though this may be regarded as a disadvantage, it is advantageous in many sensitive applications. Since the open collector output cannot source reset current when both are operated from a common supply, the NE56631-XX offers a safe interconnect to a wide variety of microprocessors.

The NE56631-XX operates at low supply currents, typically 1.5 μA, while offering high precision of the threshold detection (±3%).

Figure 9 is a functional block diagram of the NE56631-XX. The internal reference source voltage is typically 0.65 V over the temperature range. The reference voltage is connected to the non-inverting input of the threshold comparator while the inverting input monitors the supply voltage through a voltage divider network made up of R1 and R2. The output of the comparator drives the series base resistor, R3 of a common emitter amplifier, Q1. The collector of Q1 is connected through R4 to the inverting terminal of the op amp. The op amp output is connected to the series base resistor, R5 of the output common emitter transistor, Q2. The collector output of Q2 is connected to the non-inverting terminal of the op amp which drives it.

When the supply voltage sags to the threshold detection voltage, the resistor divider network supplies a voltage to the inverting terminal of the threshold comparator which is less than V_{REF}, causing the output of the comparator to go to a HIGH state. This causes the common emitter amplifier, Q1 to turn on pulling down the non-inverting terminal of the op amp, which causes its output to go to a HIGH state. This high output level turns on the output common emitter transistor, Q2. The collector output of Q2 is pulled LOW through the external pull-up resistor, thereby asserting the Active-LOW reset.

The bipolar common emitter transistor, Q1and the op amp establishes threshold hysteresis by turning on when the threshold comparator goes to a HIGH state (when V_{CC} sags to or below the threshold level). With the output of Q2 connected to the non-inverting terminal of the op amp, the non-inverting terminal of the op amp has a level near ground at about 0.4 V when the reset is asserted (Active-LOW). For the op amp to reverse its output, the comparator output and Q1 must overcome the additional pull-down voltage present on the op amp inverting input. The differential voltage required to do this establishes the hysteresis voltage of the sensed threshold voltage. Typically it is 50 mV.

When V_{CC} voltage sags, and it is below the detection Threshold (V_{SL}), the device will assert a Reset LOW output at or near ground potential. As V_{CC} voltage rises from ($V_{CC} < V_{SL}$) to V_{SH} or higher, the Reset is released and the output follows V_{CC}. Conversely, decreases in V_{CC} from ($V_{CC} > V_{SL}$) to V_{SL} will cause the output to be pulled to ground.

Hysteresis Voltage = Released Voltage – Detection Threshold Voltage

$$\Delta V_S = V_{SH} - V_{SL}$$

where:

$$V_{SH} = V_{SL} + \Delta V_S$$
$$V_{SL} = V_{SH} - \Delta V_S$$

When V_{CC} drops below the minimum operating voltage, typically 0.65 V, the output is undefined and the output reset low assertion is not guaranteed. At this level of V_{CC} the output will try to rise to V_{CC}.

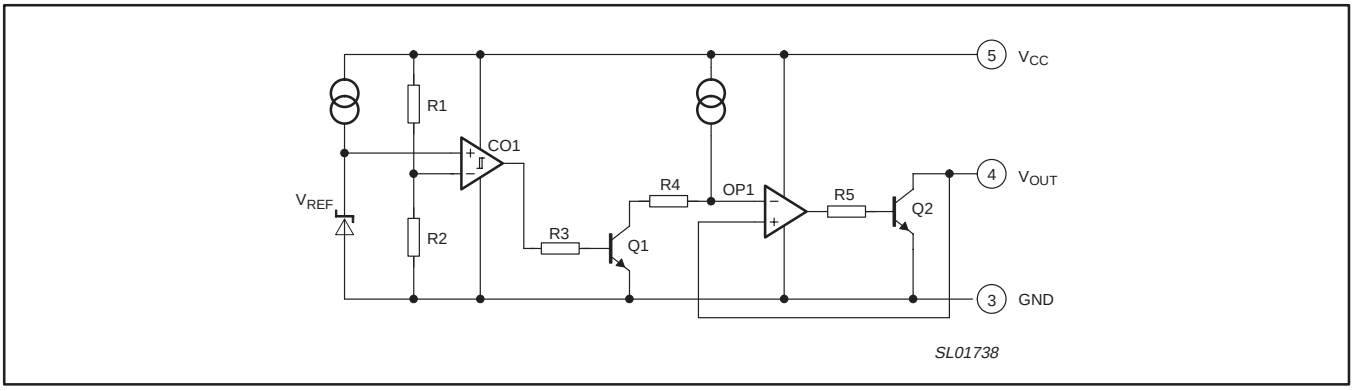


Figure 9. Functional diagram.

TIMING DIAGRAM

The Timing Diagram in Figure 10 depicts the operation of the device. Letters A–J on the Time axis indicates specific events.

A: At "A", V_{CC} begins to increase. Also the V_{OUT} voltage initially increases but abruptly decreases when V_{CC} reaches the level (approximately 0.65 V) that activates the internal bias circuitry and $\overline{\text{RESET}}$ is asserted.

B: At "B", V_{CC} reaches the threshold level of V_{SH}. At this point the device releases the hold on the V_{OUT} reset. The Reset output V_{OUT} tracks V_{CC} as it rises above V_{SH} (assuming the reset pull-up resistor R_{PU} is connected to V_{CC}). In a microprocessor-based system these events release the reset from the microprocessor, allowing the microprocessor to function normally.

C-D: At "C", V_{CC} begins to fall, causing V_{OUT} to follow. V_{CC} continues to fall until the V_{SL} undervoltage detection threshold is reached at "D". This causes a reset signal to be generated (V_{OUT} RESET goes LOW).

D-E: Between "D" and "E", V_{CC} starts rising.

E: At "E", V_{CC} rises to the V_{SH} level. Once again, the device releases the hold on the V_{OUT} reset. The Reset output tracks V_{CC} as it rises above V_{SH}.

F-G: At "F", V_{CC} is above the upper threshold and begins to fall, causing V_{OUT} to follow it. As long as V_{CC} remains above the V_{SH}, no reset signal will be triggered. Before V_{CC} falls to the V_{SH}, it begins to rise, causing V_{OUT} to follow it. At "G", V_{CC} returns to normal.

H: At event "H", V_{CC} falls until the V_{SL} undervoltage detection threshold is reached. At this level, a $\overline{\text{RESET}}$ signal is generated and V_{OUT} goes LOW.

J: At "J", the V_{CC} voltage has decreased until normal internal circuit bias is unable to maintain a V_{OUT} reset. As a result, V_{CC} may rise to less than 0.65 V. As V_{CC} decreases further, the V_{OUT} reset also decreases to zero.

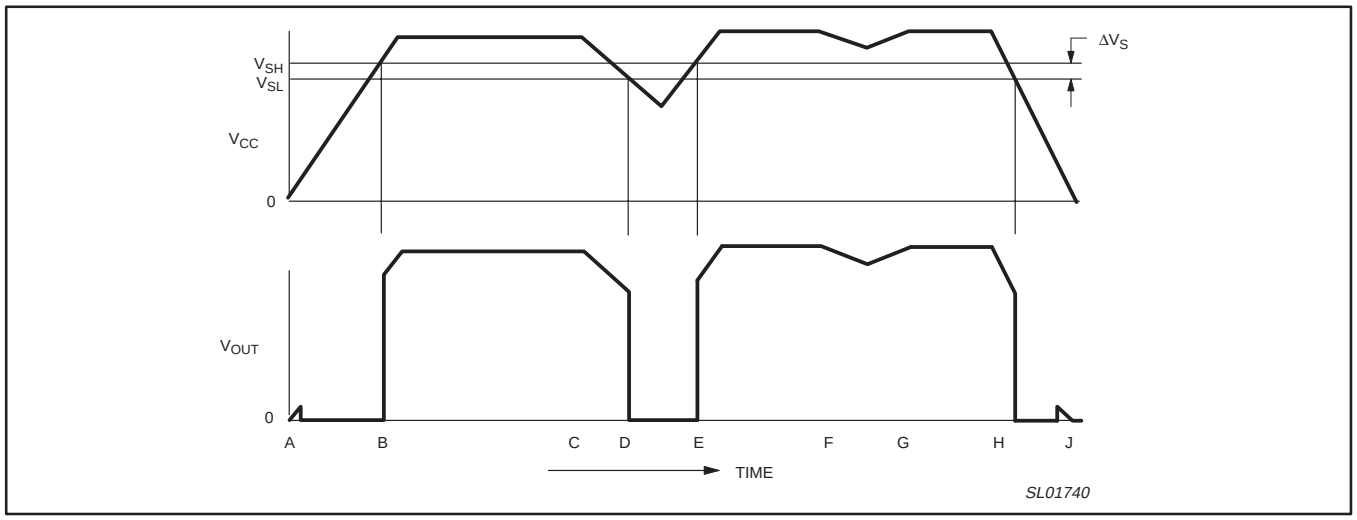


Figure 10. Timing diagram.

APPLICATION INFORMATION

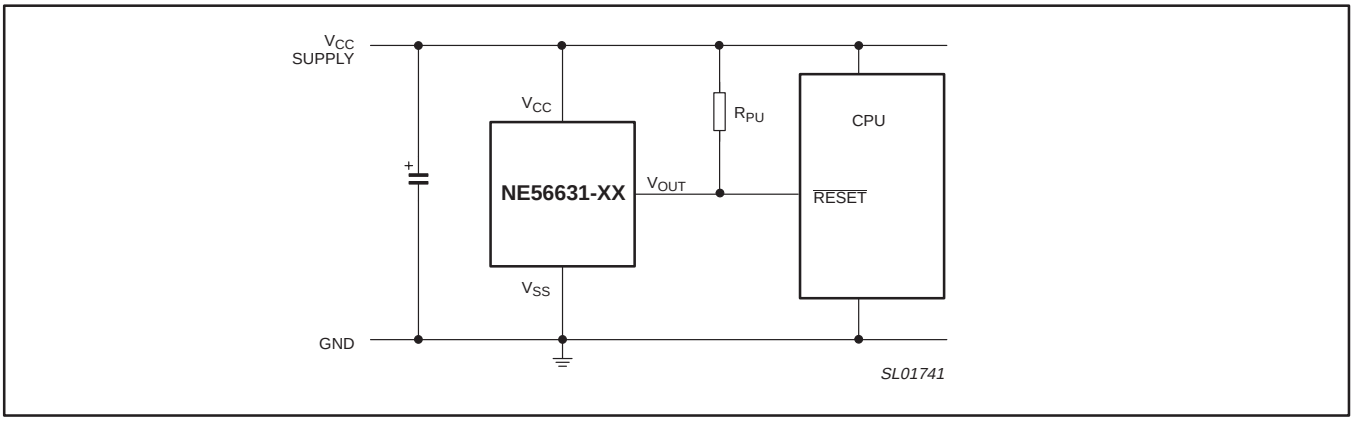


Figure 11. Conventional reset application for NE56631-XX.

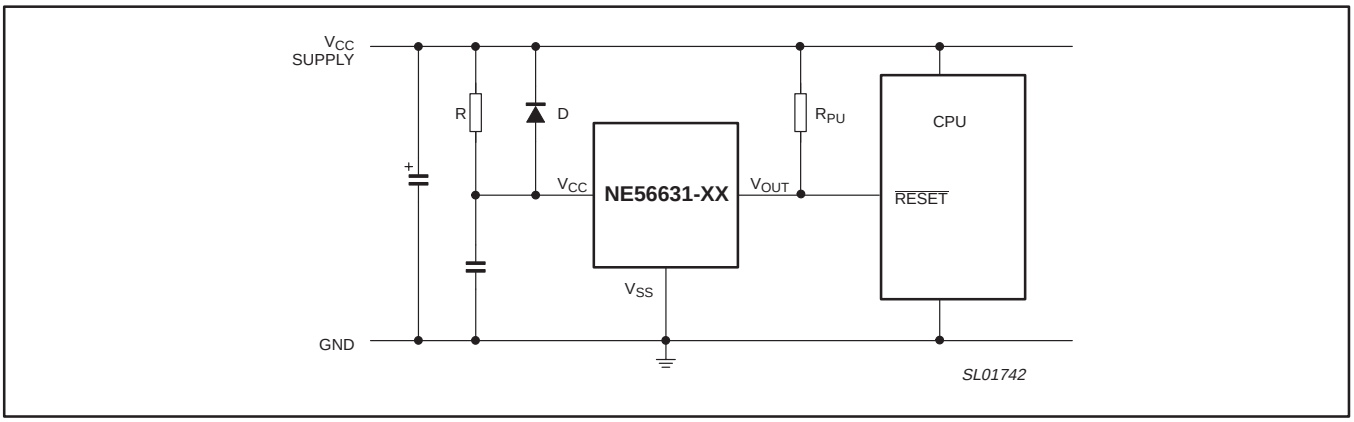


Figure 12. Power On Reset circuit for NE56631-XX.

The Power ON Reset Circuit shown in Figure 12 is an example of obtaining a stable reset condition upon power-up. If power supply rises abruptly, the $\overline{\text{RESET}}$ may go “HIGH” momentarily when V_{CC} is below the minimum operating voltage (0.85 V). To overcome this undesirable response, a resistor in placed between positive supply, V_{CC} and V_{CC} pin and a capacitor from V_{CC} pin to ground. The RC circuit solution works reasonably well for power-up as long as the power supply voltage rises faster than the RC time constant. The RC network provides the necessary reset delay to hold the microprocessor in reset until its circuitry settles down and normal operation begins. When the supply turns off, the diode provides a path for the capacitor to discharge to more quickly assert logic LOW reset.

PACKING METHOD

The NE56631-XX is packed in reels, as shown in Figure 13.

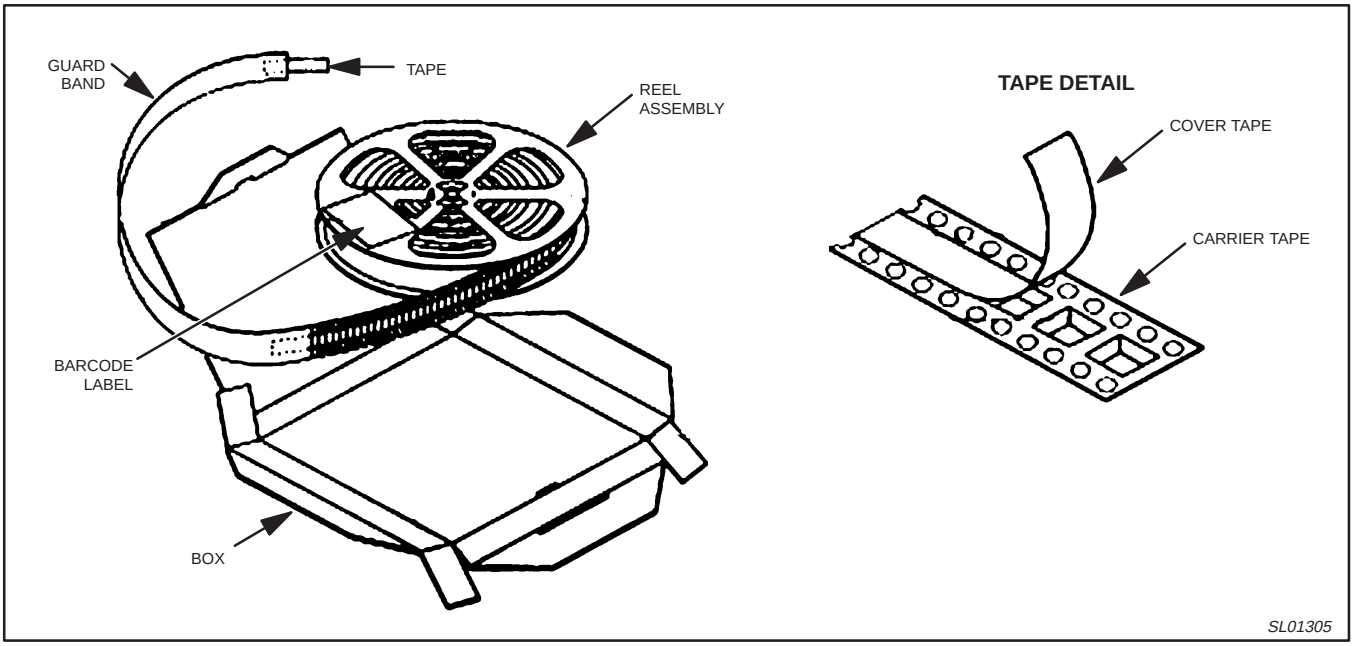
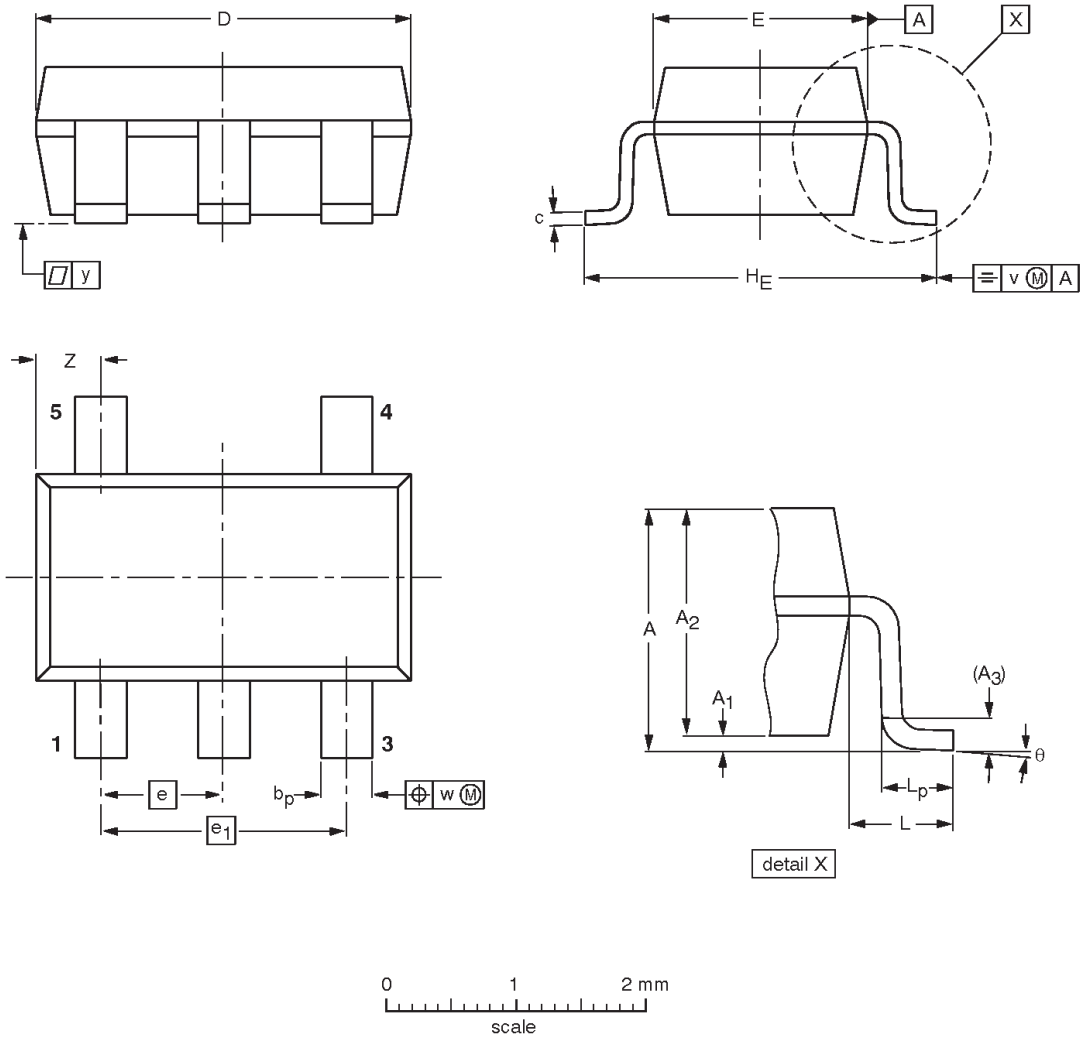


Figure 13. Tape and reel packing method.

SOT23-5: plastic small outline package; 5 leads; body width 1.5 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p			y		θ
mm	1.35	0.05 0.15	1.2 1.0	0.025	0.55 0.41	0.22 0.08	3.00 2.70	1.70 1.50	0.95	1.90	3.00 2.60	0.60	0.55 0.35			0.1		8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			
	IEC	JEDEC	EIAJ	
		MO-178		

REVISION HISTORY

Rev	Date	Description
_2	20030214	**Product data (9397 750 11131); ECN 853-2328 29155 of 06 November 2002. Supersedes data of 2002 Oct 07 (9397 750 10266).** Modifications: • Page 6, Technical discussion; third paragraph: **from** "... typically 1.5 mA, ..." **to** "... typically 1.5 µA, ..."
_1	20021007	**Product data (9397 750 10266); ECN 853–2328 27919 of 25 March 2002.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 02-03

Document order number: 9397 750 11131

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